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LV8086T

Bi-CMOS LSI

Forward/Reverse Motor Driver

Overview

LV8086T is a 2ch forward/reverse motor driver IC using D-MOS FET for output stage. As MOS circuit is used, it supports the PWM input. Its features are that the on resistance (0.75Ω typ) and current dissipation are low. It also provides protection functions such as heat protection circuit and reduced voltage detection and is optimal for the motors that need high-current.

Functions

- 2ch forward/reverse motor driver
- Low power consumption
- Built-in charge pump circuit
- Compact TSSOP24 package
- Possible to respond to 3V control voltage and 6V motor voltage device
- Low ON resistance 1.2Ω
- Built-in low voltage reset and thermal shutdown circuit
- Four mode function forward/reverse, brake, stop.

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, SGND = PGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage (For load)	VM1,2 max		-0.5 to 7.5	V
Supply voltage (For control)	V _{CC} max		-0.5 to 6.0	V
Output current	I _O max1	$t \leq 100\text{ms}$	1.4	A
Output peak current	I _O max2	$t \leq 10\text{ms}$	2.5	A
Input voltage	V _{IN} max		-0.5 to V _{CC} +0.5	V
Allowable power dissipation	Pd	* Mounted on a board	800	mW
Operating temperature	T _{opr}		-20 to +75	°C
Storage temperature	T _{stg}		-55 to +150	°C

* : Mounted on a specified board : 30×50×1.6mm, glass epoxy board.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

LV8086T

Allowable Operating Ratings at Ta = 25°C, SGND = PGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage (VM Pin)	VM		2.0 to 7.0	V
Supply voltage (VCC Pin)	VCC		2.7 to 5.5	V
Input signal voltage	V _{IN}		0 to V _{CC}	V
Input signal frequency	f max		100	kHz
Capacitor for charge pump	C1, C2, C3		0.001 to 0.1	μF

Electrical Characteristics at Ta = 25°C, VCC = VM1 = VM2 = 5.0V, SGND = PGND = 0V, unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current for load at standby	IMO	EN = 0V			1.0	μA
Supply current for control at standby	ICO	EN = 0V, IN1 = IN2 = IN3 = IN4 = 0V			1.0	μA
Current drain during operation	IC1	EN = 5V, VG at no load		0.7	1.2	mA
H-level input voltage	V _{IH}	2.7V ≤ V _{CC} ≤ 5.5V	0.6V _{CC}		V _{CC}	V
L-level input voltage	V _{IL}	2.7V ≤ V _{CC} ≤ 5.5V	0		0.2V _{CC}	V
H-level input current (IN1, IN2, IN3, IN4)	I _{IH}				1.0	μA
L-level input current (IN1, IN2, IN3, IN4)	I _{IL}		-1.0			μA
Pull-down resistance (EN1, 2)	RUP		100	200	400	kΩ

Ta = 25°C, VCC = VM = 5.0V, SGND = PGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output ON resistance	RON	Sum of ON resistances at top and bottom		0.75	1.2	Ω
Charge pump voltage	VG		8.5		10.5	V
Low-voltage detection operation voltage	VCS		2.15	2.30	2.45	V
Thermal shutdown operation temperature	Tth			180		°C
Charge pump capacity (IG = 500μA)	VGLOAD		8	9		V
IG current dissipation (Fin = 20kHz)	IG				350	μA
Charge pump start time	TVG	CVG = 0.1μF			1.0	ms
Output block	Turn on time	TPLH		0.2	0.4	μs
	Turn off time	TPHL		0.2	0.4	μs

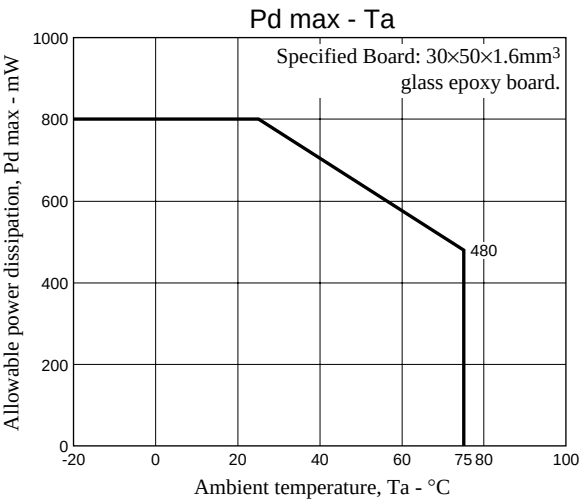
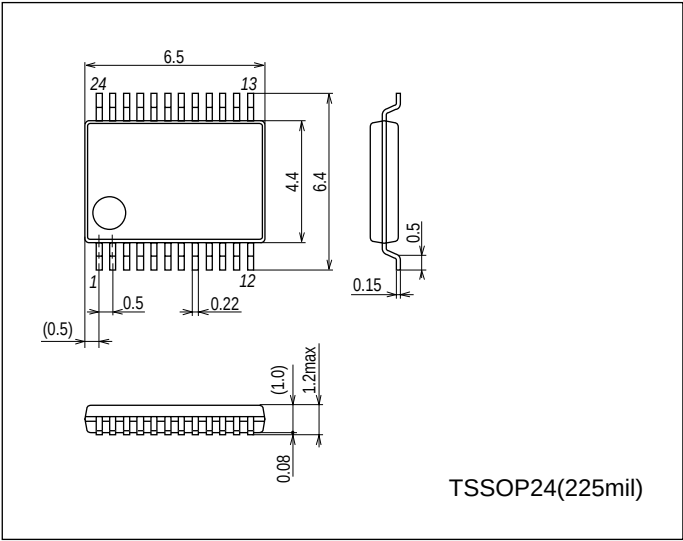
Remarks

1. It shows current dissipation of VM1,2 pin in output OFF state.
2. It shows current dissipation of VCC pin in stand-by state.
(The standard current depends on EN pin pull-down resistance.)
3. It shows current dissipation of VCC pin in state of EN = 5V (stand-by), including current dissipation of VG pin.
4. For IN1, IN2, IN3 and IN4 pins, no pull-down and pull-up resistance is needed. (High impedance pin)
5. It shows sum of upper and lower saturation voltages of OUT pin.
6. It controls charge-pump oscillation and makes specified voltage.
7. When low voltage is detected, the lower output is turned OFF.
8. When thermal protection circuit is activated, the lower output is turned OFF.
When the heat temperature is fallen, it is turned ON again.
9. IG (VG pin load current) = 500μA
10. It shows VG pin current dissipation in state of PWM input for IN pin.
11. It specifies start-up time from 10% to 90% when VG is in non-load state
(when setting the capacitor between VG and GND to 0.1μF and VCC is 5V).
12. It specifies 10% to 90% for start-up and 90% to 10% for shut-down.

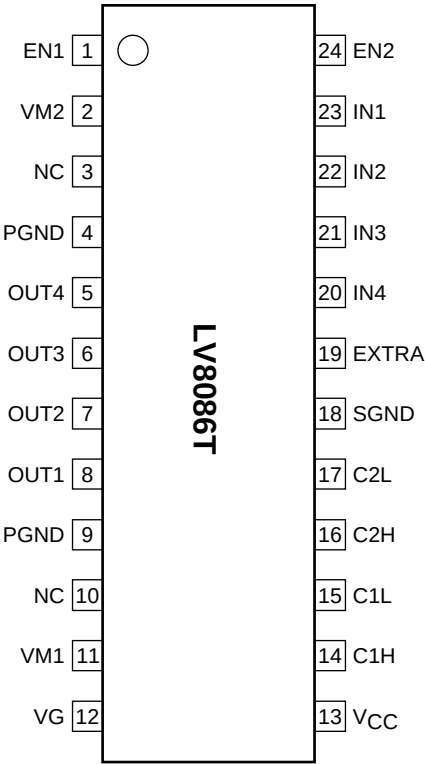
LV8086T

Package Dimensions

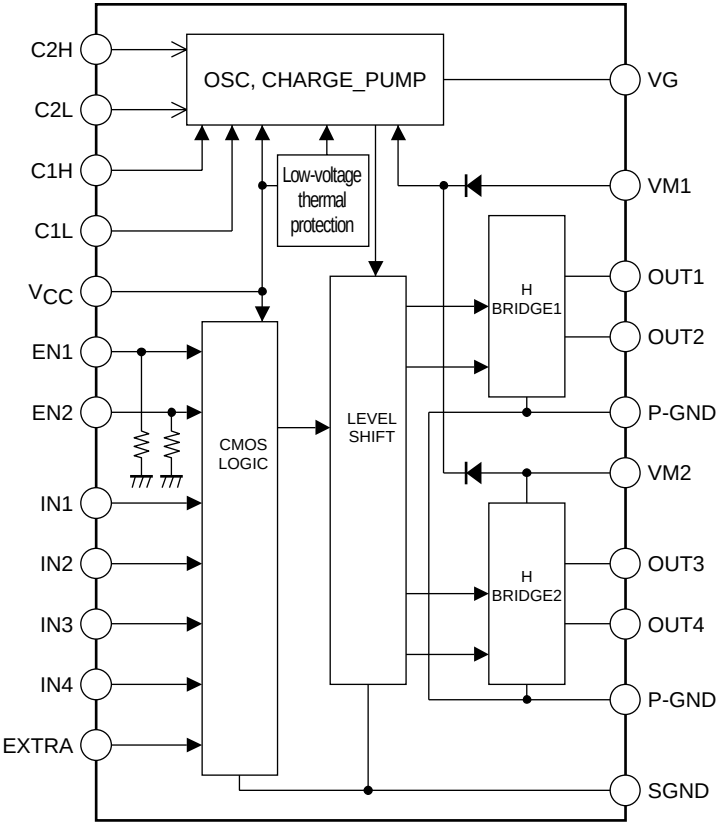
unit : mm (typ)
3260A



Pin Assignment



Block Diagram



Truth table

EXTRA	EN1 (EN2)	IN1 (IN3)	IN2 (IN4)	OUT1 (OUT3)	OUT2 (OUT4)	Circuit of Charge Pump	Mode
L	H	H	H	L	L	ON	Brake
		H	L	H	L		Forward
		L	H	L	H		Reverse
		L	L	Z	Z		Standby
	L	-	-	L	L	OFF	Standby
H	H	H	-	H	L	ON	Forward
		L	-	L	H		Reverse
	L	-	-	L	L		Brake

- : Don't care Z : High-Impedance

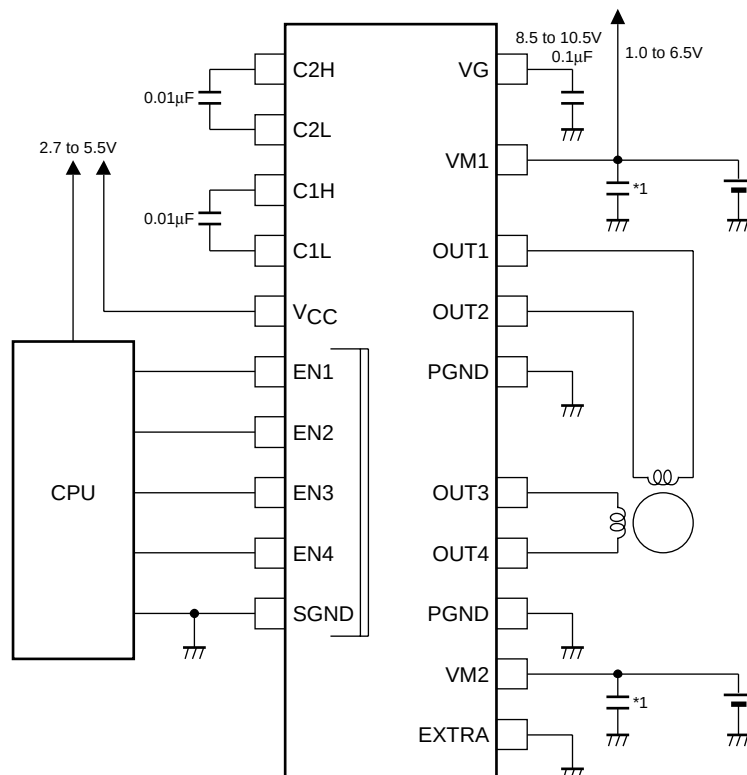
* Current drain becomes zero in the standby mode.
* The output side becomes OFF, with motor drive stopped, during voltage reduction and thermal protection.

LV8086T

Pin Functions

Pin No.	Pin name	Function	Equivalent Circuit
15 17	C1L C2L	Voltage raising capacitor connection pin	
14 16	C1H C2H	Voltage raising capacitor connection pin	
23 22 21 20 19	IN1 IN2 IN3 IN4 EXTRA	Driver output changeover	
1 24	EN1 EN2	Logic enable pin TOUT output control pin (Pull-down resistor incorporated)	
8 7 6 5	OUT1 OUT2 OUT3 OUT4 PGND	Driver output pin	
2 11	VM2 VM1	Motor power supply	
13	VCC	Logic power supply	
12	VG	Driver drive circuit power supply	
18	SGND	Logic GND	
9 4	PGND PGND	Driver GND (both terminals to be connected)	

Sample Application Circuit



*1: Connect a kickback absorption capacitor directly near IC. Coil kickback may cause rise of the voltage of VM line, and the voltage exceeding the maximum rating may be applied momentarily, resulting in deterioration or damage of IC.

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