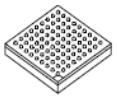
**Freescale Semiconductor**
Data Sheet: Technical Data

Document Number: MPC8535EEC
Rev. 7, 07/2015

# MPC8535E

# MPC8535E PowerQUICC III Integrated Processor Hardware Specifications



MAPBGA–783
29 mm x 29 mm

- High-performance, 32-bit e500 core, scaling up to 1.25 GHz, that implements the Power Architecture® technology
  - 36-bit physical addressing
  - Double-precision embedded floating point APU using 64-bit operands
  - Embedded vector and scalar single-precision floating-point APUs using 32- or 64-bit operands
  - Memory management unit (MMU)
- Integrated L1/L2 cache
  - L1 cache—32-Kbyte data and 32-Kbyte instruction
  - L2 cache—512-Kbyte (8-way set associative)
- DDR2/DDR3 SDRAM memory controller with full ECC support
  - One 64-bit/32-bit data bus
  - Up to 250-MHz clock (500-MHz data rate)
  - Supporting up to 16 Gbytes of main memory
  - Using ECC, detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble
  - Invoke a level of system power management by asserting MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode
  - Both hardware and software options to support battery-backed main memory
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPsec, IKE, SSL/TLS, iSCSI, SRTP, IEEE Std 802.16e™, and 3GPP.
  - XOR engine for parity checking in RAID storage applications
- Enhanced Serial peripheral interfaces (eSPI)
  - Support boot capability from eSPI
- Two enhanced three-speed Ethernet controllers (eTSECs) with SGMII support
  - Three-speed support (10/100/1000 Mbps)
  - Two IEEE Std 802.3®, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, IEEE 802.3ab, and IEEE Std 1588™-compatible controllers
  - Support for various Ethernet physical interfaces: GMII, TBI, RTBI, RGMII, MII, RGMII, RMII, and SGMII
  - Support TCP/IP acceleration and QOS features
  - MAC address recognition and RMON statistics support
  - Support ARP parsing and generating wake-up events based on the parsing results while in deep sleep mode
  - Support accepting and storing packets while in deep sleep mode
- High-speed interfaces (multiplexed) supporting:
  - Two PCI Express interfaces
    - PCI Express 1.0a compatible
    - One x4/x2/x1 PCI Express interface
    - Two x2/x1 ports
  - One SGMII interface
  - One Serial ATA (SATA) controller supports SATA I and SATA I data rates
- PCI 2.2 compatible PCI controller
- Two universal serial bus (USB) dual-role controllers comply with USB specification revision 2.0
- 133-MHz, 32-bit, enhanced local bus (eLBC) with memory controller
- Enhanced secured digital host controller (eSDHC) used for SD/MMC card interface
  - Support boot capability from eSDHC
- Integrated four-channel DMA controller
- Dual $I^2C$ and dual universal asynchronous receiver/transmitter (DUART) support
- Programmable interrupt controller (PIC)
- Power management, low standby power
  - Support Doze, Nap, Sleep, Jog, and Deep Sleep mode
  - PMC wake on: LAN activity, USB connection or remote wakeup, GPIO, internal timer, or external interrupt event
- System performance monitor
- IEEE Std 1149.1™-compatible, JTAG boundary scan
- 783-pin FC-PBGA package, 29 mm × 29 mm

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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This figure shows the major functional units within the chip.

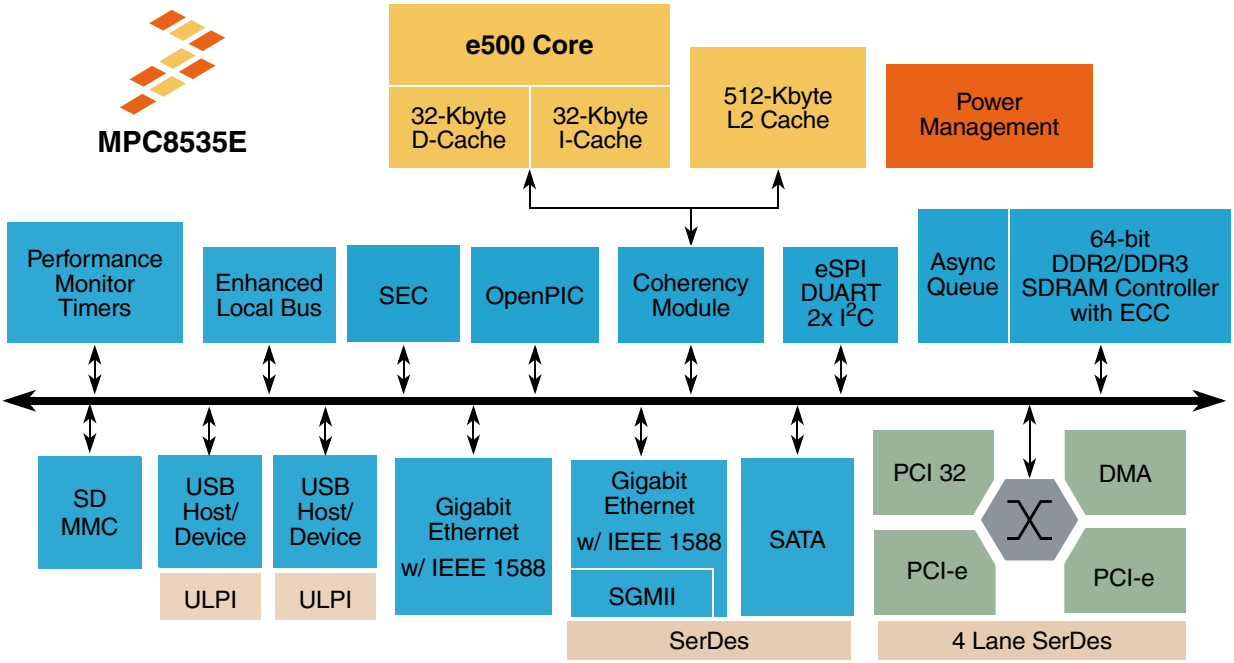



**Figure 1. Chip Block Diagram**

# 1 Pin Assignments and Reset States

### NOTE

The naming convention of TSEC1 and TSEC3 is used to allow the splitting voltage rails for the eTSEC blocks and to ease the port of existing PowerQUICC III software

### NOTE

The UART_SOUT[0:1] and $\overline{\text{TEST_SEL}}$ pins must be set to a proper state during POR configuration. See Table 1 for more details.

## 1.1 Pin Map

See Table 1 for the MPC8535E pinout, which is a subset of the MPC8536E.

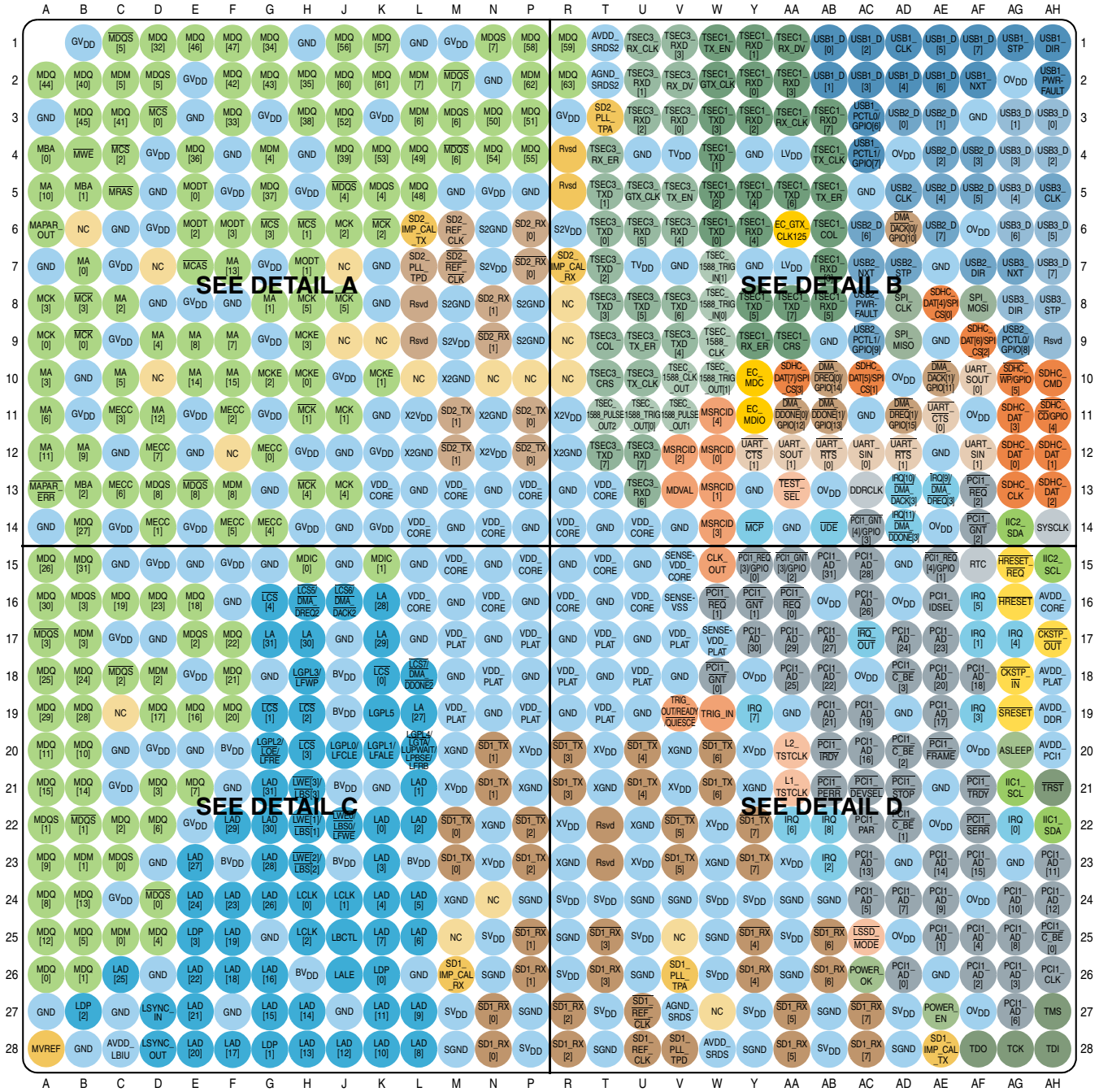
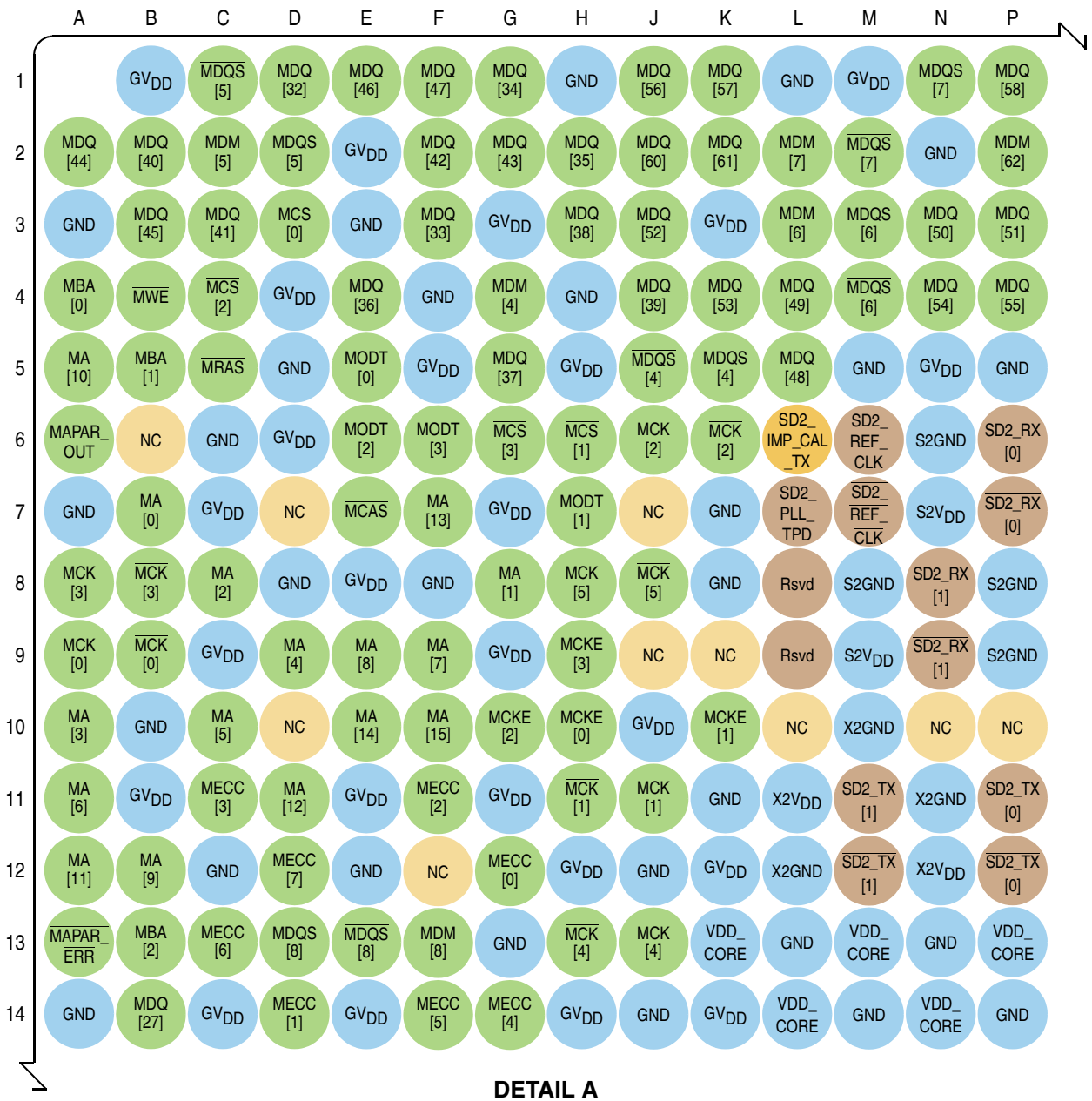
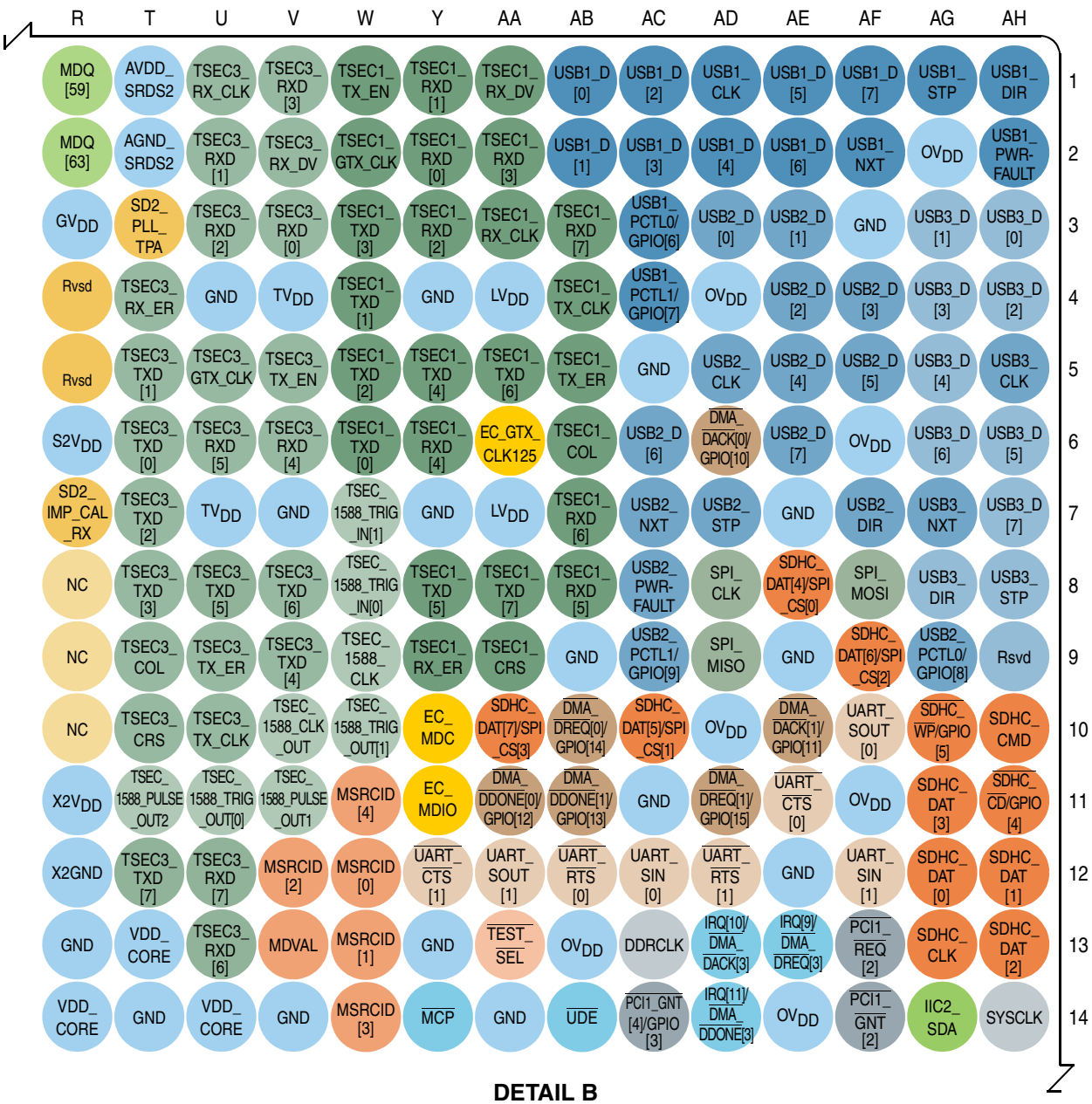



**Figure 2. Chip Pin Map Bottom View**




**DETAIL A**

**Figure 3. Chip Pin Map Detail A**




**DETAIL B**

**Figure 4. Chip Pin Map Detail B**

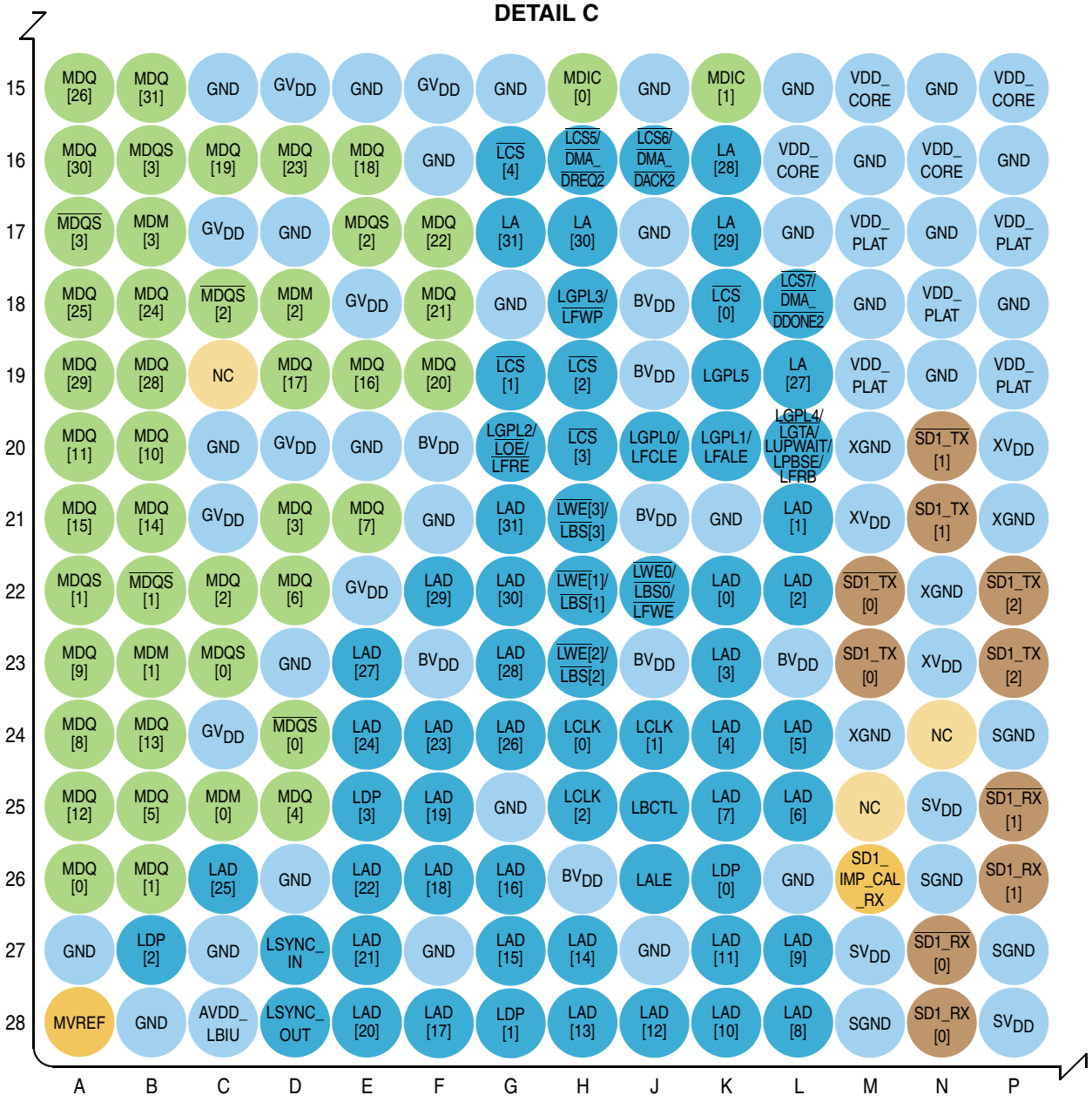



**Figure 5. Chip Pin Map Detail C**

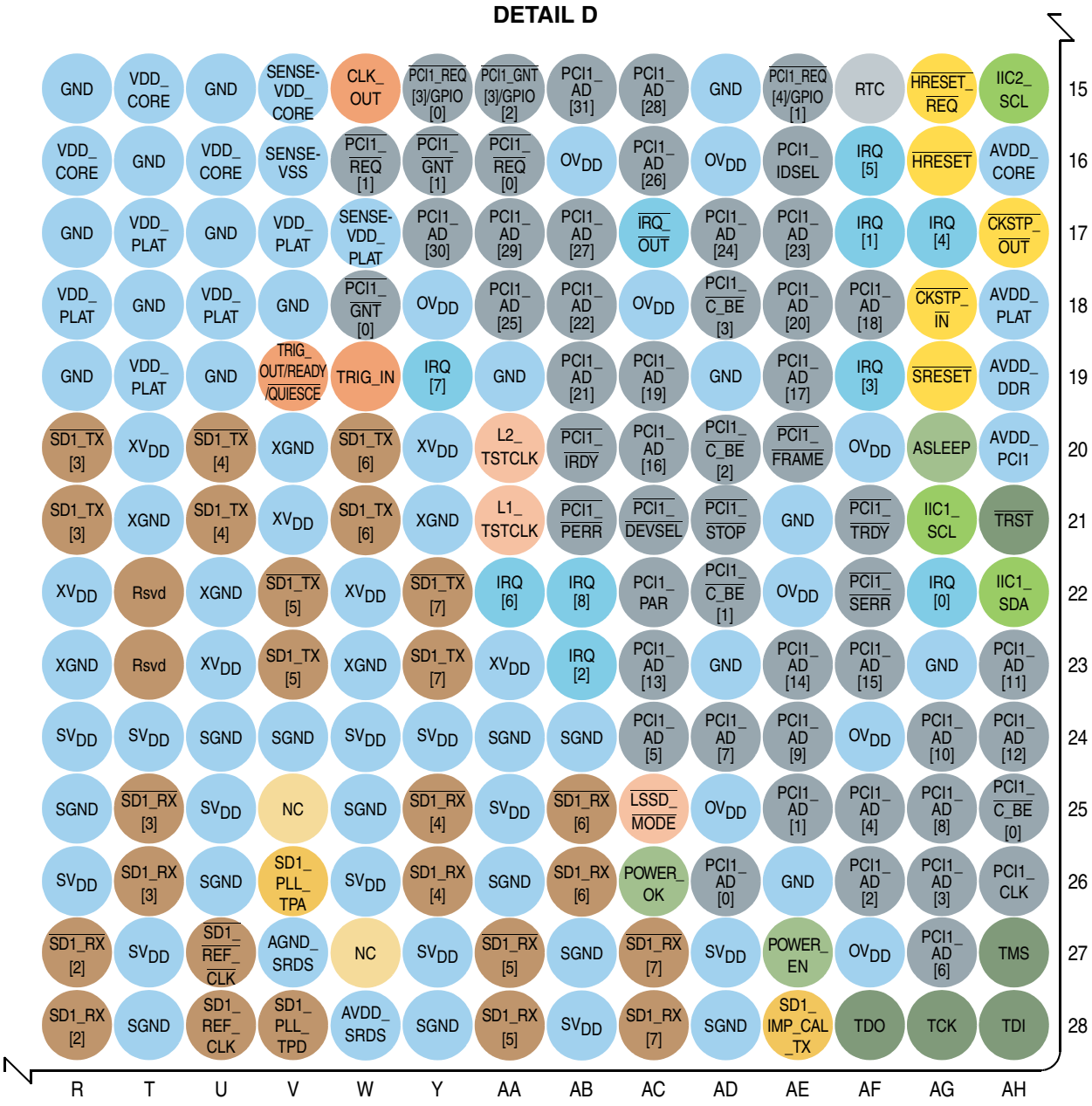



**Figure 6. Chip Pin Map Detail D**

This table provides the pin-out listing for the 783 FC-PBGA package.

**Table 1. Pinout Listing**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| **PCI** | | | | | |
| PCI1_AD[31:0] | Muxed Address / data | AB15,Y17,AA17,AC15, AB17,AC16,AA18, AD17,AE17,AB18, AB19,AE18,AC19, AF18,AE19,AC20, AF23,AE23,AC23, AH24,AH23,AG24, AE24,AG25,AD24, AG27,AC24,AF25, AG26,AF26,AE25, AD26 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI1_C_BE[3:0]}}$ | Command/Byte Enable | AD18, AD20,AD22, AH25 | I/O | $OV_{DD}$ | 29 |
| PCI1_PAR | Parity | AC22 | I/O | $OV_{DD}$ | 29 |
| $\overline{\text{PCI1_FRAME}}$ | Frame | AE20 | I/O | $OV_{DD}$ | 2,29 |
| $\overline{\text{PCI1_TRDY}}$ | Target Ready | AF21 | I/O | $OV_{DD}$ | 2,29 |
| $\overline{\text{PCI1_IRDY}}$ | Initiator Ready | AB20 | I/O | $OV_{DD}$ | 2,29 |
| $\overline{\text{PCI1_STOP}}$ | Stop | AD21 | I/O | $OV_{DD}$ | 2,29 |
| $\overline{\text{PCI1_DEVSEL}}$ | Device Select | AC21 | I/O | $OV_{DD}$ | 2,29 |
| PCI1_IDSEL | Init Device Select | AE16 | I | $OV_{DD}$ | 29 |
| $\overline{\text{PCI1_PERR}}$ | Parity Error | AB21 | I/O | $OV_{DD}$ | 2,29 |
| $\overline{\text{PCI1_SERR}}$ | System Error | AF22 | I/O | $OV_{DD}$ | 2,4,29 |
| $\overline{\text{PCI1_REQ}}$[4:3]/GPIO[1:0] | Request | AE15,Y15 | I | $OV_{DD}$ | — |
| $\overline{\text{PCI1_REQ}}$[2:1] | Request | AF13,W16 | I | $OV_{DD}$ | 29 |
| $\overline{\text{PCI1_REQ}}$[0] | Request | AA16 | I/O | $OV_{DD}$ | 29 |
| $\overline{\text{PCI1_GNT}}$[4:3]/GPIO[3:2] | Grant | AC14, AA15 | O | $OV_{DD}$ | |
| $\overline{\text{PCI1_GNT}}$[2:1] | Grant | AF14,Y16 | O | $OV_{DD}$ | 5,9,25,29 |
| $\overline{\text{PCI1_GNT}}$[0] | Grant | W18 | I/O | $OV_{DD}$ | 29 |
| PCI1_CLK | PCI Clock | AH26 | I | $OV_{DD}$ | 29 |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| **DDR SDRAM Memory Interface** | | | | | |
| MDQ[0:63] | Data | A26,B26,C22,D21,D25, B25,D22,E21,A24,A23, B20,A20,A25,B24,B21, A21,E19,D19,E16,C16, F19,F18,F17,D16,B18, A18,A15,B14,B19,A19, A16,B15,D1,F3,G1,H2, E4,G5,H3,J4,B2,C3,F2, G2,A2,B3,E1,F1,L5,L4, N3,P3,J3,K4,N4,P4,J1, K1,P1,R1,J2,K2,P2,R2 | I/O | $GV_{DD}$ | — |
| MECC[0:7] | Error Correcting Code | G12,D14,F11,C11, G14,F14,C13,D12 | I/O | $GV_{DD}$ | — |
| $\overline{\text{MAPAR_ERR}}$ | Address Parity Error | A13 | I | $GV_{DD}$ | — |
| MAPAR_OUT | Address Parity Out | A6 | O | $GV_{DD}$ | — |
| MDM[0:8] | Data Mask | C25,B23,D18,B17,G4, C2,L3,L2,F13 | O | $GV_{DD}$ | — |
| $\overline{\text{MDQS}}$[0:8] | Data Strobe | D24,B22,C18,A17,J5, C1,M4,M2,E13 | I/O | $GV_{DD}$ | — |
| MDQS[0:8] | Data Strobe | C23,A22,E17,B16,K5, D2,M3,N1,D13 | I/O | $GV_{DD}$ | — |
| MA[0:15] | Address | B7,G8,C8,A10,D9,C10, A11,F9,E9,B12,A5, A12,D11,F7,E10,F10 | O | $GV_{DD}$ | — |
| MBA[0:2] | Bank Select | A4,B5,B13 | O | $GV_{DD}$ | — |
| $\overline{\text{MWE}}$ | Write Enable | B4 | O | $GV_{DD}$ | — |
| $\overline{\text{MRAS}}$ | Row Address Strobe | C5 | O | $GV_{DD}$ | — |
| $\overline{\text{MCAS}}$ | Column Address Strobe | E7 | O | $GV_{DD}$ | — |
| $\overline{\text{MCS}}$[0:3] | Chip Select | D3,H6,C4,G6 | O | $GV_{DD}$ | — |
| MCKE[0:3] | Clock Enable | H10,K10,G10,H9 | O | $GV_{DD}$ | 11 |
| MCK[0:5] | Differential Clock 3 Pairs / DIMM | A9,J11,J6,A8,J13,H8 | O | $GV_{DD}$ | — |
| $\overline{\text{MCK}}$[0:5] | Differential Clock 3 Pairs / DIMM | B9,H11,K6,B8,H13,J8 | O | $GV_{DD}$ | — |
| MODT[0:3] | On Die Termination | E5,H7,E6,F6 | O | $GV_{DD}$ | — |
| MDIC[0:1] | Calibration | H15,K15 | I/O | $GV_{DD}$ | 26 |
| **Local Bus Controller Interface** | | | | | |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| LAD[0:31] | Muxed data / address | K22,L21,L22,K23,K24, L24,L25,K25,L28,L27, K28,K27,J28,H28,H27, G27,G26,F28,F26,F25, E28,E27,E26,F24,E24, C26,G24,E23,G23,F22, G22,G21 | I/O | $BV_{DD}$ | 5,9,29 |
| LDP[0:3] | Data parity | K26,G28,B27,E25 | I/O | $BV_{DD}$ | 29 |
| LA[27] | Burst address | L19 | O | $BV_{DD}$ | 5,9,29 |
| LA[28:31] | Port address | K16,K17,H17,G17 | O | $BV_{DD}$ | 5,7,9,29 |
| $\overline{\text{LCS}}$[0:4] | Chip selects | K18,G19,H19,H20,G16 | O | $BV_{DD}$ | 29 |
| $\overline{\text{LCS5}}$/$\overline{\text{DMA_DREQ2}}$ | Chips selects / DMA Request | H16 | I/O | $BV_{DD}$ | 1,29 |
| $\overline{\text{LCS6}}$/$\overline{\text{DMA_DACK2}}$ | Chips selects / DMA Ack | J16 | O | $BV_{DD}$ | 1,29 |
| $\overline{\text{LCS7}}$/$\overline{\text{DMA_DDONE2}}$ | Chips selects / DMA Done | L18 | O | $BV_{DD}$ | 1,29 |
| $\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/$\overline{\text{LFWE}}$ | Write enable / Byte select | J22 | O | $BV_{DD}$ | 5,9,29 |
| $\overline{\text{LWE[1:3]}}$/$\overline{\text{LBS[1:3]}}$ | Write enable / Byte select | H22,H23,H21 | O | $BV_{DD}$ | 5,9,29 |
| LBCTL | Buffer control | J25 | O | $BV_{DD}$ | 5,8,9,29 |
| LALE | Address latch enable | J26 | O | $BV_{DD}$ | 5,8,9,29 |
| LGPL0/LFCLE | UPM general purpose line 0 / FLash command latch enable | J20 | O | $BV_{DD}$ | 5,9,29 |
| LGPL1/LFALE | UPM general purpose line 1 / Flash address latch enable | K20 | O | $BV_{DD}$ | 5,9,29 |
| LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$ | UPM general purpose line 2 / Output enable/Flash read enable | G20 | O | $BV_{DD}$ | 5,8,9,29 |
| LGPL3/$\overline{\text{LFWP}}$ | UPM general purpose line 3 / Flash write protect | H18 | O | $BV_{DD}$ | 5,9,29 |
| LGPL4/$\overline{\text{LGTA}}$/LUPWAIT /LPBSE/LFRB | UPM general purpose line 4 / Target Ack/Wait/SDRAM parity byte select/Flash Ready-busy | L20 | I/O | $BV_{DD}$ | 29, 35 |
| LGPL5 | UPM general purpose line 5 / Amux | K19 | O | $BV_{DD}$ | 5,9,29 |
| LCLK[0:2] | Local bus clock | H24,J24,H25 | O | $BV_{DD}$ | 29 |
| LSYNC_IN | Synchronization | D27 | I | $BV_{DD}$ | 29 |
| LSYNC_OUT | Local bus DLL | D28 | O | $BV_{DD}$ | 29 |
| DMA | | | | | |
| $\overline{\text{DMA_DACK}}$[0:1] /GPIO[10:11] | DMA Acknowledge | AD6,AE10 | O | $OV_{DD}$ | — |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| DMA_DREQ[0:1] /GPIO[14:15] | DMA Request | AB10,AD11 | I | $OV_{DD}$ | — |
| DMA_DDONE[0:1] /GPIO[12:13] | DMA Done | AA11,AB11 | O | $OV_{DD}$ | — |
| DMA_DREQ[2]/LCS[5] | Chips selects / DMA Request | H16 | I/O | $BV_{DD}$ | 1,29 |
| DMA_DACK[2]/LCS[6] | Chips selects / DMA Ack | J16 | O | $BV_{DD}$ | 1,29 |
| DMA_DDONE[2]/LCS[7] | Chips selects / DMA Done | L18 | O | $BV_{DD}$ | 1,29 |
| DMA_DREQ[3]/IRQ[9] | External interrupt/DMA request | AE13 | I | $OV_{DD}$ | 1 |
| DMA_DACK[3]/IRQ[10] | External interrupt/DMA Ack | AD13 | I/O | $OV_{DD}$ | 1 |
| DMA_DDONE[3]/IRQ[11] | External interrupt/DMA done | AD14 | I/O | $OV_{DD}$ | 1 |
| **USB Port 1** | | | | | |
| USB1_D[7:0] | USB1 Data bits | AF1,AE2,AE1,AD2, AC2,AC1,AB2,AB1 | I/O | $OV_{DD}$ | — |
| USB1_NXT | USB1 Next data | AF2 | I | $OV_{DD}$ | — |
| USB1_DIR | USB1 Data Direction | AH1 | I | $OV_{DD}$ | — |
| USB1_STP | USB1 Stop | AG1 | O | $OV_{DD}$ | 5,9 |
| USB1_PWRFAULT | USB1 bus power fault. | AH2 | I | $OV_{DD}$ | — |
| USB1_PCTL0/GPIO[6] | USB1 Port control 0 | AC3 | O | $OV_{DD}$ | — |
| USB1_PCTL1/GPIO[7] | USB1 Port control 1 | AC4 | O | $OV_{DD}$ | — |
| USB1_CLK | USB1 bus clock | AD1 | I | $OV_{DD}$ | — |
| **USB Port 2** | | | | | |
| USB2_D[7:0] | USB2 Data bits | AE6,AC6,AF5,AE5, AF4,AE4,AE3,AD3 | I/O | $OV_{DD}$ | — |
| USB2_NXT | USB2 Next data | AC7 | I | $OV_{DD}$ | — |
| USB2_DIR | USB2 Data Direction | AF7 | I | $OV_{DD}$ | — |
| USB2_STP | USB2 Stop | AD7 | O | $OV_{DD}$ | 5,9 |
| USB2_PWRFAULT | USB2 bus power fault. | AC8 | I | $OV_{DD}$ | — |
| USB2_PCTL0/GPIO[8] | USB2 Port control 0 | AG9 | O | $OV_{DD}$ | — |
| USB2_PCTL1/GPIO[9] | USB2 Port control 1 | AC9 | O | $OV_{DD}$ | — |
| USB2_CLK | USB2 bus clock | AD5 | I | $OV_{DD}$ | — |
| — | | | | | |
| Reserved | — | AH8 | — | — | — |
| Reserved | — | AH7,AG6,AH6,AG5, AG4,AH4,AG3,AH3, AG7, AG8, AH9,AH5 | — | — | 27 |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| **Programmable Interrupt Controller** | | | | | |
| $\overline{\text{MCP}}$ | Machine check processor | Y14 | I | $OV_{DD}$ | — |
| $\overline{\text{UDE}}$ | Unconditional debug event | AB14 | I | $OV_{DD}$ | — |
| IRQ[0:8] | External interrupts | AG22,AF17,AB23, AF19,AG17,AF16, AA22,Y19,AB22 | I | $OV_{DD}$ | — |
| IRQ[9]/$\overline{\text{DMA_DREQ[3]}}$ | External interrupt/DMA request | AE13 | I | $OV_{DD}$ | 1 |
| IRQ[10]/$\overline{\text{DMA_DACK[3]}}$ | External interrupt/DMA Ack | AD13 | I/O | $OV_{DD}$ | 1 |
| IRQ[11]/$\overline{\text{DMA_DDONE[3]}}$ | External interrupt/DMA done | AD14 | I/O | $OV_{DD}$ | 1 |
| $\overline{\text{IRQ_OUT}}$ | Interrupt output | AC17 | O | $OV_{DD}$ | 2,4 |
| **Ethernet Management Interface** | | | | | |
| EC_MDC | Management data clock | Y10 | O | $OV_{DD}$ | 5,9,22 |
| EC_MDIO | Management data In/Out | Y11 | I/O | $OV_{DD}$ | — |
| **Gigabit Reference Clock** | | | | | |
| EC_GTX_CLK125 | Reference clock | AA6 | I | $LV_{DD}$ | 31 |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 1)** | | | | | |
| TSEC1_TXD[7:0] | Transmit data | AA8,AA5,Y8,Y5,W3, W5,W4,W6 | O | $LV_{DD}$ | 5,9,22 |
| TSEC1_TX_EN | Transmit Enable | W1 | O | $LV_{DD}$ | 23 |
| TSEC1_TX_ER | Transmit Error | AB5 | O | $LV_{DD}$ | 5,9 |
| TSEC1_TX_CLK | Transmit clock In | AB4 | I | $LV_{DD}$ | — |
| TSEC1_GTX_CLK | Transmit clock Out | W2 | O | $LV_{DD}$ | — |
| TSEC1_CRS | Carrier sense | AA9 | I/O | $LV_{DD}$ | 17 |
| TSEC1_COL | Collision detect | AB6 | I | $LV_{DD}$ | — |
| TSEC1_RXD[7:0] | Receive data | AB3,AB7,AB8,Y6,AA2, Y3,Y1,Y2 | I | $LV_{DD}$ | — |
| TSEC1_RX_DV | Receive data valid | AA1 | I | $LV_{DD}$ | — |
| TSEC1_RX_ER | Receive data error | Y9 | I | $LV_{DD}$ | — |
| TSEC1_RX_CLK | Receive clock | AA3 | I | $LV_{DD}$ | — |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 3)** | | | | | |
| TSEC3_TXD[7:0] | Transmit data | T12,V8,U8,V9,T8,T7, T5,T6 | O | $TV_{DD}$ | 5,9,22 |
| TSEC3_TX_EN | Transmit Enable | V5 | O | $TV_{DD}$ | 23 |
| TSEC3_TX_ER | Transmit Error | U9 | O | $TV_{DD}$ | 5,9 |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| TSEC3_TX_CLK | Transmit clock In | U10 | I | $TV_{DD}$ | — |
| TSEC3_GTX_CLK | Transmit clock Out | U5 | O | $TV_{DD}$ | — |
| TSEC3_CRS | Carrier sense | T10 | I/O | $TV_{DD}$ | 17 |
| TSEC3_COL | Collision detect | T9 | I | $TV_{DD}$ | — |
| TSEC3_RXD[7:0] | Receive data | U12,U13,U6,V6,V1,U3, U2,V3 | I | $TV_{DD}$ | — |
| TSEC3_RX_DV | Receive data valid | V2 | I | $TV_{DD}$ | — |
| TSEC3_RX_ER | Receive data error | T4 | I | $TV_{DD}$ | — |
| TSEC3_RX_CLK | Receive clock | U1 | I | $TV_{DD}$ | — |
| **IEEE 1588** | | | | | |
| TSEC_1588_CLK | Clock In | W9 | I | $LV_{DD}$ | 29 |
| TSEC_1588_TRIG_IN[0:1] | Trigger In | W8,W7 | I | $LV_{DD}$ | 29 |
| TSEC_1588_TRIG_OUT[0:1] | Trigger Out | U11,W10 | O | $LV_{DD}$ | 5,9,29 |
| TSEC_1588_CLK_OUT | Clock Out | V10 | O | $LV_{DD}$ | 5,9,29 |
| TSEC_1588_PULSE_OUT1 | Pulse Out1 | V11 | O | $LV_{DD}$ | 5,9,29 |
| TSEC_1588_PULSE_OUT2 | Pulse Out2 | T11 | O | $LV_{DD}$ | 5,9,29 |
| **eSDHC** | | | | | |
| SDHC_CMD | Command line | AH10 | I/O | $OV_{DD}$ | 29 |
| $\overline{\text{SDHC_CD}}$/GPIO[4] | Card detection | AH11 | I | $OV_{DD}$ | — |
| SDHC_DAT[0:3] | Data line | AG12,AH12,AH13, AG11 | I/O | $OV_{DD}$ | 29 |
| SDHC_DAT[4:7] / SPI_CS[0:3] | 8-bit MMC Data line / SPI chip select | AE8,AC10,AF9,AA10 | I/O | $OV_{DD}$ | 29 |
| SDHC_CLK | SD/MMC/SDIO clock | AG13 | I/O | $OV_{DD}$ | 29 |
| $\overline{\text{SDHC_WP}}$/GPIO[5] | Card write protection | AG10 | I | $OV_{DD}$ | 1, 32 |
| **eSPI** | | | | | |
| SPI_MOSI | Master Out Slave In | AF8 | I/O | $OV_{DD}$ | 29 |
| SPI_MISO | Master In Slave Out | AD9 | I | $OV_{DD}$ | 29 |
| SPI_CLK | eSPI clock | AD8 | I/O | $OV_{DD}$ | 29 |
| SPI_CS[0:3] / SDHC_DAT[4:7] | eSPI chip select / SDHC 8-bit MMC data | AE8,AC10,AF9,AA10 | I/O | $OV_{DD}$ | 29 |
| **DUART** | | | | | |
| $\overline{\text{UART_CTS}}$[0:1] | Clear to send | AE11,Y12 | I | $OV_{DD}$ | 29 |
| $\overline{\text{UART_RTS}}$[0:1] | Ready to send | AB12,AD12 | O | $OV_{DD}$ | 29 |
| UART_SIN[0:1] | Receive data | AC12,AF12 | I | $OV_{DD}$ | 29 |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| UART_SOUT[0:1] | Transmit data | AF10,AA12 | O | $OV_{DD}$ | 5,9,22, 10,29 |
| **$I^2C$ interface** | | | | | |
| IIC1_SCL | Serial clock | AG21 | I/O | $OV_{DD}$ | 4,21,29 |
| IIC1_SDA | Serial data | AH22 | I/O | $OV_{DD}$ | 4,21,29 |
| IIC2_SCL | Serial clock | AH15 | I/O | $OV_{DD}$ | 4,21,29 |
| IIC2_SDA | Serial data | AG14 | I/O | $OV_{DD}$ | 4,21,29 |
| **SerDes1(x4)** | | | | | |
| SD1_TX[7:4] | Transmit Data (+) | Y23,W21,V23,U21 | O | $XV_{DD}$ | — |
| $\overline{\text{SD1_TX}}$[7:4] | Transmit Data(-) | Y22,W20,V22,U20 | O | $XV_{DD}$ | — |
| SD1_RX[7:4] | Receive Data(+) | AC28,AB26,AA28,Y26 | I | $XV_{DD}$ | — |
| $\overline{\text{SD1_RX}}$[7:4] | Receive Data(–) | AC27,AB25,AA27,Y25 | I | $XV_{DD}$ | — |
| Reserved | — | R21,P23,N21,M23, R20,P22,N20,M22 | — | — | 18 |
| Reserved | — | T26,R28,P26,N28, T25,R27,P25,N27 | — | — | 33 |
| SD1_PLL_TPD | PLL test point Digital | V28 | O | $XV_{DD}$ | 18 |
| SD1_REF_CLK | PLL Reference clock | U28 | I | $XV_{DD}$ | — |
| $\overline{\text{SD1_REF_CLK}}$ | PLL Reference clock complement | U27 | I | $XV_{DD}$ | — |
| Reserved | — | T22 | — | — | 18 |
| Reserved | — | T23 | — | — | 18 |
| **SerDes2(x1)** | | | | | |
| SD2_TX[0] | Transmit data(+) | P11 | O | $X2V_{DD}$ | — |
| $\overline{\text{SD2_TX[0]}}$ | Transmit data(-) | P12 | O | $X2V_{DD}$ | — |
| SD2_RX[0] | Receive data(+) | P6 | I | $X2V_{DD}$ | — |
| $\overline{\text{SD2_RX[0]}}$ | Receive data(-) | P7 | I | $X2V_{DD}$ | — |
| Reserved | — | M11,M12 | — | — | 18 |
| Reserved | — | N8, N9 | — | — | 34 |
| SD2_PLL_TPD | PLL test point Digital | L7 | O | $X2V_{DD}$ | 18 |
| SD2_REF_CLK | PLL Reference clock | M6 | I | $X2V_{DD}$ | — |
| $\overline{\text{SD2_REF_CLK}}$ | PLL Reference clock complement | M7 | I | $X2V_{DD}$ | — |
| Reserved | — | L8 | — | $X2V_{DD}$ | 18 |
| Reserved | — | L9 | — | $X2V_{DD}$ | 18 |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| **General-Purpose Input/Output** | | | | | |
| GPIO[0:1]/PCI1_REQ[3:4] | GPIO/PCI request | Y15,AE15 | I/O | $OV_{DD}$ | — |
| GPIO[2:3]/PCI1_GNT[3:4] | GPIO/PCI grant | AA15,AC14 | I/O | $OV_{DD}$ | — |
| GPIO[4]/SDHC_CD | GPIO/SDHC card detection | AH11 | I/O | $OV_{DD}$ | — |
| GPIO[5]/SDHC_WP | GPIO/SDHC write protection | AG10 | I/O | $OV_{DD}$ | 32 |
| GPIO[6]/USB1_PCTL0 | GPIO/USB1 PCTL0 | AC3 | I/O | $OV_{DD}$ | — |
| GPIO[7]/USB1_PCTL1 | GPIO/USB1 PCTL1 | AC4 | I/O | $OV_{DD}$ | — |
| GPIO[8]/USB2_PCTL0 | GPIO/USB2 PCTL0 | AG9 | I/O | $OV_{DD}$ | — |
| GPIO[9]/USB2_PCTL1 | GPIO/USB2 PCTL1 | AC9 | I/O | $OV_{DD}$ | — |
| GPIO[10:11] /DMA_DACK[0:1] | GPIO/DMA Ack | AD6,AE10 | I/O | $OV_{DD}$ | — |
| GPIO[12:13] /DMA_DDONE[0:1] | GPIO/DMA done | AA11,AB11 | I/O | $OV_{DD}$ | — |
| GPIO[14:15] /DMA_DREQ[0:1] | GPIO/DMA request | AB10,AD11 | I/O | $OV_{DD}$ | — |
| **System Control** | | | | | |
| HRESET | Hard reset | AG16 | I | $OV_{DD}$ | — |
| HRESET_REQ | Hard reset - request | AG15 | O | $OV_{DD}$ | 22 |
| SRESET | Soft reset | AG19 | I | $OV_{DD}$ | — |
| CKSTP_IN | CheckStop in | AG18 | I | $OV_{DD}$ | — |
| CKSTP_OUT | CheckStop Output | AH17 | O | $OV_{DD}$ | 2,4 |
| **Debug** | | | | | |
| TRIG_IN | Trigger in | W19 | I | $OV_{DD}$ | — |
| TRIG_OUT/READY /QUIESCE | Trigger out/Ready/Quiesce | V19 | O | $OV_{DD}$ | 22 |
| MSRCID[0:1] | Memory debug source port ID | W12,W13 | O | $OV_{DD}$ | 6,9 |
| MSRCID[2:4] | Memory debug source port ID | V12, W14,W11 | O | $OV_{DD}$ | 6,9,22 |
| MDVAL | Memory debug data valid | V13 | O | $OV_{DD}$ | 6,22 |
| CLK_OUT | Clock Out | W15 | O | $OV_{DD}$ | 11 |
| **Clock** | | | | | |
| RTC | Real time clock | AF15 | I | $OV_{DD}$ | — |
| SYSCLK | System clock / PCI clock | AH14 | I | $OV_{DD}$ | — |
| DDRCLK | DDR clock | AC13 | I | $OV_{DD}$ | 30 |
| **JTAG** | | | | | |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| TCK | Test clock | AG28 | I | $OV_{DD}$ | — |
| TDI | Test data in | AH28 | I | $OV_{DD}$ | 12 |
| TDO | Test data out | AF28 | O | $OV_{DD}$ | 11 |
| TMS | Test mode select | AH27 | I | $OV_{DD}$ | 12 |
| $\overline{\text{TRST}}$ | Test reset | AH21 | I | $OV_{DD}$ | 12 |
| **DFT** | | | | | |
| L1_TSTCLK | L1 test clock | AA21 | I | $OV_{DD}$ | 19 |
| L2_TSTCLK | L2 test clock | AA20 | I | $OV_{DD}$ | 19 |
| $\overline{\text{LSSD_MODE}}$ | LSSD Mode | AC25 | I | $OV_{DD}$ | 19 |
| $\overline{\text{TEST_SEL}}$ | Test select | AA13 | I | $OV_{DD}$ | 19 |
| **Power Management** | | | | | |
| ASLEEP | Asleep | AG20 | O | $OV_{DD}$ | 9,16,22 |
| POWER_OK | Power OK | AC26 | I | $OV_{DD}$ | — |
| POWER_EN | Power enable | AE27 | O | $OV_{DD}$ | — |
| **Power and Ground Signals** | | | | | |
| OVDD | General I/O supply | Y18,AG2,AD4,AB16, AF6,AC18,AB13,AD10, AE14,AD16,AD25, AF27,AE22,AF11, AF20,AF24 | — | $OV_{DD}$ | — |
| LVDD | GMAC 1 I/O supply | AA7, AA4 | Power for TSEC1 interfaces | $LV_{DD}$ | — |
| TVDD | GMAC 3 I/O supply | V4,U7 | Power for TSEC3 interfaces | $TV_{DD}$ | — |
| GVDD | SSTL2 DDR supply | B1,B11,C7,C9,C14, C17,D4,D6,R3,D15,E2, E8,C24,E18,F5,E14, C21,G3,G7,G9,G11, H5,H12,E22,F15,J10, K3,K12,K14,H14,D20, E11,M1,N5 | Power for DDR DRAM I/O | $GV_{DD}$ | — |
| BVDD | Local bus I/O supply | L23,J18,J23,J19,F20, F23,H26,J21 | Power for Local Bus | $BV_{DD}$ | — |
| SVDD | SerDes 1 core logic supply | M27,N25,P28,R24, R26,T24,T27,U25, W24,W26,Y24,Y27, AA25,AB28,AD27 | — | $SV_{DD}$ | — |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| XVDD | SerDes 1 transceiver supply | M21,N23,P20,R22,T20, U23,V21,W22,Y20, AA23 | — | $XV_{DD}$ | — |
| S2VDD | SerDes 2 core logic supply | R6,N7,M9 | — | $S2V_{DD}$ | — |
| X2VDD | SerDes 2 transceiver supply | R11,N12,L11 | — | $X2V_{DD}$ | — |
| VDD_CORE | Core, L2 logic supply | P13,U16,L16,M15,N14, R14,P15,N16,M13, U14,T13,L14,T15,R16, K13 | — | $V_{DD_CORE}$ | — |
| VDD_PLAT | Platform logic supply | T19,T17,V17,U18,R18, N18,M19,P19,P17,M17 | — | $V_{DD_PLAT}$ | — |
| AVDD_CORE | CPU PLL supply | AH16 | — | $AV_{DD_CORE}$ | 20,28 |
| AVDD_PLAT | Platform PLL supply | AH18 | — | $AV_{DD_PLAT}$ | 20 |
| AVDD_DDR | DDR PLL supply | AH19 | — | $AV_{DD_DDR}$ | 20 |
| AVDD_LBIU | Local Bus PLL supply | C28 | — | $AV_{DD_LBIU}$ | 20 |
| AVDD_PCI1 | PCI PLL supply | AH20 | — | $AV_{DD_PCI1}$ | 20 |
| AVDD_SRDS | SerDes 1 PLL supply | W28 | — | $AV_{DD_SRDS}$ | 20 |
| AVDD_SRDS2 | SerDes 2 PLL supply | T1 | — | $AV_{DD_SRDS2}$ | 20 |
| SENSEVDD_CORE | — | V15 | — | $V_{DD_CORE}$ | 13 |
| SENSEVDD_PLAT | — | W17 | — | $V_{DD_PLAT}$ | 13 |
| GND | Ground | D5,AE7,F4,D26,D23, C12,C15,E20,D8,B10, AF3,E3,J14,K21,F8,A3, F16,E12,E15,D17,L1, F21,H1,G13,G15,G18, C6,A14,A7,G25,H4, C20,J12,J15,J17,F27, M5,J27,K11,L26,K7, K8,T14,V14,M16,M18, P14,N15,N17,N19,N2, P5,P16,P18,M14,R15, R17,R19,T16,T18,L17, U15,U17,U19,V18,C27, Y13,AE26,AA19,AE21, B28,AC11,AD19,AD23, L15,AD15,AG23,AE9, A27,V7,Y7,AC5,U4,Y4, AE12,AB9,AA14,N13, R13,L13 | — | — | — |
| XGND | SerDes 1Transceiver pad GND (xpadvss) | M20,M24,N22,P21, R23,T21,U22,V20, W23, Y21 | — | — | — |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| SGND | SerDes 1 Transceiver core logic GND (xcorevss) | M28,N26,P24,P27, R25,T28,U24,U26,V24, W25,Y28,AA24,AA26, AB24,AB27,AD28 | — | — | — |
| X2GND | SerDes 2 Transceiver pad GND (xpadvss) | R12,M10,N11,L12 | — | — | — |
| S2GND | SerDes 2 Transceiver core logic GND (xcorevss) | P8,P9,N6,M8 | — | — | — |
| AGND_SRDS | SerDes 1 PLL GND | V27 | — | — | — |
| AGND_SRDS2 | SerDes 2 PLL GND | T2 | — | — | — |
| SENSEVSS | GND Sensing | V16 | — | — | 13 |
| **Analog Signals** | | | | | |
| MVREF | SSTL2 reference voltage | A28 | Reference voltage for DDR | GVDD/2 | — |
| SD1_IMP_CAL_RX | Rx impedance calibration | M26 | — | 200Ω (±1%) to GND | — |
| SD1_IMP_CAL_TX | Tx impedance calibration | AE28 | — | 100Ω (±1%) to GND | — |
| SD1_PLL_TPA | PLL test point analog | V26 | — | AVDD_SRDS analog | 18 |
| SD2_IMP_CAL_RX | Rx impedance calibration | R7 | — | 200Ω (±1%) to GND | — |
| SD2_IMP_CAL_TX | Tx impedance calibration | L6 | — | 100Ω (±1%) to GND | — |
| SD2_PLL_TPA | PLL test point analog | T3 | — | AVDD_SRDS2 analog | 18 |
| Reserved | — | R4 | — | — | — |
| Reserved | — | R5 | — | — | — |
| **No Connect Pins** | | | | | |
| NC | — | C19,D7,D10,L10,R10, B6,F12,J7,P10,M25, W27,N24,N10,R8,J9, K9,V25,R9 | — | — | — |

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|

**Notes:**

1. All multiplexed signals may be listed only once and may not re-occur.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to $OV_{DD}$.
3. This pin must always be pulled-high.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 22.2, "CCB/SYSCLK PLL Ratio."
8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 22.3, "e500 Core PLL Ratio."
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
10. For proper state of these signals during reset, UART_SOUT[1] must be pulled down to GND through a resistor. UART_SOUT[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on UART_SOUT[0].
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the $V_{DD_CORE}$/$V_{DD_PLAT}$/GND planes internally and may be used by the core power supply to improve tracking and regulation.
15. These pins have other manufacturing or debug test functions. It's recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.
16. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
17. This pin is only an output in FIFO mode when used as Rx Flow Control.
18. Do not connect.
19. These must be pulled up (100 Ω- 1 kΩ) to OVDD.
20. Independent supplies derived from board VDD.
21. Recommend a pull-up resistor (1 KΩ) be placed on this pin to $OV_{DD}$.
22. The following pins must NOT be pulled down during power-on reset: MDVAL, UART_SOUT[0], EC_MDC, TSEC1_TXD[3], TSEC3_TXD[7], HRESET_REQ, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP.
23. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
24. General-Purpose POR configuration of user system.

**Table 1. Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|

25. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the address pins as “No Connect” or terminated through 2–10 KΩ pull-up resistors with the default of internal arbiter if the address pins are not connected to any other PCI device. The PCI block will drive the address pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
26. When operating in DDR2 mode, connect MDIC[0] to ground through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor, and connect MDIC[1] to GVDD through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect MDIC[0] to ground through an 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor, and connect MDIC[1] to GVDD through an 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
27. Connect to GND through a pull down 1 kΩ resistor.
28. It must be the same as VDD_CORE
29. The output pads are tristated and the receivers of pad inputs are disabled during the Deep Sleep state when GCR[DEEPSLEEP_Z] =1.
30. DDRCLK input is only required when the DDR controller is running in asynchronous mode. When the DDR controller is configured to run in synchronous mode via POR setting cfg_ddr_pll[0:2]=111, the DDRCLK input is not required. It is recommended to tie it off to GND when DDR controller is running in synchronous mode. See the *MPC8536E PowerQUICC III Integrated Host Processor Family Reference Manual* , Table 4-3 in section 4.2.2 “Clock Signals”, section 4.4.3.2 “DDR PLL Ratio” and Table 4-10 “DDR Complex Clock PLL Ratio” for more detailed description regarding DDR controller operation in asynchronous and synchronous modes.
31. EC_GTX_CLK125 is a 125-MHz input clock shared among all eTSEC ports in the following modes: GMII, TBI, RGMII and RTBI. If none of the eTSEC ports is operating in these modes, the EC_GTX_CLK125 input can be tied off to GND.
32. $\overline{\text{SDHC_WP}}$ is active low signal, which follows SDHC Host controller specification. However, it is reversed polarity for SD/MMC card specification.
33. Must connect to XGND.
34. Must connect to X2GND
35. For systems which boot from Local Bus(GPCM)-controlled NOR flash or (FCM) controlled NAND flash, a pullup on LGPL4 is required.

# 2 Electrical Characteristics

## 2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

## 2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

**Table 2. Absolute Maximum Ratings[1]**

| Characteristic | | Symbol | Max Value | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD_CORE}$ | –0.3 to 1.21 | V | — |
| Platform supply voltage | | $V_{DD_PLAT}$ | –0.3 to 1.1 | V | — |
| PLL core supply voltage | | $AV_{DD_CORE}$ | –0.3 to 1.21 | V | — |
| PLL other supply voltage | | $AV_{DD}$ | –0.3 to 1.1 | V | — |
| Core power supply for SerDes transceivers | | $SV_{DD}$, $S2V_{DD}$ | –0.3 to 1.1 | V | — |
| Pad power supply for SerDes transceivers and PCI Express | | $XV_{DD}$, $X2V_{DD}$ | –0.3 to 1.1 | V | — |
| DDR SDRAM Controller I/O supply voltage | DDR2 SDRAM Interface | $GV_{DD}$ | –0.3 to 1.98 | V | — |
| | DDR3 SDRAM Interface | | –0.3 to 1.65 | | |
| Three-speed Ethernet I/O | | $LV_{DD}$ (eTSEC1) | –0.3 to 3.63<br>–0.3 to 2.75 | V | 2 |
| | | $TV_{DD}$ (eTSEC3) | –0.3 to 3.63<br>–0.3 to 2.75 | V | 2 |
| PCI, DUART, system control and power management, $I^2C$, USB, eSDHC, eSPI and JTAG I/O voltage, MII management voltage | | $OV_{DD}$ | –0.3 to 3.63 | V | — |
| Local bus I/O voltage | | $BV_{DD}$ | –0.3 to 3.63<br>–0.3 to 2.75<br>–0.3 to 1.98 | V | — |
| Input voltage | DDR2/DDR3 DRAM signals | $MV_{IN}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 3 |
| | DDR2/DDR3 DRAM reference | $MV_{REF}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | — |
| | Three-speed Ethernet signals | $LV_{IN}$<br>$TV_{IN}$ | –0.3 to ($LV_{DD}$ + 0.3)<br>–0.3 to ($TV_{DD}$ + 0.3) | V | 3 |
| | Local bus signals | $BV_{IN}$ | –0.3 to ($BV_{DD}$ + 0.3) | — | — |
| | PCI, DUART, SYSCLK, system control and power management, $I^2C$, and JTAG signals | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3) | V | 3 |
| Storage temperature range | | $T_{STG}$ | –55 to 150 | $^0$C | — |

**Notes:**

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect chip reliability or cause permanent damage to the chip.
2. The 3.63-V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 2.9.2, “FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications,” for details on the recommended operating conditions per protocol.
3. (M,L,O)$V_{IN}$ and $MV_{REF}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

## 2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this chip. Note that the values in this table are the recommended and tested operating conditions. Proper chip operation outside these conditions is not guaranteed.

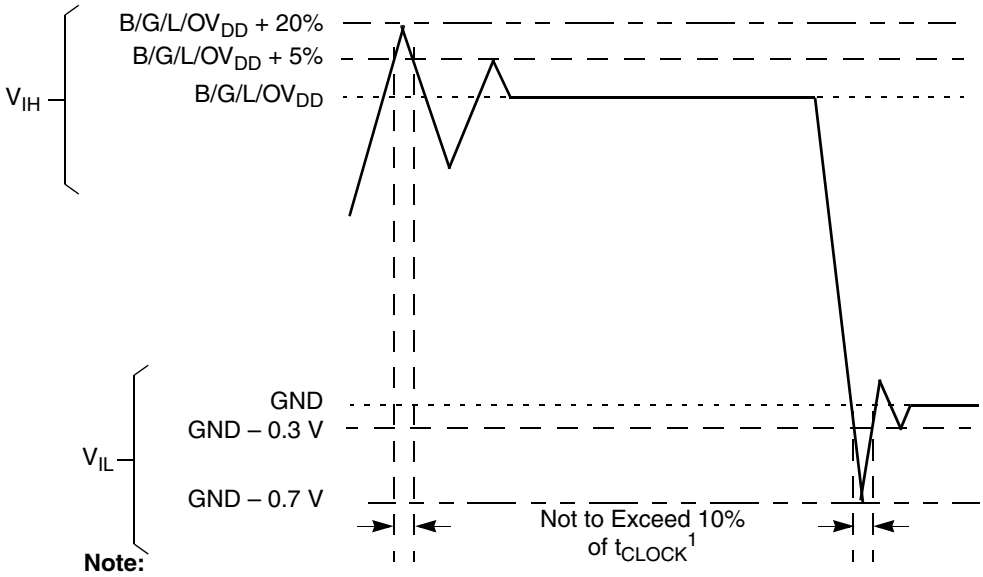
**Table 3. Recommended Operating Conditions**

| Characteristic | | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD_CORE}$ | 1.0 ± 50 mV | V | — |
| Platform supply voltage | | $V_{DD_PLAT}$ | 1.0 ± 50 mV | V | — |
| PLL core supply voltage | | $AV_{DD_CORE}$ | 1.0 ± 50 mV | V | 2 |
| PLL other supply voltage | | $AV_{DD}$ | 1.0 ± 50 mV | V | 2 |
| Core power supply for SerDes transceivers | | $SV_{DD}$ | 1.0 ± 50 mV | V | — |
| Pad power supply for SerDes transceivers and PCI Express | | $XV_{DD}$ | 1.0 ± 50 mV | V | — |
| DDR SDRAM Controller I/O supply voltage | DDR2 SDRAM Interface | $GV_{DD}$ | 1.8 V ± 90 mV | V | 3 |
| | DDR3 SDRAM Interface | | 1.5 V ± 75 mV | | |
| Three-speed Ethernet I/O voltage | | $LV_{DD}$ (eTSEC1) | 3.3 V ± 165 mV<br>2.5 V ± 125 mV | V | 5 |
| | | $TV_{DD}$ (eTSEC3) | 3.3 V ± 165 mV<br>2.5 V ± 125 mV | | |
| PCI, DUART, system control and power management, $I^2C$, USB, eSDHC, eSPI and JTAG I/O voltage, MII management voltage | | $OV_{DD}$ | 3.3 V ± 165 mV | V | 4 |
| Local bus I/O voltage | | $BV_{DD}$ | 3.3 V ± 165 mV<br>2.5 V ± 125 mV<br>1.8 V ± 90 mV | V | — |
| Input voltage | DDR2 and DDR3 SDRAM Interface signals | $MV_{IN}$ | GND to $GV_{DD}$ | V | 3 |
| | DDR2 and DDR3 SDRAM Interface reference | $MV_{REF}$ | $GV_{DD}/2$ ± 1% | V | — |
| | Three-speed Ethernet signals | $LV_{IN}$<br>$TV_{IN}$ | GND to $LV_{DD}$<br>GND to $TV_{DD}$ | V | 5 |
| | Local bus signals | $BV_{IN}$ | GND to $BV_{DD}$ | V | — |
| | PCI, Local bus, DUART, SYSCLK, system control and power management, $I^2C$, and JTAG signals | $OV_{IN}$ | GND to $OV_{DD}$ | V | 4 |
| Operating Temperature range | Commercial | $T_A$<br>$T_J$ | $T_A$= 0 (min) to<br>$T_J$= 90(max) | °C | 6 |
| | Industrial<br>standard temperature range | | $T_A$= 0 (min) to<br>$T_J$= 105 (max) | | |
| | Extended temperature range | | $T_A$= -40 (min) to<br>$T_J$= 105 (max) | | |

**Notes:**

2. This voltage is the input to the filter discussed in Section 3.2.1, "PLL Power Supply Filtering," and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter.
3. **Caution**: MVIN must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: OVIN must not exceed OVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution**: L/TVIN must not exceed L/TVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. Minimum temperature is specified with $T_A$; maximum temperature is specified with $T_J$.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.




**Note:**

1. $t_{CLOCK}$ refers to the clock period associated with the respective interface:
   For $I^2C$ and JTAG, $t_{CLOCK}$ references SYSCLK.
   For DDR, $t_{CLOCK}$ references MCLK.
   For eTSEC, $t_{CLOCK}$ references EC_GTX_CLK125.
   For eLBC, $t_{CLOCK}$ references LCLK.
   For PCI, $t_{CLOCK}$ references PCI1_CLK or SYSCLK.

2. With the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3).

**Figure 7. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$**

The core voltage must always be provided at nominal 1.0 V . (See Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. $OV_{DD}$ and $LV_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied MVREF*n* signal (nominally set to GVDD/2) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

### 2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

**Table 4. Output Drive Capability**

| Driver Type | Programmable Output Impedance (Ω) | Supply Voltage | Notes |
|---|---|---|---|
| Local bus interface utilities signals | 25<br>35 | $BV_{DD}$ = 3.3 V<br>$BV_{DD}$ = 2.5 V | 1 |
| | 45(default)<br>45(default)<br>125 | $BV_{DD}$ = 3.3 V<br>$BV_{DD}$ = 2.5 V<br>$BV_{DD}$ = 1.8 V | |
| PCI signals | 25 | $OV_{DD}$ = 3.3 V | 2 |
| | 42 (default) | | |
| DDR2 signal | 16<br>32 (half strength mode) | $GV_{DD}$ = 1.8 V | 3 |
| DDR3 signal | 20<br>40 (half strength mode) | $GV_{DD}$ = 1.5 V | 2 |
| TSEC signals | 42 | $LV_{DD}$ = 2.5/3.3 V | — |
| DUART, system control, JTAG | 42 | $OV_{DD}$ = 3.3 V | — |
| $I^2C$ | 150 | $OV_{DD}$ = 3.3 V | — |

**Notes:**

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI1_GNT1}}$ signal at reset.
3. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at $T_j$ = 105°C and at $GV_{DD}$ (min)

## 2.2 Power Sequencing

The chip requires its power rails to be applied in a specific sequence in order to ensure proper chip operation. These requirements are as follows for power up:

1. $V_{DD_PLAT}$, $V_{DD_CORE}$ (if POWER_EN is not used to control $V_{DD_CORE}$), $AV_{DD}$, $BV_{DD}$, $LV_{DD}$, $OV_{DD}$, $SV_{DD}$,$S2V_{DD}$, $TV_{DD}$, $XV_{DD}$ and $X2V_{DD}$
2. [Wait for POWER_EN to assert], then $V_{DD_CORE}$ (if POWER_EN is used to control $V_{DD_CORE}$)
3. $GV_{DD}$

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for $GV_{DD}$ is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for $GV_{DD}$ is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD platform supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the chip.

During the Deep Sleep state, the VDD core supply is removed. But all other power supplies remain applied. Therefore, there is no requirement to apply the VDD core supply before any other power rails when the silicon waking from Deep Sleep.

## 2.3 Power Characteristics

The estimated power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III chips is shown in the following table.

**Table 5. Power Dissipation [5]**

| Power Mode | Core Frequency | CCB Frequency | DDR Frequency | $V_{DD}$ Platform | $V_{DD}$ Core | Junction Temperature | Core Power | | Platform Power[9] | | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | (MHz) | (MHz) | (MHz) | (V) | (V) | (°C) | mean[7] | Max | mean[7] | Max | |
| Maximum (A) | 600 | 400 | 400 | 1.0 | 1.0 | 105 /90 | — | 4.1/3.3 | — | 4.7/3.7 | 1, 3, 8 |
| Thermal (W) | | | | | | | — | 3.7/2.9 | — | 4.7/3.7 | 1, 4, 8 |
| Typical (W) | | | | | | 65 | 1.5 | — | 1.5 | — | 1, 2 |
| Doze (W) | | | | | | | 1.2 | 1.9 | 1.4 | 1.9 | 1 |
| Nap (W) | | | | | | | 0.8 | 1.5 | 1.4 | 1.9 | 1 |
| Sleep (W) | | | | | | | 0.8 | 1.5 | 1.0 | 1.6 | 1 |
| Deep Sleep (W) | | | | | | 35 | 0 | 0 | 0.6 | 1.1 | 6 |
| Maximum (A) | 800 | 400 | 400 | 1.0 | 1.0 | 105 / 90 | — | 4.5/3.7 | — | 4.7/3.7 | 1, 3, 8 |
| Thermal (W) | | | | | | | — | 3.9/3.1 | — | 4.7/3.7 | 1, 4, 8 |
| Typical (W) | | | | | | 65 | 1.7 | — | 1.5 | — | 1, 2 |
| Doze (W) | | | | | | | 1.3 | 2.1 | 1.4 | 1.9 | 1 |
| Nap (W) | | | | | | | 0.8 | 1.5 | 1.4 | 1.9 | 1 |
| Sleep (W) | | | | | | | 0.8 | 1.5 | 1.0 | 1.6 | 1 |
| Deep Sleep (W) | | | | | | 35 | 0 | 0 | 0.6 | 1.1 | 1,6 |
| Maximum (A) | 1000 | 400 | 400 | 1.0 | 1.0 | 105 / 90 | — | 4.8/4.0 | — | 4.7/3.7 | 1, 3, 8 |
| Thermal (W) | | | | | | | — | 4.1/3.3 | — | 4.7/3.7 | 1, 4, 8 |
| Typical (W) | | | | | | 65 | 1.9 | — | 1.5 | — | 1, 2 |
| Doze (W) | | | | | | | 1.4 | 2.2 | 1.4 | 1.9 | 1 |
| Nap (W) | | | | | | | 0.8 | 1.6 | 1.4 | 1.9 | 1 |
| Sleep (W) | | | | | | | 0.8 | 1.6 | 1.0 | 1.6 | 1 |
| Deep Sleep (W) | | | | | | 35 | 0 | 0 | 0.6 | 1.1 | 1, 6 |

**Table 5. Power Dissipation (continued)[5]**

| Power Mode | Core Frequency (MHz) | CCB Frequency (MHz) | DDR Frequency (MHz) | $V_{DD}$ Platform (V) | $V_{DD}$ Core (V) | Junction Temperature (°C) | Core Power mean[7] | Core Power Max | Platform Power[9] mean[7] | Platform Power[9] Max | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Maximum (A) | 1250 | 500 | 500 | 1.0 | 1.0 | 105 / 90 | — | 5.3/4.4 | — | 5.0/4.0 | 1, 3, 8 |
| Thermal (W) | | | | | | | — | 4.4/3.6 | — | 5.0/4.0 | 1, 4, 8 |
| Typical (W) | | | | | | 65 | 2.2 | | 1.7 | | 1 |
| Doze (W) | | | | | | | 1.6 | 2.4 | 1.5 | 2.1 | 1 |
| Nap (W) | | | | | | | 0.8 | 1.6 | 1.5 | 2.1 | 1 |
| Sleep (W) | | | | | | | 0.8 | 1.6 | 1.1 | 1.7 | 1 |
| Deep Sleep (W) | | | | | | 35 | 0 | 0 | 0.6 | 1.2 | 1, 6 |

**Notes:**

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage ($V_{DD}$) and 65°C junction temperature (see Table 3) while running the Dhrystone benchmark.
3. Maximum power is the maximum power measured with the worst process and recommended core and platform voltage ($V_{DD}$) at maximum operating junction temperature (see Table 3) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.
4. Thermal power is the maximum power measured with worst case process and recommended core and platform voltage ($V_{DD}$) at maximum operating junction temperature (see Table 3) while running the Dhrystone benchmark.
6. Maximum power is the maximum number measured with USB1, eTSEC1, and DDR blocks enabled. The Mean power is the mean power measured with only external interrupts enabled and DDR in self refresh.
7. Mean power is provided for information purposes only and is the mean power consumed by a statistically significant range of devices.
8. Maximum operating junction temperature (see Table 3) for Commercial Tier is 90 $^0$C, for Industrial Tier is 105 $^0$C.
9. Platform power is the power supplied to all the $V_{DD_PLAT}$ pins.

See Section 2.23.6.1, "SYSCLK to Platform Frequency Options," for the full range of CCB frequencies that the chip supports.

# 2.4 Input Clocks

## 2.4.1 System Clock Timing

This table provides the system clock (SYSCLK) AC timing specifications for the chip.

**Table 6. SYSCLK AC Timing Specifications**

At recommended operating conditions (see Table 2) with $OV_{DD}$ = 3.3 V ± 165 mV.

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SYSCLK frequency | $f_{SYSCLK}$ | 33 | — | 133 | MHz | 1 |
| SYSCLK cycle time | $t_{SYSCLK}$ | 7.5 | — | 30 | ns | — |
| SYSCLK rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 1.0 | 2.1 | ns | 2 |
| SYSCLK duty cycle | $t_{KHK}/t_{SYSCLK}$ | 40 | — | 60 | % | — |
| SYSCLK jitter | — | — | — | +/-150 | ps | 3, 4 |

**Notes:**
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 2.23.2, "CCB/SYSCLK PLL Ratio," and Section 2.23.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
3. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
4. For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 KHz and 60 KHz on SYSCLK.

## 2.4.2 PCI Clock Timing

When the PCI controller is configured for asynchronous operation, the reference clock for the PCI controller is not the SYSCLK input, but instead the PCI_CLK. This table provides the PCI reference clock AC timing specifications for the chip.

**Table 7. PCICLK AC Timing Specifications**

At recommended operating conditions (see Table 2) with $OV_{DD}$ = 3.3 V ± 165 mV.

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| PCICLK frequency | $f_{PCICLK}$ | 33 | — | 66 | MHz | — |
| PCICLK cycle time | $t_{PCICLK}$ | 15 | — | 30 | ns | — |
| PCICLK rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 1.0 | 2.1 | ns | 1 |
| PCICLK duty cycle | $t_{KHK}/t_{PCICLK}$ | 40 | — | 60 | % | — |

**Notes:**
1. Rise and fall times for PCICLK are measured at 0.6 V and 2.7 V.

## 2.4.3 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

## 2.4.4 eTSEC Gigabit Reference Clock Timing

This table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the chip.

**Table 8. EC_GTX_CLK125 AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC_GTX_CLK125 frequency | $f_{G125}$ | — | 125 | — | MHz | — |
| EC_GTX_CLK125 cycle time | $t_{G125}$ | — | 8 | — | ns | — |
| EC_GTX_CLK rise and fall time<br>$LV_{DD}$, $TV_{DD}$ = 2.5V<br>$LV_{DD}$, $TV_{DD}$ = 3.3V | $t_{G125R}/t_{G125F}$ | — | — | <br>0.75<br>1.0 | ns | 1 |
| EC_GTX_CLK125 duty cycle<br>GMII, TBI<br>1000Base-T for RGMII, RTBI | $t_{G125H}/t_{G125}$ | <br>45<br>47 | — | <br>55<br>53 | % | 2 |

**Notes:**

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for L/TVDD=2.5V, and from 0.6 and 2.7V for L/TVDD=3.3V at 0.6 V and 2.7 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 2.9.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

## 2.4.5 DDR Clock Timing

This table provides the DDR clock (DDRCLK) AC timing specifications for the chip.

**Table 9. DDRCLK AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3V ± 5%.

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| DDRCLK frequency | $f_{DDRCLK}$ | 66 | — | 166 | MHz | 1 |
| DDRCLK cycle time | $t_{DDRCLK}$ | 6.0 | — | 15.15 | ns | — |
| DDRCLK rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 1.0 | 1.2 | ns | 2 |
| DDRCLK duty cycle | $t_{KHK}/t_{DDRCLK}$ | 40 | — | 60 | % | — |
| DDRCLK jitter | — | — | — | +/– 150 | ps | 3, 4 |

**Notes:**

1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. See Section 2.23.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
3. The DDRCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
4. For spread spectrum clocking, guidelines are +0% to –1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

### 2.4.6 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed. The “platform clock (CCB) frequency” in the following formula refers to the maximum platform (CCB) frequency of the speed bins the part belongs to, which is defined in Table 73.

For FIFO GMII mode:

FIFO TX/RX clock frequency <= platform clock frequency/3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz

For FIFO encoded mode:

FIFO TX/RX clock frequency <= platform clock frequency/3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz

### 2.4.7 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

## 2.5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the chip. This table provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

**Table 10. RESET Initialization Timing Specifications**

| Parameter/Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Required assertion time of $\overline{\text{HREST}}$ | 100 | — | μs | — |
| Minimum assertion time for $\overline{\text{SRESET}}$ | 3 | — | Sysclk | 1 |
| PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation | 100 | — | μs | — |
| Input setup time for POR configurations (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$ | 4 | — | SYSCLKs | 1 |
| Input hold time for all POR configurations (including PLL config) with respect to negation of $\overline{\text{HRESET}}$ | 2 | — | SYSCLKs | 1 |
| Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{HRESET}}$ | — | 5 | SYSCLKs | 1 |
| $\overline{\text{HRESET}}$ rise time | — | 1 | SYSCLK | — |

**Notes:**

1. SYSCLK is the primary clock input for the chip.

This table provides the PLL lock times.

**Table 11. PLL Lock Times**

| Parameter/Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|
| PLL lock times | — | 100 | μs | — |
| Local bus PLL | — | 50 | μs | — |
| PCI bus lock time | — | 50 | μs | — |

## 2.6 DDR2 and DDR3 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the chip. Note that DDR2 SDRAM is $GV_{DD}$(type) = 1.8 V and DDR3 SDRAM is $GV_{DD}$(type) = 1.5 V.

### 2.6.1 DDR2 and DDR3 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM component(s) of the chip when interfacing to DDR2 SDRAM.

**Table 12. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}$(typ) = 1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O supply voltage | $GV_{DD}$ | 1.7 | 1.9 | V | 1 |
| I/O reference voltage | $MV_{REF}$ | 0.49 × $GV_{DD}$ | 0.51 × $GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | $MV_{REF}$ – 0.04 | $MV_{REF}$ + 0.04 | V | 3 |
| Input high voltage | $V_{IH}$ | $MV_{REF}$+ 0.125 | $GV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | $MV_{REF}$ – 0.125 | V | — |
| Output leakage current | $I_{OZ}$ | –50 | 50 | μA | 4 |
| Output high current ($V_{OUT}$ = 1.420 V) | $I_{OH}$ | –13.4 | — | mA | — |
| Output low current ($V_{OUT}$ = 0.280 V) | $I_{OL}$ | 13.4 | — | mA | — |

**Notes:**
1. $GV_{DD}$ is expected to be within 50 mV of the DRAM $GV_{DD}$ at all times.
2. $MV_{REF}$ is expected to be equal to 0.5 × $GV_{DD}$, and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}$ may not exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the chip. It is the supply to which far end signal termination is made and is expected to be equal to $MV_{REF}$. This rail should track variations in the DC level of $MV_{REF}$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ $GV_{DD}$.

This table provides the recommended operating conditions for the DDR SDRAM controller of the chip when interfacing to DDR3 SDRAM.

**Table 13. DDR3 SDRAM Interface DC Electrical Characteristics for $GV_{DD}$(typ) = 1.5 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O supply voltage | $GV_{DD}$ | 1.425 | 1.575 | V | 1 |
| I/O reference voltage | $MV_{REF}n$ | 0.49 × $GV_{DD}$ | 0.51 × $GV_{DD}$ | V | 2 |
| Input high voltage | $V_{IH}$ | $MV_{REF}n$ + 0.100 | $GV_{DD}$ | V | — |
| Input low voltage | $V_{IL}$ | GND | $MV_{REF}n$ – 0.100 | V | — |
| Output leakage current | $I_{OZ}$ | –50 | 50 | μA | 3 |

**Notes:**
1. $GV_{DD}$ is expected to be within 50 mV of the DRAM $GV_{DD}$ at all times.
2. $MV_{REF}n$ is expected to be equal to 0.5 × $GV_{DD}$, and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±1% of the DC value.
3. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ $GV_{DD}$.

This table provides the DDR capacitance when $GV_{DD}$(type) = 1.8 V.

**Table 14. DDR2 SDRAM Capacitance for $GV_{DD}$(typ)=1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{IO}$ | 6 | 8 | pF | 1, 2 |
| Delta input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{DIO}$ | — | 0.5 | pF | 1, 2 |

**Note:**
1. This parameter is sampled. $GV_{DD}$ = 1.8 V ± 0.090 V (for DDR2), f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = $GV_{DD}$/2, $V_{OUT}$ (peak-to-peak) = 0.2 V.
2. This parameter is sampled. $GV_{DD}$ = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = $GV_{DD}$/2, $V_{OUT}$ (peak-to-peak) = 0.175 V.

This table provides the current draw characteristics for $MV_{REF}$.

**Table 15. Current Draw Characteristics for $MV_{REF}$**

| Parameter/Condition | | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Current draw for $MV_{REF}n$ | DDR2 SDRAM | $I_{MVREFn}$ | — | 1500 | μA | 1 |
| | DDR3 SDRAM | | | 1250 | | |

1.The voltage regulator for $MV_{REF}$ must be able to supply up to 1500 μA or 1250 uA current for DDR2 or DDR3 respectively.

## 2.6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM Controller interface. The DDR controller supports both DDR2 and DDR3 memories. Please note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 667 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this document.

### 2.6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

These tables provide the input AC timing specifications for the DDR controller.

**Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface**

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5%

| Parameter | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| AC input low voltage | 667 | $V_{ILAC}$ | — | $MV_{REF}$ – 0.20 | V |
| | <=533 | | — | $MV_{REF}$ – 0.25 | V |
| AC input high voltage | 667 | $V_{IHAC}$ | $MV_{REF}$ + 0.20 | — | V |
| | <=533 | | $MV_{REF}$ + 0.25 | — | V |

### Table 17. DDR3 SDRAM Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with $GV_{DD}$ of 1.5 V ± 5%. DDR3 data rate is between 606MHz and 667MHz.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | $MV_{REF}$ – 0.175 | V | — |
| AC input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.175 | — | V | — |

### Table 18. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Controller Skew for MDQS—MDQ/MECC | $t_{CISKEW}$ | — | — | ps | 1, 2 |
| 667 MHz | — | –240 | 240 | — | 3 |
| 533 MHz | — | –300 | 300 | — | — |
| 400 MHz | — | –365 | 365 | — | — |

**Note:**

1. $t_{CISKEW}$ represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called $t_{DISKEW}$. This can be determined by the following equation: $t_{DISKEW}$ =+/-(T/4 - abs($t_{CISKEW}$)) where T is the clock period and abs($t_{CISKEW}$) is the absolute value of $t_{CISKEW}$.
3. Maximum DDR2 and DDR3 frequency is 667MHz.

This figure shows the DDR2 and DDR3 SDRAM interface input timing diagram.

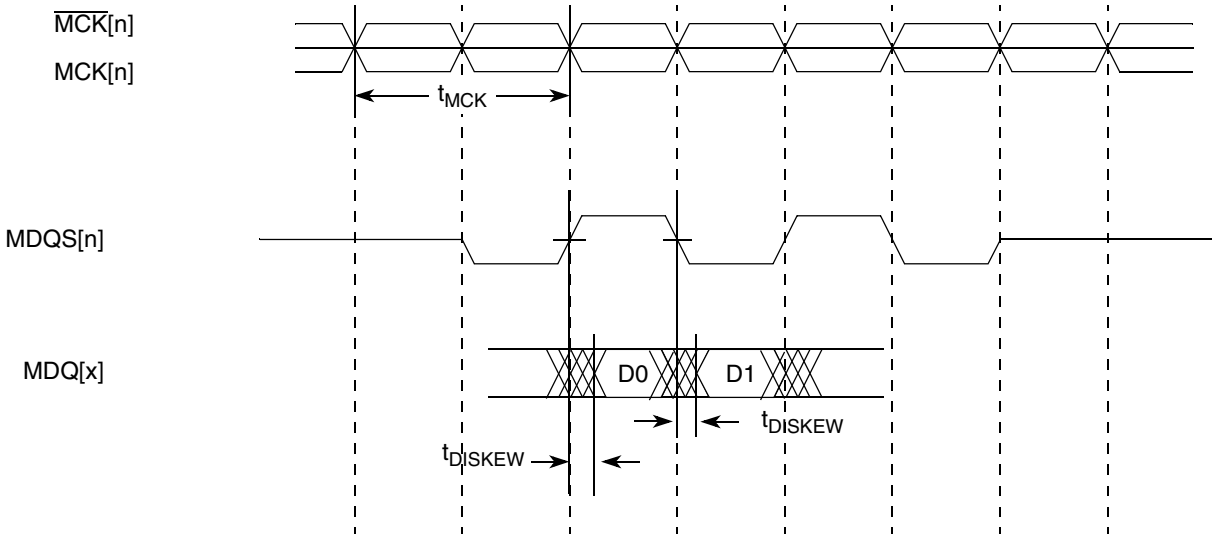



**Figure 8. DDR SDRAM Input Timing Diagram**

### 2.6.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

This table contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

**Table 19. DDR SDRAM Output AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing | $t_{MCK}$ | 3.0 | 5 | ns | 2 |
| ADDR/CMD output setup with respect to MCK | $t_{DDKHAS}$ | | | ns | 3 |
| 667 MHz | | 1.10 | — | | 7 |
| 533 MHz | | 1.48 | — | | |
| 400 MHz | | 1.95 | — | | |
| ADDR/CMD output hold with respect to MCK | $t_{DDKHAX}$ | | | ns | 3 |
| 667 MHz | | 1.10 | — | | 7 |
| 533 MHz | | 1.48 | — | | |
| 400 MHz | | 1.95 | — | | |
| $\overline{\text{MCS}}$[n] output setup with respect to MCK | $t_{DDKHCS}$ | | | ns | 3 |
| 667 MHz | | 1.10 | — | | 7 |
| 533 MHz | | 1.48 | — | | |
| 400 MHz | | 1.95 | — | | |
| $\overline{\text{MCS}}$[n] output hold with respect to MCK | $t_{DDKHCX}$ | | | ns | 3 |
| 667 MHz | | 1.10 | — | | 7 |
| 533 MHz | | 1.48 | — | | |
| 400 MHz | | 1.95 | — | | |
| MCK to MDQS Skew | $t_{DDKHMH}$ | | | ns | 4 |
| <= 667 MHz | | –0.6 | 0.6 | | 7 |
| MDQ/MECC/MDM output setup with respect to MDQS | $t_{DDKHDS}$, $t_{DDKLDS}$ | | | ps | 5 |
| 667 MHz | | 450 | — | | 7 |
| 533 MHz | | 538 | — | | |
| 400 MHz | | 700 | — | | |
| MDQ/MECC/MDM output hold with respect to MDQS | $t_{DDKHDX}$, $t_{DDKLDX}$ | | | ps | 5 |
| 667 MHz | | 450 | — | | 7 |
| 533 MHz | | 538 | — | | |
| 400 MHz | | 700 | — | | |
| MDQS preamble start | $t_{DDKHMP}$ | | | ns | 6 |

**Table 19. DDR SDRAM Output AC Timing Specifications (continued)**

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| <= 667 MHz | | $0.9 \times t_{MCK}$ | | | 7 |
| MDQS epilogue end | $t_{DDKHME}$ | | | ns | 6 |
| <= 667 MHz | | $0.4 \times t_{MCK}$ | $0.6 \times t_{MCK}$ | | 7 |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that $t_{DDKHMP}$ follows the symbol conventions described in note 1.
7. Maximum DDR2 and DDR3 frequency is 667 MHz

**NOTE**

For the ADDR/CMD setup and hold specifications in Table 19, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.

This figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement ($t_{DDKHMH}$).

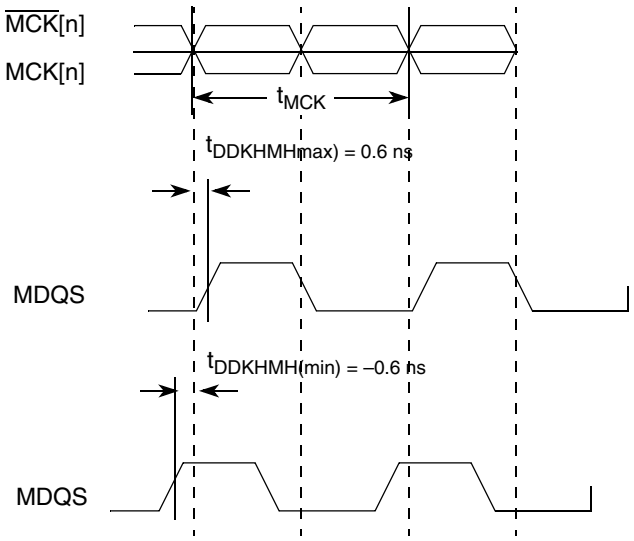



**Figure 9. Timing Diagram for tDDKHMH**

This figure shows the DDR SDRAM output timing diagram.

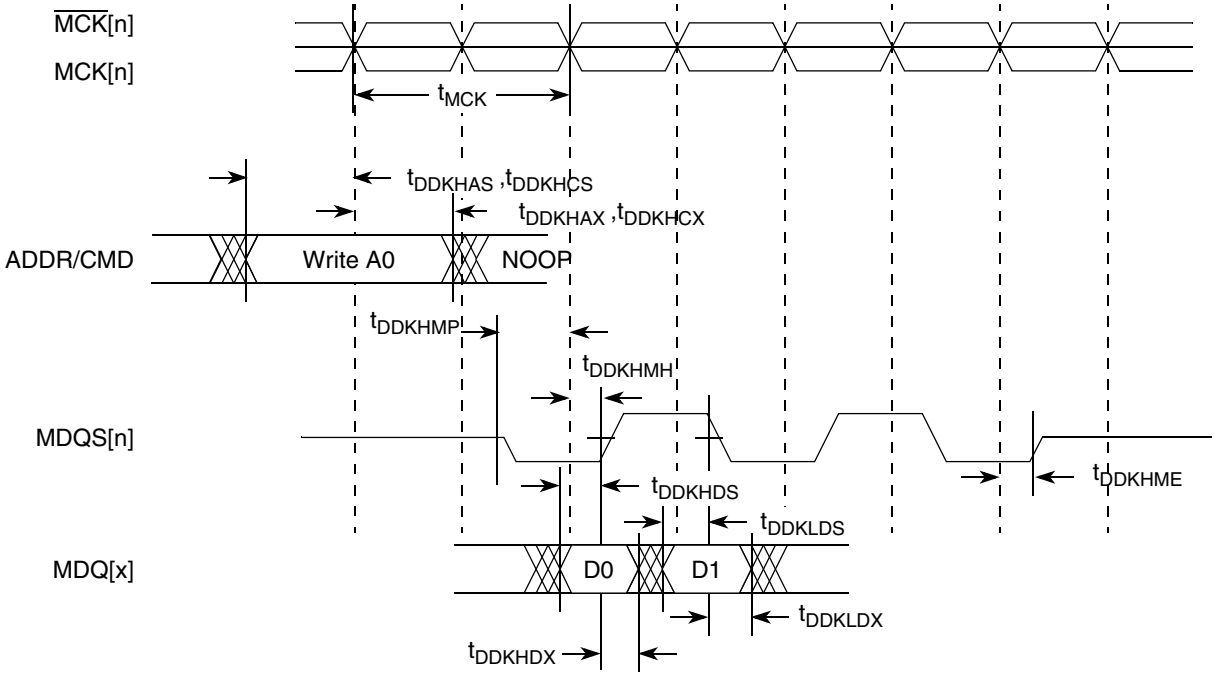



**Figure 10. DDR SDRAM Output Timing Diagram**

This figure provides the AC test load for the DDR bus.

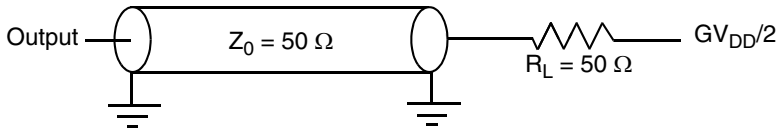



**Figure 11. DDR AC Test Load**

## 2.7 eSPI

This section describes the DC and AC electrical specifications for the eSPI of the chip.

### 2.7.1 eSPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the chip eSPI.

**Table 20. SPI DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –6.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 6.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | 0 V ≤ $V_{IN}$ ≤ $OV_{DD}$ | — | ±10 | μA |

### 2.7.2 eSPI AC Timing Specifications

This table and provide the eSPI input and output AC timing specifications.

**Table 21. SPI AC Timing Specifications[1]**

| Characteristic | Symbol [2] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| SPI_MOSI output—Master data hold time | $t_{NIKHOX}$ | 0.5 | — | ns | 3 |
| | $t_{NIKHOX}$ | 4.0 | | | 4 |
| SPI_MOSI output—Master data delay | $t_{NIKHOV}$ | — | 6.0 | ns | 3 |
| | $t_{NIKHOV}$ | | 7.4 | | 4 |
| SPI_CS outputs—Master data hold time | $t_{NIKHOX2}$ | 0 | — | ns | — |

**Table 21. SPI AC Timing Specifications[1] (continued)**

| Characteristic | Symbol [2] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| SPI_CS outputs—Master data delay | $t_{NIKHOV2}$ | — | 6.0 | ns | — |
| SPI inputs—Master data input setup time | $t_{NIIVKH}$ | 5 | — | ns | — |
| SPI inputs—Master data input hold time | $t_{NIIXKH}$ | 0 | — | ns | — |

**Notes:**

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{NIKHOV}$ symbolizes the NMSI outputs internal timing (NI) for the time $t_{SPI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
3. SPCOM[RxDelay] is set to 0.
4. SPCOM[RxDelay] is set to 1.

This figure provides the AC test load for the SPI.

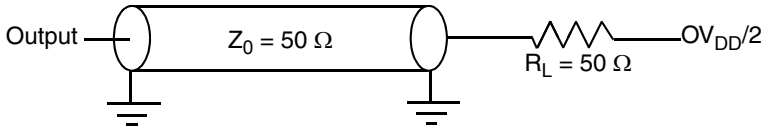
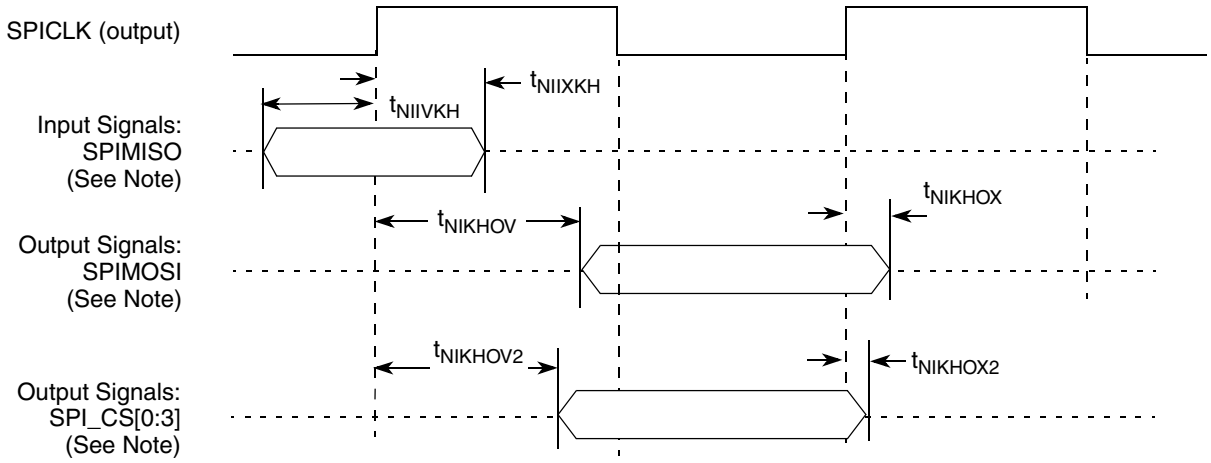



**Figure 12. SPI AC Test Load**

This figure represents the AC timing from Table 21. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.




**Note:** The clock edge is selectable on SPI.

**Figure 13. SPI AC Timing in Master mode (Internal Clock) Diagram**

## 2.8 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the chip.

### 2.8.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

**Table 22. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | – 0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V |

**Note:**

1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

### 2.8.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

**Table 23. DUART AC Timing Specifications**

| Parameter | Value | Unit | Notes |
|---|---|---|---|
| Minimum baud rate | CCB clock/1,048,576 | baud | 2 |
| Maximum baud rate | CCB clock/16 | baud | 2,3 |
| Oversample rate | 16 | — | 4 |

**Notes:**

2. CCB clock refers to the platform clock.
3. Actual attainable baud rate will be limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8$^{th}$ sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16$^{th}$ sample.

## 2.9 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

## 2.9.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps) — FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all FIFO mode, gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC), and serial gigabit media independent interface (SGMII). The RGMII, RTBI and FIFO mode interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can operate at 3.3V.

The GMII, MII, or TBI interface timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in Section 2.10, "Ethernet Management Interface Electrical Characteristics."

The electrical characteristics for SGMII is specified in Section 2.9.3, "SGMII Interface Electrical Characteristics." The SGMII interface conforms (with exceptions) to the Serial-GMII Specification Version 1.8.

### 2.9.1.1 GMII, MII, TBI, RGMII, RMII and RTBI DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in the following tables. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

**Table 24. GMII, MII, RMII, and TBI DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage 3.3 V | $LV_{DD}$<br>$TV_{DD}$ | 3.13 | 3.47 | V | 1, 2 |
| Output high voltage ($LV_{DD}/TV_{DD}$ = Min, IOH = –4.0 mA) | VOH | 2.40 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Output low voltage ($LV_{DD}/TV_{DD}$ = Min, IOL = 4.0 mA) | VOL | GND | 0.50 | V | — |
| Input high voltage | $V_{IH}$ | 1.90 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | 0.90 | V | — |
| Input high current ($V_{IN}$ = $LV_{DD}$, $V_{IN}$ = $TV_{DD}$) | $I_{IH}$ | — | 40 | μA | 1, 2,3 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –600 | — | μA | 3 |

**Notes:**

1 $LV_{DD}$ supports eTSECs 1.
2 $TV_{DD}$ supports eTSECs 3.
3 The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbols referenced in Table 1 and Table 2.

**Table 25. RGMII, RTBI, and FIFO DC Electrical Characteristics**

| Parameters | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage 2.5 V | $LV_{DD}/TV_{DD}$ | 2.37 | 2.63 | V | 1,2 |
| Output high voltage ($LV_{DD}/TV_{DD}$ = Min, IOH = –1.0 mA) | $V_{OH}$ | 2.00 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Output low voltage ($LV_{DD}/TV_{DD}$ = Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | GND – 0.3 | 0.40 | V | — |
| Input high voltage | $V_{IH}$ | 1.70 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | 0.70 | V | — |
| Input high current ($V_{IN}$ = $LV_{DD}$, $V_{IN}$ = $TV_{DD}$) | $I_{IH}$ | — | 10 | μA | 1, 2,3 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –15 | — | μA | 3 |

**Note:**

1 $LV_{DD}$ supports eTSECs 1.

2 $TV_{DD}$ supports eTSECs 3.

3 Note that the symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbols referenced in Table 1 and Table 2.

## 2.9.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

### 2.9.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 2.4.6, "Platform to FIFO Restrictions."

A summary of the FIFO AC specifications appears in the following tables.

**Table 26. FIFO Mode Transmit AC Timing Specification**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK, GTX_CLK clock period[2] | $t_{FIT}$ | 6.0 | 8.0 | 100 | ns |
| TX_CLK, GTX_CLK duty cycle | $t_{FITH}$ | 45 | 50 | 55 | % |
| TX_CLK, GTX_CLK peak-to-peak jitter | $t_{FITJ}$ | — | — | 250 | ps |

**Table 26. FIFO Mode Transmit AC Timing Specification (continued)**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Rise time TX_CLK (20%–80%) | $t_{FITR}$ | — | — | 0.75 | ns |
| Fall time TX_CLK (80%–20%) | $t_{FITF}$ | — | — | 0.75 | ns |
| GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time | $t_{FITDX}$[1] | 0.5 | — | 3.0 | ns |

**Note:**

1. Data valid $t_{FITDV}$ to GTX_CLK Min Setup time is a function of clock period and max hold time. (Min Setup = Cycle time – Max Hold)
2. The minimum cycle period (or maximum frequency) of the RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See Section 2.4.6, "Platform to FIFO Restrictions," for more detailed description.

**Table 27. FIFO Mode Receive AC Timing Specification**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period[1] | $t_{FIR}$ | 6.0 | 8.0 | 100 | ns |
| RX_CLK duty cycle | $t_{FIRH}/t_{FIRH}$ | 45 | 50 | 55 | % |
| RX_CLK peak-to-peak jitter | $t_{FIRJ}$ | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | $t_{FIRR}$ | — | — | 0.75 | ns |
| Fall time RX_CLK (80%–20%) | $t_{FIRF}$ | — | — | 0.75 | ns |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{FIRDV}$ | 1.5 | — | — | ns |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{FIRDX}$ | 0.5 | — | — | ns |

**Note:**

1. The minimum cycle period (or maximum frequency) of the RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See Section 2.4.6, "Platform to FIFO Restrictions," for more detailed description.

Timing diagrams for FIFO appear in the following figures.

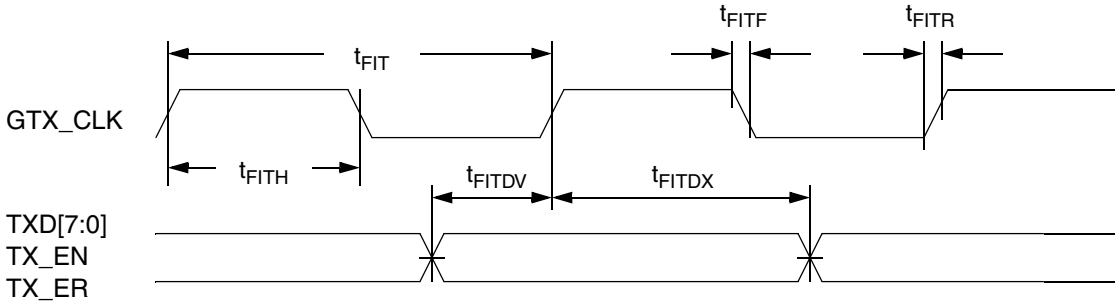



**Figure 14. FIFO Transmit AC Timing Diagram**

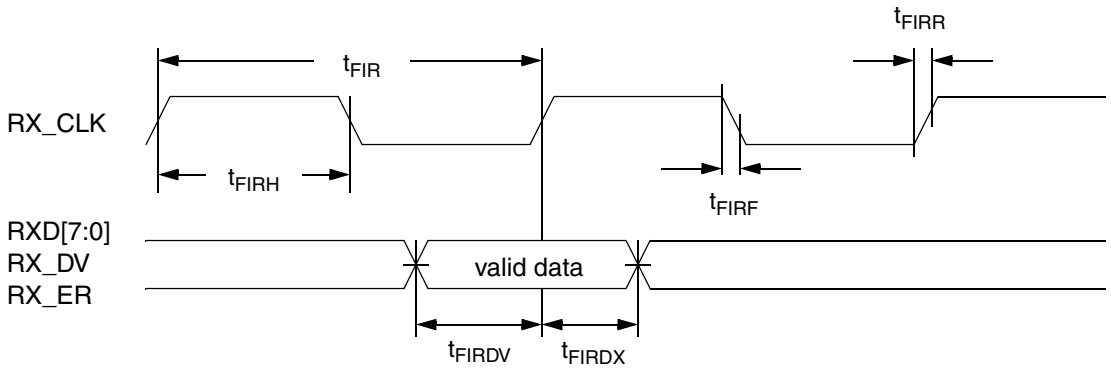



**Figure 15. FIFO Receive AC Timing Diagram**

### 2.9.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

#### 2.9.2.2.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

**Table 28. GMII Transmit AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| GTX_CLK clock period | $t_{GTK}$ | — | 8.0 | — | ns |
| GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay | $t_{GTKHDX}$[3] | 0.5 | — | 5.0 | ns |
| GTX_CLK data clock rise time (20%-80%) | $t_{GTXR}$ | — | — | 1.0 | ns |
| GTX_CLK data clock fall time (80%-20%) | $t_{GTXF}$ | — | — | 1.0 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GTKHDV}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, $t_{GTKHDX}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GTX}$ represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Data valid $t_{GTKHDV}$ to GTX_CLK Min Setup time is a function of clock period and max hold time. (Min Setup = Cycle time - Max Hold)

This figure shows the GMII transmit AC timing diagram.

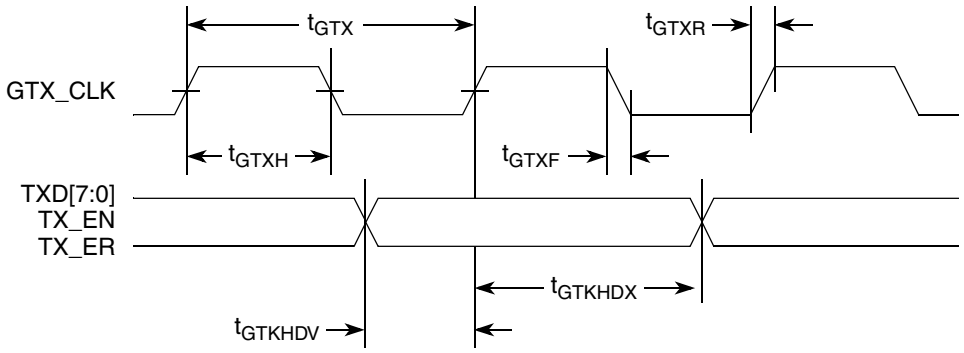



**Figure 16. GMII Transmit AC Timing Diagram**

### 2.9.2.2.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

**Table 29. GMII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{GRX}$ | — | 8.0 | — | ns |
| RX_CLK duty cycle | $t_{GRXH}/t_{GRX}$ | 35 | — | 65 | % |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{GRDVKH}$ | 2.0 | — | — | ns |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{GRDXKH}$ | 0 | — | — | ns |
| RX_CLK clock rise (20%-80%) | $t_{GRXR}$ | — | — | 1.0 | ns |
| RX_CLK clock fall time (80%-20%) | $t_{GRXF}$ | — | — | 1.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GRDVKH}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{RX}$ clock reference (K) going to the high state (H) or setup time. Also, $t_{GRDXKL}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{GRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GRX}$ represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

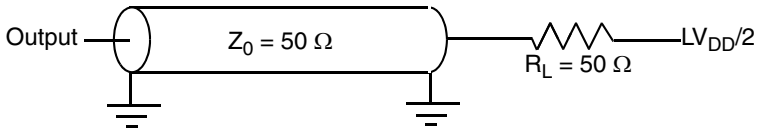



**Figure 17. eTSEC AC Test Load**

This figure shows the GMII receive AC timing diagram.

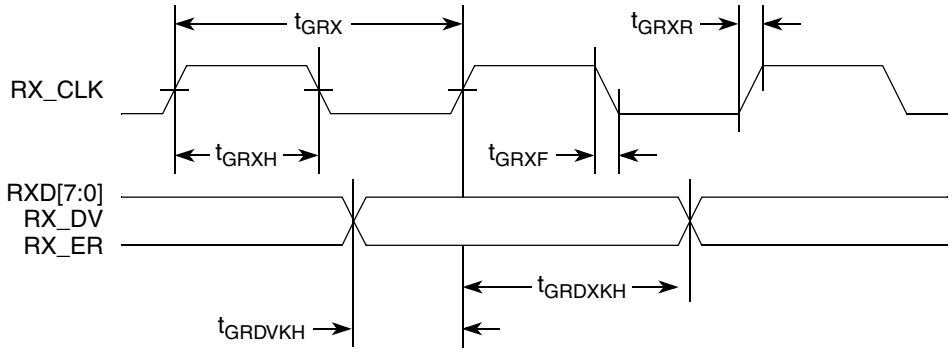



**Figure 18. GMII Receive AC Timing Diagram**

### 2.9.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

#### 2.9.2.3.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

**Table 30. MII Transmit AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK clock period 10 Mbps | $t_{MTX}$ | — | 400 | — | ns |
| TX_CLK clock period 100 Mbps | $t_{MTX}$ | — | 40 | — | ns |
| TX_CLK duty cycle | $t_{MTXH}/t_{MTX}$ | 35 | — | 65 | % |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | $t_{MTKHDX}$ | 1 | 5 | 15 | ns |
| TX_CLK data clock rise (20%-80%) | $t_{MTXR}$ | 1.0 | — | 4.0 | ns |
| TX_CLK data clock fall (80%-20%) | $t_{MTXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

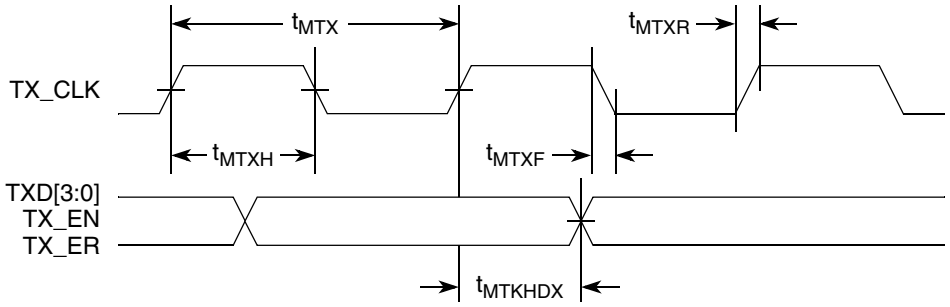



**Figure 19. MII Transmit AC Timing Diagram**

### 2.9.2.3.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

**Table 31. MII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period 10 Mbps | $t_{MRX}$ | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | $t_{MRX}$ | — | 40 | — | ns |
| RX_CLK duty cycle | $t_{MRXH}/t_{MRX}$ | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$ | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | $t_{MRDXKH}$ | 10.0 | — | — | ns |
| RX_CLK clock rise (20%–80%) | $t_{MRXR}$ | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time (80%–20%) | $t_{MRXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

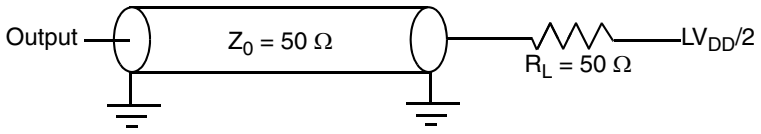



**Figure 20. eTSEC AC Test Load**

This figure shows the MII receive AC timing diagram.

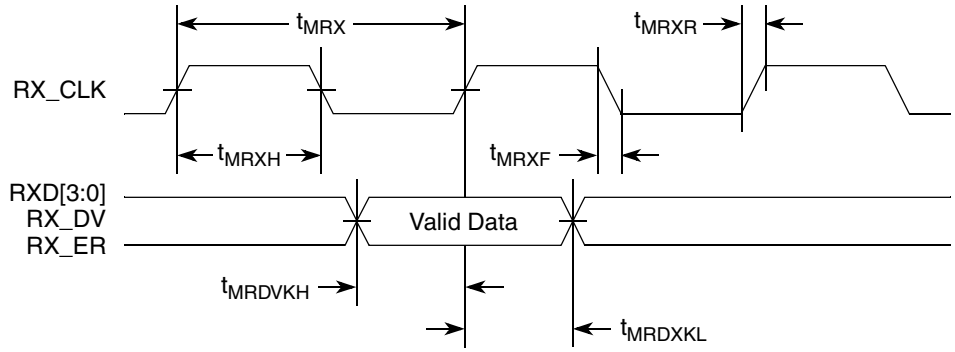



**Figure 21. MII Receive AC Timing Diagram**

## 2.9.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

### 2.9.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

**Table 32. TBI Transmit AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| GTX_CLK clock period | $t_{TTX}$ | — | 8.0 | — | ns |
| GTX_CLK duty cycle | $t_{TTXH}/t_{TTX}$ | 40 | — | 60 | % |
| GTX_CLK to TCG[9:0] delay time | $t_{TTKHDX}$[2] | 1.0 | — | 5.0 | ns |
| GTX_CLK rise (20%–80%) | $t_{TTXR}$ | — | — | 1.0 | ns |
| GTX_CLK fall time (80%–20%) | $t_{TTXF}$ | — | — | 1.0 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state )(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TTKHDV}$ symbolizes the TBI transmit timing (TT) with respect to the time from $t_{TTX}$ (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, $t_{TTKHDX}$ symbolizes the TBI transmit timing (TT) with respect to the time from $t_{TTX}$ (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{TTX}$ represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Data valid $t_{TTKHDV}$ to GTX_CLK Min Setup time is a function of clock period and max hold time. (Min Setup = Cycle time - Max Hold)

This figure shows the TBI transmit AC timing diagram.

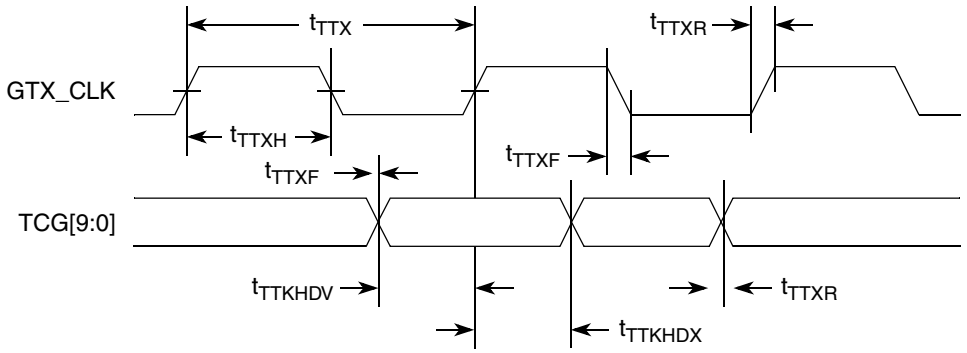



**Figure 22. TBI Transmit AC Timing Diagram**

### 2.9.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

**Table 33. TBI Receive AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition[2] | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Clock period for TBI Receive Clock 0, 1 | $t_{TRX}$ | — | 16.0 | — | ns |
| Skew for TBI Receive Clock 0, 1 | $t_{SKTRX}$ | 7.5 | — | 8.5 | ns |
| Duty cycle for TBI Receive Clock 0, 1 | $t_{TRXH}/t_{TRX}$ | 40 | — | 60 | % |
| RCG[9:0] setup time to rising edge of TBI Receive Clock 0, 1 | $t_{TRDVKH}$ | 2.5 | — | — | ns |
| RCG[9:0] hold time to rising edge of TBI Receive Clock 0, 1 | $t_{TRDXKH}$ | 1.5 | — | — | ns |
| Clock rise time (20%-80%) for TBI Receive Clock 0, 1 | $t_{TRXR}$ | 0.7 | — | 2.4 | ns |
| Clock fall time (80%-20%) for TBI Receive Clock 0, 1 | $t_{TRXF}$ | 0.7 | — | 2.4 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TRDVKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{TRDXKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{TRX}$ represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. The signals “TBI Receive Clock 0” and “TBI Receive Clock 1” refer to TSECn_RX_CLK and TSECn_TX_CLK pins respectively. These two clock signals are also referred as PMA_RX_CLK[0:1].

This figure shows the TBI receive AC timing diagram.

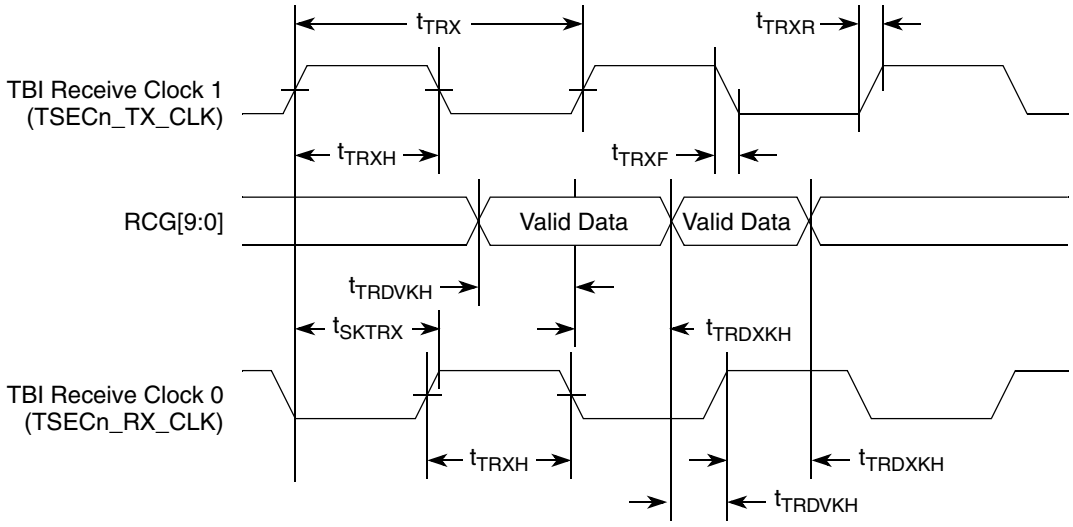



**Figure 23. TBI Receive AC Timing Diagram**

### 2.9.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC*n* pin (no receive clock is used on in this mode, whereas for the dual-clock mode this is the PMA0 receive clock). The 125-MHz transmit clock is applied on the  in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in the following table.

**Table 34. TBI single-clock Mode Receive AC Timing Specification**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3 V ± 5%

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{TRR}$ | 7.5 | 8.0 | 8.5 | ns |
| RX_CLK duty cycle | $t_{TRRH}$ | 40 | 50 | 60 | % |
| RX_CLK peak-to-peak jitter | $t_{TRRJ}$ | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | $t_{TRRR}$ | — | — | 1.0 | ns |
| Fall time RX_CLK (80%–20%) | $t_{TRRF}$ | — | — | 1.0 | ns |
| RCG[9:0] setup time to RX_CLK rising edge | $t_{TRRDV}$ | 2.0 | — | — | ns |
| RCG[9:0] hold time to RX_CLK rising edge | $t_{TRRDX}$ | 1.0 | — | — | ns |

A timing diagram for TBI receive appears in the following figure.

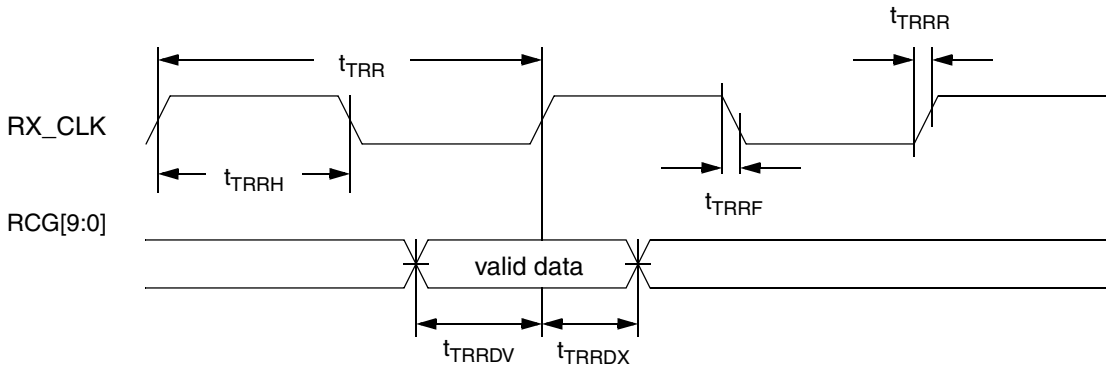



**Figure 24. TBI Single-Clock Mode Receive AC Timing Diagram**

## 2.9.2.6 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

**Table 35. RGMII and RTBI AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 2.5 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT_TX}$ | –500 | 0 | 500 | ps |
| Data to clock input skew (at receiver) [2] | $t_{SKRGT_RX}$ | 1.0 | — | 2.8 | ns |
| Clock period duration [3] | $t_{RGT}$ | 7.2 | 8.0 | 8.8 | ns |
| Duty cycle for 1000BASE-T[4] | $t_{RGTH}/t_{RGT}$ | 45 | — | 55 | % |
| Duty cycle for 10BASE-T and 100BASE-TX [3, 4] | $t_{RGTH}/t_{RGT}$ | 40 | 50 | 60 | % |
| Rise time (20%–80%) | $t_{RGTR}$ | — | — | 0.75 | ns |
| Fall time (20%–80%) | $t_{RGTF}$ | — | — | 0.75 | ns |

**Notes:**

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of $t_{RGT}$ represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, $t_{RGT}$ scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transition to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three $t_{RGT}$ of the lowest speed transitioned between.

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

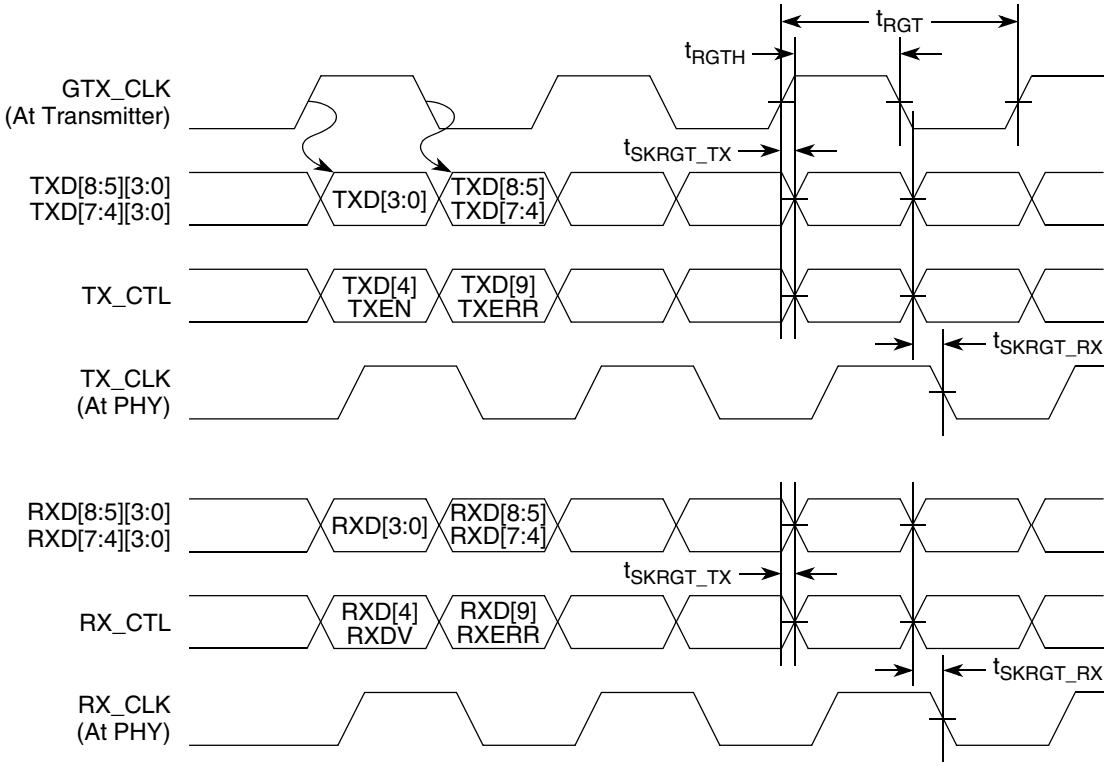



**Figure 25. RGMII and RTBI AC Timing and Multiplexing Diagrams**

## 2.9.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

### 2.9.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in the following table.

**Table 36. RMII Transmit AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TSECn_TX_CLK clock period | $t_{RMT}$ | 15.0 | 20.0 | 25.0 | ns |
| TSECn_TX_CLK duty cycle | $t_{RMTH}$ | 35 | 50 | 65 | % |
| TSECn_TX_CLK peak-to-peak jitter | $t_{RMTJ}$ | — | — | 250 | ps |

**Table 36. RMII Transmit AC Timing Specifications (continued)**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Rise time TSECn_TX_CLK (20%–80%) | $t_{RMTR}$ | 1.0 | — | 2.0 | ns |
| Fall time TSECn_TX_CLK (80%–20%) | $t_{RMTF}$ | 1.0 | — | 2.0 | ns |
| TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay | $t_{RMTDX}$ | 2.0 | — | 10.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

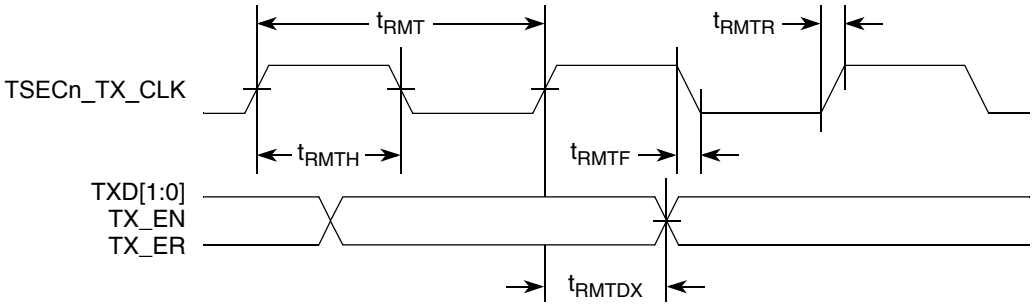



**Figure 26. RMII Transmit AC Timing Diagram**

## 2.9.2.7.2 RMII Receive AC Timing Specifications

**Table 37. RMII Receive AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TSECn_RX_CLK clock period | $t_{RMR}$ | 15.0 | 20.0 | 25.0 | ns |
| TSECn_RX_CLK duty cycle | $t_{RMRH}$ | 35 | 50 | 65 | % |
| TSECn_RX_CLK peak-to-peak jitter | $t_{RMRJ}$ | — | — | 250 | ps |
| Rise time TSECn_RX_CLK (20%–80%) | $t_{RMRR}$ | 1.0 | — | 2.0 | ns |

**Table 37. RMII Receive AC Timing Specifications (continued)**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Fall time TSECn_RX_CLK (80%–20%) | $t_{RMRF}$ | 1.0 | — | 2.0 | ns |
| RXD[1:0], CRS_DV, RX_ER setup time to TSECn_RX_CLK rising edge | $t_{RMRDV}$ | 4.0 | — | — | ns |
| RXD[1:0], CRS_DV, RX_ER hold time to TSECn_RX_CLK rising edge | $t_{RMRDX}$ | 2.0 | — | — | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

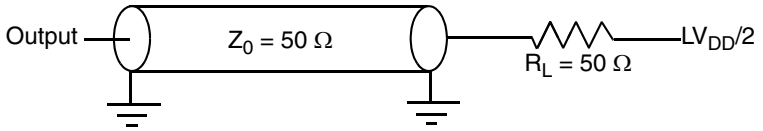



**Figure 27. eTSEC AC Test Load**

This figure shows the RMII receive AC timing diagram.

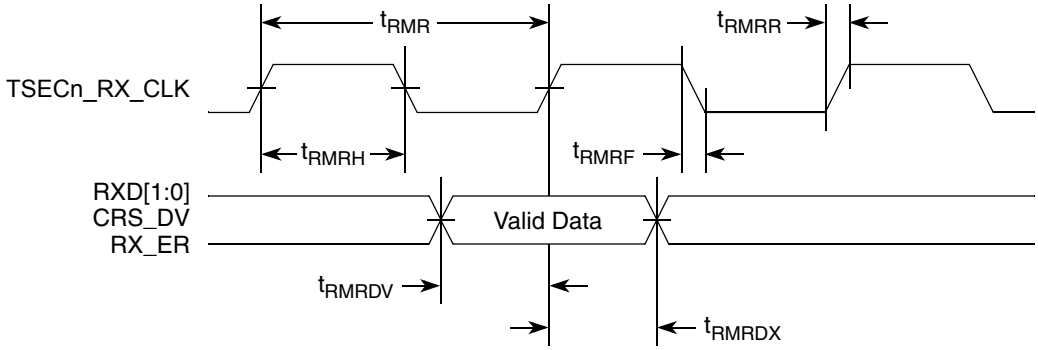



**Figure 28. RMII Receive AC Timing Diagram**

## 2.9.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes 2 interface of the chip as shown in Figure 29, where $C_{TX}$ is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to S2GND (xcorevss). The reference circuit of the SerDes transmitter and receiver is shown in Figure 68.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in Section 3.6, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the eTSEC EC_GTX_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$ pins.

### 2.9.3.1 DC Requirements for SGMII SD2_REF_CLK and SD2_REF_CLK

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 2.20, "High-Speed Serial Interfaces."

### 2.9.3.2 AC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$

This table lists the SGMII SerDes reference clock AC requirements. Please note that SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

**Table 38. SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$ AC Requirements**

| Symbol | Parameter Description | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time | — | 10 (8) | — | ns | 1 |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 100 | ps | — |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location | –50 | — | 50 | ps | 2,3 |

**Notes:**

1. 8 ns applies only when 125 MHz SerDes2 reference clock frequency is selected via cfg_srds_sgmii_refclk during POR.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10E-12.
3. Total peak-to-peak deterministic jitter "Dj" should be less than or equal to 50 ps.

### 2.9.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

The following tables describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2_TX}}$[n]) as depicted in Figure 30.

**Table 39. SGMII DC Transmitter Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage | $X2V_{DD}$ | 0.95 | 1.0 | 1.05 | V | — |
| Output high voltage | VOH | — | — | $X2V_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$ | mV | 1 |
| Output low voltage | VOL | $X2V_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$ | — | — | mV | 1 |
| Output ringing | $V_{RING}$ | — | — | 10 | % | — |
| Output differential voltage[2, 3, 5] | $\lvert V_{OD}\rvert$ | 323 | 500 | 725 | mV | Equalization setting: 1.0x |
| | | 296 | 459 | 665 | | Equalization setting: 1.09x |
| | | 269 | 417 | 604 | | Equalization setting: 1.2x |
| | | 243 | 376 | 545 | | Equalization setting: 1.33x |
| | | 215 | 333 | 483 | | Equalization setting: 1.5x |
| | | 189 | 292 | 424 | | Equalization setting: 1.71x |
| | | 162 | 250 | 362 | | Equalization setting: 2.0x |
| Output offset voltage | $V_{OS}$ | 425 | 500 | 575 | mV | 1, 4 |
| Output impedance (single-ended) | $R_O$ | 40 | — | 60 | Ω | — |
| Mismatch in a pair | $\Delta R_O$ | — | — | 10 | % | — |
| Change in $V_{OD}$ between “0” and “1” | $\Delta \lvert V_{OD}\rvert$ | — | — | 25 | mV | — |
| Change in $V_{OS}$ between “0” and “1” | $\Delta V_{OS}$ | — | — | 25 | mV | — |
| Output current on short to GND | $I_{SA}$, $I_{SB}$ | — | — | 40 | mA | — |

**Notes:**

1. This will not align to DC-coupled SGMII. $X2V_{DD\text{-}Typ}$=1.0V.
2. $\lvert V_{OD}\rvert = \lvert V_{SD2_TXn} - V_{\overline{SD2_TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**AB** (for SerDes 2 lanes A & B) or XMITEQ**EF** (for SerDes 2 lanes E & E) bit field of the chip’s SerDes 2 control register:
   - The MSbit (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude - power up default);
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. $V_{OS}$ is also referred to as output common mode voltage.
   - 5.The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $X2V_{DD\text{-}Typ}$=1.0V, no common mode offset variation (VOS =550mV), SerDes2 transmitter is terminated with 100-Ω differential load between SD2_TX[n] and SD2_TX[n].

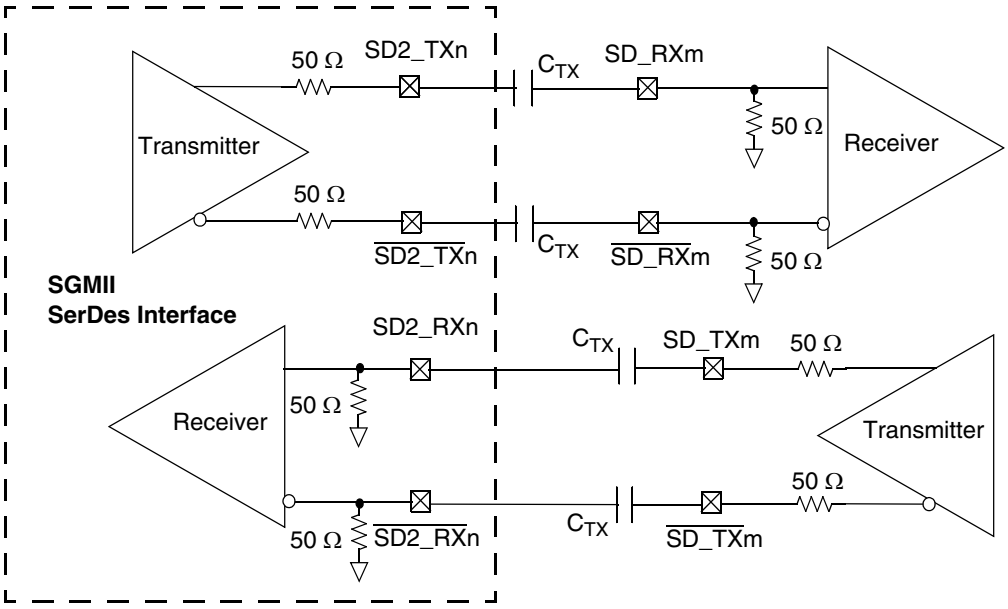



**Figure 29. 4-Wire AC-Coupled SGMII Serial Link Connection Example**

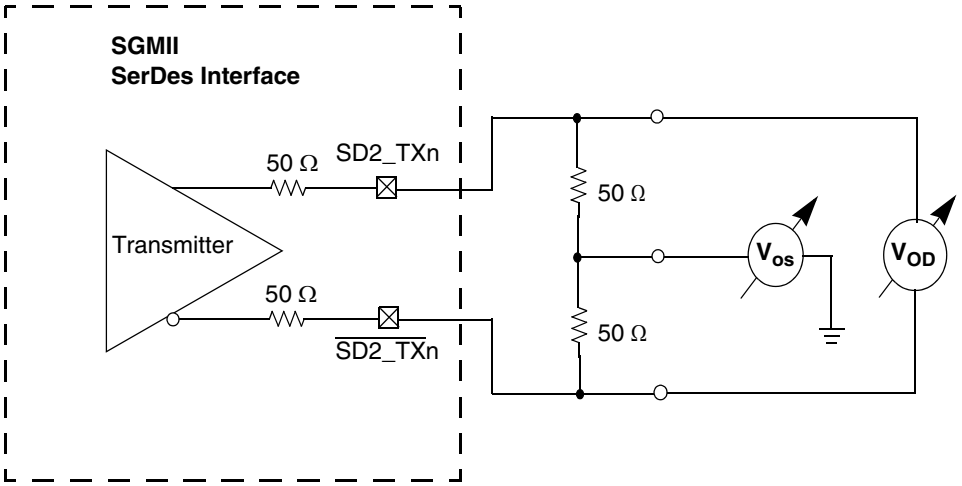



**Figure 30. SGMII Transmitter DC Measurement Circuit**

**Table 40. SGMII DC Receiver Electrical Characteristics**

| Parameter | | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Supply Voltage | | $X2V_{DD}$ | 0.95 | 1.0 | 1.05 | V | — |
| DC Input voltage range | | — | N/A | | | — | 1 |
| Input differential voltage | LSTS = 0 | $V_{RX_DIFFp\text{-}p}$ | 100 | — | 1200 | mV | 2, 4 |
| | LSTS = 1 | | 175 | — | | | |
| Loss of signal threshold | LSTS = 0 | VLOS | 30 | — | 100 | mV | 3, 4 |
| | LSTS = 1 | | 65 | — | 175 | | |
| Input AC common mode voltage | | $V_{CM_ACp\text{-}p}$ | — | — | 100 | mV | 5 |

**Table 40. SGMII DC Receiver Electrical Characteristics (continued)**

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Receiver differential input impedance | $Z_{RX_DIFF}$ | 80 | 100 | 120 | Ω | — |
| Receiver common mode input impedance | $Z_{RX_CM}$ | 20 | — | 35 | Ω | — |
| Common mode input voltage | $V_{CM}$ | — | $V_{xcorevss}$ | — | V | 6 |

**Notes:**
1. Input must be externally AC-coupled.
2. $V_{RX_DIFFp\text{-}p}$ is also referred to as peak to peak input differential voltage
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. See Table 72 for further explanation.
4. The LSTS shown in the table refers to the LSTSA or LSTSE bit field of chip's SerDes 2 control register.
5. $V_{CM_ACp\text{-}p}$ is also referred to as peak to peak AC common mode voltage.
6. On-chip termination to S2GND (xcorevss).

### 2.9.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2_TX}}$[n]) or at the receiver inputs (SD2_RX[n] and $\overline{\text{SD2_RX}}$[n]) as depicted in Figure 32 respectively.

#### 2.9.3.4.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

**Table 41. SGMII Transmit AC Timing Specifications**

At recommended operating conditions with $X2V_{DD}$ = 1.0V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Deterministic Jitter | JD | — | — | 0.17 | UI p-p | — |
| Total Jitter | JT | — | — | 0.35 | UI p-p | — |
| Unit Interval | UI | 799.92 | 800 | 800.08 | ps | 1 |
| $V_{OD}$ fall time (80%-20%) | tfall | 50 | — | 120 | ps | — |
| $V_{OD}$ rise time (20%-80%) | $t_{rise}$ | 50 | — | 120 | ps | — |

**Notes:**
1. Each UI is 800 ps ± 100 ppm.

### 2.9.3.4.2 SGMII Receive AC Timing Specifications

This table provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 31 shows the SGMII Receiver Input Compliance Mask eye diagram.

**Table 42. SGMII Receive AC Timing Specifications**

At recommended operating conditions with $X2V_{DD}$ = 1.0V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Deterministic Jitter Tolerance | JD | 0.37 | — | — | UI p-p | 1 |
| Combined Deterministic and Random Jitter Tolerance | JDR | 0.55 | — | — | UI p-p | 1 |
| Sinusoidal Jitter Tolerance | JSIN | 0.1 | — | — | UI p-p | 1 |
| Total Jitter Tolerance | JT | 0.65 | — | — | UI p-p | 1 |
| Bit Error Ratio | BER | — | — | $10^{-12}$ | | — |
| Unit Interval | UI | 799.92 | 800 | 800.08 | ps | 2 |
| AC Coupling Capacitor | $C_{TX}$ | 5 | — | 200 | nF | 3 |

**Notes:**

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the chip transmitter outputs.

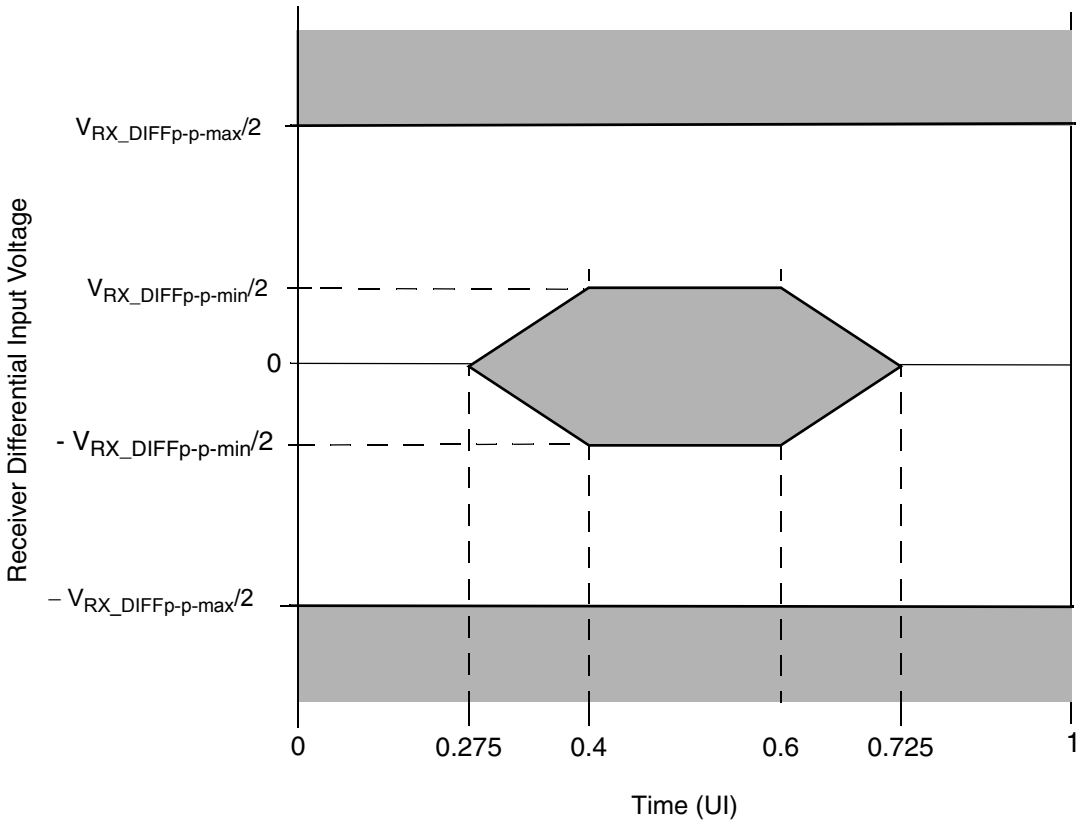



**Figure 31. SGMII Receiver Input Compliance Mask**

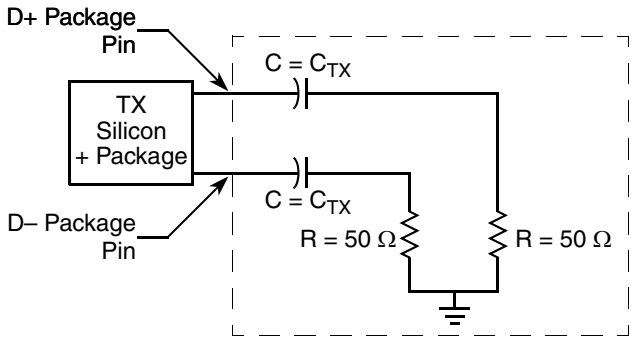



**Figure 32. SGMII AC Test/Measurement Load**

## 2.9.4 eTSEC IEEE 1588 AC Specifications

This figure shows the data and command output timing diagram.

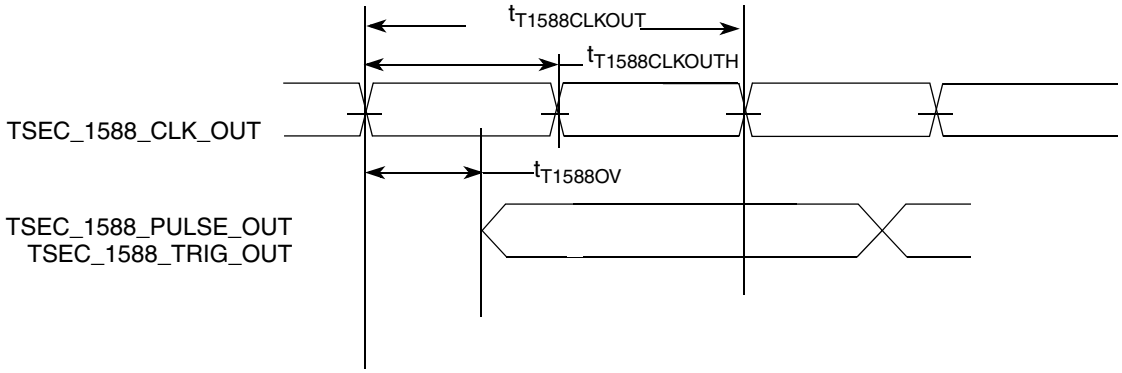



**Figure 33. eTSEC IEEE 1588 Output AC timing**

[1] The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

This figure provides the data and command input timing diagram.

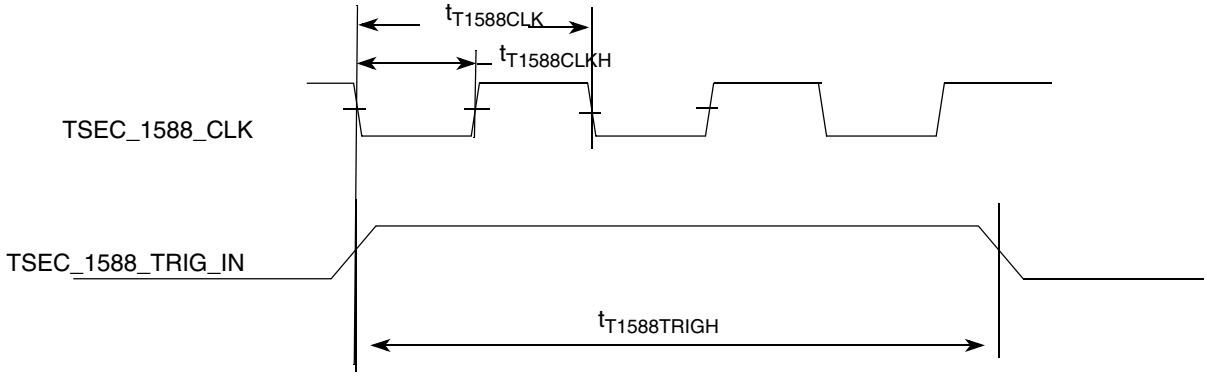



**Figure 34. eTSEC IEEE 1588 Input AC timing**

The IEEE 1588 AC timing specifications are in the following table.

**Table 43. eTSEC IEEE 1588 AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TSEC_1588_CLK clock period | $t_{T1588CLK}$ | 3.8 | — | $T_{TX_CLK}$*7 | ns | 1 |
| TSEC_1588_CLK duty cycle | $t_{T1588CLKH}$ /$t_{T1588CLK}$ | 40 | 50 | 60 | % | — |
| TSEC_1588_CLK peak-to-peak jitter | $t_{T1588CLKINJ}$ | — | — | 250 | ps | — |
| Rise time eTSEC_1588_CLK (20%–80%) | $t_{T1588CLKINR}$ | 1.0 | — | 2.0 | ns | — |
| Fall time eTSEC_1588_CLK (80%–20%) | $t_{T1588CLKINF}$ | 1.0 | — | 2.0 | ns | — |
| TSEC_1588_CLK_OUT clock period | $t_{T1588CLKOUT}$ | 2*$t_{T1588CLK}$ | — | — | ns | — |
| TSEC_1588_CLK_OUT duty cycle | $t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$ | 30 | 50 | 70 | % | — |
| TSEC_1588_PULSE_OUT | $t_{T1588OV}$ | 0.5 | — | 3.0 | ns | — |
| TSEC_1588_TRIG_IN pulse width | $t_{T1588TRIGH}$ | 2*$t_{T1588CLK_MAX}$ | — | — | ns | 2 |

**Note:**

1. When TMR_CTRL[CKSEL]=00, the external TSEC_1588_CLK input is selected as the 1588 timer reference clock source, with the timing defined in the Table above. The maximum value of $t_{T1588CLK}$ is defined in terms of $T_{TX_CLK}$, which is the maximum clock cycle period of the equivalent interface speed that the eTSEC1 port is running.
   When eTSEC1 is configured to operate in the parallel mode, the $T_{TX_CLK}$ is the maximum clock period of the TSEC1_TX_CLK. When eTSEC1 operates in SGMII mode, the maximum value of $t_{T1588CLK}$ is defined in terms of the recovered clock from SGMII SerDes. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns respectively.
   See the *MPC8536E PowerQUICC III Integrated Communications Processor Reference Manual* for a description of TMR_CTRL registers.
2. It need to be at least two times of clock period of clock selected by TMR_CTRL[CKSEL]. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for a description of TMR_CTRL registers.

## 2.10 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals EC_MDIO (management data input/output) and EC_MDC (management data clock). The electrical characteristics for GMII, SGMII, RGMII, RMII, TBI and RTBI are specified in Section 2.9, “Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management”

### 2.10.1 MII Management DC Electrical Characteristics

The EC_MDC and EC_MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for EC_MDIO and EC_MDC are provided in the following table.

**Table 44. MII Management DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage (3.3 V) | $OV_{DD}$ | 3.13 | 3.47 | V |
| Output high voltage ($OV_{DD}$ = Min, $I_{OH}$ = –4.0 mA) | $V_{OH}$ | 2.40 | $OV_{DD}$ + 0.3 | V |
| Output low voltage ($OV_{DD}$ =Min, $I_{OL}$ = 4.0 mA) | $V_{OL}$ | GND | 0.40 | V |
| Input high voltage | $V_{IH}$ | 2.0 | — | V |
| Input low voltage | $V_{IL}$ | — | 0.90 | V |
| Input high current ($OV_{DD}$ = Max, $V_{IN}$ [1] = 2.1 V) | $I_{IH}$ | — | 40 | μA |
| Input low current ($OV_{DD}$ = Max, $V_{IN}$ = 0.5 V) | $I_{IL}$ | –600 | — | μA |

**Note:**

1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

### 2.10.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

**Table 45. MII Management AC Timing Specifications**

At recommended operating conditions with OVDD is 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC_MDC frequency | $f_{MDC}$ | 0.74 | 2.5 | 8.3 | MHz | 2 |
| EC_MDC period | $t_{MDC}$ | 120 | 400 | 1350 | ns | — |
| EC_MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | — |
| EC_MDC to EC_MDIO delay | $t_{MDKHDX}$ | (16 * $t_{plb_clk}$)-3 | — | (16 * $t_{plb_clk}$)+3 | ns | 3,5,6 |
| EC_MDIO to EC_MDC setup time | $t_{MDDVKH}$ | 5 | — | — | ns | — |

**Table 45. MII Management AC Timing Specifications (continued)**

At recommended operating conditions with OVDD is 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC_MDIO to EC_MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | — |
| EC_MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | — |
| EC_MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | — |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency ($f_{CCB}$). The actual EC_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of chip's MIIMCFG register, based on the platform (CCB) clock running for the chip. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, $f_{MDC}$ = 533/(2*4*8) = 533/64 = 8.3 MHz. That is, for a system running at a particular platform frequency ($f_{CCB}$), the EC_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. See the MPC8536E reference manual's MIIMCFG register section for more detail.
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods +/-3ns. For example, with a platform clock of 333MHz, the min/max delay is 48ns +/-3ns. Similarly, if the platform clock is 400MHz, the min/max delay is 40ns +/-3ns).
5. $t_{CLKplb_clk}$ is the platform (CCB) clock
6. EC_MDC to EC_MDIO Data valid $t_{MDKHDV}$ is a function of clock period and max delay time $t_{MDKHDX}$. (Min Setup = Cycle time - Max Hold)

This figure shows the MII management AC timing diagram.

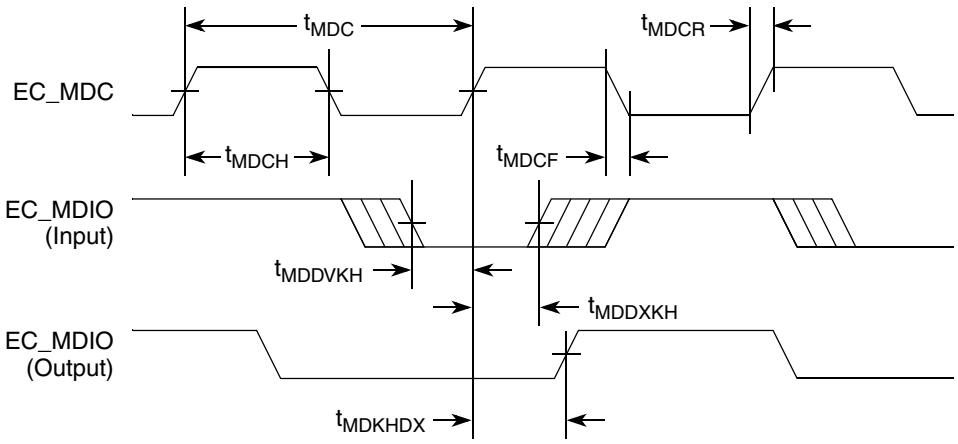



**Figure 35. MII Management Interface Timing Diagram**

## 2.11 USB

This section provides the AC and DC electrical specifications for the USB interface of the chip.

## 2.11.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the USB interface.

**Table 46. USB DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |

**Note:**

1. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 2.11.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the chip.

**Table 47. USB General Timing Parameters[6]**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| usb clock cycle time | $t_{USCK}$ | 15 | — | ns | 2-5 |
| Input setup to usb clock - all inputs | $t_{USIVKH}$ | 4 | — | ns | 2-5 |
| input hold to usb clock - all inputs | $t_{USIXKH}$ | 1 | — | ns | 2-5 |
| usb clock to output valid - all outputs | $t_{USKHOV}$ | — | 7 | ns | 2-5 |
| Output hold from usb clock - all outputs | $t_{USKHOX}$ | 2 | — | ns | 2-5 |

**Notes:**

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{USIXKH}$ symbolizes usb timing (US) for the input (I) to go invalid (X) with respect to the time the usb clock reference (K) goes high (H). Also, $t_{USKHOX}$ symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to 0.4 × $OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.
6. When switching the data pins from outputs to inputs using the USBn_DIR pin, the output timings will be violated on that cycle because the output buffers are tristated asynchronously. This should not be a problem, because the PHY should not be functionally looking at these signals on that cycle as per ULPI specifications

This figures provide the AC test load and signals for the USB, respectively.

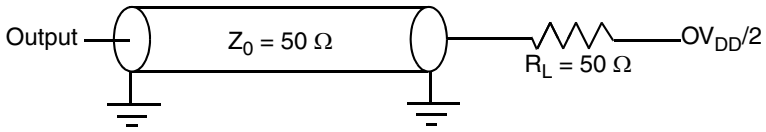



**Figure 36. USB AC Test Load**

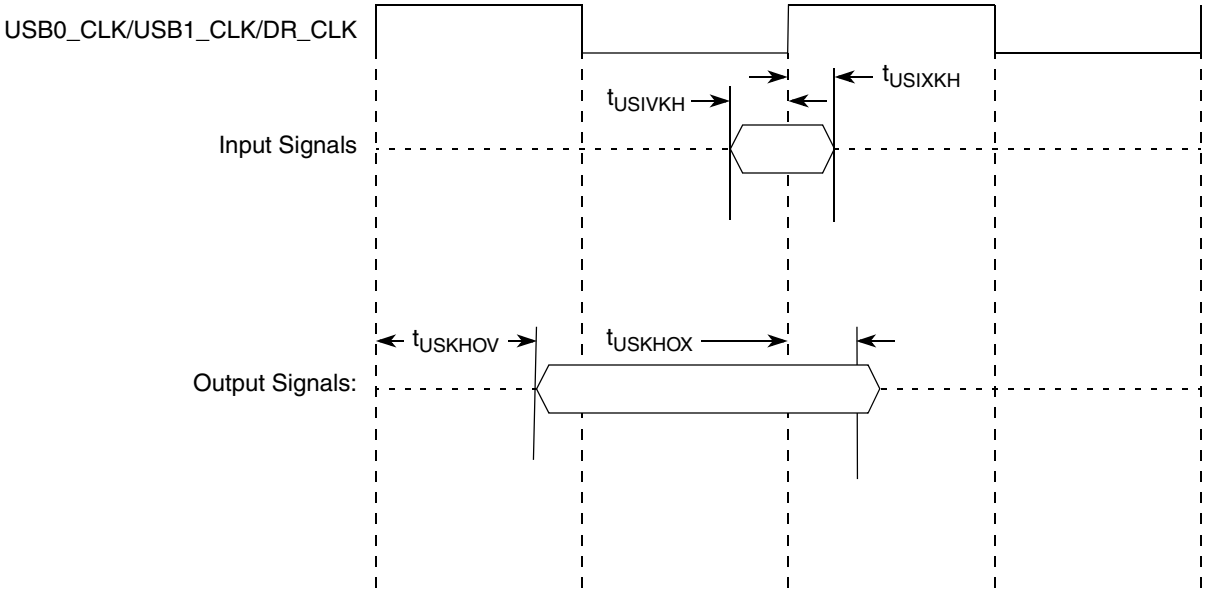



**Figure 37. USB Signals**

## 2.12 Enhanced Local Bus Controller (eLBC)

This section describes the DC and AC electrical specifications for the local bus interface of the chip.

### 2.12.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface operating at $BV_{DD}$ = 3.3 V DC.

**Table 48. Local Bus DC Electrical Characteristics (3.3 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 3.3V | $BV_{DD}$ | 3.13 | 3.47 | V |
| High-level input voltage | $V_{IH}$ | 1.9 | $BV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V |

**Note:**

1. The symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

This table provides the DC electrical characteristics for the local bus interface operating at $BV_{DD}$ = 2.5 V DC.

**Table 49. Local Bus DC Electrical Characteristics (2.5 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 2.5V | $BV_{DD}$ | 2.37 | 2.63 | V |
| High-level input voltage | $V_{IH}$ | 1.70 | $BV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.7 | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IH}$ | — | 10 | μA |
| | $I_{IL}$ | | –15 | |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –1 mA) | $V_{OH}$ | 2.0 | $BV_{DD}$ + 0.3 | V |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 1 mA) | $V_{OL}$ | GND – 0.3 | 0.4 | V |

**Note:**

1. Note that the symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

This table provides the DC electrical characteristics for the local bus interface operating at $BV_{DD}$ = 1.8 V DC.

**Table 50. Local Bus DC Electrical Characteristics (1.8 V DC)**

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage 1.8V | $BV_{DD}$ | — | 1.71 | 1.89 | V |
| High-level input voltage | $V_{IH}$ | — | 0.65*$BV_{DD}$ | 0.3+$BV_{DD}$ | V |
| Low-level input voltage | $V_{IL}$ | — | –0.3 | 0.35*$BV_{DD}$ | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | -15 | 10 | μA |
| High-level output voltage | $V_{OH}$ | $I_{OH}$ = –100 μA | $BV_{DD}$ – 0.2 | — | V |
| | | $I_{OH}$ = –2 mA | $BV_{DD}$ – 0.45 | — | |
| Low-level output voltage | $V_{OL}$ | $I_{OH}$ = 100 μA | — | 0.2 | V |
| | | $I_{OH}$ = 2 mA | — | 0.45 | |

**Note:**

1. Note that the symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

## 2.12.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface at $BV_{DD}$ = 3.3 V DC. For information about the frequency range of local bus see Section 2.23.1, “Clock Ranges.”

**Table 51. Local Bus General Timing Parameters ($BV_{DD}$ = 3.3 V DC)**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 7.5 | 12 | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | $t_{LBKSKEW}$ | | 150 | ps | 7 |
| Input setup to local bus clock (except LUPWAIT) | $t_{LBIVKH1}$ | 1.8 | — | ns | 3, 4 |
| LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 1.7 | — | ns | 3, 4 |
| Input hold from local bus clock (except LUPWAIT) | $t_{LBIXKH1}$ | 1.0 | — | ns | 3, 4 |
| LUPWAIT input hold from local bus clock | $t_{LBIXKH2}$ | 1.0 | — | ns | 3, 4 |
| LALE output transition to LAD/LDP output transition (LATCH setup and hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 2.3 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 2.4 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 2.3 | ns | 3 |
| Local bus clock to LALE assertion | $t_{LBKHOV4}$ | — | 2.3 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKHOX1}$ | 0.7 | — | ns | 3 |

**Table 51. Local Bus General Timing Parameters ($BV_{DD}$ = 3.3 V DC) (continued)**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Output hold from local bus clock for LAD/LDP | $t_{LBKHOX2}$ | 0.7 | — | ns | 3 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKHOZ1}$ | — | 2.5 | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKHOZ2}$ | — | 2.5 | ns | 5 |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This table describes the general timing parameters of the local bus interface at $BV_{DD}$ = 2.5 V DC.

**Table 52. Local Bus General Timing Parameters ($BV_{DD}$ = 2.5 V DC)**

| Parameter | Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Local bus cycle time | — | $t_{LBK}$ | 7.5 | 12 | ns | 2 |
| Local bus duty cycle | — | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | — | $t_{LBKSKEW}$ | — | 150 | ps | 7 |
| Input setup to local bus clock (except LUPWAIT) | — | $t_{LBIVKH1}$ | 1.9 | — | ns | 3, 4 |
| LUPWAIT input setup to local bus clock | — | $t_{LBIVKH2}$ | 1.8 | — | ns | 3, 4 |
| Input hold from local bus clock (except LUPWAIT) | — | $t_{LBIXKH1}$ | 1.1 | — | ns | 3, 4 |
| LUPWAIT input hold from local bus clock | — | $t_{LBIXKH2}$ | 1.1 | — | ns | 3, 4 |
| LALE output transition to LAD/LDP output transition (LATCH setup and hold time) | — | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | — | $t_{LBKHOV1}$ | — | 2.4 | ns | — |
| Local bus clock to data valid for LAD/LDP | — | $t_{LBKHOV2}$ | — | 2.5 | ns | 3 |
| Local bus clock to address valid for LAD | — | $t_{LBKHOV3}$ | — | 2.4 | ns | 3 |
| Local bus clock to LALE assertion | — | $t_{LBKHOV4}$ | — | 2.4 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | — | $t_{LBKHOX1}$ | 0.8 | — | ns | 3 |

**Table 52. Local Bus General Timing Parameters ($BV_{DD}$ = 2.5 V DC) (continued)**

| Parameter | Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Output hold from local bus clock for LAD/LDP | — | $t_{LBKHOX2}$ | 0.8 | — | ns | 3 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | — | $t_{LBKHOZ1}$ | — | 2.6 | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | — | $t_{LBKHOZ2}$ | — | 2.6 | ns | 5 |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This table describes the general timing parameters of the local bus interface at $BV_{DD}$ = 1.8 V DC.

**Table 53. Local Bus General Timing Parameters ($BV_{DD}$ = 1.8 V DC)**

| Parameter | Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Local bus cycle time | — | $t_{LBK}$ | 7.5 | 12 | ns | 2 |
| Local bus duty cycle | — | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | — | $t_{LBKSKEW}$ | | 150 | ps | 7 |
| Input setup to local bus clock (except LUPWAIT) | — | $t_{LBIVKH1}$ | 2.4 | — | ns | 3, 4 |
| LUPWAIT input setup to local bus clock | — | $t_{LBIVKH2}$ | 1.9 | — | ns | 3, 4 |
| Input hold from local bus clock (except LUPWAIT) | — | $t_{LBIXKH1}$ | 1.1 | — | ns | 3, 4 |
| LUPWAIT input hold from local bus clock | — | $t_{LBIXKH2}$ | 1.1 | — | ns | 3, 4 |
| LALE output transition to LAD/LDP output transition (LATCH setup and hold time) | — | $t_{LBOTOT}$ | 1.2 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | — | $t_{LBKHOV1}$ | — | 3.2 | ns | — |
| Local bus clock to data valid for LAD/LDP | — | $t_{LBKHOV2}$ | — | 3.2 | ns | 3 |
| Local bus clock to address valid for LAD | — | $t_{LBKHOV3}$ | — | 3.2 | ns | 3 |
| Local bus clock to LALE assertion | — | $t_{LBKHOV4}$ | — | 3.2 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | — | $t_{LBKHOX1}$ | 0.9 | — | ns | 3 |

**Table 53. Local Bus General Timing Parameters ($BV_{DD}$ = 1.8 V DC) (continued)**

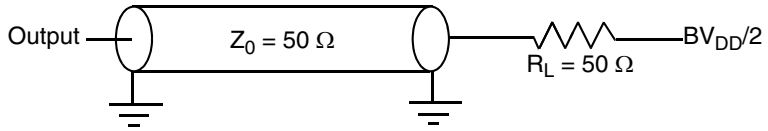
| Parameter | Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Output hold from local bus clock for LAD/LDP | — | $t_{LBKHOX2}$ | 0.9 | — | ns | 3 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | — | $t_{LBKHOZ1}$ | — | 2.6 | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | — | $t_{LBKHOZ2}$ | — | 2.6 | ns | 5 |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 1.8-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This figure provides the AC test load for the local bus.

**Figure 38. Local Bus AC Test Load**



This figures show the local bus signals.

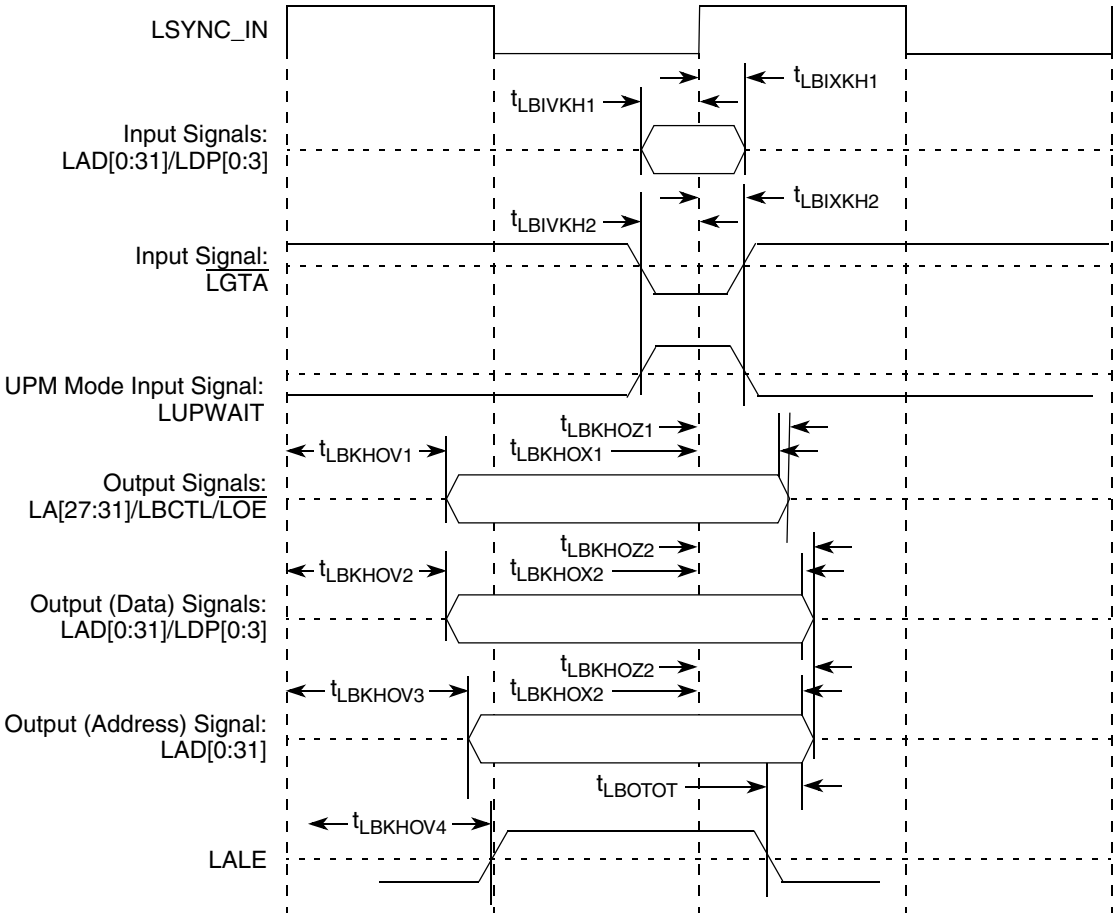



**Figure 39. Local Bus Signals, Non-Special Signals Only (PLL Enabled)**

## NOTE

In PLL bypass mode, some signals are launched and captured on the opposite edge of LCLK[n] to that used in PLL Enable Mode. In this mode, output signals are launched at the falling edge of the LCLK[n] and inputs signals are captured at the rising edge of LCLK[n] with the exception of LGTA/LUPWAIT (which is captured at the falling edge of the LCLK[n]).

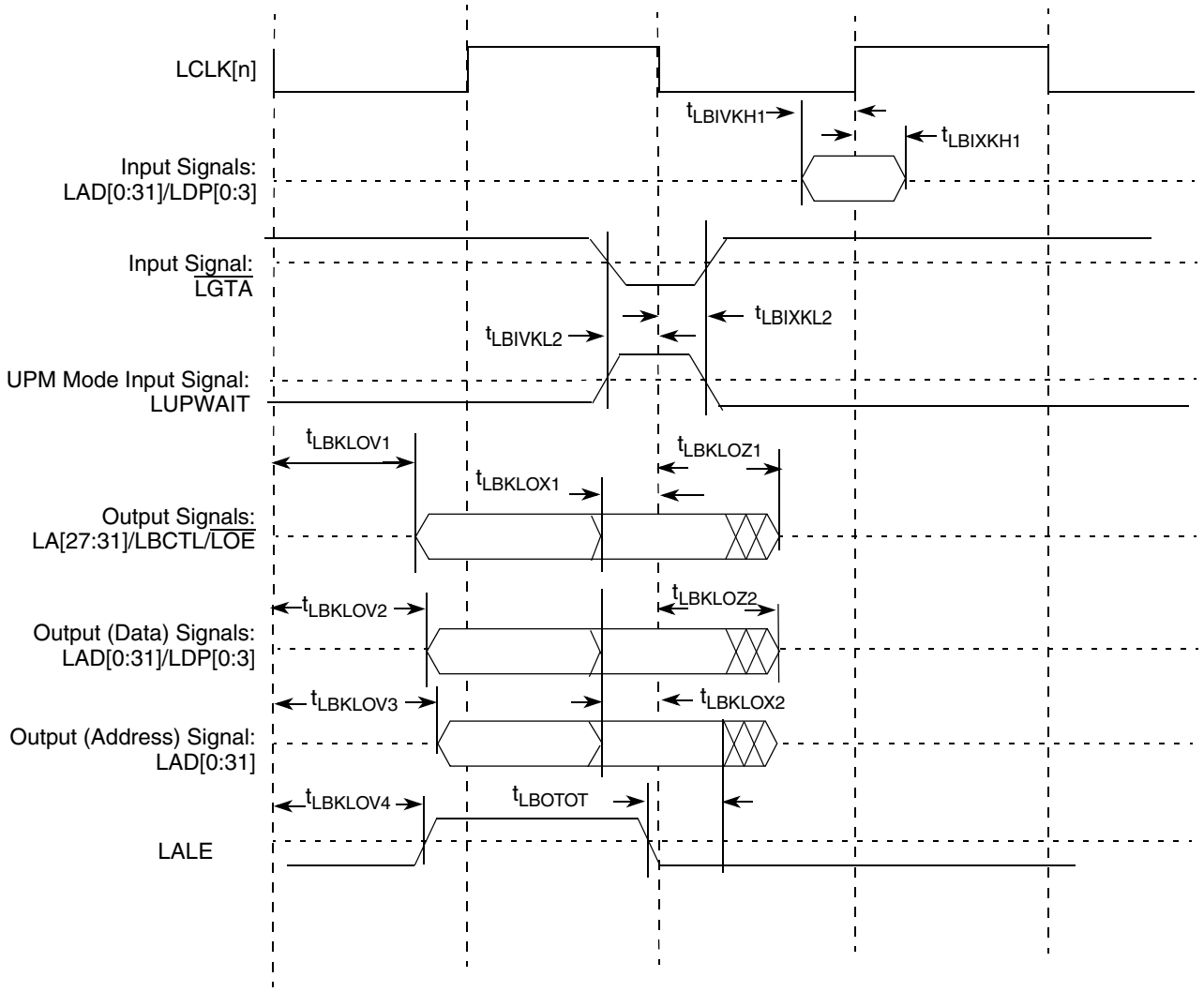



**Figure 40. Local Bus Signals (PLL Bypass Mode)**

This table describes the general timing parameters of the local bus interface at $V_{DD}$ = 3.3 V DC with PLL disabled.

**Table 54. Local Bus General Timing Parameters—PLL Bypassed**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 12 | — | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | — |
| Input setup to local bus clock (except LUPWAIT) | $t_{LBIVKH1}$ | 5.1 | — | ns | 4, 5 |
| LUPWAIT input setup to local bus clock | $t_{LBIVKL2}$ | 4.2 | — | ns | 4, 5 |
| Input hold from local bus clock (except LUPWAIT) | $t_{LBIXKH1}$ | -1.4 | — | ns | 4, 5 |
| LUPWAIT input hold from local bus clock | $t_{LBIXKL2}$ | -2.0 | — | ns | 4, 5 |
| LALE output transition to LAD/LDP output transition (LATCH hold time) | $t_{LBOTOT}$ | 1.4 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKLOV1}$ | — | 0.5 | ns | 4 |

**Table 54. Local Bus General Timing Parameters—PLL Bypassed (continued)**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus clock to data valid for LAD/LDP | $t_{LBKLOV2}$ | — | 0.5 | ns | 4 |
| Local bus clock to address valid for LAD, and LALE | $t_{LBKLOV3}$ | — | 0.5 | ns | 4 |
| Local bus clock to LALE assertion | $t_{LBKLOV4}$ | — | 0.5 | ns | 4 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKLOX1}$ | — | 2.2 | ns | 4,8 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKLOX2}$ | — | 2.2 | ns | 4,8 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKLOZ1}$ | — | 0.1 | ns | 7 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKLOZ2}$ | — | 0.1 | ns | 7 |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is guaranteed with LBCR[AHD] = 0.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. These timing parameters for PLL bypass mode are defined in the opposite direction of the PLL enabled output hold timing parameters.

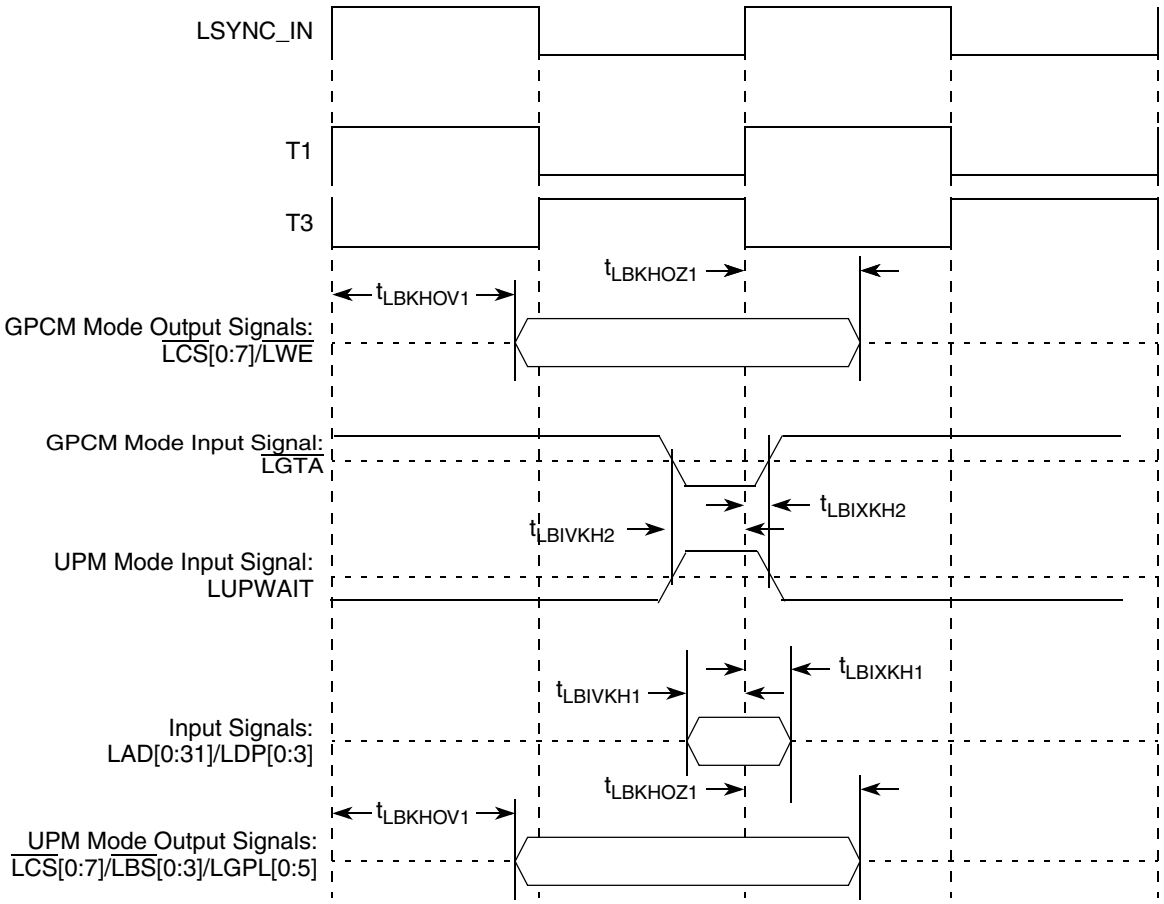



**Figure 41. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4(PLL Enabled)**

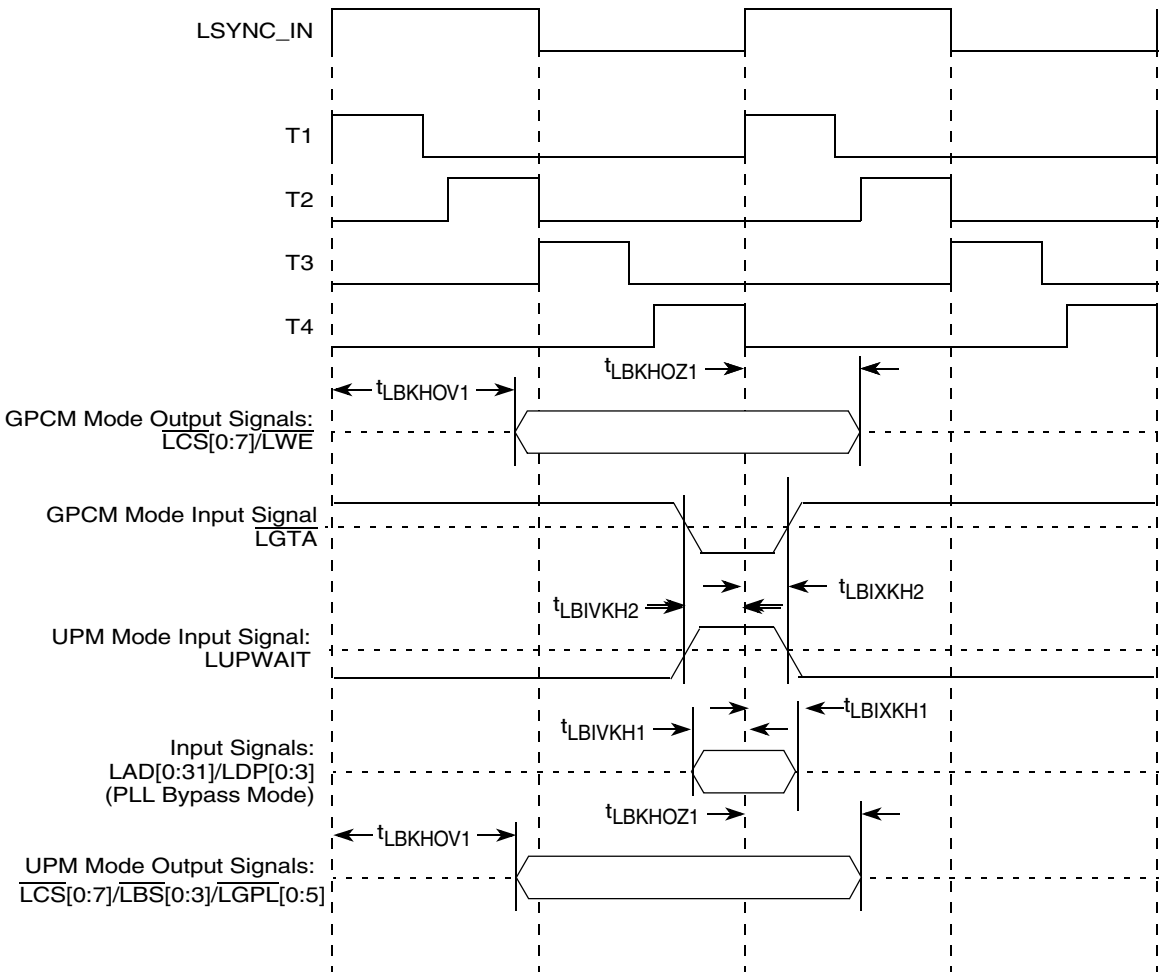



**Figure 42. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 8 or 16(PLL Enabled)**

## 2.13 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface of the chip.

### 2.13.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface of the chip.

**Table 55. eSDHC interface DC Electrical Characteristics**

At recommended operating conditions (see Table 3)

| Characteristic | Symbol | Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 0.625 * OVDD | OVDD+0.3 | V | — |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.25 * OVDD | V | — |
| Input/Output leakage current | $I_{IN}/I_{OZ}$ | — | –10 | 10 | uA | — |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = -100 uA @OVDDmin | 0.75 * OVDD | — | V | — |

**Table 55. eSDHC interface DC Electrical Characteristics (continued)**

At recommended operating conditions (see Table 3)

| Characteristic | Symbol | Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 100uA @OVDDmin | — | 0.125 * OVDD | V | — |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = -100 uA | $OV_{DD}$ - 0.2 | — | — | 2 |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 2 mA | — | 0.3 | — | 2 |

**Notes:**

1. The min $V_{IL}$ and $V_{IH}$ values are based on the respective min and max $OV_{IN}$ values found in Table 3.
2. Open drain mode for MMC cards only.

## 2.13.2 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications as defined in the following figure.

**Table 56. eSDHC AC Timing Specifications**

At recommended operating conditions (see Table 3)

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| SD_CLK clock frequency:<br>SD/SDIO Full speed/high speed mode<br>MMC Full speed/high speed mode | $f_{SHSCK}$ | <br>0 | <br>25/50<br>20/52 | MHz | 2, 5 |
| SD_CLK clock frequency - identification mode | $f_{SIDCK}$ | 0<br>100 | 400 | KHz | 3, 5 |
| SD_CLK clock low time - High speed/Full speed mode | $t_{SHSCKL}$ | 7/10 | — | ns | 5 |
| SD_CLK clock high time - High speed/Full speed mode | $t_{SHSCKH}$ | 7/10 | — | ns | 5 |
| SD_CLK clock rise and fall times | $t_{SHSCKR}$/<br>$t_{SHSCKF}$ | — | 3 | ns | 5 |
| Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK | $t_{SHSIVKH}$ | 2.5 | — | ns | 4,5,6 |
| Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK | $t_{SHSIXKH}$ | 2.5 | — | ns | 5,6 |
| Output delay time: SD_CLK to SD_CMD, SD_DATx valid | $t_{SHSKHOV}$ | –3 | 3 | ns | 5,6 |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full speed mode, clock frequency value can be 0–25 MHz for a SD/SDIO card and 0–20 MHz for a MMC card. In high speed mode, clock frequency value can be 0–50 MHz for a SD/SDIO card and 0–52MHz for a MMC card.
3. 0 Hz means to stop the clock. The given minimum frequency range is for cases were a continuous clock is required.
4. To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1 ns.
5. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF
6. The parameter values apply to both full speed and high speed modes.

This figure provides the eSDHC clock input timing diagram.

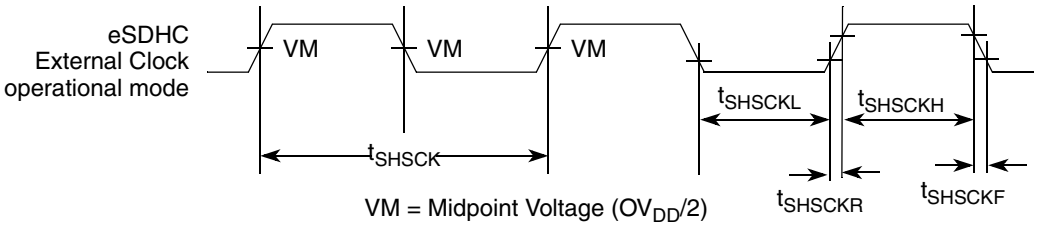



**Figure 43. eSDHC Clock Input Timing Diagram**

This figure provides the data and command input/output timing diagram.

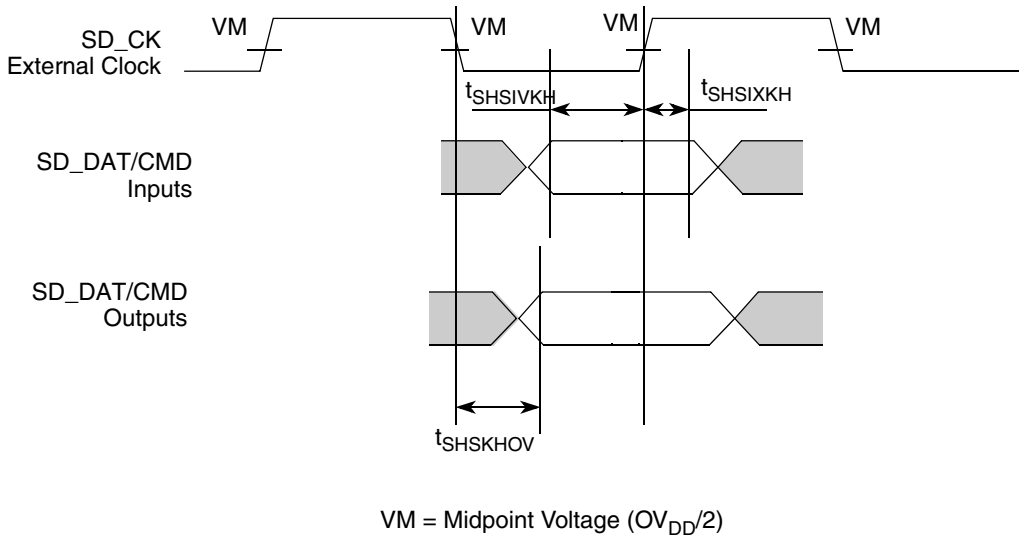



**Figure 44. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock**

## 2.14 Programmable Interrupt Controller (PIC)

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).

## 2.15 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the chip.

### 2.15.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the JTAG interface.

**Table 57. JTAG DC Electrical Characteristics**

| Parameter | Symbol [1] | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | -0.3 | 0.8 | V |

**Table 57. JTAG DC Electrical Characteristics (continued)**

| Parameter | Symbol [1] | Min | Max | Unit |
|---|---|---|---|---|
| Input current ($V_{IN}$[1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = -2 mA) | $V_{OH}$ | 2.4 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V |

**Notes:**

1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$.

## 2.15.2 JTAG AC Electrical Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the chip.

This table provides the JTAG AC timing specifications as defined in the following figures.

**Table 58. JTAG AC Timing Specifications (Independent of SYSCLK)**

At recommended operating conditions (see Table 3).

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ & $t_{JTGF}$ | 0 | 2 | ns | — |
| $\overline{\text{TRST}}$ assert time | $t_{TRST}$ | 25 | — | ns | 2 |
| Input setup times: | $t_{JTDVKH}$ | 4 | — | ns | |
| Input hold times: | $t_{JTDXKH}$ | 10 | — | ns | |
| Output Valid times: | $t_{JTKLDV}$ | — | 10 | ns | 3 |
| Output hold times: | $t_{JTKLDX}$ | 0 | — | ns | 3 |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3.) The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure provides the AC test load for TDO and the boundary-scan outputs.

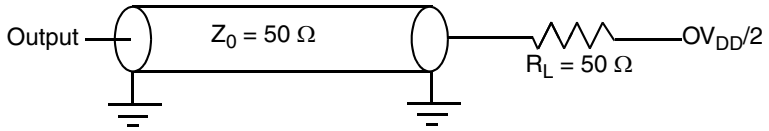



**Figure 45. AC Test Load for the JTAG Interface**

This figure provides the JTAG clock input timing diagram.

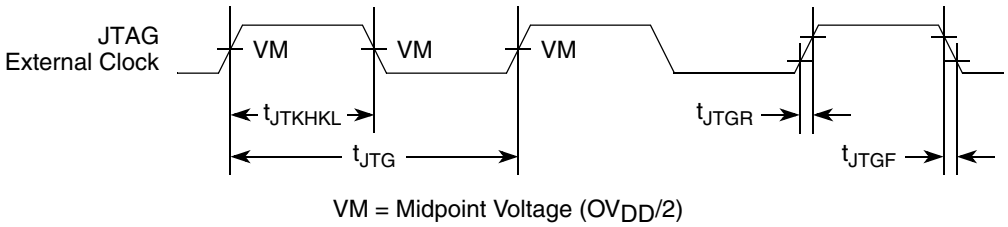



**Figure 46. JTAG Clock Input Timing Diagram**

This figure provides the $\overline{\text{TRST}}$ timing diagram.

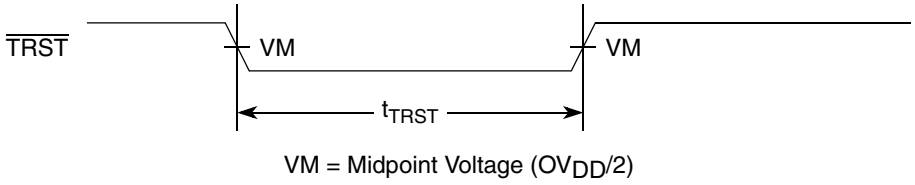



**Figure 47. $\overline{\text{TRST}}$ Timing Diagram**

This figure provides the boundary-scan timing diagram.

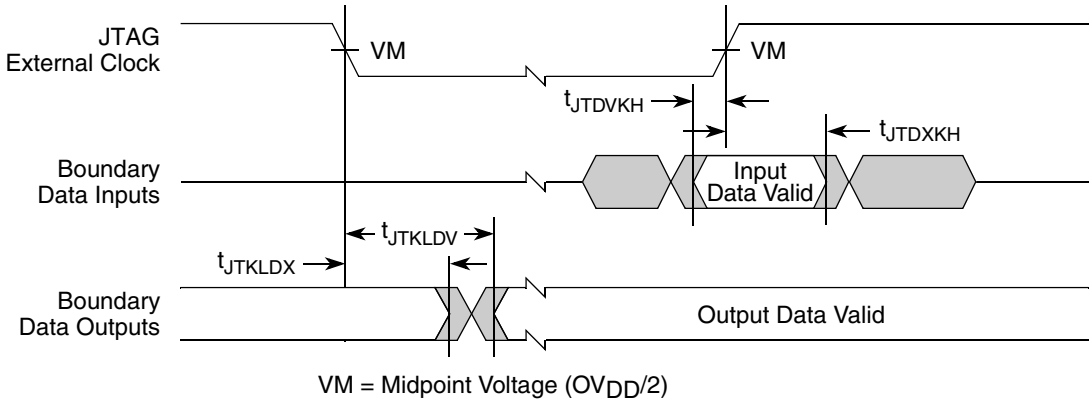



**Figure 48. Boundary-Scan Timing Diagram**

## 2.16 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) of the chip. Note that the external cabled applications or long backplane applications (Gen1x & Gen2x) are not supported.

## 2.16.1 Requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in the following table.

**Table 59. Reference Clock Input Requirements**

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SD2_REF_CLK/_B reference clock cycle time | $t_{CLK_REF}$ | 100 | — | 150 | MHz | 1 |
| SD2_REF_CLK/_B frequency tolerance | $t_{CLK_TOL}$ | –350 | 0 | +350 | ppm | — |
| SD_REF_CLK/_B rise/fall time (80%-20%) | $t_{CLK_RISE}/t_{CLK_FALL}$ | — | — | 1 | ns | — |
| SD_REF_CLK/_B duty cycle (@50% X2VDD) | $t_{CLK_DUTY}$ | 45 | 50 | 55 | % | — |
| SD_REF_CLK/_B cycle to cycle clock jitter (period jitter) | $t_{CLK_CJ}$ | — | — | 100 | ps | — |
| SD_REF_CLK/_B phase jitter (peak-to-peak) | $t_{CLK_PJ}$ | –50 | — | +50 | ps | 2,3 |

**Note:**

1. Only 100/125/150 MHz have been tested, other in between values will not work correctly with the rest of the system.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10E-12.
3. Total peak-to-peak deterministic jitter “Dj” should be less than or equal to 50 ps.

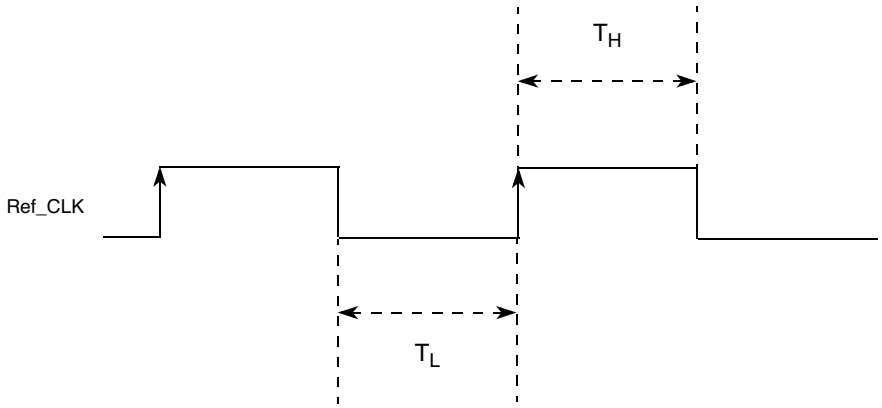



**Figure 49. Reference Clock Timing Waveform**

## 2.16.2 Differential Transmitter (TX) Output Characteristics

This table provides the differential transmitter (TX) output characteristics for the SATA interface.

**Table 60. Differential Transmitter (TX) Output Characteristics**

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Channel Speed<br>1.5G<br>3.0G | $t_{CH_SPEED}$ | — | <br>1.5<br>3.0 | — | Gbps | — |
| Unit Interval<br>1.5G<br>3.0G | $T_{UI}$ | 666.4333<br>333.2167 | 666.4333<br>333.3333 | 670.2333<br>335.1167 | ps | — |
| DC Coupled Common Mode Voltage | $V_{dc_cm}$ | 200 | 250 | 450 | mV | 3 |
| TX Diff Output Voltage<br>1.5G<br>3.0G | $V_{SATA_TXDIFF}$ | 400<br>400 | 500<br>— | 600<br>700 | mV | — |
| TX rise/fall time<br>1.5G<br>3.0G | $t_{SATA_20\text{-}80TX}$ | 100<br>67 | —<br>— | 273<br>136 | ps | — |
| TX differential skew | $t_{SATA_TXSKEW}$ | — | — | 20 | ps | — |
| TX Differential pair impedance<br>1.5G | $Z_{SATA_TXDIFFIM}$ | <br>85 | <br>— | <br>115 | ohm | — |
| TX Single ended impedance<br>1.5G | $Z_{SATA_TXSEIM}$ | <br>40 | <br>— | <br>— | ohm | — |
| TX AC common mode voltage (peak to peak)<br>1.5G<br>3.0G | $V_{SATA_TXCMMOD}$ | <br>—<br>— | <br>—<br>— | <br>—<br>50 | mV | — |
| OOB Differential Delta | $V_{SATA_OOBvdoff}$ | — | — | 25 | mV | 1 |
| OOB Common mode Delta | $V_{SATA_OOBcm}$ | — | — | 50 | mV | 1 |
| TX Rise/Fall Imbalance | $T_{SATA_TXR/Fbal}$ | — | — | 20 | % | — |
| TX Amplitude Imbalance | $T_{SATA_TXampbal}$ | — | — | 10 | % | — |
| TX Differential Mode Return loss<br>150 MHz - 300 MHz<br>300 MHz - 600 MHz<br>600 MHz - 1.2 GHz<br><br>1.2 GHz - 2.4 GHz<br>2.4 GHz - 3.0 GHz<br>3.0 GHz - 5.0 GHz | $RL_{SATA_TXDD11}$ | <br>—<br>—<br>—<br><br>—<br>—<br>— | <br>—<br>—<br>—<br><br>—<br>—<br>— | <br>14<br>8<br>6<br><br>6<br>3<br>1 | dB | 1, 2 |

**Table 60. Differential Transmitter (TX) Output Characteristics (continued)**

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| TX Common Mode Return loss<br>150 MHz - 300 MHz<br>300 MHz - 600 MHz<br>600 MHz - 1.2 GHz<br><br>1.2 GHz - 2.4 GHz<br>2.4 GHz - 3.0 GHz<br>3.0 GHz - 5.0 GHz | $RL_{SATA_TXCC11}$ | <br><br>—<br>—<br>—<br><br><br>—<br>—<br>— | <br><br>—<br>—<br>—<br><br><br>—<br>—<br>— | <br><br>5<br>5<br>2<br><br><br>2<br>1<br>1 | <br><br>dB | <br><br>1, 2 |
| TX Impedance Balance<br><br>150 MHz - 300 MHz<br>300 MHz - 600 MHz<br>600 MHz - 1.2 GHz<br><br>1.2 GHz - 2.4 GHz<br>2.4 GHz - 3.0 GHz<br>3.0 GHz - 5.0 GHz | $RL_{SATA_TXDC11}$ | <br><br>—<br>—<br>—<br><br><br>—<br>—<br>— | <br><br>—<br>—<br>—<br><br><br>—<br>—<br>— | <br><br>30<br>20<br>10<br><br><br>10<br>4<br>4 | <br><br>dB | <br><br>1, 2 |
| Deterministic jitter<br>1.5G<br>3.0G | $U_{SATA_TXDJ}$ | — | — | <br>0.18<br>0.14 | UI | — |
| Total Jitter<br>1.5G<br>3.0G | $U_{SATA_TXTJ}$ | — | — | <br>0.42<br>0.32 | UI | — |

**Notes:**
1. Only applies when operating in 3.0Gb data rate mode.
2. The max value stated for 3.0 GHz - 5.0 GHz range only applies to Gen2i mode and not to Gen2m mode.
3. Only applies to Gen1i mode.

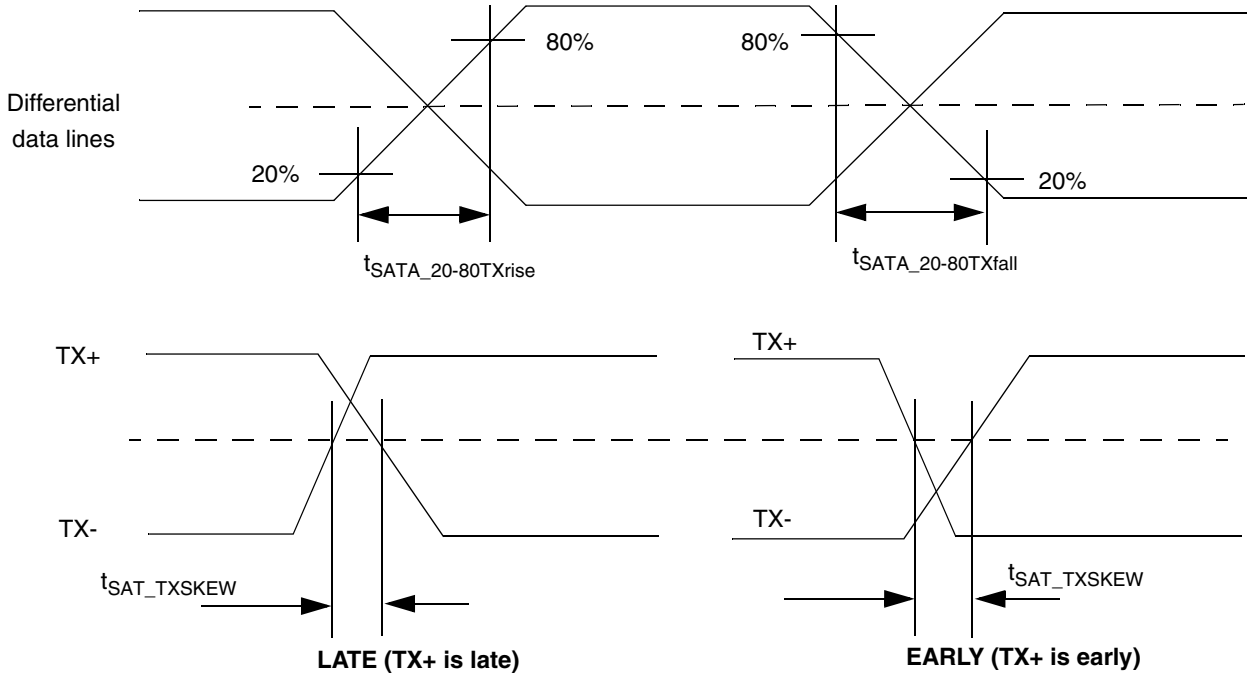



**Figure 50. Signal Rise and Fall Times and Differential Skew**

## 2.16.3 Differential Receiver (RX) Input Characteristics

This table provides the differential receiver (RX) input characteristics for the SATA interface.

**Table 61. Differential Receiver (RX) Input Characteristics**

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| RX Differential Input Voltage<br>1.5G<br>3.0G | $V_{SATA_RXDIFF}$ | <br>240<br>240 | <br>400<br>— | <br>600<br>750 | mVp-p | 1 |
| RX rise/fall time<br>1.5G<br>3.0G | $t_{SATA_20\text{-}80RX}$ | 100<br>67 | —<br>— | 273<br>136 | ps | — |
| RX Differential skew<br>1.5G<br>3.0G | $t_{SATA_RXSKEW}$ | —<br>— | —<br>— | —<br>50 | ps | — |
| RX Differential pair impedance<br>1.5G | $Z_{SATA_RXDIFFIM}$ | 85 | — | 115 | ohm | — |
| RX Single-Ended impedance<br>1.5G | $Z_{SATA_RXSEIM}$ | 40 | — | — | ohm | — |
| DC Coupled Common Mode Voltage | $V_{dc_cm}$ | 200 | 250 | 450 | mV | 5 |

**Table 61. Differential Receiver (RX) Input Characteristics (continued)**

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| RX Differential Mode Return loss<br>150 MHz - 300 MHz<br>300 MHz - 600 MHz<br>600 MHz - 1.2 GHz<br><br>1.2 GHz - 2.4 GHz<br>2.4 GHz - 3.0 GHz<br>3.0 GHz - 5.0 GHz | $RL_{SATA_RXDD11}$ | <br><br>—<br>—<br>—<br><br>—<br>—<br>— | <br><br>—<br>—<br>—<br><br>—<br>—<br>— | <br><br>18<br>14<br>10<br><br>8<br>3<br>1 | dB | 2, 3 |
| RX Common Mode Return loss<br>150 MHz - 300 MHz<br>300 MHz - 600 MHz<br>600 MHz - 1.2 GHz<br><br>1.2 GHz - 2.4 GHz<br>2.4 GHz - 3.0 GHz<br>3.0 GHz - 5.0 GHz | $RL_{SATA_RXCC11}$ | <br><br>—<br>—<br>—<br><br>—<br>—<br>— | <br><br>—<br>—<br>—<br><br>—<br>—<br>— | <br><br>5<br>5<br>2<br><br>2<br>2<br>1 | dB | 2, 3, 4 |
| RX Impedance Balance<br><br>150 MHz - 300 MHz<br>300 MHz - 600 MHz<br>600 MHz - 1.2 GHz<br><br>1.2 GHz - 2.4 GHz<br>2.4 GHz - 3.0 GHz<br>3.0 GHz - 5.0 GHz | $RL_{SATA_RXDC11}$ | <br><br>—<br>—<br>—<br><br>—<br>—<br>— | <br><br>—<br>—<br>—<br><br>—<br>—<br>— | <br><br>30<br>30<br>20<br><br>10<br>4<br>4 | dB | 2, 3 |
| Deterministic jitter<br>1.5G<br>3.0G | $U_{SATA_RXDJ}$ | — | — | <br>0.4<br>0.47 | UI | — |
| Total Jitter<br>1.5G<br>3.0G | $U_{SATA_RXTJ}$ | — | — | <br>0.65<br>0.65 | UI | — |

**Notes:**
1. The min values apply only to Gen1m, and Gen2m. the min values for Gen1i is 325 mVp-p and for Gen2i is 275 mVp-p.
2. Only applies when operating in 3.0Gb data rate mode.
3. The max value stated for 3.0 GHz - 5.0 GHz range only applies to Gen2i mode and not to Gen2m mode.
4. The max value stated for 2.4 GHz - 3.0 GHz range only applies to Gen2i mode for Gen2m the value is 1.
5. Only applies to Gen1i mode.

## 2.16.4 Out-of-Band (OOB) Electrical Characteristics

This table provides the Out-of-Band (OOB) electrical characteristics for the SATA interface of the chip.

**Table 62. Out-of-Band (OOB) Electrical Characteristics**

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| OOB Signal Detection Threshold<br>1.5G<br>3.0G | $V_{SATA_OOBDETE}$ | <br>50<br>75 | <br>100<br>125 | <br>200<br>200 | <br>mVp-p | — |
| UI During OOB Signaling | $T_{SATA_UIOOB}$ | 646.67 | 666.67 | 686.67 | ps | — |
| COMINIT/ COMRESET and COMWAKE Transmit Burst Length | $T_{SATA_UIOOBTXB}$ | — | 160 | — | UI | — |
| COMINIT/ COMRESET Transmit Gap Length | $T_{SATA_UIOOBTXGap}$ | — | 480 | — | UI | — |
| COMWAKE Transmit Gap Length | $T_{SATA_UIOOBTXWakeGap}$ | — | 160 | — | UI | — |
| COMWAKE Gap Detection Windows | $T_{SATA_OOBDetWakeGap}$ | 55 | — | 175 | ns | — |
| COMINIT/ COMRESET<br>Gap Detection Windows | $T_{SATA_OOBDetCOMGap}$ | 175 | — | 525 | ns | — |

# 2.17 $I^2C$

This section describes the DC and AC electrical characteristics for the $I^2C$ interfaces of the chip.

## 2.17.1 $I^2C$ DC Electrical Characteristics

This table provides the DC electrical characteristics for the $I^2C$ interfaces.

**Table 63. $I^2C$ DC Electrical Characteristics**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage 3.3 V | $OV_{DD}$ | 3.13 | 3.47 | V | — |
| Input high voltage level | $V_{IH}$ | $0.7 \times OV_{DD}$ | $OV_{DD} + 0.3$ | V | — |
| Input low voltage level | $V_{IL}$ | –0.3 | $0.3 \times OV_{DD}$ | V | — |
| Low level output voltage | $V_{OL}$ | 0 | $0.2 \times OV_{DD}$ | V | 1 |

**Table 63. I²C DC Electrical Characteristics (continued)**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Pulse width of spikes which must be suppressed by the input filter | $t_{I2KHKL}$ | 0 | 50 | ns | 2 |
| Input current each I/O pin (input voltage is between 0.1 × $OV_{DD}$ and 0.9 × $OV_{DD}$(max) | $I_I$ | –10 | 10 | μA | 3 |
| Capacitance for each I/O pin | $C_I$ | — | 10 | pF | — |

**Notes:**

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if $OV_{DD}$ is switched off.

## 2.17.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interfaces.

**Table 64. I²C AC Electrical Specifications**

All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 63).

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| SCL clock frequency | $f_{I2C}$ | 0 | 400 | kHz | — |
| Low period of the SCL clock | $t_{I2CL}$ | 1.3 | — | μs | — |
| High period of the SCL clock | $t_{I2CH}$ | 0.6 | — | μs | — |
| Setup time for a repeated START condition | $t_{I2SVKH}$ | 0.6 | — | μs | — |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | $t_{I2SXKL}$ | 0.6 | — | μs | — |
| Data setup time | $t_{I2DVKH}$ | 100 | — | ns | — |
| Data hold time:<br>CBUS compatible masters<br>I²C bus devices | $t_{I2DXKL}$ | <br>—<br>0 | <br>—<br>— | μs | 2 |
| Data output delay time | $t_{I2OVKL}$ | — | 0.9 | μs | 3 |
| Set-up time for STOP condition | $t_{I2PVKH}$ | 0.6 | — | μs | — |
| Rise time of both SDA and SCL signals | $t_{I2CR}$ | — | 300 | ns | 4 |
| Fall time of both SDA and SCL signals | $t_{I2CF}$ | — | 300 | ns | 4 |

**Table 64. I²C AC Electrical Specifications (continued)**

All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 63).

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Bus free time between a STOP and START condition | $t_{I2KHDX}$ | 1.3 | — | μs | — |
| Noise margin at the LOW level for each connected device (including hysteresis) | $V_{NL}$ | $0.1 \times OV_{DD}$ | — | V | — |
| Noise margin at the HIGH level for each connected device (including hysteresis) | $V_{NH}$ | $0.2 \times OV_{DD}$ | — | V | — |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{I2DVKH}$ symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{I2SXKL}$ symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the $t_{I2C}$ clock reference (K) going to the low (L) state or hold time. Also, $t_{I2PVKH}$ symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the Vihmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the chip acts as the I²C bus master while transmitting, the chip drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. For details of the I²C frequency calculation, refer to *Determining the I²C Frequency Divider Ratio for SCL* (AN2919). Note that the I²C Source Clock Frequency is half of the CCB clock frequency for the chip.
3. The maximum $t_{I2DVKH}$ has only to be met if the chip does not stretch the LOW period ($t_{I2CL}$) of the SCL signal.
4. $C_B$ = capacitance of one bus line in pF.

This figure provides the AC test load for the I²C.

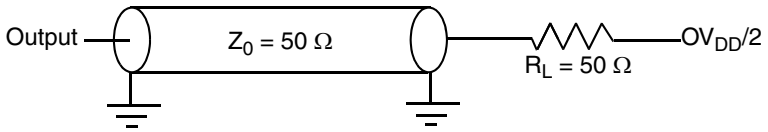



**Figure 51. I²C AC Test Load**

This figure shows the AC timing diagram for the I²C bus.

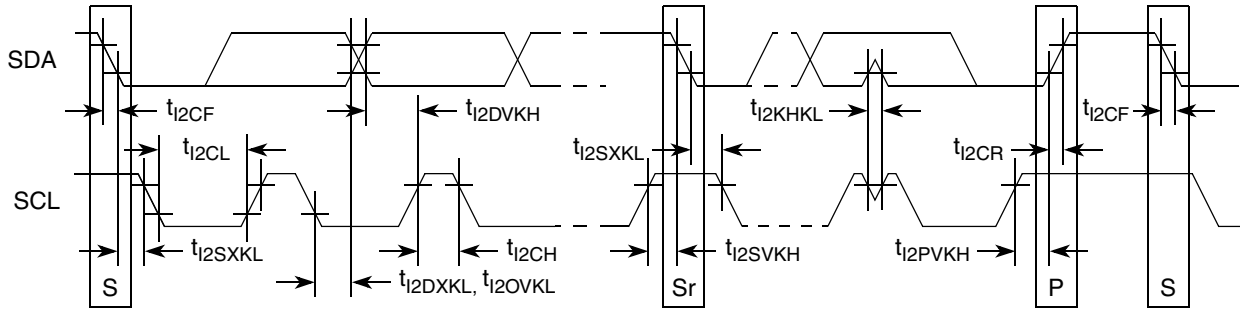



**Figure 52. I²C Bus AC Timing Diagram**

## 2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the chip.

### 2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface.

**Table 65. GPIO DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | – 0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V |

**Note:**

1. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

### 2.18.2 GPIO AC Electrical Specifications

This table provides the GPIO input and output AC timing specifications.

**Table 66. GPIO Input and Output AC Timing Specifications[1]**

| Characteristic | Symbol [2] | Min | Unit | Notes |
|---|---|---|---|---|
| GPIO inputs—minimum pulse width | $t_{PIWID}$ | 7.5 | ns | 3 |
| GPIO outputs—minimum pulse width | $t_{GTOWID}$ | 12 | ns | — |

**Notes:**

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least $t_{PIWID}$ ns to ensure proper operation.
3. The minimum pulse width is a function of the MPX/Platform clock. The minimum pulse width must be greater than or equal to 4 times the MPX/Platform clock period.

This figure provides the AC test load for the GPIO.

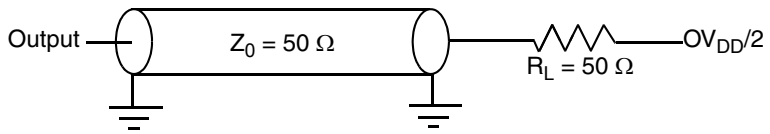



**Figure 53. GPIO AC Test Load**

# 2.19 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the chip.

## 2.19.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

**Table 67. PCI DC Electrical Characteristics [1]**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$ [2] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V |

**Notes:**

1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 2.19.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. This table provides the PCI AC timing specifications at 66 MHz.

**Table 68. PCI AC Timing Specifications at 66 MHz**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| SYSCLK to output valid | $t_{PCKHOV}$ | — | 6.0 | ns | 2, 3 |
| Output hold from SYSCLK | $t_{PCKHOX}$ | 2.0 | — | ns | 2 |
| SYSCLK to output high impedance | $t_{PCKHOZ}$ | — | 14 | ns | 2, 4 |
| Input setup to SYSCLK | $t_{PCIVKH}$ | 3.0 | — | ns | 2, 5 |
| Input hold from SYSCLK | $t_{PCIXKH}$ | 0 | — | ns | 2, 5 |
| $\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time | $t_{PCRVRH}$ | 10 × $t_{SYS}$ | — | clocks | 6, 7 |
| $\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time | $t_{PCRHRX}$ | 0 | 50 | ns | 7 |

**Table 68. PCI AC Timing Specifications at 66 MHz (continued)**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion | $t_{PCRHFV}$ | 10 | — | clocks | 8 |
| Rise time (20%–80%) | $t_{PCICLK}$ | 0.6 | 2.1 | ns | — |
| Failing time (20%–80%) | $t_{PCICLK}$ | 0.6 | 2.1 | ns | — |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{PCIVKH}$ symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, $t_{SYS}$, reference (K) going to the high (H) state or setup time. Also, $t_{PCRHFV}$ symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter $t_{SYS}$ indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 22, "Clocking."
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter $t_{PCRHFV}$ is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 μs.

This figure provides the AC test load for PCI.

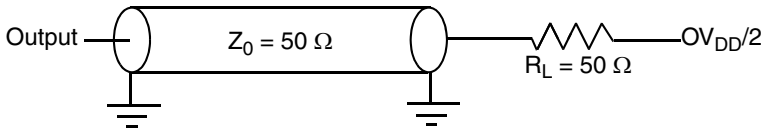



**Figure 54. PCI AC Test Load**

This figure shows the PCI input AC timing conditions.

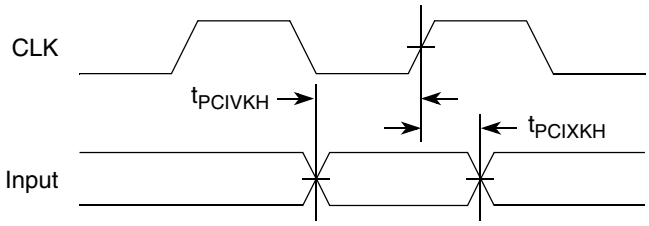



**Figure 55. PCI Input AC Timing Measurement Conditions**

This figure shows the PCI output AC timing conditions.

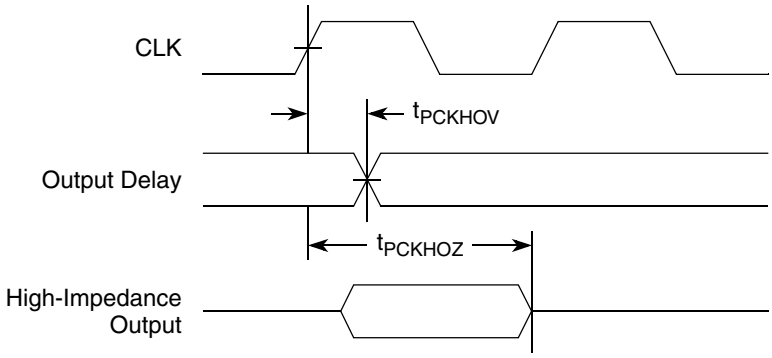



**Figure 56. PCI Output AC Timing Measurement Condition**

## 2.20 High-Speed Serial Interfaces

This chip features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface is dedicated for PCI Express data transfers. The SerDes2 can be used for SGMII or SATA.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

### 2.20.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 57 shows how the signals are defined. For illustration purposes, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SDn_TX and $\overline{\text{SDn_TX}}$) or a receiver input (SDn_RX and $\overline{\text{SDn_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

The transmitter output signals and the receiver input signals SDn_TX, $\overline{\text{SDn_TX}}$, SDn_RX and $\overline{\text{SDn_RX}}$ each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, $V_{OD}$** (or **Differential Output Swing**):

The Differential Output Voltage (or Swing) of the transmitter, $V_{OD}$, is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The $V_{OD}$ value can be either positive or negative.

3. **Differential Input Voltage, $V_{ID}$** (or **Differential Input Swing**):

The Differential Input Voltage (or Swing) of the receiver, $V_{ID}$, is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The $V_{ID}$ value can be either positive or negative.

4. **Differential Peak Voltage, $V_{DIFFp}$**

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential

peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

6. **Common Mode Voltage, $V_{cm}$**

The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = V_{SDn_TX} + V_{\overline{SDn_TX}} = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

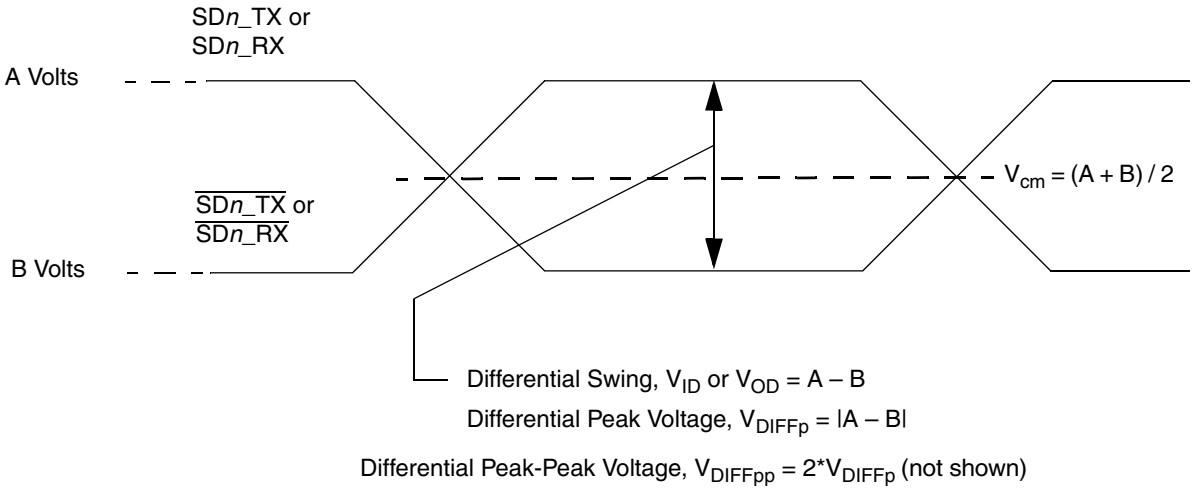



**Figure 57. Differential Voltage Definitions for Transmitter or Receiver**

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing ($V_{OD}$) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, $V_{OD}$ is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage ($V_{DIFFp}$) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

## 2.20.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks for PCI Express are SD1_REF_CLK and, $\overline{SD1_REF_CLK}$. The SerDes reference clocks for the SATA and SGMII interfaces are SD2_REF_CLK and, $\overline{SD2_REF_CLK}$.

The following sections describe the SerDes reference clock requirements and some application information.

### 2.20.2.1 SerDes Reference Clock Receiver Characteristics

Figure 58 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $X2V_{DD}$ are specified in Table 2 and Table 3.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SDn_REF_CLK and $\overline{SDn_REF_CLK}$ are internally AC-coupled differential inputs as shown in Figure 58. Each differential clock input (SD*n*_REF_CLK or $\overline{SDn_REF_CLK}$) has a 50-Ω termination to SGND (xcorevss) followed by on-chip AC-coupling.

— The external reference clock driver must be able to drive this termination.
— The SerDes reference clock input can be either differential or single-ended. See the Differential Mode and Single-ended Mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1V above SnGND (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800mV with the common mode voltage at 400mV.
  — If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ inputs cannot drive 50 Ω to SnGND (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  — This requirement is described in detail in the following sections.

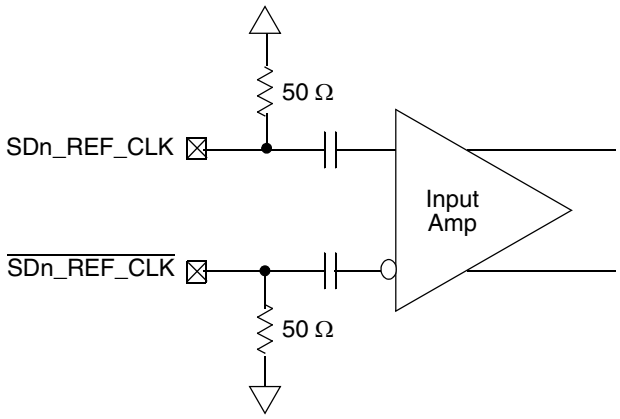



**Figure 58. Receiver of SerDes Reference Clocks**

### 2.20.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the chip's SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400mV and 1600mV differential peak-peak (or between 200mV and 800mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800mV and greater than 200mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in Section 2.20.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 59 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SnGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SnGND). Figure 60 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SDn_REF_CLK input amplitude (single-ended swing) must be between 400mV and 800mV peak-peak (from Vmin to Vmax) with $\overline{\text{SDn_REF_CLK}}$ either left unconnected or tied to ground.
  - The SDn_REF_CLK input average voltage must be between 200 and 400 mV. Figure 61 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SDn_REF_CLK}}$) through the same source impedance as the clock input (SDn_REF_CLK) in use.

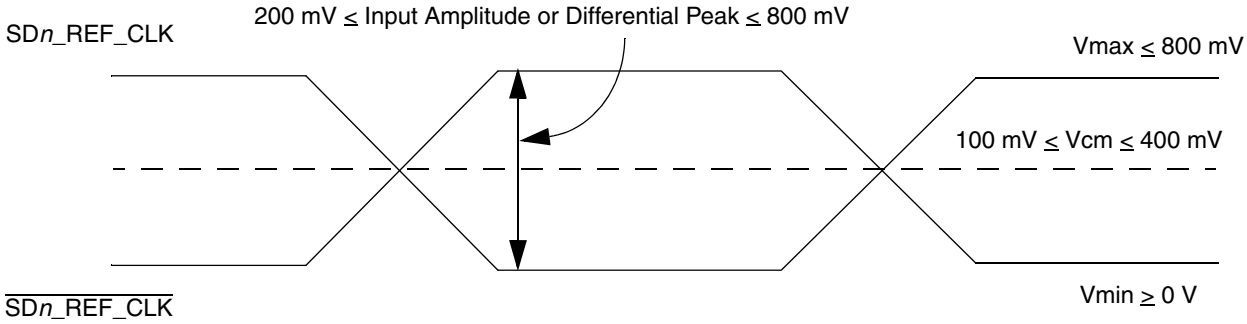



**Figure 59. Differential Reference Clock Input DC Requirements (External DC-Coupled)**

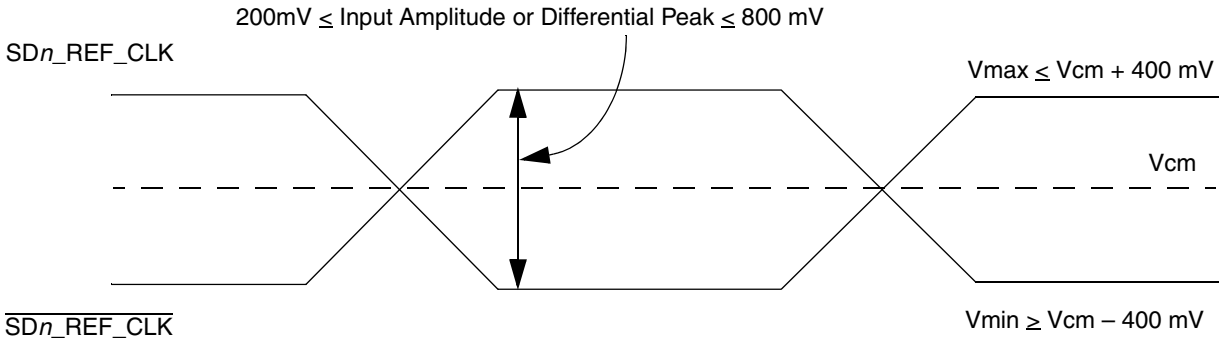



**Figure 60. Differential Reference Clock Input DC Requirements (External AC-Coupled)**

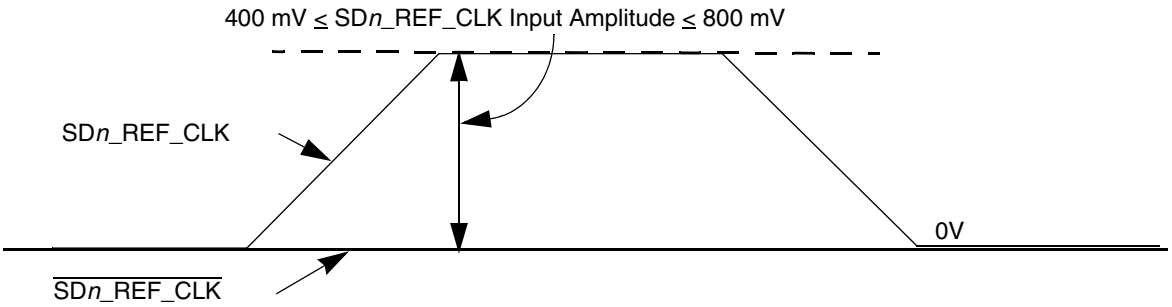



**Figure 61. Single-Ended Reference Clock Input DC Requirements**

### 2.20.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SnGND (xcorevss), the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL (Low Voltage Positive Emitter-Coupled Logic) outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

**NOTE**

Figure 62 to Figure 65 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the chip's SerDes reference clock receiver requirement provided in this document.

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with chip's SerDes reference clock input's DC requirement.

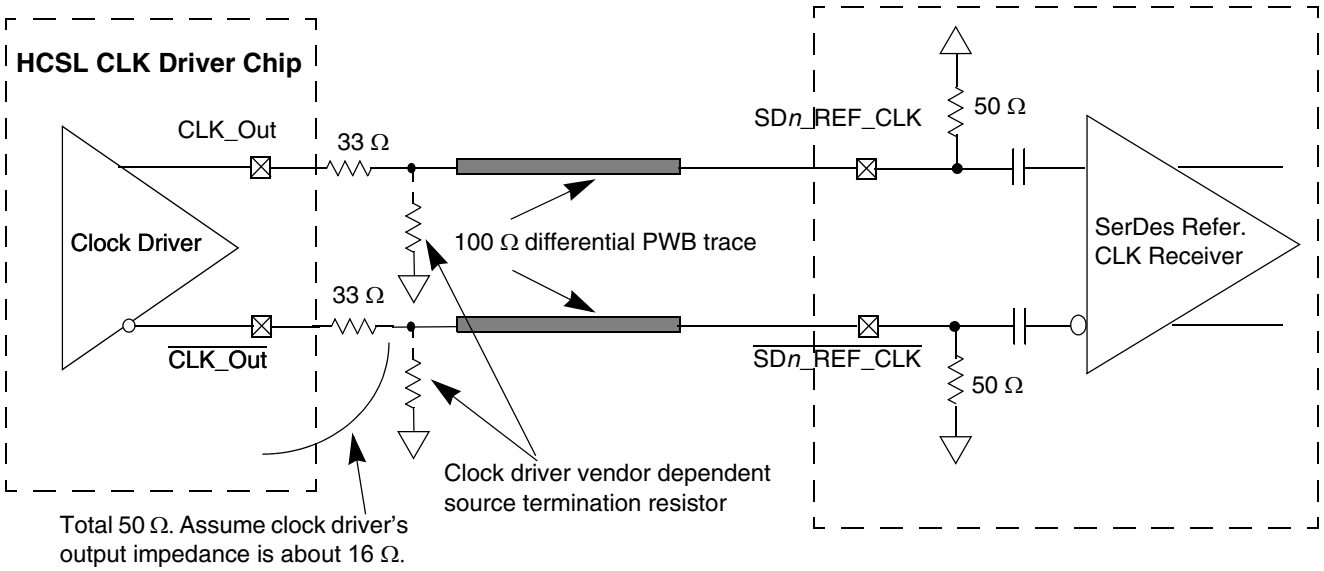



**Figure 62. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)**

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the chip's SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

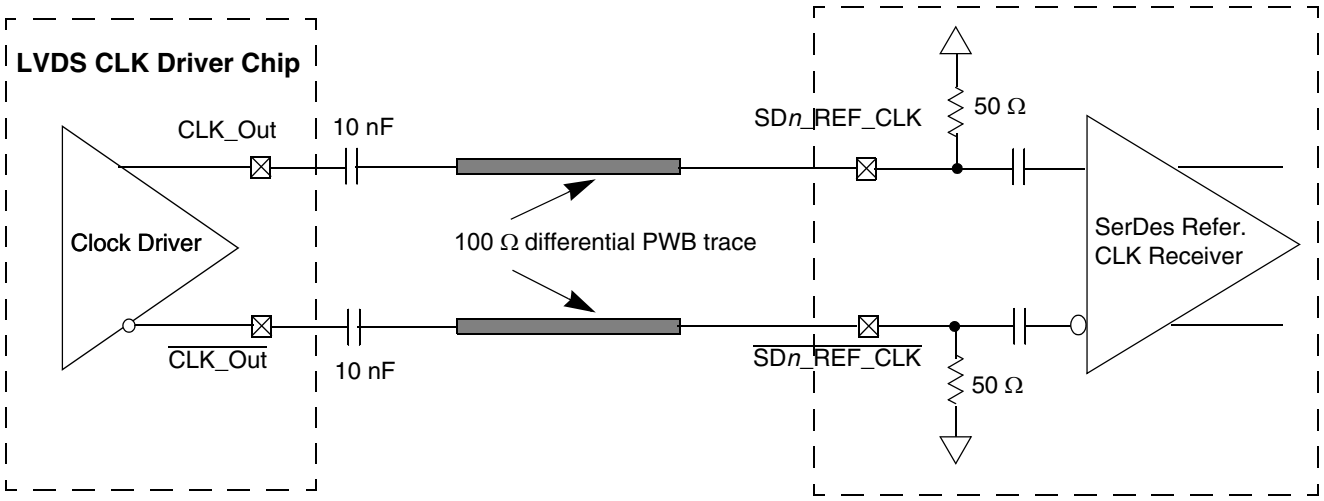



**Figure 63. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)**

This figure shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with chip's SerDes reference clock input's DC requirement, AC-coupling has to be used. This figure assumes that the LVPECL clock driver's output impedance is 50Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140Ω to 240Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the chip's SerDes reference clock's differential input amplitude requirement (between 200mV and 800mV differential peak). For example, if the LVPECL output's differential peak is 900mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

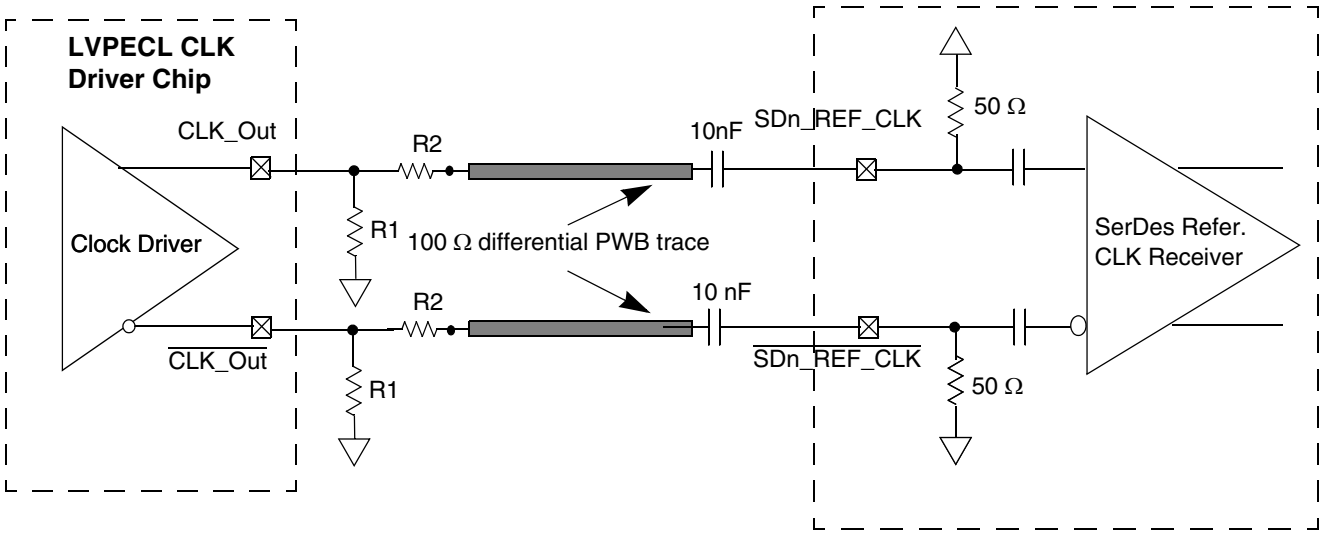



**Figure 64. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)**

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with chip's SerDes reference clock input's DC requirement.

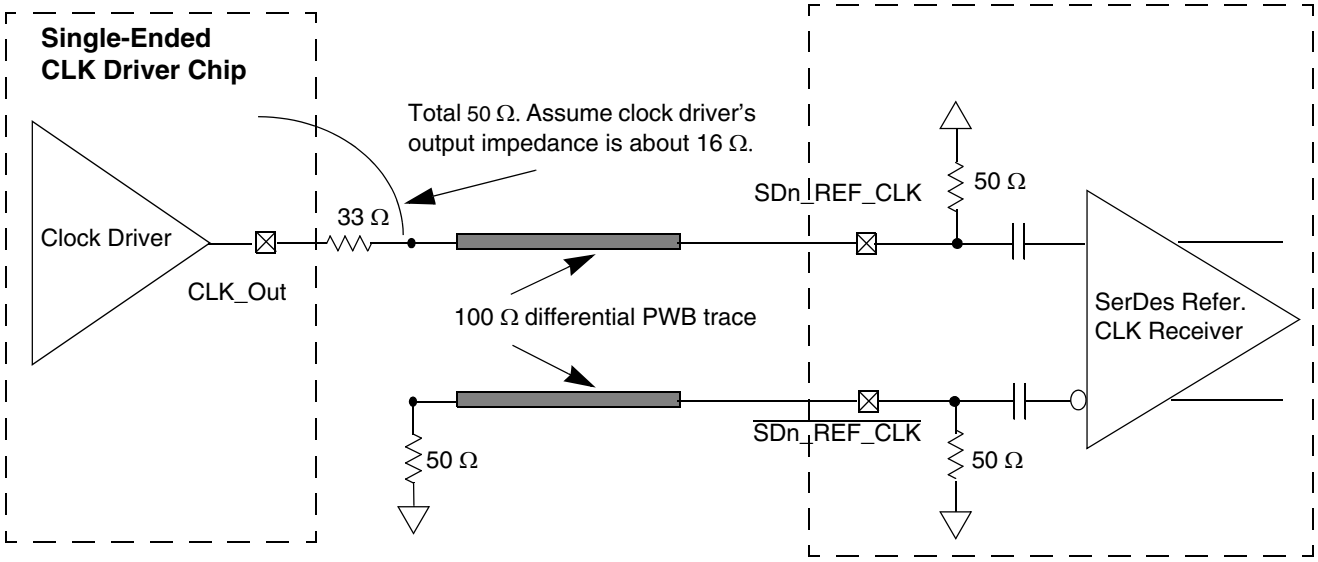



**Figure 65. Single-Ended Connection (Reference Only)**

### 2.20.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15MHz is filtered by the PLL. The most problematic phase noise occurs in the 1-15MHz range. The source impedance of the clock driver should be 50 ohms to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters common to SGMII and PCI Express protocols.

**Table 69. SerDes Reference Clock Common AC Parameters**

At recommended operating conditions with $XV_{DD_SRDS1}$ or $XV_{DD_SRDS2}$ = 1.0V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Rising Edge Rate | Rise Edge Rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Falling Edge Rate | Fall Edge Rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Differential Input High Voltage | $V_{IH}$ | +200 | — | mV | 2 |
| Differential Input Low Voltage | $V_{IL}$ | — | –200 | mV | 2 |
| Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn_REF_CLK}}$) matching | Rise-Fall Matching | — | 20 | % | 1, 4 |

**Notes:**

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{\text{SDn_REF_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 66.
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for $\overline{\text{SDn_REF_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SDn_REF_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SDn_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SDn_REF_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 67.

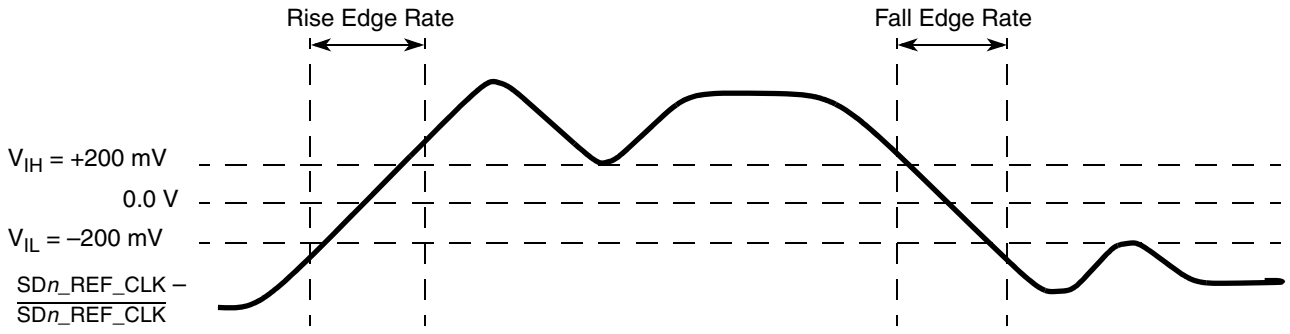



**Figure 66. Differential Measurement Points for Rise and Fall Time**

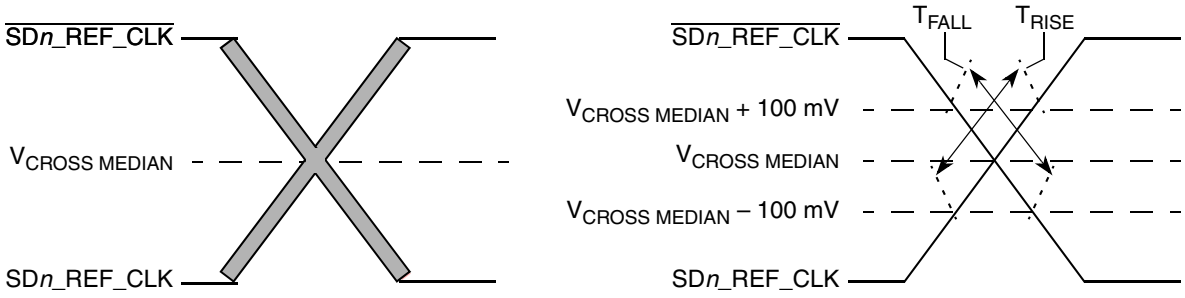



**Figure 67. Single-Ended Measurement Points for Rise and Fall Time Matching**

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. See the following sections for detailed information:

- Section 2.9.3.2, "AC Requirements for SGMII SD2_REF_CLK and SD2_REF_CLK"
- Section 2.21.2, "AC Requirements for PCI Express SerDes Clocks"

#### 2.20.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/$\overline{\text{SD1_REF_CLK}}$ were designed to work with a spread spectrum clock (+0 to -0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/$\overline{\text{SD2_REF_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

### 2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

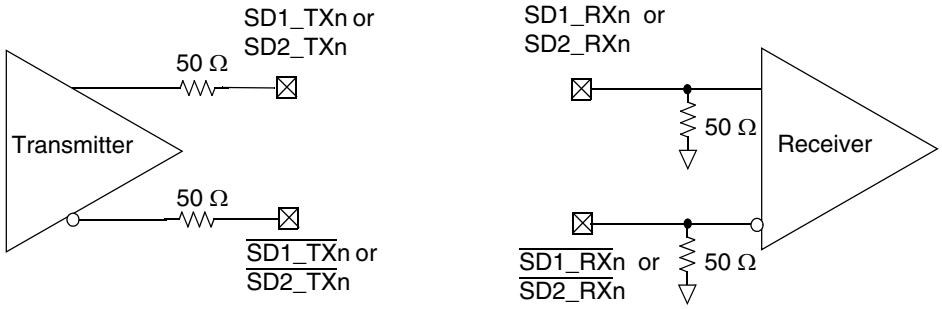



**Figure 68. SerDes Transmitter and Receiver Reference Circuits**

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, SATA or SGMII) in this document based on the application usage:

- Section 2.9.3, "SGMII Interface Electrical Characteristics"
- Section 2.21, "PCI Express"
- Section 2.16, "Serial ATA (SATA)"

Please note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

## 2.21 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the chip.

### 2.21.1 DC Requirements for PCI Express SD1_REF_CLK and $\overline{\text{SD1_REF_CLK}}$

For more information, see Section 2.20.2, "SerDes Reference Clocks."

### 2.21.2 AC Requirements for PCI Express SerDes Clocks

This table lists AC requirements.

**Table 70. SD1_REF_CLK and $\overline{\text{SD1_REF_CLK}}$ AC Requirements**

| Symbol | Parameter Description | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time | — | 10 | — | ns | 1 |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 100 | ps | — |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location | –50 | — | 50 | ps | 1,2,3 |

**Notes:**
1. Tj at BER of 10E-6 86 ps Max.
2. Total peak-to-peak deterministic jitter "Dj" should be less than or equal to 42 ps.
3. Limits from "PCI Express CEM Rev 2.0" and measured per "PCI Express Rj, D, and Bit Error Rates".

### 2.21.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million 15 (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

### 2.21.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this chip. For further details as well as the specifications of the transport and data link layer, please use the PCI Express Base Specification. REV. 1.0a document.

#### 2.21.4.1 Differential Transmitter (TX) Output

This table defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

**Table 71. Differential Transmitter (TX) Output Specifications**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| UI | Unit Interval | 399.88 | 400 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1. |
| $V_{TX\text{-}DIFFp\text{-}p}$ | Differential Peak-to-Peak Output Voltage | 0.8 | — | 1.2 | V | $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ See Note 2. |

**Table 71. Differential Transmitter (TX) Output Specifications (continued)**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $V_{TX\text{-}DE\text{-}RATIO}$ | De- Emphasized Differential Output Voltage (Ratio) | –3.0 | –3.5 | –4.0 | dB | Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 2. |
| $T_{TX\text{-}EYE}$ | Minimum TX Eye Width | 0.70 | — | — | UI | The maximum Transmitter jitter can be derived as $T_{TX\text{-}MAX\text{-}JITTER}$ = 1 – $T_{TX\text{-}EYE}$= 0.3 UI. See Notes 2 and 3. |
| $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ | Maximum time between the jitter median and maximum deviation from the median. | — | — | 0.15 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3. |
| $T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$ | D+/D- TX Output Rise/Fall Time | 0.125 | — | — | UI | See Notes 2 and 5 |
| $V_{TX\text{-}CM\text{-}ACp}$ | RMS AC Peak Common Mode Output Voltage | — | — | 20 | mV | $V_{TX\text{-}CM\text{-}ACp}$ = RMS($\lvert V_{TXD+} + V_{TXD-}\rvert/2 - V_{TX\text{-}CM\text{-}DC}$)<br>$V_{TX\text{-}CM\text{-}DC}$ = $DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$<br>See Note 2 |
| $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$ | Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle | 0 | — | 100 | mV | $\lvert V_{TX\text{-}CM\text{-}DC\ (during\ L0)} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ (During\ Electrical\ Idle)}\rvert$<=100 mV<br>$V_{TX\text{-}CM\text{-}DC}$ = $DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ [L0]<br>$V_{TX\text{-}CM\text{-}Idle\text{-}DC}$ = $DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ [Electrical Idle]<br>See Note 2. |
| $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ | Absolute Delta of DC Common Mode between D+ and D– | 0 | — | 25 | mV | $\lvert V_{TX\text{-}CM\text{-}DC\text{-}D+} - V_{TX\text{-}CM\text{-}DC\text{-}D-}\rvert$ <= 25 mV<br>$V_{TX\text{-}CM\text{-}DC\text{-}D+}$ = $DC_{(avg)}$ of $\lvert V_{TX\text{-}D+}\rvert$<br>$V_{TX\text{-}CM\text{-}DC\text{-}D-}$ = $DC_{(avg)}$ of $\lvert V_{TX\text{-}D-}\rvert$<br>See Note 2. |
| $V_{TX\text{-}IDLE\text{-}DIFFp}$ | Electrical Idle differential Peak Output Voltage | 0 | — | 20 | mV | $V_{TX\text{-}IDLE\text{-}DIFFp}$ = $\lvert V_{TX\text{-}IDLE\text{-}D+} - V_{TX\text{-}IDLE\text{-}D-}\rvert$ <= 20 mV<br>See Note 2. |
| $V_{TX\text{-}RCV\text{-}DETECT}$ | The amount of voltage change allowed during Receiver Detection | — | — | 600 | mV | The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6. |
| $V_{TX\text{-}DC\text{-}CM}$ | The TX DC Common Mode Voltage | 0 | — | 3.6 | V | The allowed DC Common Mode voltage under any conditions. See Note 6. |
| $I_{TX\text{-}SHORT}$ | TX Short Circuit Current Limit | — | — | 90 | mA | The total current the Transmitter can provide when shorted to its ground |
| $T_{TX\text{-}IDLE\text{-}MIN}$ | Minimum time spent in Electrical Idle | 50 | — | — | UI | Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set |

**Table 71. Differential Transmitter (TX) Output Specifications (continued)**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $T_{TX-IDLE-SET-TO-IDLE}$ | Maximum time to transition to a valid electrical idle after sending an electrical Idle ordered set | — | — | 20 | UI | After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0. |
| $T_{TX-IDLE-TO-DIFF-DATA}$ | Maximum time to transition to valid TX specifications after leaving an electrical idle condition | — | — | 20 | UI | Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle |
| $RL_{TX-DIFF}$ | Differential Return Loss | 12 | — | — | dB | Measured over 50 MHz to 1.25 GHz. See Note 4 |
| $RL_{TX-CM}$ | Common Mode Return Loss | 6 | — | — | dB | Measured over 50 MHz to 1.25 GHz. See Note 4 |
| $Z_{TX-DIFF-DC}$ | DC Differential TX Impedance | 80 | 100 | 120 | Ω | TX DC Differential mode Low Impedance |
| $Z_{TX-DC}$ | Transmitter DC Impedance | 40 | — | — | Ω | Required TX D+ as well as D- DC Impedance during all states |
| $L_{TX-SKEW}$ | Lane-to-Lane Output Skew | — | — | 500 + 2 UI | ps | Static skew between any two Transmitter Lanes within a single Link |
| $C_{TX}$ | AC Coupling Capacitor | 75 | — | 200 | nF | All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8. |
| $T_{crosslink}$ | Crosslink Random Timeout | 0 | — | 1 | ms | This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note 7. |

**Notes:**

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 52 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 50)
3. A $T_{TX-EYE}$ = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 52). Note that the series capacitors $C_{TX}$ is optional for the return loss measurement.
5. Measured between 20-80% at transmitter package pins into a test load as shown in Figure 52 for both $V_{TX-D+}$ and $V_{TX-D-}$.
6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a
7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a
8. SerDes transmitter does not have $C_{TX}$ built-in. An external AC Coupling capacitor is required.

### 2.21.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 69 is specified using the passive compliance/test measurement load (see Figure 71) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**NOTE**

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

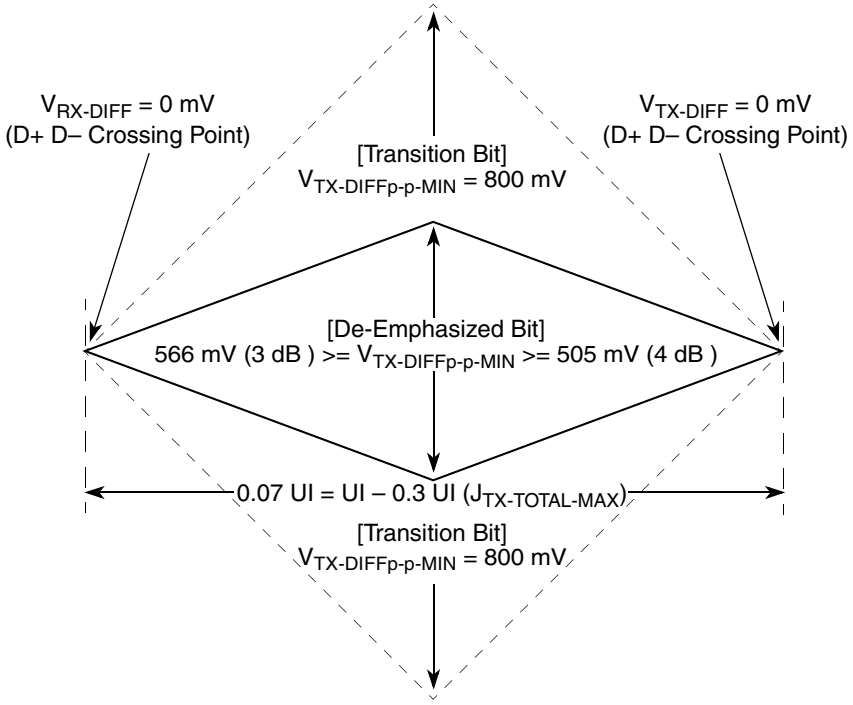



**Figure 69. Minimum Transmitter Timing and Voltage Output Compliance Specifications**

### 2.21.4.3 Differential Receiver (RX) Input Specifications

This table defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

**Table 72. Differential Receiver (RX) Input Specifications**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| UI | Unit Interval | 399.88 | 400 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1. |
| $V_{RX-DIFFp-p}$ | Differential Peak-to-Peak Output Voltage | 0.175 | — | 1.200 | V | $V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ See Note 2. |
| $T_{RX-EYE}$ | Minimum Receiver Eye Width | 0.4 | — | — | UI | The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3. |
| $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and maximum deviation from the median. | — | — | 0.3 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7. |
| $V_{RX-CM-ACp}$ | AC Peak Common Mode Input Voltage | — | — | 150 | mV | $V_{RX-CM-ACp} = \|V_{RXD+} - V_{RXD-}\|/2 + V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\|V_{RX-D+} + V_{RX-D-}\|/2$ See Note 2 |
| $RL_{RX-DIFF}$ | Differential Return Loss | 15 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and –300 mV, respectively. See Note 4 |
| $RL_{RX-CM}$ | Common Mode Return Loss | 6 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4 |
| $Z_{RX-DIFF-DC}$ | DC Differential Input Impedance | 80 | 100 | 120 | Ω | RX DC Differential mode impedance. See Note 5 |
| $Z_{RX-DC}$ | DC Input Impedance | 40 | 50 | 60 | Ω | Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 2 and 5. |
| $Z_{RX-HIGH-IMP-DC}$ | Powered Down DC Input Impedance | 200 k | — | — | Ω | Required RX D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 6. |
| $V_{RX-IDLE-DET-DIFFp-p}$ | Electrical Idle Detect Threshold | 65 | — | 175 | mV | $V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ Measured at the package pins of the Receiver |
| $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ | Unexpected Electrical Idle Enter Detect Threshold Integration Time | — | — | 10 | ms | An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition. |

**Table 72. Differential Receiver (RX) Input Specifications (continued)**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $L_{TX-SKEW}$ | Total Skew | — | — | 20 | ns | Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself. |

**Notes:**
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 71 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 70). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 71). Note: that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

## 2.22 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 70 is specified using the passive compliance/test measurement load (see Figure 71) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 71) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 70) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**NOTE**

The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50. probes—see Figure 71). Note that the series capacitors, CTX, are optional for the return loss measurement.

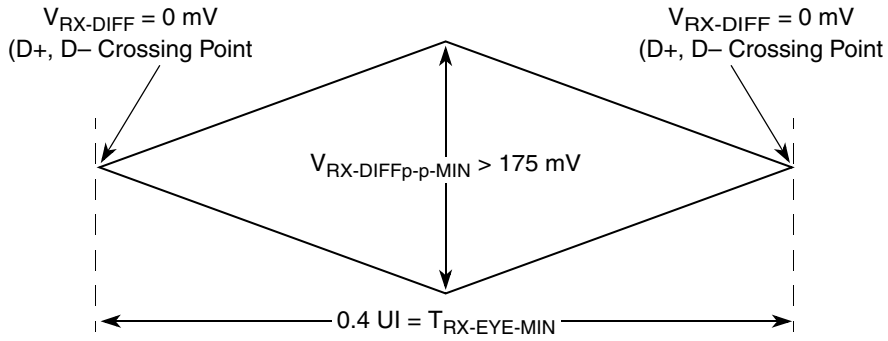



**Figure 70. Minimum Receiver Eye Timing and Voltage Compliance Specification**

## 2.22.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in the following figure.

**NOTE**

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

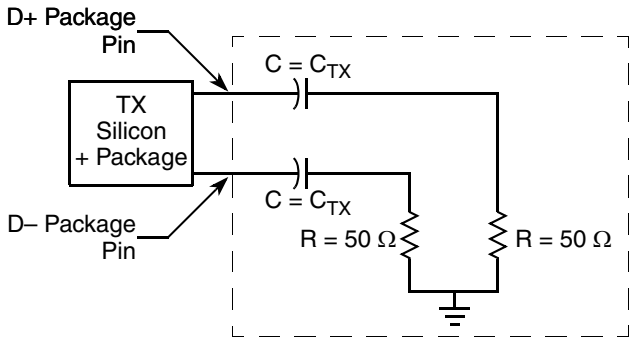



**Figure 71. Compliance Test/Measurement Load**

# 2.23 Clocking

This section describes the PLL configuration of the chip. Note that the platform clock is identical to the core complex bus (CCB) clock.

## 2.23.1 Clock Ranges

This table provides the clocking specifications for the processor cores and Table 74 provides the clocking specifications for the memory bus.

**Table 73. Processor Core Clocking Specifications**

| Characteristic | Maximum Processor Core Frequency | | | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | 600 MHz | | 800 MHz | | 1000 MHz | | 1250 MHz | | | |
| | Min | Max | Min | Max | Min | Max | Min | Max | | |
| e500 core processor frequency | 600 | 600 | 600 | 800 | 600 | 1000 | 600 | 1250 | MHz | 1, 2, 3 |
| CCB frequency | 400 | 400 | 400 | 400 | 333 | 400 | 333 | 500 | | |
| DDR Data Rate | 400 | 400 | 400 | 400 | 400 | 400 | 400 | 667 | | |

**Notes**:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 2.23.2, “CCB/SYSCLK PLL Ratio,” Section 2.23.3, “e500 Core PLL Ratio,“and Section 2.23.4, “DDR/DDRCLK PLL Ratio,” for ratio settings.
2. The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.
3. As defined by JEDEC, the minimum allowed data rate for DDR3 is 606 MHz data rate. Therefore, only the processors with a DDR data rate of 667 MHz support DDR3.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL. This table provides the clocking specifications for the memory bus.

**Table 74. Memory Bus Clocking Specifications**

| Characteristic | Min | Max | Unit | Notes |
|---|---|---|---|---|
| DDR Memory bus clock speed | 200 | 250 | MHz | 1, 2, 3, 4, 5 |

**Notes:**

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 2.23.2, “CCB/SYSCLK PLL Ratio,” Section 2.23.3, “e500 Core PLL Ratio,” and Section 2.23.4, “DDR/DDRCLK PLL Ratio,” for ratio settings.
2. The Memory bus clock refers to the chip’s memory controllers’ MCK[0:5] and $\overline{\text{MCK}}$[0:5] output clocks, running at half of the DDR data rate.
3. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform (CCB) frequency. If the desired DDR data rate is higher than the platform (CCB) frequency, asynchronous mode must be used.
4. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. See Section 2.23.4, “DDR/DDRCLK PLL Ratio.” The memory bus clock speed must be less than or equal to the CCB clock rate which in turn must be less than the DDR data rate.
5. See Table 73 for a list of supported ranges of DDR data to corresponding processor frequency.

## 2.23.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in the following table:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values.

**Table 75. CCB Clock Ratio**

| Binary Value of LA[28:31] Signals | CCB:SYSCLK Ratio | Binary Value of LA[28:31] Signals | CCB:SYSCLK Ratio |
|---|---|---|---|
| 0000 | Reserved | 1000 | 8:1 |
| 0001 | Reserved | 1001 | 9:1 |
| 0010 | Reserved | 1010 | 10:1 |
| 0011 | 3:1 | 1011 | Reserved |
| 0100 | 4:1 | 1100 | 12:1 |
| 0101 | 5:1 | 1101 | Reserved |
| 0110 | 6:1 | 1110 | Reserved |
| 0111 | Reserved | 1111 | Reserved |

## 2.23.3 e500 Core PLL Ratio

This table describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE and LGPL2 at power up, as shown in this table.

**Table 76. e500 Core to CCB Clock Ratio**

| Binary Value of LBCTL, LALE, LGPL2 Signals | e500 core: CCB Clock Ratio | Binary Value of LBCTL, LALE, LGPL2 Signals | e500 core: CCB Clock Ratio |
|---|---|---|---|
| 000 | 4:1 | 100 | 2:1 |
| 001 | 9:2 | 101 | 5:2 |
| 010 | Reserved | 110 | 3:1 |
| 011 | 3:2 | 111 | 7:2 |

## 2.23.4 DDR/DDRCLK PLL Ratio

The DDR memory controller complex can be synchronous with, or asynchronous to, the CCB, depending on configuration.

The following table describes the clock ratio between the DDR memory controller complex and the DDR/DDRCLK PLL reference clock, DDRCLK, which is not the memory bus clock.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for the DDR controller to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode.

In asynchronous mode, the DDR PLL rate to DDRCLK ratios listed in Table 77 reflects the DDR data rate to DDRCLK ratio, since the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output.

Please note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode.

The DDRCLKDR configuration register in the Global Utilities block allows the DDR controller to be run in a divided down mode where the DDR bus clock is half the speed of the default configuration. Changing of these defaults must be completed prior to initialization of the DDR controller.

**Table 77. DDR Clock Ratio**

| Functional Signals | Reset Configuration Name | Value (Binary) | DDR:DDRCLK Ratio |
|---|---|---|---|
| TSEC_1588_TRIG_OUT[0:1], TSEC1_1588_CLK_OUT | cfg_ddr_pll[0:2] | 000 | 3:1 |
| | | 001 | 4:1 |
| | | 010 | 6:1 |
| | | 011 | 8:1 |
| | | 100 | 10:1 |
| | | 101 | 12:1 |
| | | 110 | Reserved |
| | | 111 | Synchronous mode |

## 2.23.5 PCI Clocks

The integrated PCI controller in this chip supports PCI input clock frequency in the range of 33–66 MHz. The PCI input clock can be applied from SYSCLK in synchronous mode or PCI1_CLK in asynchronous mode. For specifications on the PCI1_CLK, refer to the PCI 2.2 Specification.

The use of PCI1_CLK is optional if SYSCLK is in the range of 33–66 MHz. If SYSCLK is outside this range then use of PCI1_CLK is required as a separate PCI clock source, asynchronous with respect to SYSCLK.

## 2.23.6 Frequency Options

### 2.23.6.1 SYSCLK to Platform Frequency Options

This table shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

**Table 78. Frequency Options of SYSCLK with Respect to Memory Bus Speeds**

| CCB to SYSCLK Ratio | SYSCLK (MHz) | | | | | | |
|---|---|---|---|---|---|---|---|
| | 33.33 | 41.66 | 66.66 | 83 | 100 | 111 | 133.33 |
| | Platform /CCB Frequency (MHz) | | | | | | |
| 3 | | | | | | 333 | 400 |
| 4 | | | | 333 | 400 | 444 | |
| 5 | | | 333 | 415 | 500 | | |
| 6 | | | 400 | 500 | | | |
| 8 | | 333 | | | | | |
| 10 | 333 | 417 | | | | | |
| 12 | 400 | 500 | | | | | |

## 2.24 Thermal

This section describes the thermal specifications of the chip.

### 2.24.1 Thermal Characteristics

This table provides the package thermal characteristics.

**Table 79. Package Thermal Characteristics**

| Characteristic | JEDEC Board | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction-to-ambient Natural Convection | Single layer board (1s) | $R_{\theta JA}$ | 23 | °C/W | 1, 2 |
| Junction-to-ambient Natural Convection | Four layer board (2s2p) | $R_{\theta JA}$ | 18 | °C/W | 1, 2 |
| Junction-to-ambient (@200 ft/min) | Single layer board (1s) | $R_{\theta JA}$ | 18 | °C/W | 1, 2 |

**Table 79. Package Thermal Characteristics (continued)**

| Characteristic | JEDEC Board | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction-to-ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JA}$ | 14 | °C/W | 1, 2 |
| Junction-to-board thermal | — | $R_{\theta JB}$ | 10 | °C/W | 3 |
| Junction-to-case thermal | — | $R_{\theta JC}$ | < 0.1 | °C/W | 4 |

**Notes**

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 °C/W

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease.For system thermal modeling, the chip's thermal model without a lid is shown in Figure 72 The substrate is modeled as a block 29 x 29 x 1.2 mm with an in-plane conductivity of 19.8 W/m•K and a through-plane conductivity of 1.13 W/m•K. The solder balls and air are modeled as a single block 29 x 29 x 0.5 mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 9.6 x 9.57 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 7.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to the case outline for actual dimensions.

## 2.24.2 Recommended Thermal Model

This table shows the chip's thermal model.

**Table 80. Thermal Model**

| Conductivity | Value | Units |
|---|---|---|
| **Die (9.6x9.6 × 0.85 mm)** | | |
| Silicon | Temperature dependent | — |
| **Bump/Underfill (9.6 x 9.6 × 0.07 mm) Collapsed Thermal Resistance** | | |
| Kz | 7.5 | W/m•K |
| **Substrate (29 × 29 × 1.2 mm)** | | |
| Kx | 19.8 | W/m•K |
| Ky | 19.8 | |
| Kz | 1.13 | |
| **Solder and Air (29 × 29 × 0.5 mm)** | | |
| Kx | 0.034 | W/m•K |
| Ky | 0.034 | |
| Kz | 12.1 | |

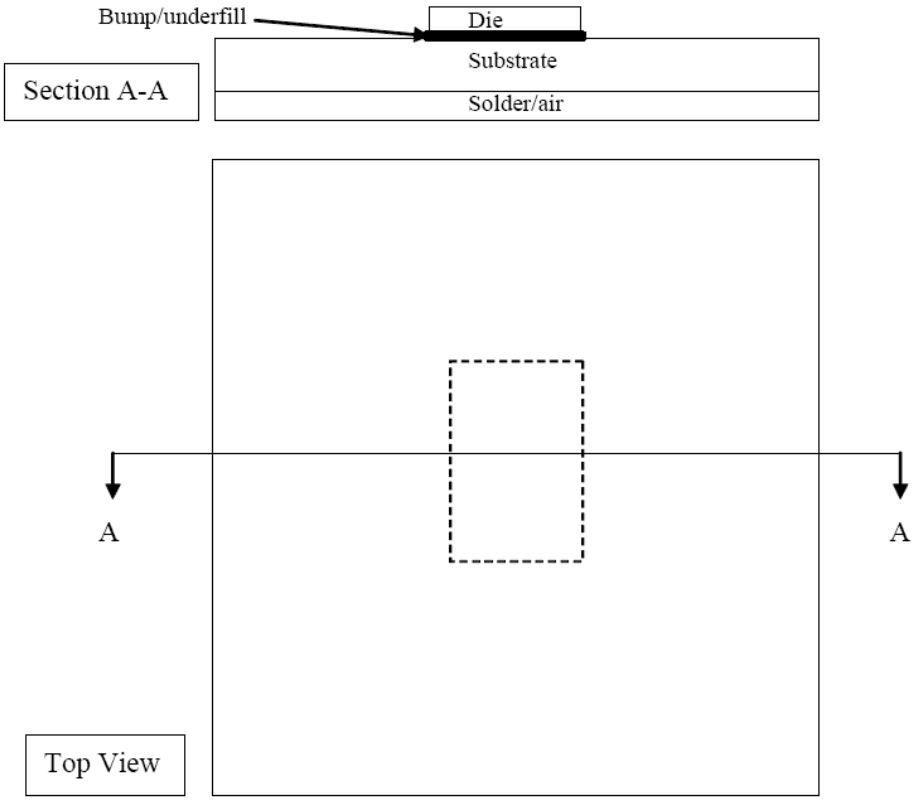



**Figure 72. System-Level Thermal Model for the Chip (Not to Scale)**

The Flotherm library files of the parts have a dense grid to accurately capture the laminar boundary layer for flow over the part in standard JEDEC environments, as well as the heat spreading in the board under the package. In a real system, however, the part will require a heat sink to be mounted on it. In this case, the predominant heat flow path will be from the die to the heat sink. Grid density lower than currently in the package library file will suffice for these simulations. The user will need to determine the optimal grid for their specific case.

## 2.24.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in the following figure. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

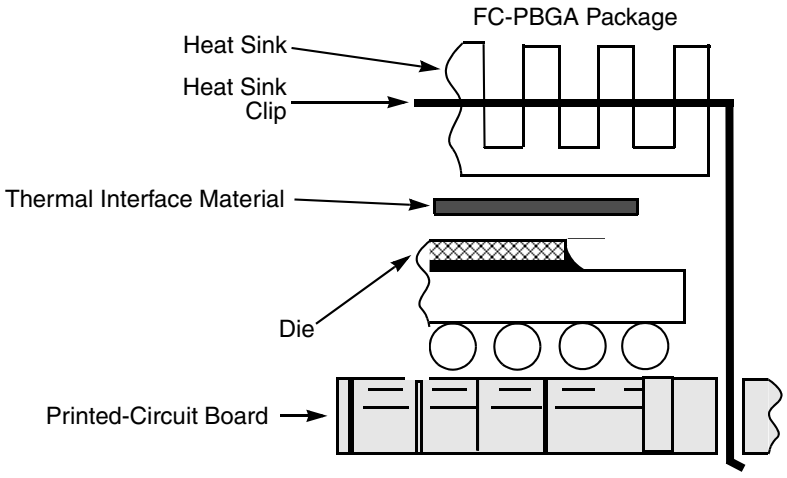



**Figure 73. Package Exploded Cross-Sectional View with Several Heat Sink Options**

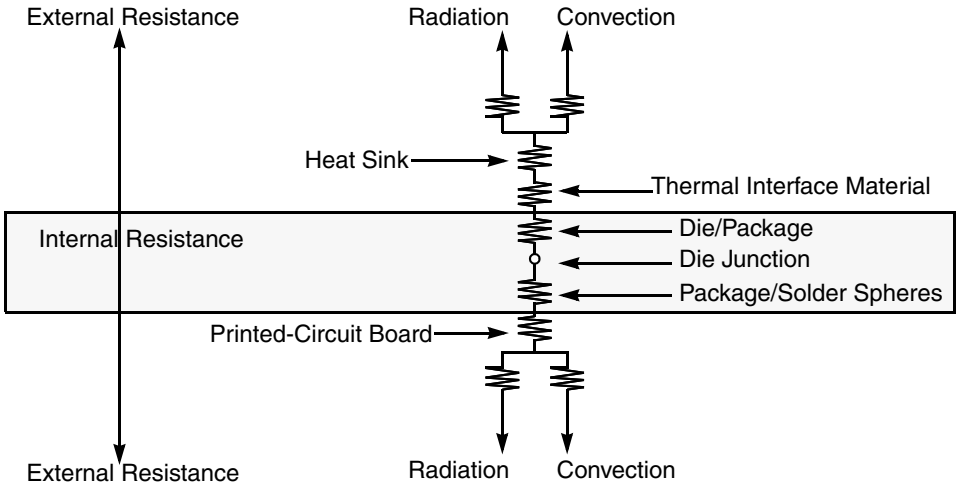
The system board designer can choose between several types of heat sinks to place on the chip. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Advanced Thermal Solutions, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the chip to function in various environments.

### 2.24.3.1 Internal Package Conduction Resistance

For the packaging technology, shown in Table 70, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.




(Note the internal versus external package resistance)

**Figure 74. Package with Heat Sink Mounted to a Printed-Circuit Board**

The heat sink removes most of the heat from the chip for most applications. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

#### 2.24.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increased contact pressure. This performance characteristic chart is generally provided by the thermal interface vendors.

# 3 Hardware Design Considerations

This section provides electrical and thermal design recommendations for successful application of the chip.

## 3.1 System Clocking

This chip includes seven PLLs:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 2.23.2, “CCB/SYSCLK PLL Ratio.”
- The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 2.23.3, “e500 Core PLL Ratio.”
- The PCI PLL generates the clocking for the PCI bus
- The local bus PLL generates the clock for the local bus.
- There is a PLL for the SerDes1 block to be used for PCI Express interface
- There is a PLL for the SerDes2 block to be used for SGMII and SATA interfaces.
- The DDR PLL generates the DDR clock from the externally supplied DDRCLK input in asynchronous mode. The frequency ratio between the DDR clock and DDRCLK is described in Section 2.23.4, “DDR/DDRCLK PLL Ratio.”

## 3.2 Power Supply Design and Sequencing

### 3.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}$_PLAT, $AV_{DD}$_CORE, $AV_{DD}$_PCI, $AV_{DD}$_LBIU, and $AV_{DD}$_SRDS respectively). The $AV_{DD}$ level should always be equivalent to $V_{DD}$, and preferably these voltages will be derived directly from $V_{DD}$ through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 75, one to each of the $AV_{DD}$ pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific $AV_{DD}$ pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the $AV_{DD}$ pin, which is on the periphery of 783 FC-PBGA the footprint, without the inductance of vias.

This figure shows the PLL power supply filter circuit.

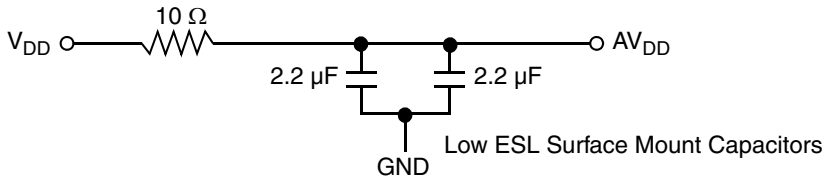
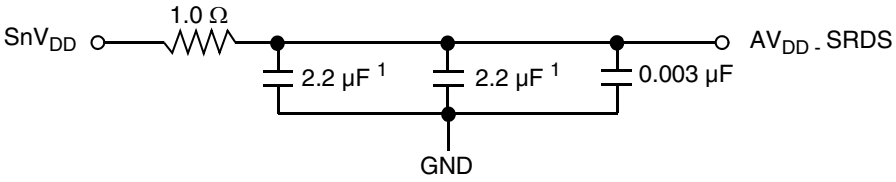



**Figure 75. Chip PLL Power Supply Filter Circuit**

The $AV_{DD}$_SRDS*n* signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 76. For maximum effectiveness, the filter circuit is placed as closely as possible to the $AV_{DD}$_SRDS*n* balls to ensure it filters out as much noise as possible. The ground connection should be near the $AV_{DD}$_SRDS*n* balls. The 0.003-µF capacitor is closest to the balls, followed by the 1-µF capacitor, and finally the 1 ohm resistor to the board supply plane. The capacitors are connected from $AV_{DD}$_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.




1. An 0805 sized capacitor is recommended for system initial bring-up

**Figure 76. SerDes PLL Power Supply Filter Circuit**

Note the following:

- $AV_{DD}$ should be a filtered version of $SV_{DD}$.
- Signals on the SerDes interface are fed from the $XV_{DD}$ power plane.

## 3.3 Pin States in Deep Sleep State

In all low power mode by default, all input and output pads remain driven as per normal functional operation. The inputs remain enabled.

The exception is that in Deep Sleep mode, GCR[DEEPSLEEP_Z] can be used to tristate a subset of output pads, and disable the receivers of input pads as defined in Table 1. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for details.

## 3.4 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, this chip can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each $V_{DD}$, $TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ pin of the chip. These decoupling capacitors should receive their power from separate $V_{DD}$,$TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$, and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors must be placed directly under the chip using a standard escape pattern as much as possible. If some caps are to be placed surrounding the part it should be routed with short and large trace to minimize the inductance.

These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the $V_{DD}$, $TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values types and quantity of bulk capacitors.

## 3.5 SerDes Block Power Supply Decoupling Recommendations

he SerDes1 and SerDes2 blocks require a clean, tightly regulated source of power ($SnV_{DD}$ and $XnV_{DD}$) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the chip. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the chip as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor from each SerDes supply ($SnV_{DD}$ and $XnV_{DD}$) to the board ground plane on each side of the chip. This should be done for all SerDes supplies.
- Third, between the chip and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

## 3.6 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to $V_{DD,}TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external $V_{DD,}TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ and GND pins of the chip.

## 3.7 Pull-Up and Pull-Down Resistor Requirements

The chip requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including $I^2C$ pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 78. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

The following pins must NOT be pulled down during power-on reset: TSEC1_TXD[3], HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP. The UART_SOUT[0:1] and TEST_SEL pins must be set to a proper state during POR configuration. Please refer to the pinlist table (see Table 62) of the individual chip for more details.

See the PCI 2.2 specification for all pull-ups required for PCI.

## 3.8 Output Buffer DC Impedance

The chip drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for $I^2C$).

To measure $Z_0$ for the single-ended drivers, an external resistor is connected from the chip pad to $OV_{DD}$ or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 77). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and $R_P$ is trimmed until the voltage at the pad equals $OV_{DD}/2$. $R_P$ then becomes the resistance of the pull-up devices. $R_P$ and $R_N$ are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

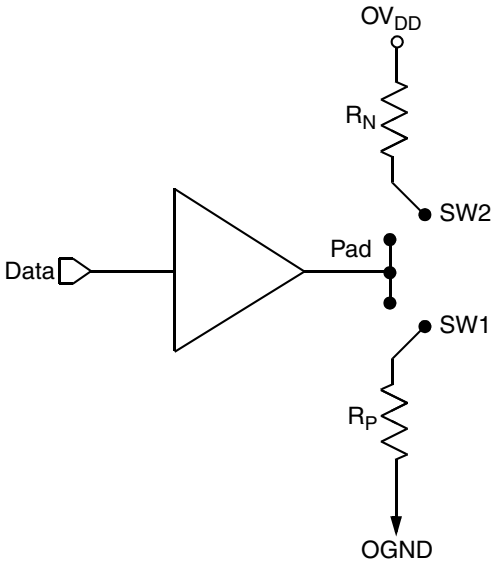



**Figure 77. Driver Impedance Measurement**

This table summarizes the signal impedance targets. The driver impedances are targeted at minimum $V_{DD}$, nominal $OV_{DD}$, 105°C.

**Table 81. Impedance Characteristics**

| Impedance | Local Bus, Ethernet, DUART, Control, Configuration, Power Management | PCI | DDR DRAM | Symbol | Unit |
|---|---|---|---|---|---|
| $R_N$ | 45 Target | 45 Target (cfg_pci_impd=1)<br>25 Target (cfg_pci_impd=0) | 18 Target (full strength mode)<br>36 Target (full strength mode) | $Z_0$ | Ω |
| $R_P$ | 45 Target | 45 Target (cfg_pci_impd=1)<br>25 Target (cfg_pci_impd=0) | 18 Target (full strength mode)<br>36 Target (full strength mode) | $Z_0$ | Ω |

**Note:** Nominal supply voltages. See Table 1.

## 3.9 Configuration Pin Muxing

The chip provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the chip into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

## 3.10 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 78. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredicatable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The chip requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 78 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 79, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

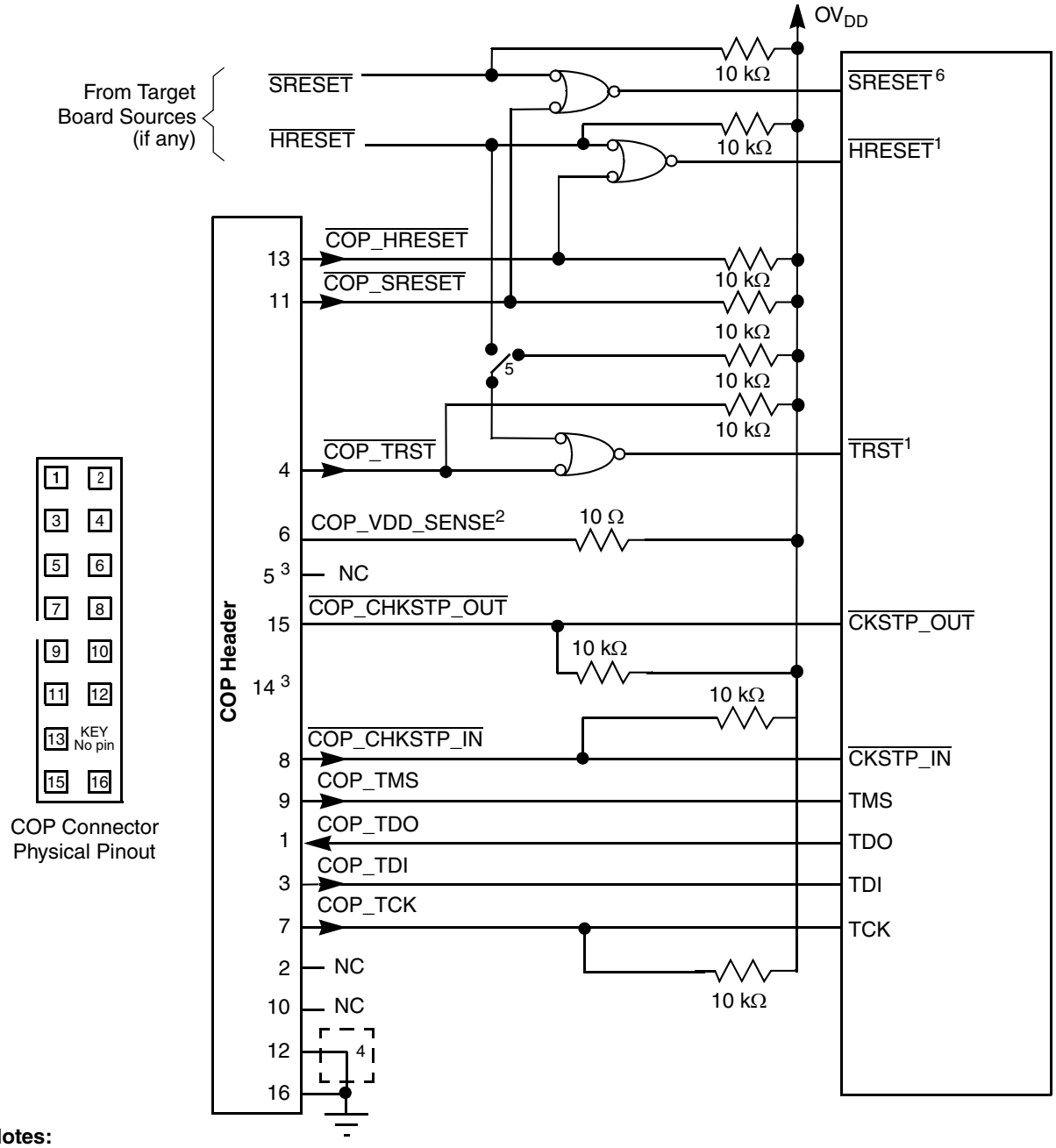
The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 79 is common to all known emulators.

### 3.10.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 78. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, or TDO.




**Notes:**

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

**Figure 78. JTAG Interface Connection**

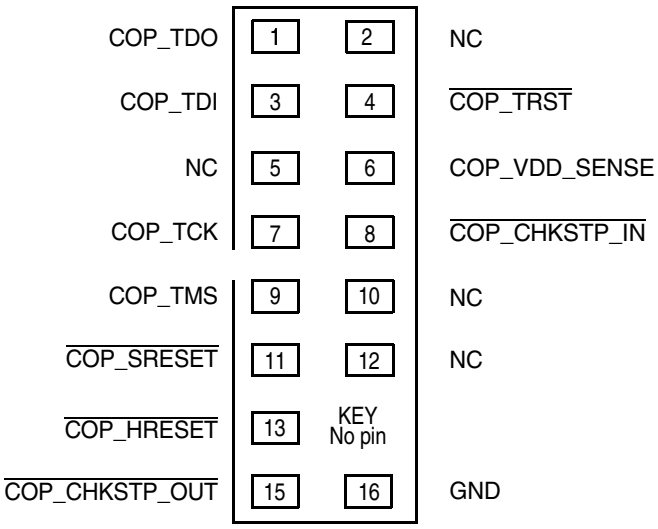



**Figure 79. COP Connector Physical Pinout**

## 3.11 Guidelines for High-Speed Interface Termination

### 3.11.1 SerDes1 Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins. There are several reserved pins that need to be either left floating or connected to XGND. See SerDes1 in Table 1 for details.

The following pins must be left unconnected (float):

- SD1_TX[7:4]
- $\overline{\text{SD1_TX[7:4]}}$
- Reserved pins T22, T23

The following pins must be connected to XGND:

- SD1_RX[7:4]
- $\overline{\text{SD1_RX[7:4]}}$
- SD1_REF_CLK
- $\overline{\text{SD1_REF_CLK}}$

The POR configuration pin cfg_io_ports[0:2] on TSEC3_TXD[6:3] can be used to power down SerDes 1 block for power saving. Note that both SVDD and XVDD must remain powered.

### 3.11.2 SerDes 1 Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD1_TX[7:4]
- $\overline{\text{SD1_TX[7:4]}}$
- Reserved pins: T22, T23

The following pins must be connected to XGND if not used:

- SD1_RX[7:4]
- $\overline{\text{SD1_RX[7:4]}}$
- SD1_REF_CLK
- $\overline{\text{SD1_REF_CLK}}$

### 3.11.3 SerDes 2 Interface Entirely Unused

If the high-speed SerDes 2 interface (SGMII/ SATA) is not used at all, the unused pin should be terminated as described in this section. There are several Reserved pins that need to be either left floating or connected to X2GND. See SerDes2 in Table 1Table 1 for details.

The following pins must be left unconnected (float):

- SD2_TX[0]
- $\overline{\text{SD2_TX[0]}}$
- Reserved pins L8, L9

The following pins must be connected to X2GND:

- SD2_RX[0]
- $\overline{\text{SD2_RX[0]}}$
- SD2_REF_CLK
- $\overline{\text{SD2_REF_CLK}}$

The POR configuration pin cfg_srds2_prtcl[0:2] on TSEC1_TXD[2], TSEC3_TXD[2], TSEC_1588_PUSLE_OUT1 can be used to power down SerDes 2 block for power saving. Note that both S2VDD and X2VDD must remain powered.

# 4 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 4.1, “Part Numbering Nomenclature.”

## 4.1 Part Numbering Nomenclature

This table shows the part numbering nomenclature.

**Table 82. Part Numbering Nomenclature**

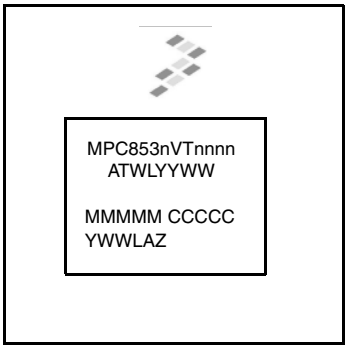
| MPC | *nnnn* | *E* | *C* | *VT* | *AA* | *X* | *R* |
|---|---|---|---|---|---|---|---|
| **Product Code** | **Part Identifier** | **Security Engine** | **Tiers and Temperature Range** | **Package [1]** | **Processor Frequency [2]** | **DDR Frequency [3]** | **Revision Level** |
| MPC | 8536<br>8535 | E = included | • A = Commercial tier standard temperature range (0° to 90°C)<br>• B or Blank = industrial tier standard temperature range (0° to 105°C)<br>• C = Industrial tier extended temperature range (–40° to 105°C) | • VT = FC-PBGA (Pb-free)[4]<br>• PX = plastic standard<br>• VJ = lead-free FC-PBGAs[5] | • AK = 600 MHz<br>• AN = 800 MHz<br>• AQ = 1000 MHz<br>• AT = 1250 MHz<br>• AU = 1333 MHz<br>• AV = 1500 MHz | • G = 400 MHz<br>• H = 500 MHz<br>• J = 533 MHz<br>• L = 667 MHz | • Blank = Ver. 1.0 or 1.1 (SVR = 0x803F0190, 0x803F0191)<br>• A = Ver. 1.2 (SVR = 0x803F0192) |
| | | Blank = not included | | | | | • Blank = Ver. 1.0 or 1.1 (SVR = 0x80370190, 0x80370191)<br>• A = Ver. 1.2 (SVR = 0x80370192) |

**Notes:**

1. See Section 5, “Package Information,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. See Table 84 for the corresponding maximum platform frequency.
4. The VT part number is ROHS-compliant, with the permitted exception of the C4 die bumps.
5. The VJ part number is entirely lead-free, including the C4 die bumps.

## 4.2 Part Marking

Parts are marked as in the example shown in the following figure.




FC-PBGA

**Notes:**
MMMMM is the 5-digit mask number.
ATWLYYWW is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

**Figure 80. Part Marking for FC-PBGA**

## 4.3 Part Numbering

This table lists all part numbers that are offered for the chip.

**Table 83. MPC8535 Part Numbers Commercial Tier**

| Core/Platform/ DDR (MHz) | Standard Temp Without Security | Standard Temp With Security | Notes |
|---|---|---|---|
| 600/400/400 | MPC8535AVJAKG(A) | MPC8535EAVJAKG(A) | — |
| 800/400/400 | MPC8535AVJANG(A) | MPC8535EAVJANG(A) | — |
| 1000/400/400 | MPC8535AVJAQG(A) | MPC8535EAVJAQG(A) | — |
| 1250/500/500 | MPC8535AVJATH(A) | MPC8535EAVJATH(A) | — |
| 1250/500/667 | MPC8535AVJATLA | MPC8535EAVJATLA | — |

**Note:**
1. The last letter A indicates a Rev 1.2 silicon. It would be Rev 1.0 or Rev 1.1 silicon without a letter A

**Table 84. MPC8535 Part Numbers Industrial Tier**

| Core/Platform/ DDR (MHz) | Standard Temp Without Security | Standard Temp With Security | Extended Temp Without Security | Extended Temp With Security | Notes |
|---|---|---|---|---|---|
| 600/400/400 | MPC8535BVJAKG(A) | MPC8535EBVJAKG(A) | MPC8535CVJAKG(A) | MPC8535ECVJAKG(A) | 1 |
| 800/400/400 | MPC8535BVJANG(A) | MPC8535EBVJANG(A) | MPC8535CVJANG(A) | MPC8535ECVJANG(A) | |
| 1000/400/400 | MPC8535BVJAQG(A) | MPC8535EBVJAQG(A) | MPC8535CVJAQG(A) | MPC8535ECVJAQG(A) | |
| 1250/500/500 | MPC8535BVJATH(A) | MPC8535EBVJATH(A) | MPC8535CVJATH(A) | MPC8535ECVJATH(A) | |
| 1250/500/667 | MPC8535BVJATLA | — | — | — | 2 |

**Note:**

1. The last letter A indicates a Rev 1.2 silicon. It would be Rev 1.0 or Rev 1.1 silicon without a letter A.
2. Contact a Freescale sales representative for more information.

# 5 Package Information

This section details package parameters, pin assignments, and dimensions.

## 5.1 Package Parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA) without a lid.

| | |
|---|---|
| Package outline | 29 mm × 29 mm |
| Interconnects | 783 |
| Pitch | 1 mm |
| Minimum module height | 2.23 mm |
| Maximum module height | 2.8 mm |
| Solder Balls | 96.5Sn/3.5Ag |
| Ball diameter (typical) | 0.6 mm |

## 5.2 Mechanical Dimensions of the FC-PBGA

The mechanical dimensions and bottom surface nomenclature of the 783 FC-PBGA package are shown in the following figure.

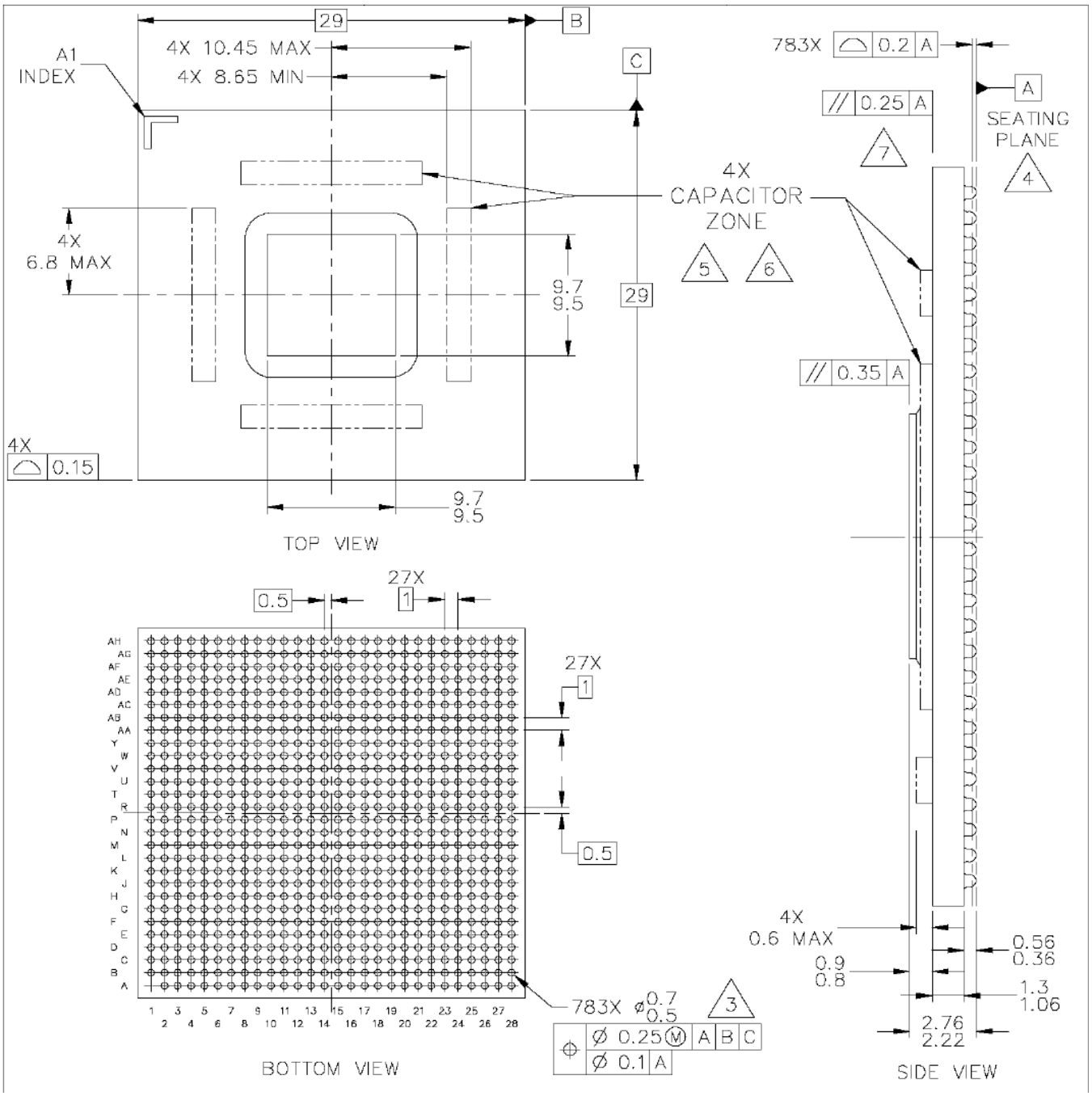



**Figure 81. Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA**

### NOTES for Figure 81

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

5. Capacitors may not be present on all devices
6. Caution must be taken not to short exposed metal capacitor pads on package top.
7. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

# 6 Product Documentation

The following documents are required for a complete description of the chip and are needed to design properly with the part.

- *MPC8536E PowerQUICC III Integrated Processor Reference Manual* (document number: MPC8536ERM)
- *e500 PowerPC Core Reference Manual* (document number: E500CORERM)

# 7 Document Revision History

This table provides a revision history for this hardware specification.

**Table 85. Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 7 | 07/2015 | • In Section 4, “Ordering Information,” added back the “A” temperature range parts and the MPC8535 Part Numbers Commercial Tier table. |
| 6 | 09/2014 | • In Table 82, “Part Numbering Nomenclature,” added footnotes 4 and 5, and updated the Package and Tiers and Temperature Range columns.<br>• In Section 4, “Ordering Information,” removed the “A” temperature range parts and the MPC8535 Part Numbers Commercial Tier table.<br>• Updated Table 73 and added note 3.<br>• Updated and added note 5 to Table 74.<br>• Updated section title to Section 4.1, “Part Numbering Nomenclature.”<br>• In Table 73, updated the DDR data rate for the 1250 MHz maximum column.<br>• Updated Table 84 and added note 2. |
| 5 | 09/2011 | Removed PVDD from Table 1, “Pinout Listing.” |
| 4 | 06/2011 | • In Table 1, “Pinout Listing,” updated the power supply for TSEC3 pins to TVDD.<br>• Updated Table 56, “eSDHC AC Timing Specifications.”<br>• In Section 4.3, “Part Numbering,” added an extra bin (1250/500/667) to support DDR3. |
| 3 | 11/2010 | • In Table 1, “Pinout Listing,” added the following note: “For systems that boot from Local Bus (GPCM)-controlled NOR flash or (FCM) controlled NAND flash, a pullup on LGPL4 is required...” In addition, updated footnote 26 and added footnote 29 to PCI1_AD.<br>• Updated Table 21<br>• Updated Figure 25, “RGMII and RTBI AC Timing and Multiplexing Diagrams.”<br>• In Table 44, “MII Management DC Electrical Characteristics,” changed the Voh/Vol values for MDIO/MDC.<br>• Added Note 6 regarding USB*n*_DIR pin to Table 47, “USB General Timing Parameters6.”<br>• In Table 64, “I2C AC Electrical Specifications,” updated footnote 2.<br>• In Table 82, ,Table 83, , Table 84,added the Revision Level A for Rev 1.2 |
| 2 | 09/2009 | **Note:**<br>• In Section 1, “Pin Assignments and Reset States,”updated the first sentence of the note to say, “The UART_SOUT[0:1] and TEST_SEL pins must be set to a proper state during POR configuration.”<br>• In Table 40, “SGMII DC Receiver Electrical Characteristics,” changed LSTSAB to LSTSA and LSTSEF to LSTSE for Note 4.<br>• Updated Die value and Bump/Underfill value in Table 84<br>**Note:** Updated Figure 81, “Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA,” and its notes. |

**Table 85. Document Revision History (continued)**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 1 | 09/2009 | • In Table 3, “Recommended Operating Conditions,” for $V_{DD_CORE}$, removed 1.1 ± 55 mV.<br>• In Table 5, “Power Dissipation 5,” remove note 5.<br>• In Table 5, ”Power Dissipation 5,” changed an “—” to “0.” |
| 0 | 08/2009 | Initial public release. |

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