



SANYO Semiconductors

DATA SHEET

# LA2000

Monolithic Linear IC  
Audio Level Sensor

## Overview

The LA2000 is an IC for detecting interprogram spaces to pick out the starting point of a program immediately preceding or following a musical program recorded on tape, and to detect end of tape.

## Used in

- Radio-cassette recorders
- Cassette decks
- Car stereos
- Detection of spaces between programs recorded on tape
- Detection of end of tape
- Other

## Applications

- Detection of spaces between programs recorded on tape
- Detection of end of tape
- Other

## Features

- Has transistors capable of driving plungers with maximum 600mA, and a protective diode to prevent induced reverse voltages.
- Can provide designated time delays by externally connected capacitors and resistors.
- Has a comparator with stable hysteresis to handle variations in power supply voltage.
- Detects unrecorded portions of tape.

## Specifications

### Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$ max		15	V
Flow-in current	$I_6$ max		600	mA
Allowable power dissipation	$P_d$ max		540	mW
Operating temperature	$T_{opr}$		-20 to +75	°C
Storage temperature	$T_{stg}$		-40 to +125	°C

Note : 1. The voltage at pin 8 must not exceed the supply voltage at pin 9.

2. The maximum current flowing into pin 8 should be no greater than 0.5mA.

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**SANYO Semiconductor Co., Ltd.**

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## Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Operating voltage range	$V_{CC\ op}$		3.5 to 14	V

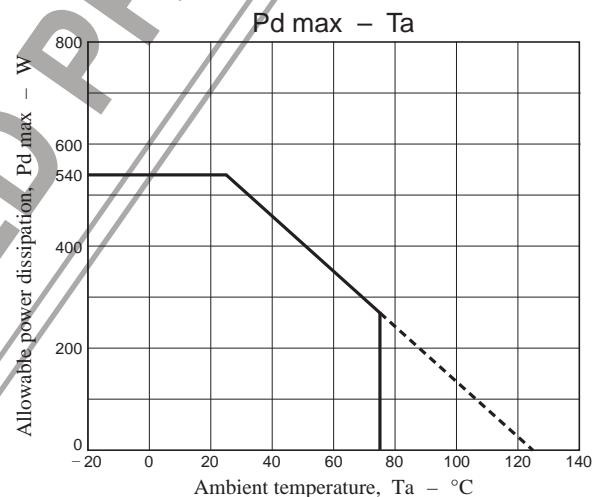
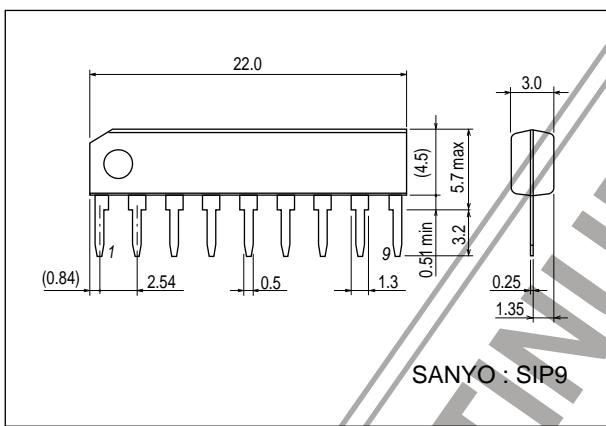
### **Electrical Characteristics** at $T_a = 25^\circ\text{C}$ , $V_{CC} = 9.0\text{V}$ , $f = 1\text{kHz}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	$I_{CC}$	$f = 1\text{kHz}$ , $V_{IN} = -45\text{dB}$		6	12	mA
Output transistor saturating voltage	$V_{CE(\text{sat})}$	$I_6 = 600\text{mA}$		1.5	2.5	V
Output diode forward voltage	$V_F$	$I_F = 600\text{mA}$		1.5	2.0	V
Output-off level in input equivalent	$V_{IN}$	$f = 1\text{kHz}$	-43	-50	-54	dBm
Comparator-on level	$V_{TH-H}$		3.0	3.5	4.0	V
Comparator-off level	$V_{TH-L}$		1.8	2.2	2.6	V
Pin 8 high level	$V_8$ pin		0.45	0.55		V
Output transistor leakage current	$I_{L-TR}$				100	$\mu\text{A}$
Output diode leakage current	$I_{L-Di}$				100	$\mu\text{A}$

## Package Dimensions

unit : mm (typ)

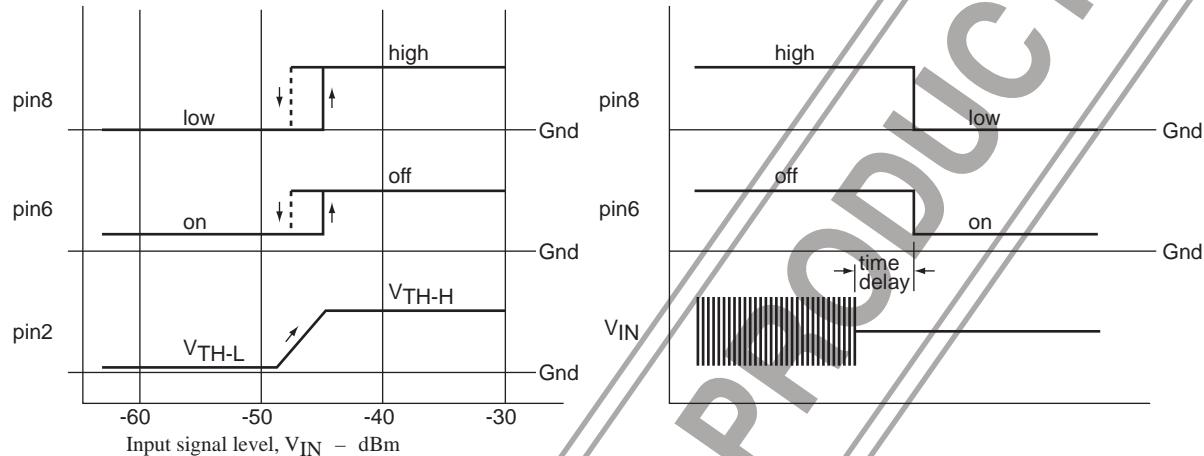
3017D



## 1. Description of external parts

- C1 • Input coupling capacitor : 0.47 to 2.2 $\mu$ F recommended.
- C2 • NF capacitor : Capacitance is reduced, so the off level in input equivalent becomes lower in the bass frequency range. We recommend 1 to 10 $\mu$ F.
- C3, R1 • For designation of time delays : Any time delay can be obtained by adequate choice of C3 and R1. We recommend 150k to 500k $\Omega$  for R1.
- C4, R3 • Power supply ripple filter
- R2 • Bias resistor : For diode when pin 8 is used to drive external transistors. A 1k $\Omega$  resistor is recommended.

## 2. Individual pins and their operations



As shown above, when input level is raised and the pin 2 voltage reaches the  $V_{TH-H}$  level of the comparator, pins 6 and 8 turn over. ( $V_{IN} = -45$  dBm).

- Pin 6 is for driving plungers. When it is on the “L” side, pin 6 turns on and can draw current up to 600mA maximum (restricted by duty-cycle chart). It is not to be on continuously for more than 3 seconds.
- Pin 7 is a diode that prevents reverse voltages induced when the plunger is turned off from on.
- Pin 8 functions in phase with pin 6 and can drive external transistors (such as for MUTE).

## 3. Time delays and obtaining CRs

When input signals that have been applied at a level not less than -45dBm are removed, discharging occurs through the CR connected at pin 2, lowering pin 2 potential. A time delay is provided before the hysteresis comparator turns over.

$$\frac{E_1}{E_0} = -\frac{t}{e^\tau}$$

$E_0$  : Initial voltage  
 $E_1$  : Threshold voltage  
 $\tau$  : Time constant

Accordingly,

$$t = -\tau \ln \frac{E_1}{E_0}$$

$E_1/E_0$ , within the IC, is 0.26. A desired time is obtained by an appropriate choice of  $\tau$  ( $\tau = C_3 R_1$ ). Therefore, the time delay is obtained by the following formula :

$$t = 1.34 \times C_3 R_1 \text{ (sec)}$$

We recommend 150k to 500k $\Omega$  for R when determining CR.

## 4. IC usage notes

## • Maximum ratings

When maximum ratings are surpassed, destruction or deterioration may result. Use the IC in the range where the maximum rating is not exceeded.

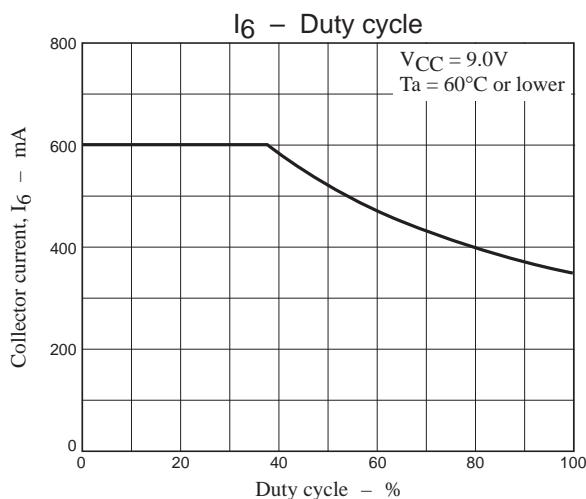
## • Interpin short circuits and reverse insertions

These cause destruction or deterioration of the IC : be careful when mounting on circuit board.

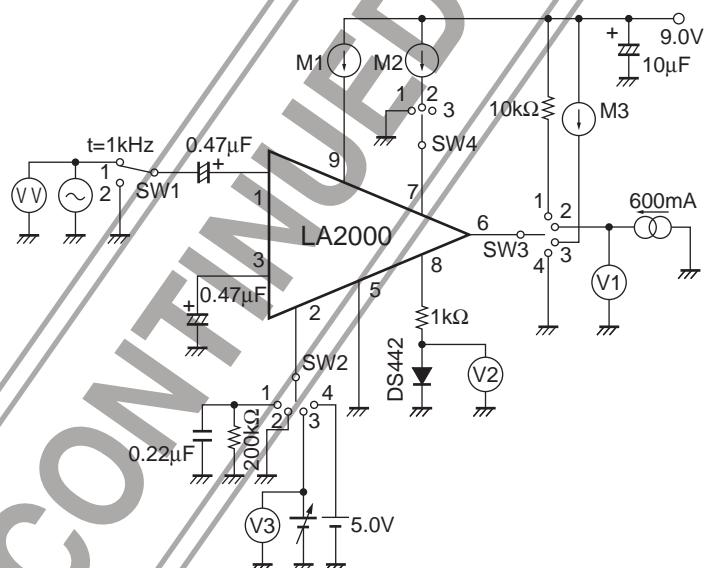
## • Voltage applied to pin 8 should never exceed pin 9 voltage.

## • The current flowing into pin 8 is to be 0.5mA maximum.

## • Pin 4 is unconnected, but is not to be used for GND or an interconnecting terminal.

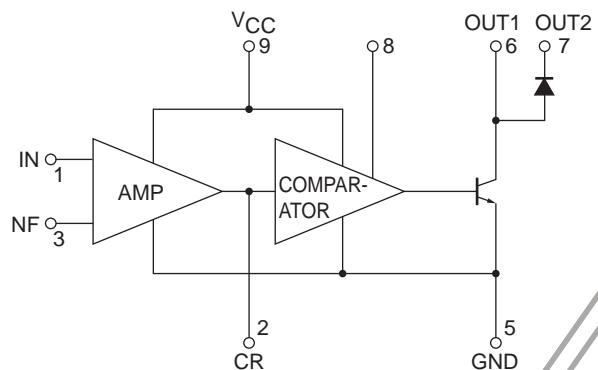


Note : I<sub>C</sub> = 600mA continuous is within 3 seconds  
I<sub>C</sub> = 300mA continuous is within 30 seconds  
I<sub>C</sub> = 100mA or less can be left on at all times.

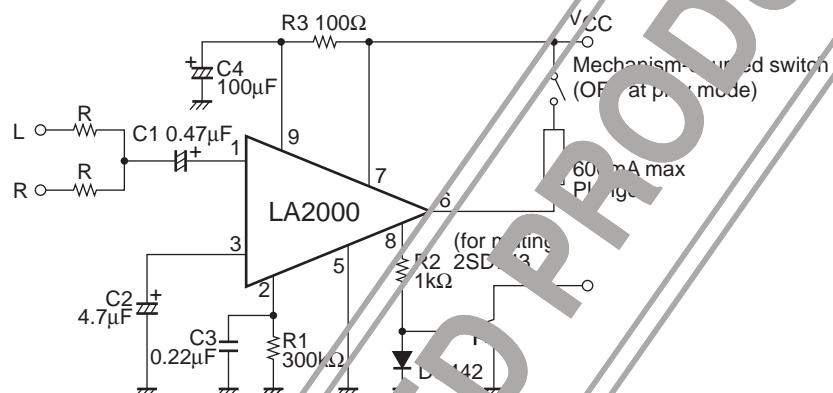
**Test Circuit****Test Conditions**

Test items	Symbol	SW-1	SW-2	SW-3	SW-4	Conditions
Circuit current	I <sub>CC</sub>	1	1	1	3	Measure current flowing into pin 9 at V <sub>IN</sub> = -45dB
Output transistor saturation voltage	V <sub>CE(sat)</sub>	2	2	2	3	Measure V <sub>IN</sub> at pin 6
Output diode forward voltage	V <sub>F</sub>	2	4	2	1	Measure V <sub>IN</sub> at pin 6
Output-off level in input equivalent	V <sub>IN</sub>	1	1	1	3	Input level (V.V) when pin 6 turns over
Comparator-on leve	V <sub>H</sub>	2	3	1	3	Measure V <sub>3</sub> When pin 6 turns over
Comparator-off level	V <sub>L</sub>	2	3	1	3	Measure V <sub>3</sub> When pin 6 turns over
Pin 8 high level	V <sub>p-8</sub>	2	4	1	3	Measure V <sub>2</sub> at pin 8
Output transistor leakage current	I <sub>TL</sub>	2	4	3	3	Measure M3
Output diode leakage current	I <sub>DL</sub>	2	4	4	2	Measure M2

## Block Diagram

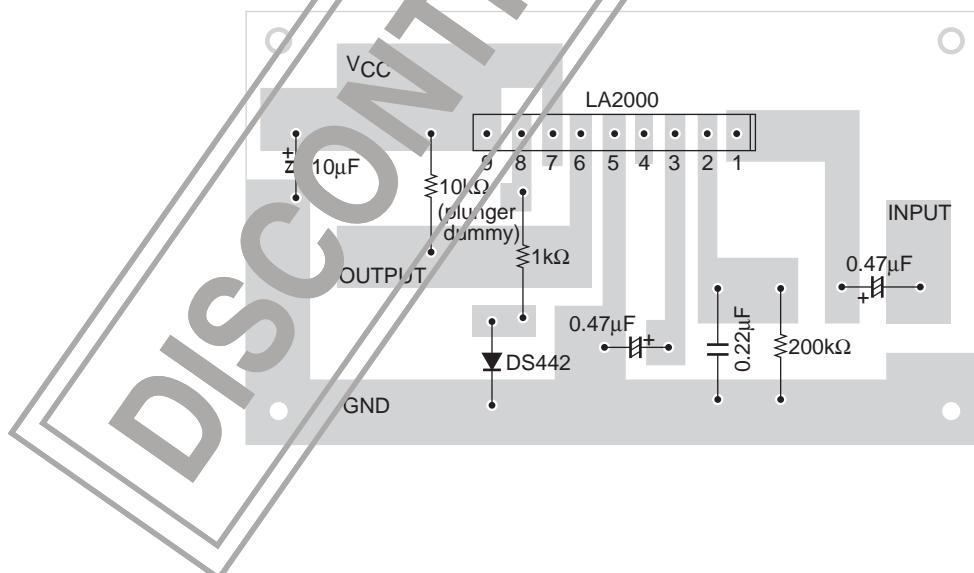


## Sample Application Circuit 1

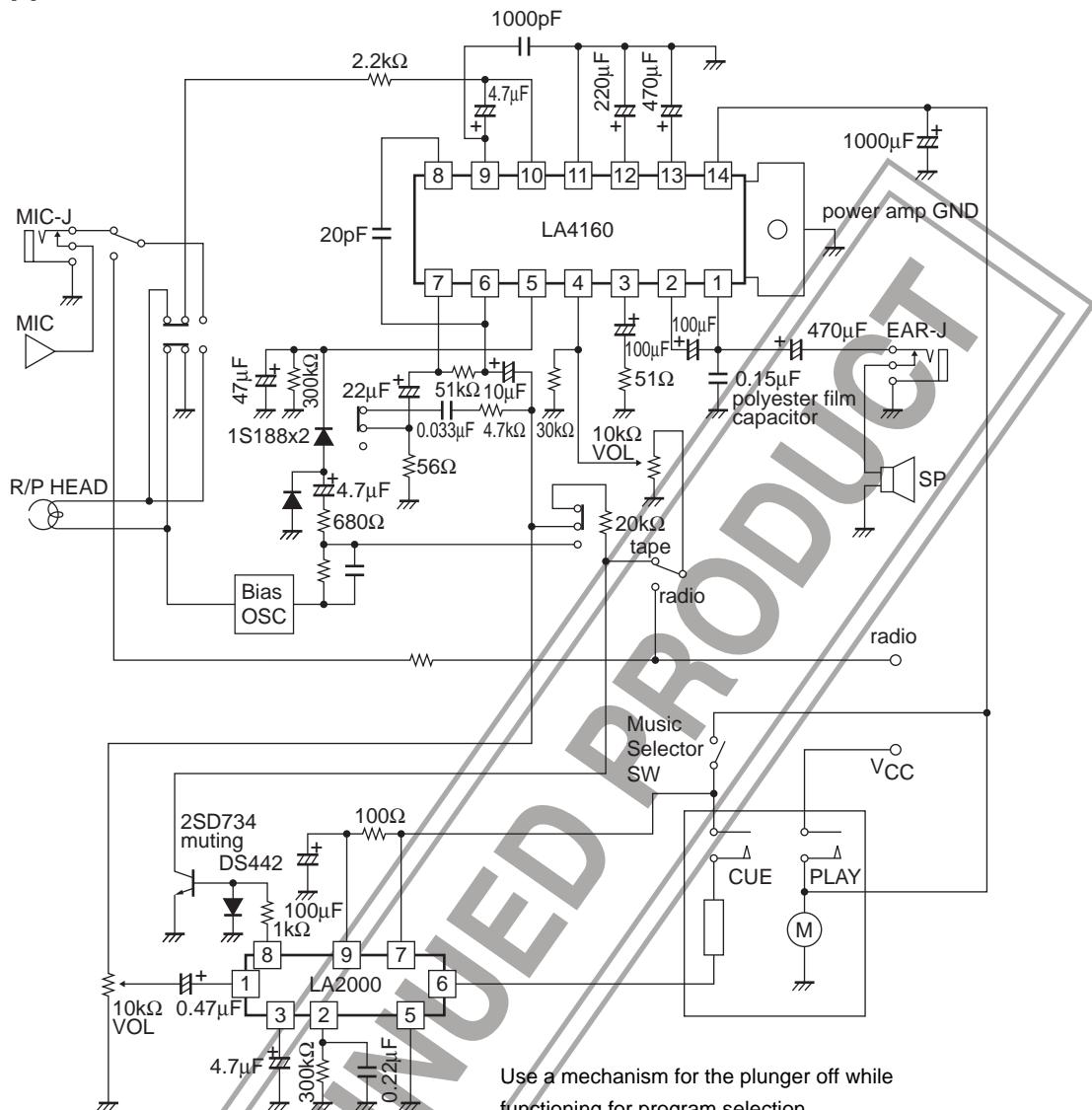


Pin 4 is unconnected but is not intended for GND or an interconnection terminal.

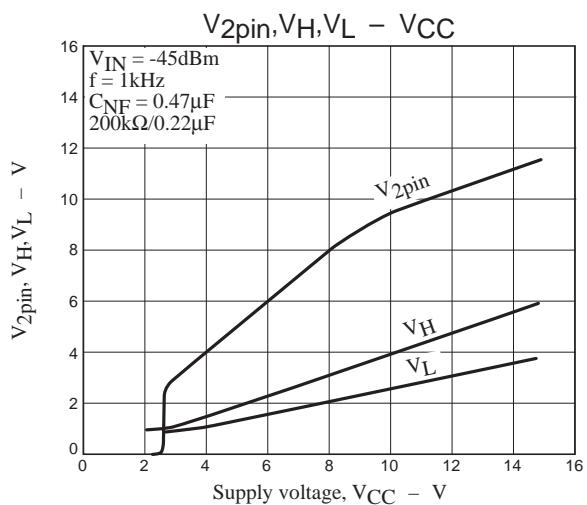
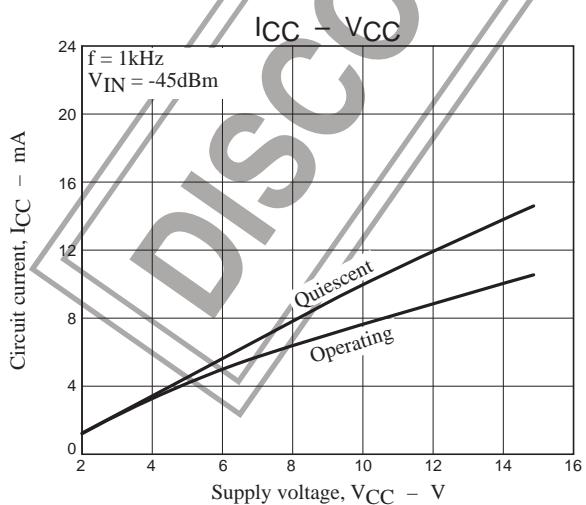
## Sample Printed Pattern (copper foil side)

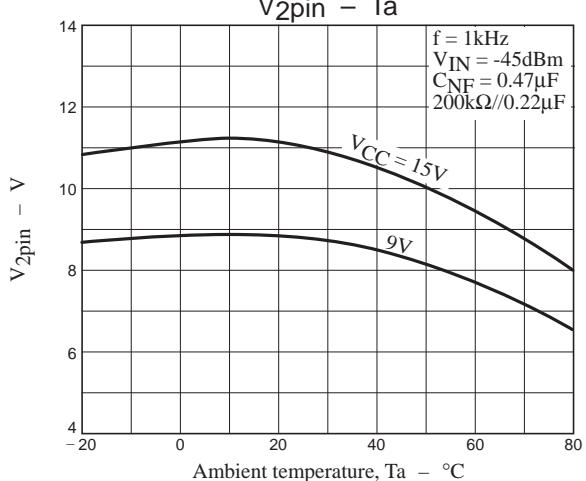
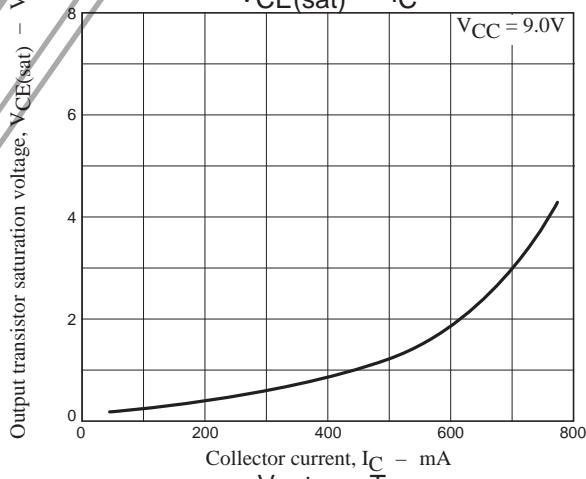
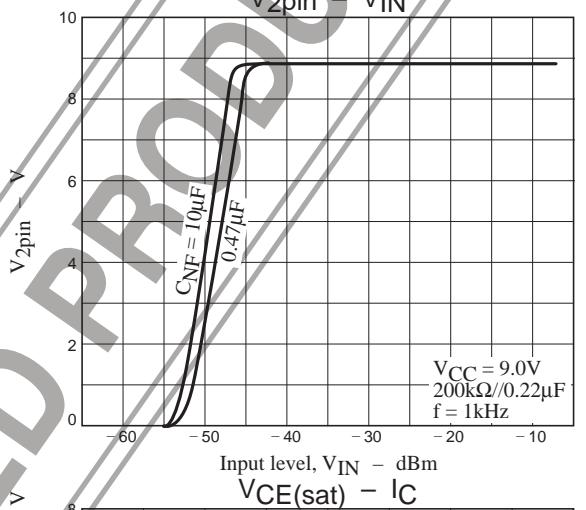
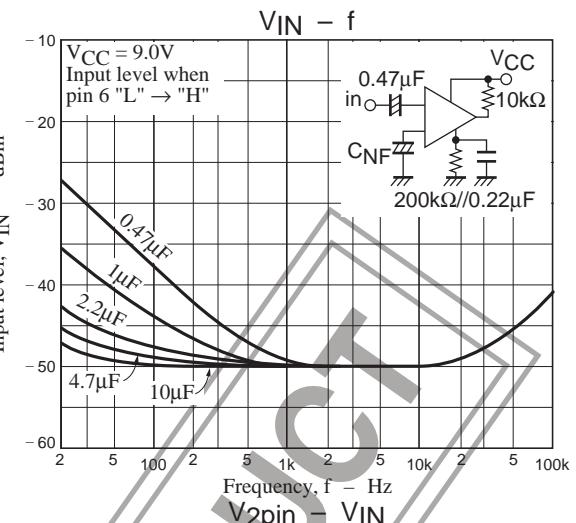
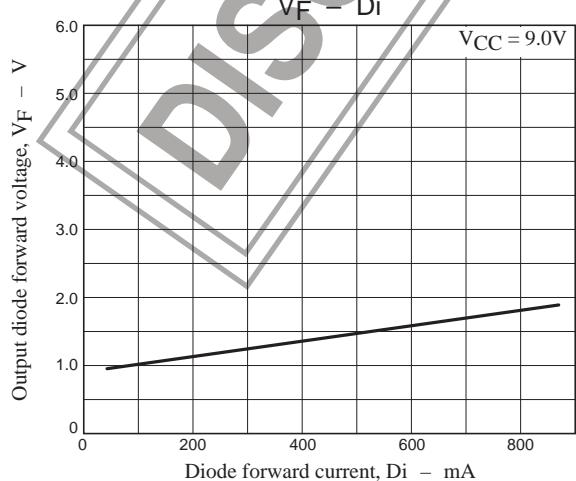
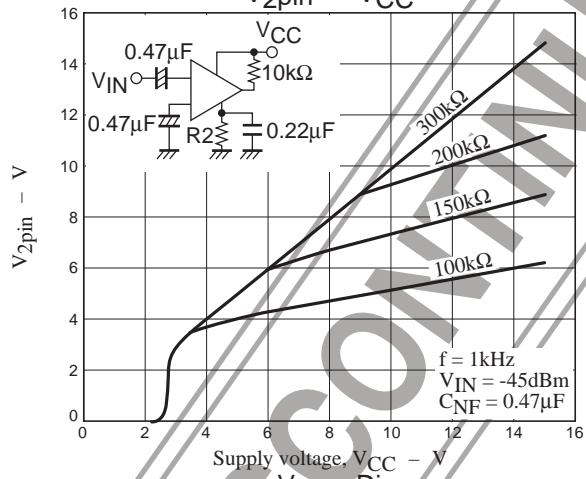
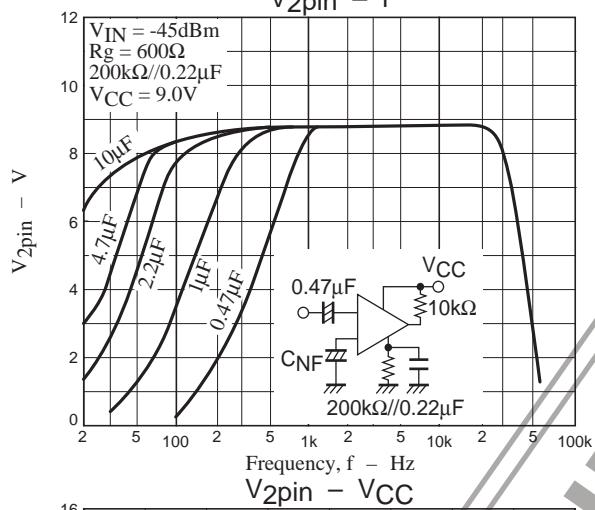
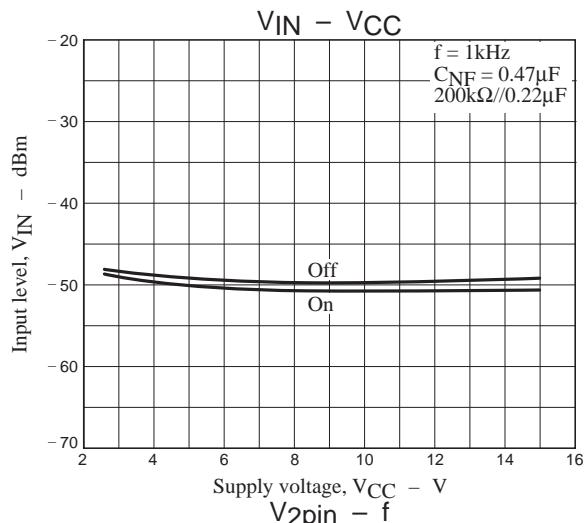


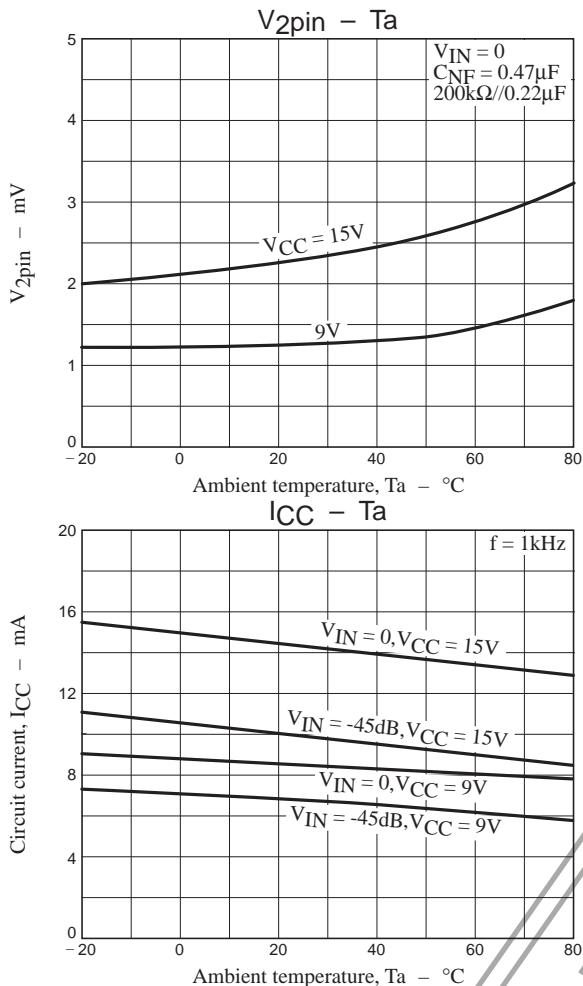
Sample Application Circuit 2



Use a mechanism for the plunger off while functioning for program selection







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