



# DAC8043

## CMOS 12-Bit Serial Input Multiplying DIGITAL-TO-ANALOG CONVERTER

### FEATURES

- 12-BIT ACCURACY IN 8-PIN SOIC
- FAST 3-WIRE SERIAL INTERFACE
- LOW INL AND DNL:  $\pm 1/2$  LSB max
- GAIN ACCURACY TO  $\pm 1$  LSB max
- LOW GAIN TEMPCO: 5 ppm/ $^{\circ}$ C max
- OPERATES WITH +5V SUPPLY
- TTL/CMOS COMPATIBLE
- ESD PROTECTED

### APPLICATIONS

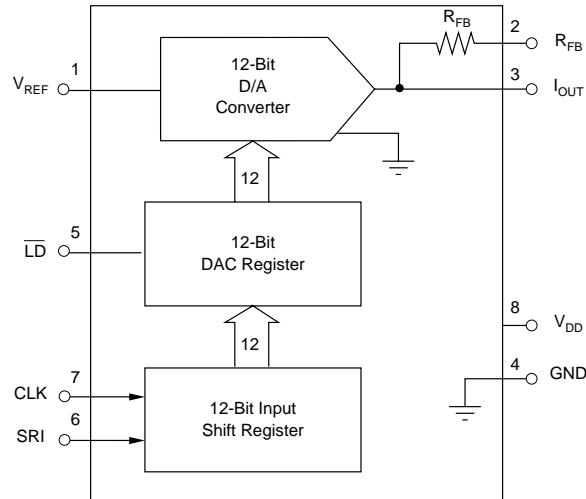
- AUTOMATIC CALIBRATION
- MOTION CONTROL
- MICROPROCESSOR CONTROL SYSTEMS
- PROGRAMMABLE AMPLIFIER/ATTENUATORS
- DIGITALLY CONTROLLED FILTERS

### DESCRIPTION

The DAC8043 is a 12-bit current output multiplying digital-to-analog converter (DAC) that is packaged in a space-saving, surface-mount 8-pin SOIC. Its 3-wire serial interface saves additional circuit board space which results in low power dissipation. When used with microprocessors having a serial port, the DAC8043 minimizes the digital noise feedthrough from its input to output. The serial port can be used as a dedicated analog bus and kept inactive while the DAC8043 is in use. Serial interfacing reduces the complexity of opto or transformer isolation applications.

The DAC8043 contains a 12-bit serial-in, parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC, and control logic. Serial input (SRI) data is clocked into the input register on the rising edge of the clock (CLK) pulse. When the new data word had been clocked in, it is loaded into the DAC register by taking the LD input low. Data in the DAC register is converted to an output current by the D/A converter.

The DAC8043 operates from a single +5V power supply which makes the DAC8043 an ideal low power, small size, high performance solution for several applications.



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# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

At  $V_{DD} = +5V$ ;  $V_{REF} = +10V$ ;  $I_{OUT} = GND = 0V$ ;  $T_A = \text{Full Temperature Range}$  specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC8043U			DAC8043UC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>STATIC PERFORMANCE</b>									
Resolution	N		12			12			Bits
Nonlinearity <sup>(1)</sup>	INL				$\pm 1$			$\pm 1/2$	LSB
Differential Nonlinearity <sup>(2)</sup>	DNL				$\pm 1$			$\pm 1/2$	LSB
Gain Error <sup>(3)</sup>	FSE	$T_A = +25^\circ C$ $T_A = \text{Full Temp Range}$			$\pm 2$			$\pm 1$	LSB
Gain Tempco <sup>(5)</sup>	$TC_{FSE}$	$\Delta V_{DD} = \pm 5\%$ $T_A = +25^\circ C$	$\pm 0.0006$	$\pm 0.002$	$\pm 2$	$\pm 0.0006$	$\pm 0.002$	$\pm 5$	$\text{ppm}/^\circ C$
Power Supply Rejection Ratio	PSRR	$T_A = \text{Full Temp Range}$			$\pm 5$			$\pm 5$	%/%
Output Leakage Current <sup>(4)</sup>	$I_{LKG}$	$T_A = +25^\circ C$ $T_A = \text{Full Temp Range}$			$\pm 100$			$\pm 25$	nA
Zero Scale Error <sup>(7, 12)</sup>	$I_{ZSE}$	$T_A = +25^\circ C$ $T_A = \text{Full Temp Range}$	7	11	0.03	7	11	0.03	LSB
Input Resistance <sup>(8)</sup>	$R_{IN}$				0.60			0.15	LSB
					15			15	$\text{k}\Omega$
<b>AC PERFORMANCE</b>									
Output Current Settling Time <sup>(5, 6)</sup>	$t_S$	$T_A = +25^\circ C$ $V_{REF} = 0V$		0.25	1		0.25	1	$\mu\text{s}$
Digital-to-Analog Glitch Energy <sup>(5, 10)</sup>	Q	$I_{OUT} = \text{Load} = 100\Omega$ $C_{EXT} = 13\text{pF}$		2	20		2	20	$\text{nVs}$
Feedthrough Error <sup>(5, 11)</sup> ( $V_{REF}$ to $I_{OUT}$ )	FT	$V_{REF} = 20\text{Vp-p}$ at $f = 10\text{kHz}$ Digital Input = 0000 0000 0000		0.7	1		0.7	1	$\text{mVp-p}$
Total Harmonic Distortion <sup>(5)</sup>	THD	$T_A = +25^\circ C$ $V_{REF} = 6V_{RMS}$ at $1\text{kHz}$		-85			-85		$\text{dB}$
Output Noise Voltage Density <sup>(5, 13)</sup>	$e_N$	$DAC \text{ Register Loaded with all 1s}$ $10\text{Hz to } 100\text{kHz}$ Between $R_{FB}$ and $I_{OUT}$			17			17	$\text{nV}/\sqrt{\text{Hz}}$
<b>DIGITAL INPUTS</b>									
Digital Input High	$V_{IH}$		2.4			2.4			V
Digital Input Low	$V_{IL}$				0.8			0.8	V
Input Leakage Current <sup>(9)</sup>	$I_{IL}$	$V_{IN} = 0V$ to $+5V$			$\pm 1$			$\pm 1$	$\mu\text{A}$
Input Capacitance <sup>(5, 11)</sup>	$C_{IN}$	$V_{IN} = 0V$			8			8	$\text{pF}$
<b>ANALOG OUTPUTS</b>									
Output Capacitance <sup>(5)</sup>	$C_{OUT}$	Digital Inputs = $V_{IH}$ Digital Inputs = $V_{IL}$		110			110		$\text{pF}$
				80			80		$\text{pF}$
<b>TIMING CHARACTERISTICS<sup>(5, 14)</sup></b>									
Data Setup Time	$t_{DS}$	$T_A = \text{Full Temperature Range}$	40			40			ns
Data Hold Time	$t_{DH}$	$T_A = \text{Full Temperature Range}$	80			80			ns
Clock Pulse Width High	$t_{CH}$	$T_A = \text{Full Temperature Range}$	90			90			ns
Clock Pulse Width Low	$t_{CL}$	$T_A = \text{Full Temperature Range}$	120			120			ns
Load Pulse Width	$t_{LD}$	$T_A = \text{Full Temperature Range}$	120			120			ns
LSB Clock into Input Register to Load DAC Register Time	$t_{ASB}$	$T_A = \text{Full Temperature Range}$	0			0			ns
<b>POWER SUPPLY</b>									
Supply Voltage	$V_{DD}$		4.75	5	5.25	4.75	5	5.25	V
Supply Current	$I_{DD}$	Digital Inputs = $V_{IH}$ or $V_{IL}$ Digital Inputs = 0V or $V_{DD}$			500			500	$\mu\text{A}$
					100			100	$\mu\text{A}$

NOTES: (1)  $\pm 1/2$  LSB =  $\pm 0.012\%$  of Full Scale. (2) All grades are monotonic to 12-bits over temperature. (3) Using internal feedback resistor. (4) Applies to  $I_{OUT}$ ; All digital inputs = 0V. (5) Guaranteed by design and not tested. (6)  $I_{OUT}$  Load =  $100\Omega$ ,  $C_{EXT} = 13\text{pF}$ , digital input = 0V to  $V_{DD}$  or  $V_{DD}$  to 0V. Extrapolated to 1/2 LSB:  $t_s$  = propagation delay ( $t_{PD}$ ) +  $9\tau$  where  $\tau$  = measured time constant of the final RC decay. (7)  $V_{REF} = +10V$ , all digital inputs = 0V. (8) Absolute temperature coefficient is less than  $\pm 50\text{ppm}/^\circ C$ . (9) Digital inputs are CMOS gates:  $I_{IN}$  is typically 1nA at  $+25^\circ C$ . (10)  $V_{REF} = 0V$ , all digital inputs = 0V to  $V_{DD}$  or  $V_{DD}$  to 0V. (11) All digital inputs = 0V. (12) Calculated from worst case  $R_{REF}$ :  $I_{ZSE}$  (in LSBS) =  $(R_{REF} \times I_{LKG} \times 4096)/V_{REF}$ . (13) Calculations from  $en = \sqrt{4K \cdot TRB}$  where: K = Boltzmann constant,  $J/K$ ; R = resistance,  $\Omega$ ; T = Resistor temperature,  $^\circ K$ ; B = bandwidth, Hz. (14) Tested at  $V_{IN} = 0V$  or  $V_{DD}$ .

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## WAFER TEST LIMITS

At  $V_{DD} = +5V$ ;  $V_{REF} = +10V$ ;  $I_{OUT} = GND = 0V$ ;  $T_A = +25^\circ C$ .

PARAMETER	SYMBOL	CONDITIONS	LIMIT	DAC8043 UNITS
<b>STATIC ACCURACY</b> Resolution Integral Nonlinearity Differential Nonlinearity Gain Error Power Supply Rejection Ratio Output Leakage Current ( $I_{OUT}$ )	N INL DNL $G_{FSE}$ PSRR $I_{LKG}$	Using Internal Feedback Resistor $\Delta V_{DD} = \pm 5\%$ Digital Inputs = $V_{IL}$	12 $\pm 1$ $\pm 1$ $\pm 2$ $\pm 0.002$ $\pm 5$	Bits min LSB max LSB max LSB max %% max nA max
<b>REFERENCE INPUT</b> Input Resistance	$R_{IN}$		7/15	$k\Omega$ min/max
<b>DIGITAL INPUTS</b> Digital Input HIGH Digital Input LOW Input Leakage Current	$V_{IH}$ $V_{IL}$ $I_{IL}$	$V_{IN} = 0V$ to $V_{DD}$	2.4 0.8 $\pm 1$	V min V max $\mu A$ max
<b>POWER SUPPLY</b> Supply Current	$I_{DD}$	Digital Inputs = $V_{IH}$ or $V_{IL}$ Digital Inputs = 0V to $V_{DD}$	500 100	$\mu A$ max $\mu A$ max

NOTE: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND .....	0V, +7V
$V_{REF}$ to GND .....	$\pm 25V$
$V_{RFB}$ to GND .....	$\pm 25V$
Digital Input Voltage Range .....	$-0.3V$ to $V_{DD}$
Output Voltage (Pin 3) .....	$-0.3V$ to $V_{DD}$
Operating Temperature Range	
AD .....	$0^\circ C$ to $+70^\circ C$
U, UC .....	$-40^\circ C$ to $+85^\circ C$
Junction Temperature .....	$+150^\circ C$
Storage Temperature .....	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (soldering, 10s) .....	$+300^\circ C$
$\theta_{JA}$ .....	$+100^\circ C/W$
$\theta_{JC}$ .....	$+42^\circ C/W$

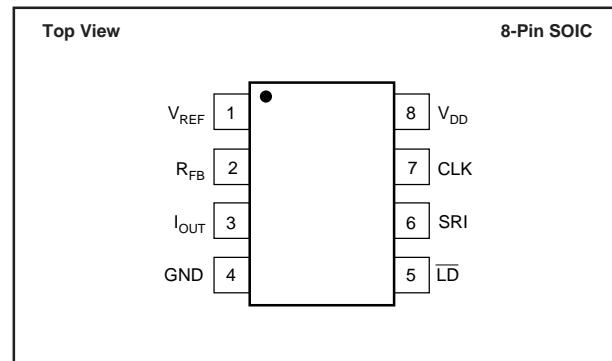
**CAUTION:** 1. Do not apply voltages higher than  $V_{DD}$  or less than GND potential on any terminal except  $V_{REF}$  (Pin 1) and  $R_{FB}$  (Pin 2). 2. The digital control inputs are ESD protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. 3. Use proper anti-static handling procedures. 4. Absolute Maximum Ratings apply to both packaged devices. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

## PACKAGE/ORDERING INFORMATION

PRODUCT	INL	TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
DAC8043U	1LSB	$-40^\circ C$ to $+85^\circ C$	8-pin SOIC	182
DAC8043UC	1/2LSB	$-40^\circ C$ to $+85^\circ C$	8-pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN CONFIGURATION



## ELECTROSTATIC DISCHARGE SENSITIVITY

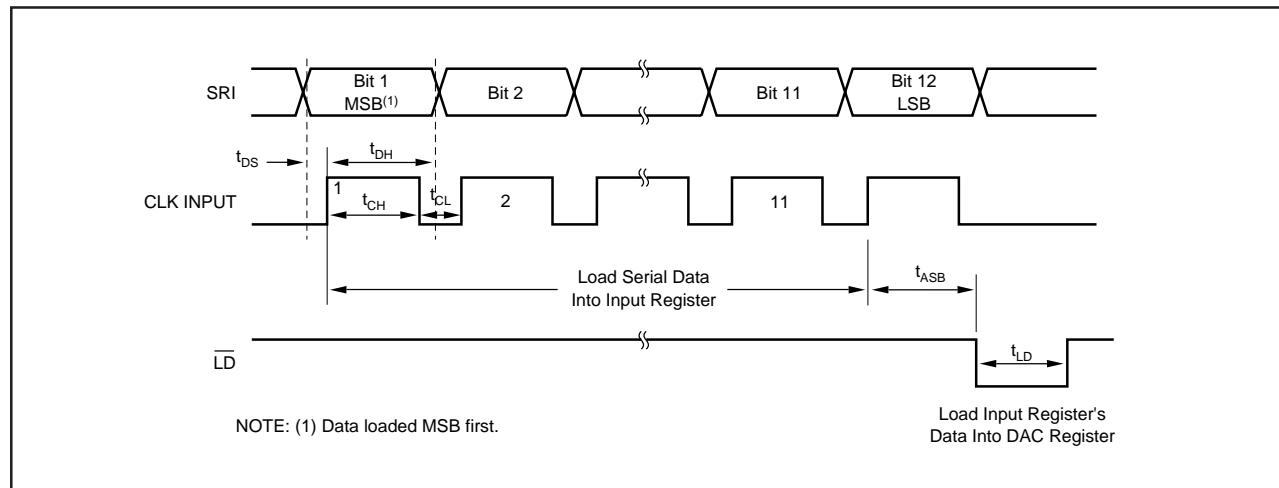
Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

**Digital Inputs:** All digital inputs of the DAC8043 incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500 $\Omega$ ) applied to each digital input.

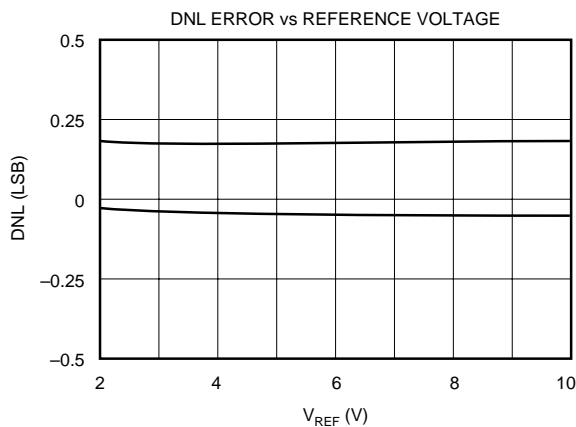
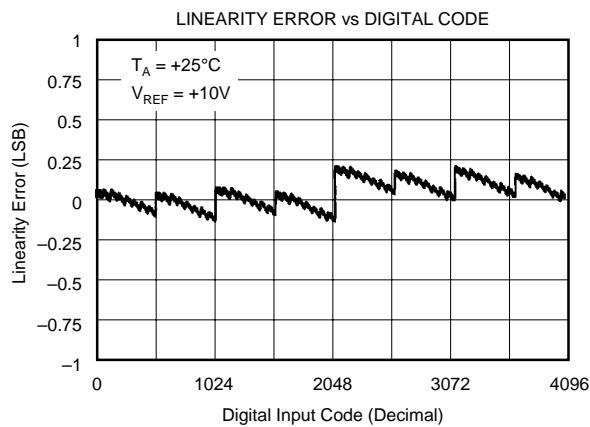
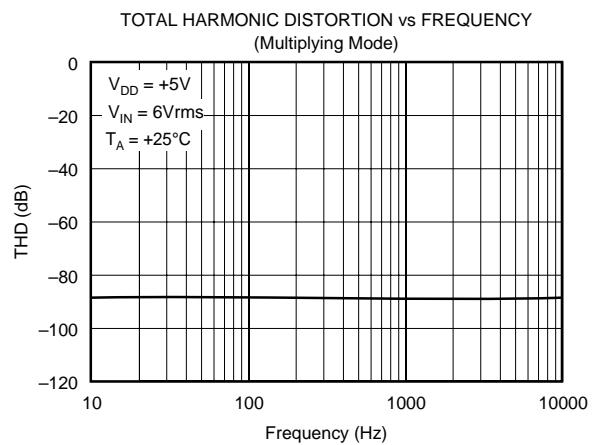
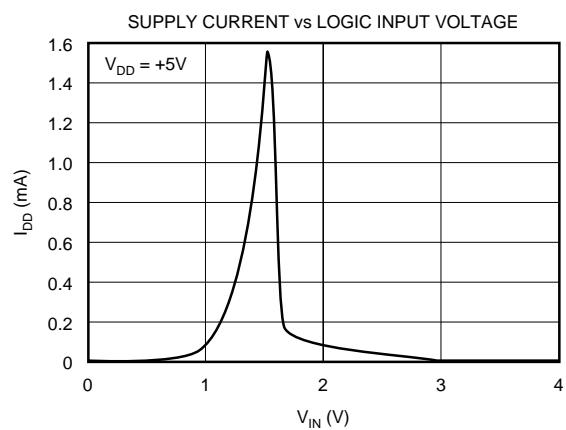
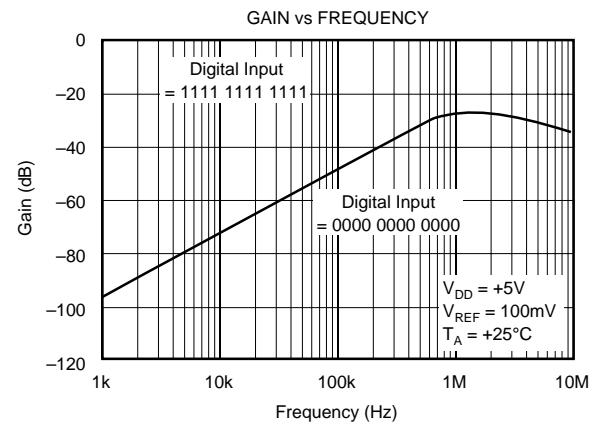
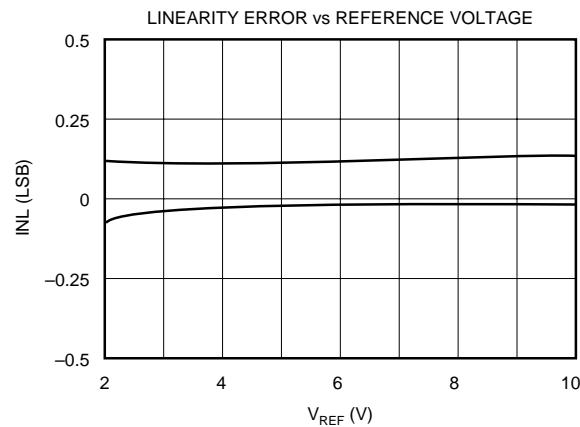
**Analog Pins:** Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500 $\Omega$ ) applied to each pin.  $V_{REF}$  and  $R_{FB}$  show some sensitivity.

## WRITE CYCLE TIMING DIAGRAM



## TYPICAL PERFORMANCE CURVES

At  $V_{DD} = +5V$ ;  $V_{REF} = +10V$ ;  $I_{OUT} = GND = 0V$ ;  $T_A = \text{Full Temperature Range}$  specified under Absolute Maximum Ratings, unless otherwise noted.



# DISCUSSION OF SPECIFICATIONS

## RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line, after zero and full scale errors have been adjusted to zero.

## DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output when the input code changes by 1LSB. A differential nonlinearity specification of 1LSB maximum guarantees monotonicity.

## GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC8043 is  $-(4095/4096)V_{REF}$ . Gain error may be adjusted to zero using external trims as shown in Figure 4.

## OUTPUT LEAKAGE CURRENT

The current which appears at  $I_{OUT}$  with the DAC loaded with all zeros.

## OUTPUT CAPACITANCE

The parasitic capacitance measured from  $I_{OUT}$  to GND.

## FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from  $V_{REF}$  to  $I_{OUT}$  with the DAC loaded with all zeros.

## OUTPUT CURRENT SETTLING TIME

The time required for the output current to settle to within  $\pm 0.01\%$  of final value for a full scale step.

## DIGITAL-TO-ANALOG GLITCH ENERGY

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to digital-to-analog glitch is charge injected by digital logic switching transients.

## CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of a DAC8043. The current from the  $V_{REF}$  pin is switched between  $I_{OUT}$  and GND by 12 single-pole double-throw CMOS switches. This main-

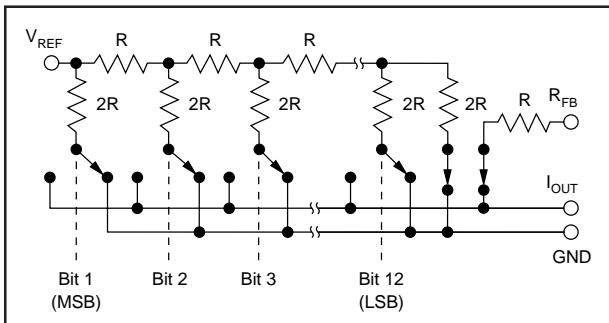


FIGURE 1. Simplified Circuit Diagram for the DAC.

tains a constant current in each leg of the ladder regardless of the input code. The input resistance at  $V_{REF}$  is therefore constant and can be driven by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to  $\pm 20V$ .

A CMOS switch transistor, included in series with the ladder terminating resistor and in series with the feedback resistor,  $R_{FB}$ , compensates for the temperature drift of the ON resistance of the ladder switches.

Figure 2 shows an equivalent circuit for the DAC.  $C_{OUT}$  is the output capacitance due to the N-channel switches and varies from about 80pF to 110pF with digital input code. The current source  $I_{LKG}$  is the combination of surface and junction leakages to the substrate.  $I_{LKG}$  approximately doubles every 10°C.  $R_O$  is the equivalent output resistance of the D/A and it varies with input code.

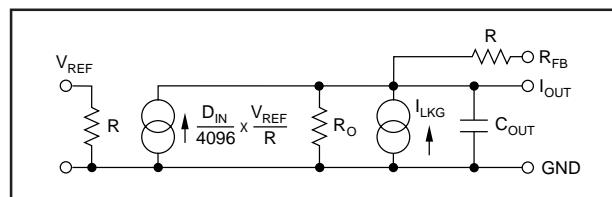


FIGURE 2. Equivalent Circuit for the DAC.

## INSTALLATION

### ESD PROTECTION

All digital inputs of the DAC8043 incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model, 100pF and 1500Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

### POWER SUPPLY CONNECTIONS

The DAC8043 is designed to operate on  $V_{DD} = +5V \pm 5\%$ . For optimum performance and noise rejection, power supply decoupling capacitors  $C_D$  should be added as shown in the application circuits. These capacitors (1μF tantalum recommended) should be located close to the D/A. Output op amp analog common (+ input) should be connected as near to the GND pins of the DAC8043 as possible.

### WIRING PRECAUTIONS

To minimize AC feedthrough when designing a PC board, care should be taken to minimize capacitive coupling between the  $V_{REF}$  lines and the  $I_{OUT}$  lines. Coupling from any of the digital control or data lines might degrade the glitch performance. Solder the DAC8043 directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance).

## AMPLIFIER OFFSET VOLTAGE

The output amplifier used with the DAC8043 should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op amp multiplied by the “noise gain” of the circuit. This “noise gain” is equal to  $(R_F/R_O + 1)$  where  $R_O$  is the output impedance of the D/A  $I_{OUT}$  terminal and  $R_F$  is the feedback network impedance. The nonlinearity occurs due to the output impedance varying with code. If the 0 code case is excluded (where  $R_O = \infty$ ), the  $R_O$  will vary from  $R$  to  $3R$  providing a “noise gain” variation between  $4/3$  and  $2$ . In addition, the variation of  $R_O$  is nonlinear with code, and the largest steps in  $R_O$  occur at major code transitions where the worst differential nonlinearity is also likely to be experienced. The nonlinearity seen at the amplifier output is

$$2V_{OS} - 4V_{OS}/3 = 2V_{OS}/3.$$

Thus, to maintain good nonlinearity the op amp offset should be much less than  $1/2$ LSB.

## UNIPOLAR CONFIGURATION

Figure 3 shows DAC8043 in a typical unipolar (two-quadrant) multiplying configuration. The analog output values

DATA INPUT	ANALOG OUTPUT
MSB ↓      ↓ LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096) = $-1/2V_{REF}$
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0 Volts

TABLE I. Unipolar Output Code.

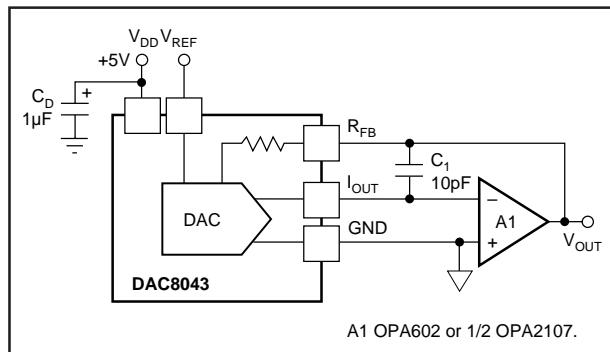


FIGURE 3. Unipolar Configuration.

versus digital input code are listed in Table I. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C1 provides phase compensation to minimize settling time and overshoot when using a high speed operational amplifier.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 4 may be used. Resistor R2 induces a positive gain error greater than worst-case initial negative gain error. Trim resistor R1 provides a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2.

## BIPOLAR CONFIGURATION

Figure 5 shows the DAC8043 in a typical bipolar (four-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602 or a dual amplifier such as the OPA2107. C1 provides phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R1–R2 should be ratio-matched to 0.01% to ensure the specified gain error performance.

DATA INPUT	ANALOG OUTPUT
MSB ↓      ↓ LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0001	$+V_{REF}$ (1/2048)
1000 0000 0000	0 Volts
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

TABLE II. Bipolar Output Code.

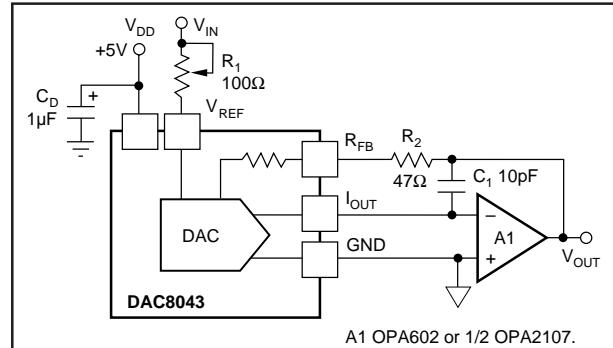


FIGURE 4. Unipolar Configuration with Gain Trim.

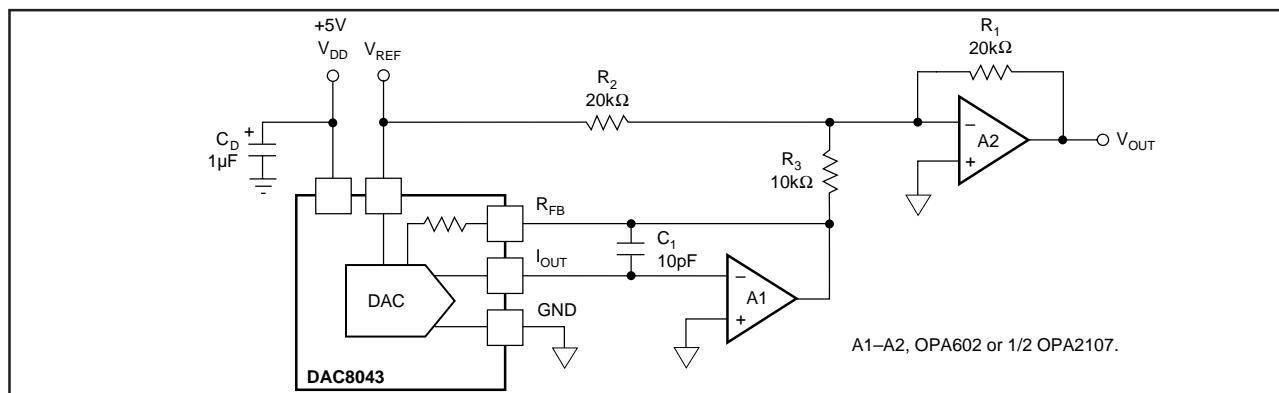


FIGURE 5. Bipolar Configuration.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
DAC8043U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC8043U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC8043U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC8043UC	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC8043UC/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC8043UC/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC8043UCG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC8043UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

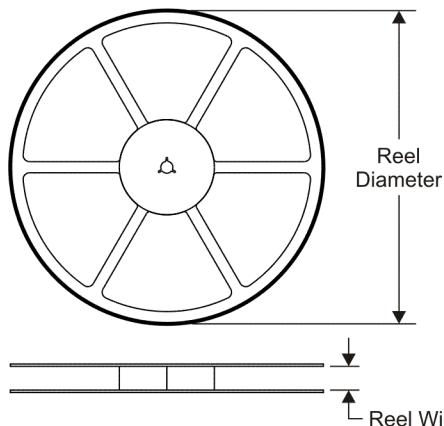
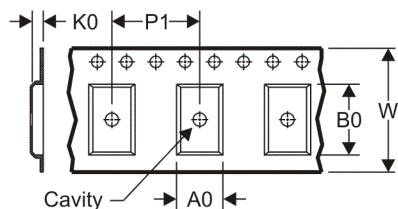
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

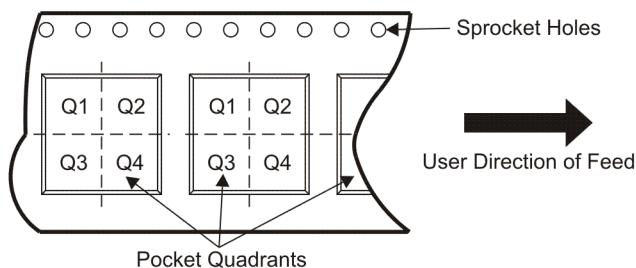
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


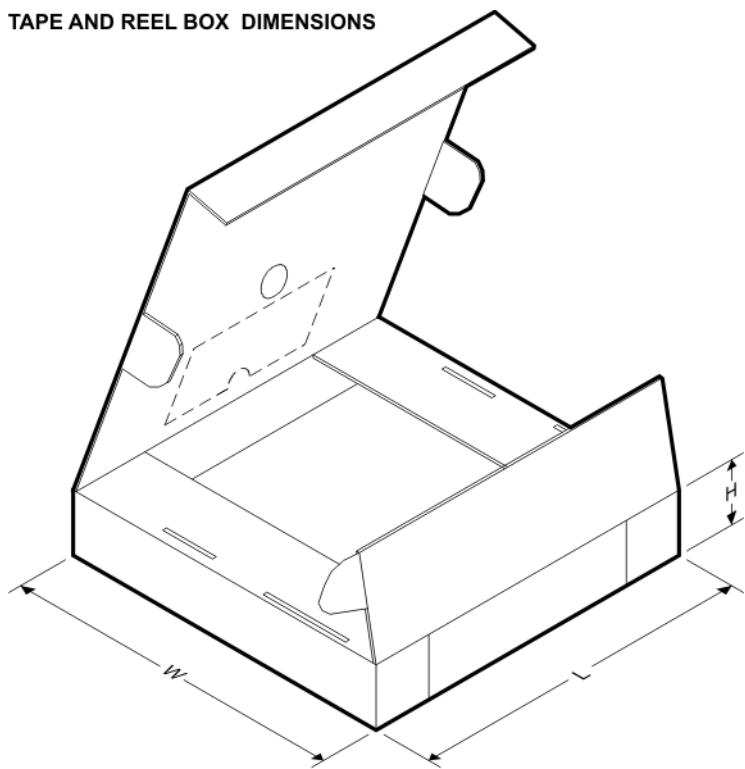
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8043U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
DAC8043UC/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8043U/2K5	SOIC	D	8	2500	346.0	346.0	29.0
DAC8043UC/2K5	SOIC	D	8	2500	346.0	346.0	29.0

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