

Switch-Dimmable LED Driver

Features

- Four-level Switch Dimming
- Highly Accurate Current Regulator
- Output Overcurrent or Short-circuit Protection
- IC Overtemperature Protection

Applications

- Switch-dimmable LED Bulbs and Fixtures

General Description

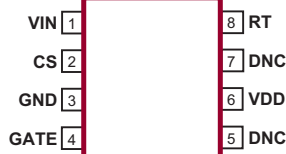
The HV9801A LED driver is ideally suited for switch-dimmable applications using LED bulbs and fixtures.

Through switch dimming, the lamp can be adjusted to four discrete brightness levels by rapid cycling of the light switch. The brightness levels are traversed in an up-and-down manner. Brightness resumes at the highest level when power is removed for more than a second.

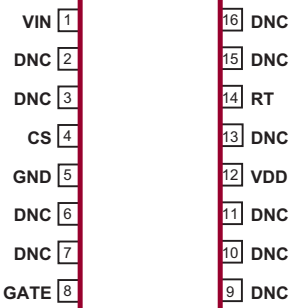
The device can be powered directly from rectified AC through an internal V_{DD} regulator rated at 450V.

Package Types

8-lead SOIC
(Top view)



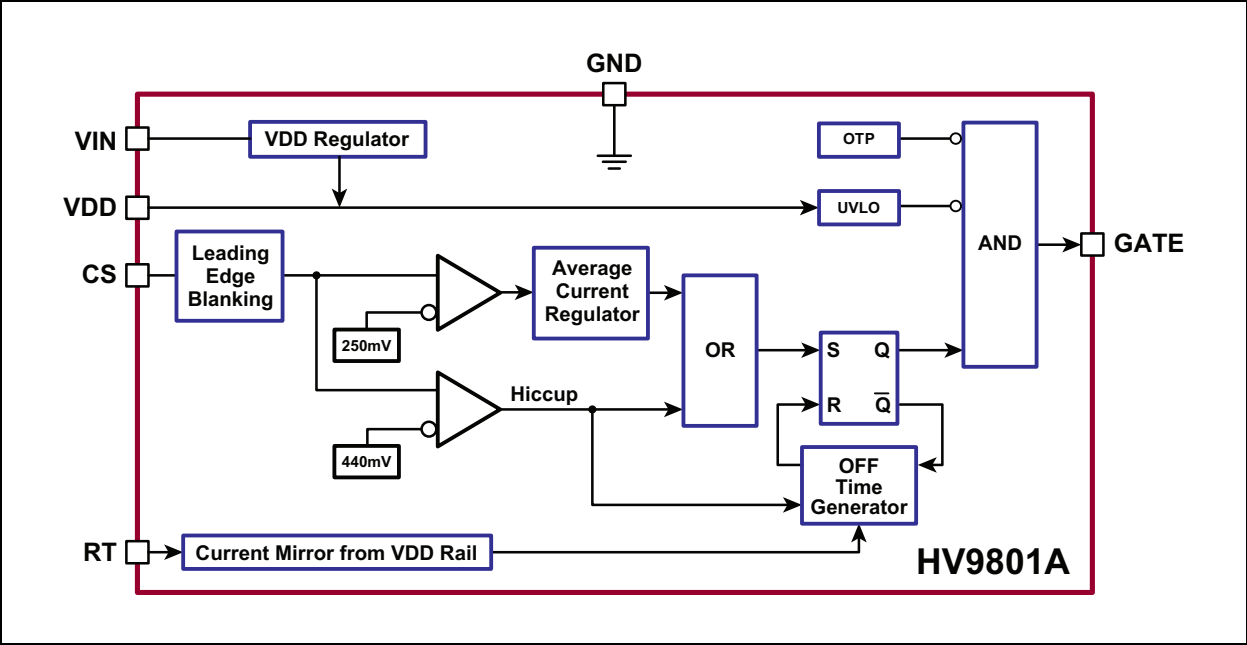
16-lead SOIC
(Top view)



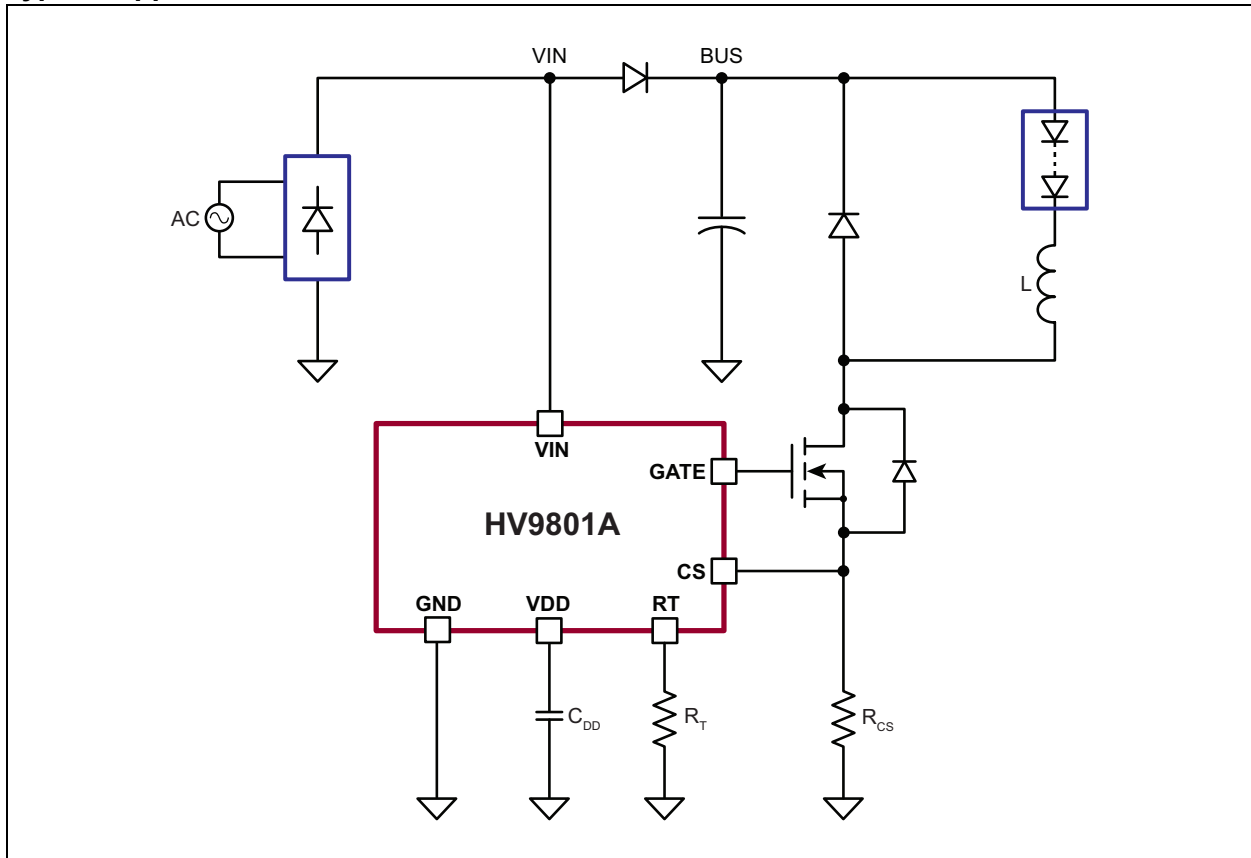
See [Table 2-1](#) for pin information.

HV9801A

Functional Block Diagram



Typical Application Circuit



HV9801A

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{IN}	470V
V_{DD}	12V
V_{CS} , V_{GATE}	-0.3V to (V_{DD} +0.3V)
Junction Temperature Range, T_J	-40°C to +150°C
Storage Temperature Range, T_S	-65°C to +150°C
Power Dissipation ($T_A = 25^\circ\text{C}$):	
8-lead SOIC	650 mW
16-lead SOIC	1000 mW

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Specifications are at $T_A = 25^\circ\text{C}$, $V_{IN} = 15\text{V}$ unless otherwise noted.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
INPUT						
Input Voltage	V_{IN}	15	—	450	V	Note 2
Input Current	I_{IN}	—	1	2	mA	
Supply Current, OTP Shutdown	$I_{IN, OT}$	—	—	500	μA	Note 1
V_{DD} REGULATOR						
Undervoltage Lockout Threshold	V_{UVLO}	6.45	6.7	7.1	V	V_{IN} rising (Note 2)
Undervoltage Lockout Hysteresis	ΔV_{UVLO}	—	500	—	mV	V_{IN} falling
Maximum Input Current, Limited by UVLO	I_{UVLO}	3.5	—	—	mA	$T_A = 25^\circ\text{C}$ (Note 1)
		1.5	—	—	mA	$T_A = 125^\circ\text{C}$ (Note 1)
Output Voltage	V_{DD}	7.25	7.5	7.75	V	$C_{GATE} = 500\text{ pF}$, $R_T = 226\text{ k}\Omega$
Line Regulation	$\Delta V_{DD, LINE}$	—	—	1	V	$V_{IN} = 15\text{V to } 450\text{V}$, $C_{GATE} = 500\text{ pF}$, $R_T = 226\text{ k}\Omega$
V_{DD} Voltage Margin	$\Delta V_{DD(UV)}$	500	—	—	mV	$\Delta V_{DD(UV)} = V_{DD} - V_{UVLO}$, FALL (Note 2)
Load Regulation	$\Delta V_{DD, LOAD}$	—	—	100	mV	$I_{VDD} = 0\text{ mA to } 1\text{ mA}$, $C_{GATE} = 500\text{ pF}$, $R_T = 226\text{ k}\Omega$
SWITCH DIMMING						
Supply Current after Power Loss	I_{VDDX}	—	—	700	μA	Note 2
Undervoltage Lockout during V_{IN} Power Loss	$V_{UVLO, DIM}$	—	3.5	—	V	V_{IN} falling
Power Loss, Qualification Time	T_{PL1}	—	60	—	ms	V_{IN} falling below V_{UVLO} (Note 1)
Power Loss, Time to Reset	T_{PL2}	—	1	—	s	
PWM Dimming Frequency	F_{PWM}	—	1.2	—	kHz	
LED CURRENT REGULATOR						
Current Sense Threshold	V_{CST}	236	250	256	mV	Note 2

Note 1: Determined by characterization; not production tested

2: Specifications apply over the full operating ambient temperature range of $-40^\circ\text{C} < T_A < +125^\circ\text{C}$.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Specifications are at $T_A = 25^\circ\text{C}$, $V_{IN} = 15\text{V}$ unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Leading Edge Blanking Time	T _{LEB}	110	—	260	ns	Note 2
Minimum On-time	T _{ONX}	—	—	760	ns	V _{CS} = V _{CST} + 30 mV
Maximum Duty Cycle Maintaining Regulation	D _{MAX}	80	—	—	%	LED current falls beyond this duty cycle
SHORT-CIRCUIT PROTECTION						
Hiccup Threshold	V _{CSH}	—	440	—	mV	
V _{CS} High to Gate Low Delay	T _{DLY}	—	—	180	ns	V _{CS} = V _{CSH} + 30 mV
Hiccup Time	T _{SCH}	—	750	—	μs	
Minimum On-time	T _{ONXSC}	—	—	430	ns	V _{CS} = V _{DD}
T _{OFF} TIMER						
Off-time	T _{OFF}	32	40	48	μs	R _T = 1 MΩ
		8	10	12		R _T = 226 kΩ
GATE DRIVER						
Sourcing Current	I _{SRC}	165	—	—	mA	V _{GATE} = 0V
Sinking Current	I _{SINK}	165	—	—	mA	V _{GATE} = V _{DD}
Rise Time	t _r	—	30	50	ns	C _{GATE} = 500 pF
Fall Time	t _f	—	30	50	ns	C _{GATE} = 500 pF
OVERTEMPERATURE PROTECTION						
Trip Temperature	T _{TRIP}	—	140	—	°C	Note 1
Hysteresis	ΔT _{TRIP}	—	20	—	°C	Note 1

Note 1: Determined by characterization; not production tested

2: Specifications apply over the full operating ambient temperature range of $-40^\circ\text{C} < T_A < +125^\circ\text{C}$.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	-40	—	+125	$^\circ\text{C}$	
Maximum Junction Temperature	T_J	-40	—	+150	$^\circ\text{C}$	
Storage Temperature	T_S	-65	—	+150	$^\circ\text{C}$	
PACKAGE THERMAL RESISTANCE						
8-lead SOIC	θ_{JA}	—	101	—	$^\circ\text{C/W}$	
16-lead SOIC	θ_{JA}	—	83	—	$^\circ\text{C/W}$	

HV9801A

2.0 PIN DESCRIPTION

The details on the pins of HV9801A are listed on [Table 2-1](#). See location of pins in [Package Types](#).

TABLE 2-1: PIN FUNCTION TABLE

Pin Name	8-lead SOIC Pin Number	16-lead SOIC Pin Number	Description
VIN	1	1	Connect to bridge rectifier output. Supplies power to the V_{DD} regulator. Detects light switch power-off event through loss of bridge rectifier output voltage. Do not connect excessive capacitance before or after the bridge to allow V_{IN} to drop rapidly after loss of power.
CS	2	4	Current sense input
GND	3	5	Ground
GATE	4	8	Gate driver output
VDD	6	12	V_{DD} regulator output. Connect a high-frequency bypass and a hold-up capacitor at V_{DD} . Bypass capacitor to be 100 nF minimum. See Section 3.0 “Application Information” for hold-up capacitance.
RT	8	14	Off-time programming input. Connect programming resistor to GND.
DNC	5, 7	2, 3, 6, 7, 9, 10, 11, 13, 15, 16	Stands for “Do Not Connect.”

3.0 APPLICATION INFORMATION

3.1 Current Control

3.1.1 CONTINUOUS CONDUCTION MODE (CCM)

The HV9801A is designed to control a buck converter operating in CCM.

Continuous Conduction Mode operation is characterized by converter operation with non-zero inductor current throughout the switching cycle. Such operation can be achieved by proper selection of the inductance.

3.1.2 LED CURRENT

The HV9801A regulates the LED current with an accuracy far superior to that of competing Peak Current mode controllers.

Average LED current is set by the current sense resistor R_{CS} and the current regulator reference voltage. See [Equation 3-1](#) and [Equation 3-2](#).

EQUATION 3-1:

$$V = I \times R$$

EQUATION 3-2:

$$250mV = I_{LED} \times R_{CS}$$

For example, a 2Ω resistor corresponds to a 125 mA (average) LED current.

3.1.3 CURRENT CONTROL PERFORMANCE

The control method of the HV9801A virtually eliminates the regulation errors associated with Peak Current mode controllers, such as errors caused by inductor tolerance, propagation delay of the current sense comparator, tolerance in the oscillator frequency or off-timer and changes in line and load voltage.

[Figure 3-1](#) compares the load regulation of the HV9801A and that of a device with peak current control. The graph clearly shows the difference in load regulation between the HV9801A and the HV9910B, which is a peak current regulator.

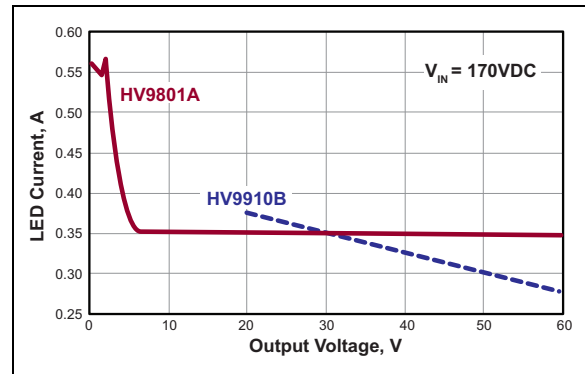


FIGURE 3-1: Output Characteristics of the HV9801A LED Driver.

3.2 Duty Cycle, Off-time, On-time and Inductor

3.2.1 DUTY CYCLE

The duty cycle (D) is related to the load voltage (V_{LED}) and input voltage (V_{BUS}) by the simple relation shown in [Equation 3-3](#) and [Equation 3-4](#).

EQUATION 3-3:

$$V_{OUT} = D \times V_{IN}$$

EQUATION 3-4:

$$V_{LED} = D \times V_{BUS}$$

3.2.2 OFF-TIME

The HV9801A operates with constant off-time control, which avoids subharmonic oscillation.

Switching period and switching frequency are related to on-time and off-time as shown in [Equation 3-5](#) and [Equation 3-6](#).

EQUATION 3-5:

$$T_{SW} = T_{ON} + T_{OFF}$$

EQUATION 3-6:

$$F_{SW} = \frac{1}{T_{SW}}$$

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On-time is related to off-time and duty cycle. See [Equation 3-7](#).

EQUATION 3-7:

$$D = \frac{T_{ON}}{(T_{ON} + T_{OFF})}$$

$$T_{ON} = [D / (1 - D)] \times T_{OFF}$$

With a given T_{OFF} , the HV9801A dynamically adjusts T_{ON} to regulate the LED current. Specifically, T_{ON} adapts to the duty cycle associated with the given V_{BUS} and V_{LED} .

3.2.3 OFF-TIME PROGRAMMING

Off-time is programmed by the R_T resistor as illustrated in [Equation 3-8](#).

EQUATION 3-8:

$$T_{OFF} = (A \times R_T) + B$$

Where: $A = 40 \text{ ps} / \Omega$ and $B = 300 \text{ ns}$

For instance, a 200 k Ω resistor corresponds to 8.3 μs off-time.

An acceptable range for R_T is 30 k Ω to 1 M Ω , corresponding to an off-time range between 1.5 μs and 40.3 μs .

3.2.4 INDUCTOR

Because the converter should operate in CCM, the inductor current should not fall to zero within a switching cycle and the inductor current ripple should be sized accordingly.

A common choice for peak-to-peak inductor current ripple (PPR) is 30% to 40% of nominal LED current.

Inductance can be calculated from the current drop during off-time as shown in [Equation 3-9](#) and [Equation 3-10](#).

EQUATION 3-9:

$$L \times \Delta I = V \times \Delta T$$

EQUATION 3-10:

$$L \times \text{PPR} \times I_{LED} = V_{LED} \times T_{OFF}$$

For example, 30% PPR on 350 mA average current equates to 105 mA ripple, which together with 5 μs off-time and 30V LED string voltage corresponds to 1.43 mH inductance.

A design with 30V LED voltage and 150V bus voltage corresponds to a 20% duty cycle, while a 120V bus voltage coincides with a 25% duty cycle. A 20% duty cycle corresponds to 1.25 μs on-time, and a 25% duty

cycle corresponds to 1.67 μs on-time. Hence, the switching frequency is 160 kHz at 150V bus voltage and 150 kHz at 120V bus voltage.

3.2.5 MAXIMUM DUTY CYCLE

Duty cycle should be limited to the specified maximum of 80%. Accordingly, the targeted LED string voltage and the bus voltage are limited to the same ratio. Operation at a larger desired duty cycle than the maximum duty cycle results in an LED current lower than programmed.

3.2.6 MINIMUM DUTY CYCLE

Duty cycle is limited on the low side by the minimum on-time specification (760 ns). Operation at a smaller desired on-time than the minimum causes the LED current to exceed the programmed value.

LED string voltage cannot be made arbitrarily low. Minimum LED string voltage can be determined with [Equation 3-11](#).

EQUATION 3-11:

$$D_{MIN} = \frac{T_{ONX}}{(T_{OFF} + T_{ONX})}$$

$$V_{LED} = D_{MIN} \times V_{BUS}$$

For instance, with 5 μs off-time, the duty cycle should be kept above 13%. Such a duty cycle corresponds to an LED string voltage of 19.5V at 150V bus voltage.

A design that needs a lower LED string voltage requires a longer off-time.

3.2.7 SHORT-CIRCUIT PROTECTION

An increase in the LED current sense signal above 440 mV (176% of nominal) trips the short-circuit comparator, thereby causing the converter to switch to Hiccup mode. In Hiccup mode, off-time is lengthened to about 750 μs to allow the inductor current to drop to a safe level.

Without the extended off-time, the inductor current increases with every switching cycle, causing an overcurrent damage to the converter.

The off-time extension can be observed in [Figure 3-2](#) below.

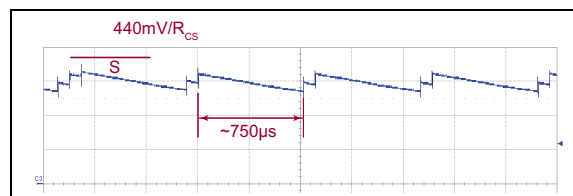


FIGURE 3-2: Short-circuit Inductor Current.

3.2.8 LEADING EDGE BLANKING

The MOSFET drain current and the current sense signal exhibit a spike at the start of a switching cycle, which arises from the MOSFET gate charging current and the current required for discharging the MOSFET drain node. These two currents typically exceed the inductor by quite a margin.

The current sense signal is blanked at the start of the switching cycle in order to avoid a premature trigger of the current sense and the short-circuit protection comparators.

3.2.9 V_{DD} REGULATOR

The V_{DD} regulator generates a source of regulated voltage for operation of internal and external circuits from the power applied at the V_{IN} pin. Alternatively, the V_{DD} voltage can be supplied from a source directly connected to the V_{DD} pin.

3.3 Switch Dimming

3.3.1 GENERAL

Lamp brightness can be adjusted to one of four discrete levels by rapidly cycling power with the light switch. The brightness levels are traversed in an up-and-down manner, the four levels being 100%, 50%, 25% and 12.5%. Brightness resumes at the highest level when power is removed for more than a second.

Reduction of LED current is accomplished through PWM dimming with a PWM dimming frequency of about 1 kHz. The PWM frequency is generated by an internal oscillator, and the PWM duty cycle is controlled by digital logic.

Turning the light switch off and on within one second adjusts LED current to the next level in each dimming step. The direction of dimming depends on the existing position in the dimming sequence. The illustration in [Figure 3-3](#) shows more details. The sequence starts at 100% and adjusts to the next lower level by the first dimming step and then adjusts to the next lower level by the next dimming step. Upon reaching the lowest or highest level, the direction of the sequence reverses. Therefore, the actual overall dimming sequence is 100%, 50%, 25%, 12.5%, 25%, 50%, 100%, and the sequence repeats as the dimming steps continue. When power is removed for more than one second, the dimming sequence is terminated and the brightness is reset to 100% upon turn-on of the light switch.

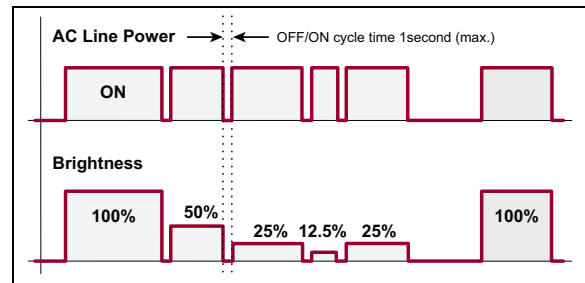


FIGURE 3-3: LED Brightness and AC Line Power.

3.3.2 V_{DD} CAPACITOR

The V_{DD} voltage should be maintained for at least one second and above the 3.5V level after loss of V_{IN} power to allow certain timing circuits to function.

The minimum V_{DD} capacitance required can be calculated with [Equation 3-12](#).

EQUATION 3-12:

$$C \times \Delta V = I \times \Delta T$$

$$C_{DD} \times (7.5V - 3.5V) = I_{VDDX} \times 1s$$

With 700 μA of I_{VDDX} the bypass capacitance should be 175 μF .

3.3.3 DETECTION OF POWER CYCLING

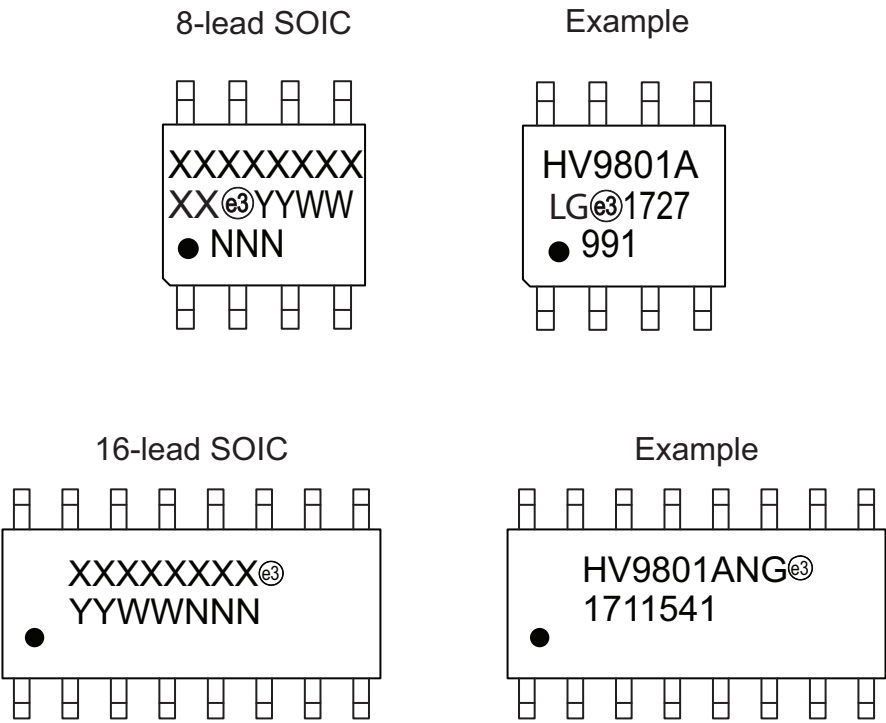
The presence of AC line power is detected at the V_{IN} pin. To this end, loss of AC power should result in a rapidly falling voltage at the output of the bridge rectifier.

The V_{IN} voltage drops due to the current draw from the V_{DD} regulator. In order to facilitate a quick drop in voltage, a diode should be added to isolate the bus capacitor from the V_{IN} pin as shown in the [Typical Application Circuit](#).

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4.0 PACKAGING INFORMATION

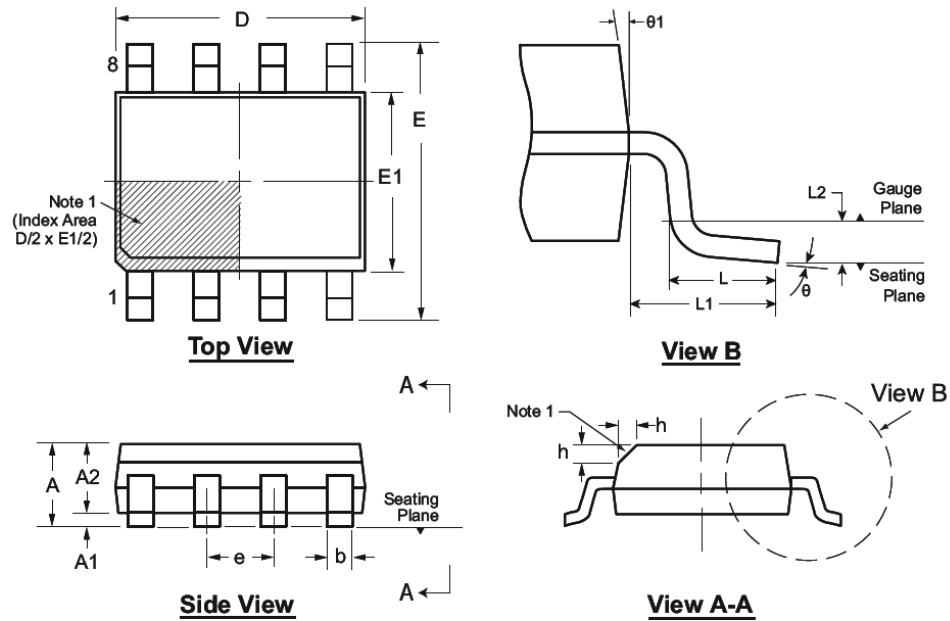
4.1 Package Marking Information



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC [®] designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

8-Lead SOIC (Narrow Body) Package Outline (LG/TG) 4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier, an embedded metal marker, or a printed indicator.

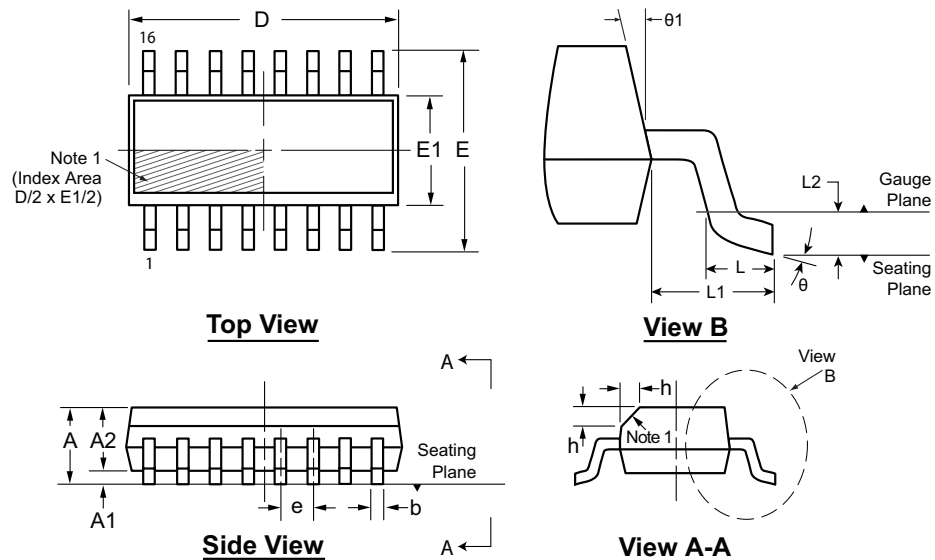
Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

16-Lead SOIC (Narrow Body) Package Outline (NG) 9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

APPENDIX A: REVISION HISTORY

Revision A (September 2017)

- Converted Supertex Doc# DSFP-HV9801A to Microchip DS20005692A
- Updated the part marking format
- Removed the 16-lead SOIC Narrow (NG) M934 media type
- Changed the quantity of the 8-lead SOIC (Narrow) LG package from 2500/Reel to 3300/Reel
- Made minor text changes throughout the document

HV9801A

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	HV9801A	=	Switch-Dimmable LED Driver		
Packages:	LG	=	8-lead SOIC		
	NG	=	16-lead SOIC		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	3300/Reel for an LG Package		
		=	45/Tube for an NG Package		

Examples:

a) HV9801ALG-G: Switch-Dimmable LED Driver, 8-lead SOIC Package, 3300/Reel

b) HV9801ANG-G: Switch-Dimmable LED Driver, 16-lead SOIC Package, 45/Tube

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