IS31FL3238

18-CHANNEL LED DRIVER

July 2019

GENERAL DESCRIPTION

IS31FL3238 is an LED driver with 18 constant current channels. Each channel can be pulse width modulated (PWM) by 16 bits for smooth LED brightness control. In addition, each channel has an 8-bit output current control register which allows fine tuning the current for rich RGB color mixing, e.g., a pure white color LED application. The maximum output current of each channel is designed to be 78mA, which can be adjusted by one 8-bit global control register. Proprietary programmable algorithms are used in IS31FL3238 to minimize audible noise caused by the MLCC decoupling capacitor. All registers can be programmed via a high speed I2C (1MHz).

IS31FL3238 can be turned off with minimum current consumption by either pulling the SDB pin low or by using the software shutdown feature.

IS31FL3238 is available in QFN-28 (5mm×5mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- 2.7V to 5.5V VCC supply
- 1MHz I2C interface, automatic address increment function with readout function
- Four selectable I2C addresses
- Accurate color rendition
  - Selectable 16-bit PWM 256/1024/4096/65536
  - 8-bit dot correction
  - 8-bit global current adjust
- Open/Short detect function
- 62kHz PWM frequency (8-bit PWM)
- Temperature detect function
- EMI/noise reduction technology
  - Spread spectrum
  - Selectable 6 phase delay
  - 180 degree phase delay
- -40°C to +125°C temperature range
- QFN-28 (5mm×5mm) package

APPLICATIONS

- AI-speakers and smart home devices
- Hand-held devices for LED display
- LED in home appliances

TYPICAL APPLICATION CIRCUIT

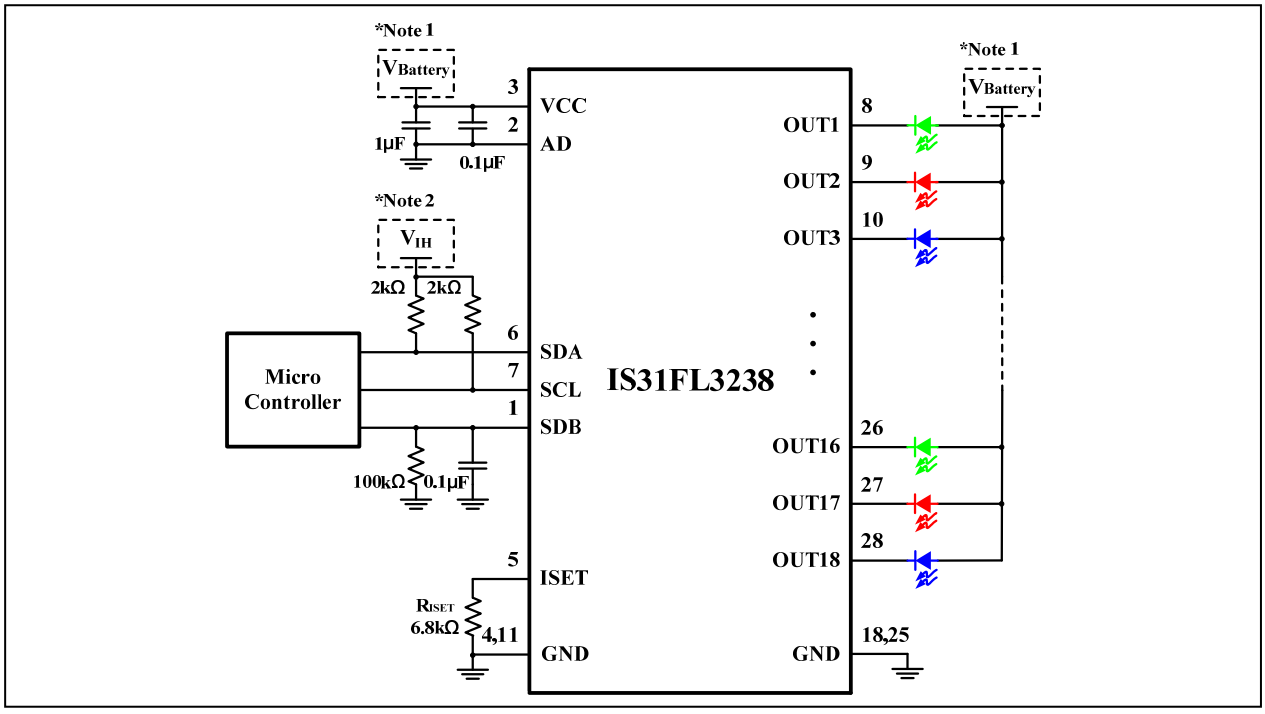


Figure 1 Typical Application Circuit

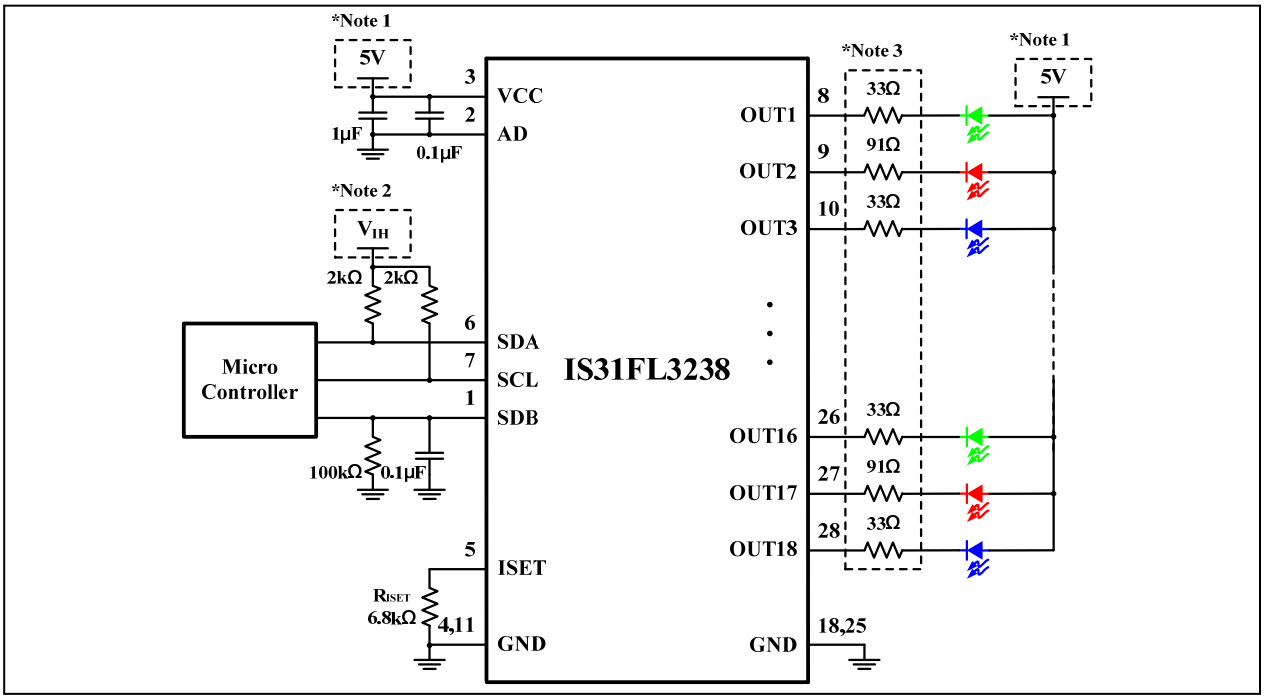


Figure 2 Typical Application Circuit

Note 1: V_{LED+} should be same as VCC voltage.

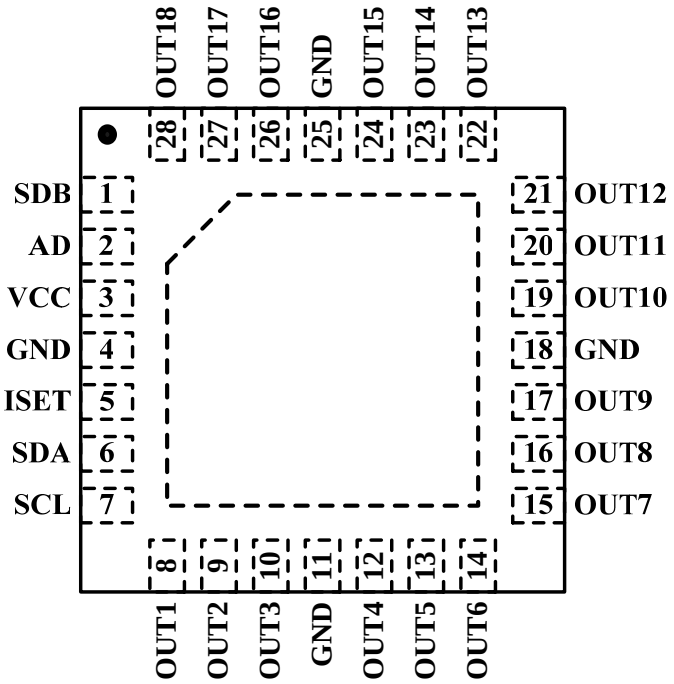
Note 2: V_{IH} is the high level voltage for IS31FL3238, which is usually same as VCC of Micro Controller, e.g. if VCC of Micro Controller is 3.3V, V_{IH}=3.3V. If V_{CC}=5V and V_{IH} is lower than 2.8V, recommend to add a level shift circuit.

Note 3: These resistors are optional to help reduce the power of IS31FL3238 only (values are for V_{LED+}=5V).

Note 4: The output current is set up to 23mA when R_{ISET} = 6.8kΩ. The maximum global output current can be set by external resistor, R_{ISET}. Please refer to the detail application information in R_{ISET} section.

Note 5: The IC should be placed far away from the antenna in order to prevent the EMI.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-28	

PIN DESCRIPTION

No.	Pin	Description
1	SDB	Shutdown the chip when pulled low.
2	AD	I2C address setting.
3	VCC	Power supply.
4,11,18,25	GND	Ground.
5	ISET	Input terminal used to connect an external resistor. This regulates the global output current. When R_{ISET}= 6.8kΩ, I_{OUT}= 23mA.
6	SDA	I2C serial data.
7	SCL	I2C serial clock.
8~10	OUT1~OUT3	Output channel 1~3 for LEDs.
12~17	OUT4~OUT9	Output channel 4~9 for LEDs.
19~24	OUT10~OUT15	Output channel 10~15 for LEDs.
26~28	OUT16~OUT18	Output channel 16~18 for LEDs.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3238-QFLS4-TR	QFN-28, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at SCL, SDA, SDB, OUT1 to OUT18	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	39.5°C/W
ESD (HBM) ESD (CDM)	±8kV ±750V

Note 6: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Typical values are T_A = 25°C, V_{CC} = 5V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{OUT}	Maximum output current	V_{CC}= 5V, V_{OUT}= 0.8V, R_{ISET}= 2kΩ, GCC= 0xFF, Scaling= 0xFF (Note 7)		78		mA
	Output current	V_{CC}= 5V, V_{OUT}= 0.4V, R_{ISET}= 6.8kΩ, GCC= 0xFF, Scaling= 0xFF		23		mA
ΔI_{MAT}	I_{OUT} mismatch in chip	R_{ISET}= 6.8kΩ, GCC= 0xFF, Scaling= 0xFF, I_{OUT}= 23mA	-8		8	%
ΔI_{OUT}	I_{OUT} mismatch between chip	R_{ISET}= 6.8kΩ, GCC= 0xFF, Scaling= 0xFF, I_{OUT}= 23mA	-8		8	%
V_{HR}	Headroom voltage	R_{ISET}= 6.8kΩ, GCC= 0xFF, Scaling= 0xFF, I_{OUT}= 23mA		0.2	0.35	V
I_{CC}	Quiescent power supply current	V_{CC}= 5V, R_{ISET}= 6.8kΩ, GCC= 0xFF, Scaling= 0xFF, I_{OUT}= 23mA, PWM= 0x00		5	10	mA
		V_{CC}= 3.6V, R_{ISET}= 6.8kΩ, GCC= 0xFF, Scaling= 0xFF, I_{OUT}= 23mA, PWM= 0x00		4	7	mA
I_{SD}	Shutdown current	V_{CC}= 5V, R_{ISET}= 6.8kΩ, V_{SDB}= 0V or software shutdown		2	3	μA
		V_{CC}= 3.6V, R_{ISET}= 6.8kΩ, V_{SDB}= 0V or software shutdown		1	2	μA
I_{OZ}	Output leakage current	V_{SDB}= 0V or software shutdown, V_{OUT}= 5.5V			0.1	μA
f_{OUT}	PWM frequency of output	OSC= 8MHz, PWM Resolution= 8bit		31.5		kHz
T_{SD}	Thermal shutdown	(Note 8)		165		°C
T_{SD_HY}	Hysteresis	(Note 8)		20		°C
Logic Electrical Characteristics (SDA, SCL, SDB, AD)						
V_{IL}	Logic "0" input voltage	V_{CC}= 2.7V~5.5V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC}= 2.7V~5.5V	1.4			V
I_{IL}	Logic "0" input current	V_{INPUT}= 0V (Note 8)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT}= V_{CC} (Note 8)		5		nA

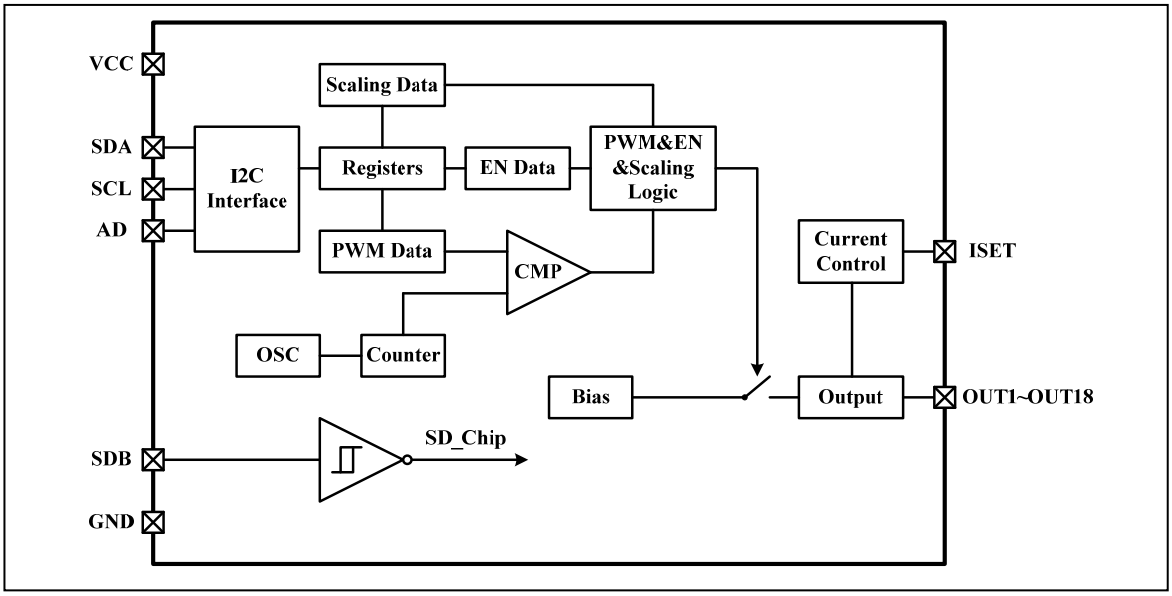
DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 8)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	µs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	µs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	µs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	µs
$t_{HD, DAT}$	Data hold time	-		-	-		-	µs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	µs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	µs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 7: The recommended minimum value of R_{ISET} is 2kΩ.

Note 8: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3238 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3238 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin. The complete slave address is:

Table 1 Slave Address

Bit	A7:A3	A2:A1	A0
Value	01101	AD	0/1

AD connected to GND, AD = 00;
AD connected to VCC, AD = 11;
AD connected to SCL, AD = 01;
AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3238.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3238's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3238 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3238, the register address byte is sent, most significant bit first. IS31FL3238 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3238 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3238, load the address of the data register that the first data byte is intended for. During the IS31FL3238 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3238 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3238 (Figure 6).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3238 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3238 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3238 to the master (Figure 7).

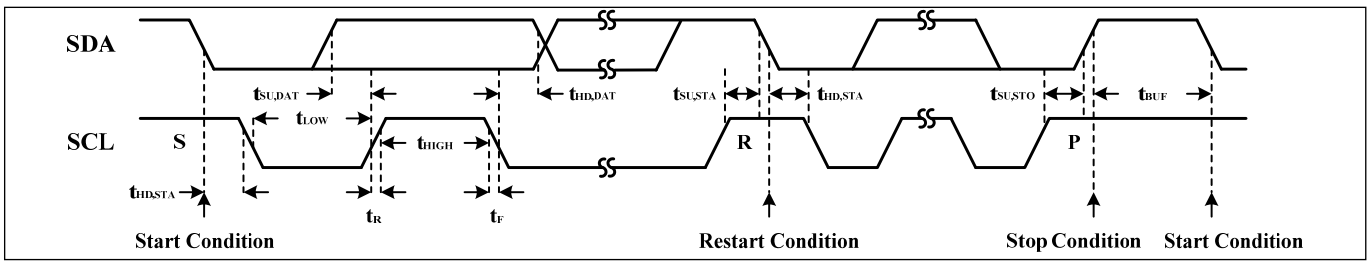


Figure 3 Interface Timing

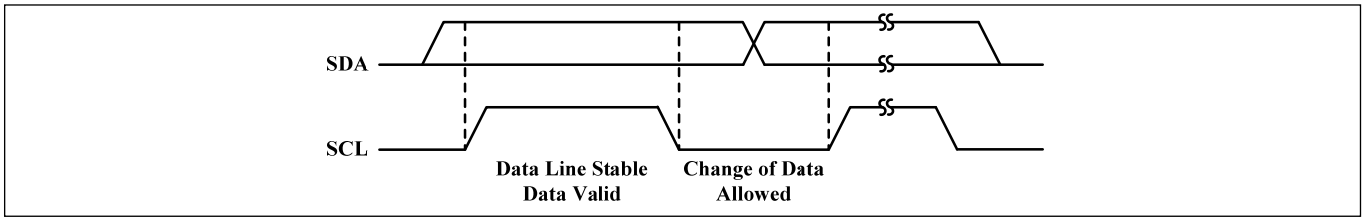


Figure 4 Bit Transfer

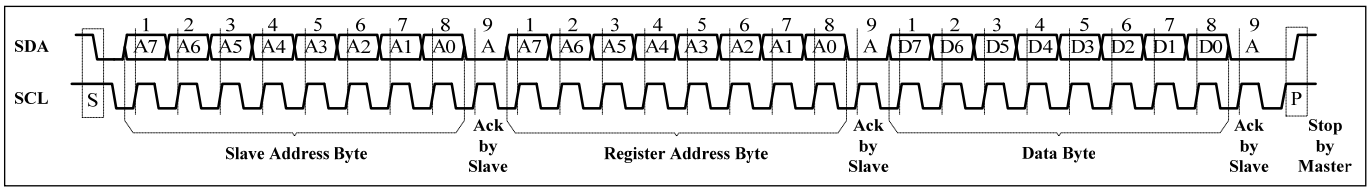


Figure 5 Writing to IS31FL3238 (Typical)

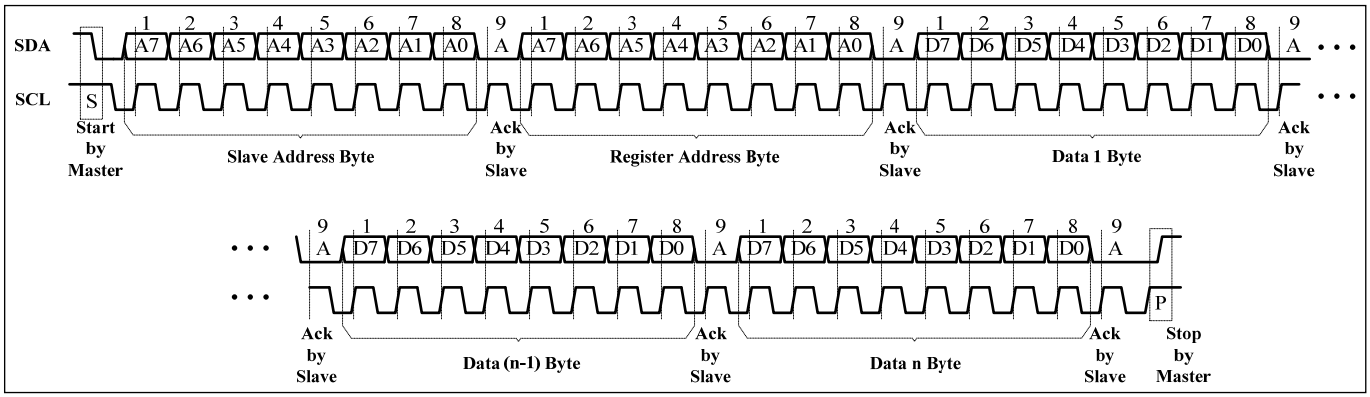


Figure 6 Writing to IS31FL3238 (Automatic Address Increment)

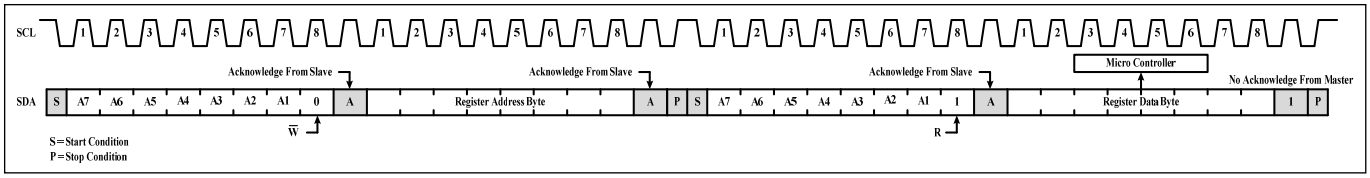


Figure 7 Reading from IS31FL3238

REGISTER DEFINITIONS

Table 2 Register Function

Address	Name	Function	R/W	Table	Default
00h	Control Register	Power control register	R/W	3	0000 0000
01h~48h	PWM Register	Channel [18:1] PWM register byte	R/W	5	
49h	Update Register	Update the PWM and scaling data	W	-	
4Ah~6Dh	LED Scaling Register	Control each channel's DC current	R/W	7	
6Eh	Global Current Control Register	Control global DC current/SSD	R/W	8	
70h	Phase Delay and Clock Phase Register	Phase delay and clock phase	R/W	9	
71h	Open Short Detect Enable Register	Open short detect enable	R/W	10	
72h~76h	LED Open/Short Register	Open short information	R/W	11	
77h	Temperature Sensor Register	Temperature information	R/W	12	
78h	Spread Spectrum Register	Spread spectrum control register	R/W	13	
7Fh	Reset Register	Reset all registers	W	-	

Table 3 00h Control Register

Bit	D7	D6:D4	D3	D2:D1	D0
Name	-	OSC	-	PMS	SSD
Default	0	000	0	00	0

The Control Register sets software shutdown mode, internal oscillator clock frequency and PWM resolution. The internal oscillator clock frequency and the PWM resolution will decide the output PWM frequency. Recommend using lower than 500Hz option or higher than 20kHz options to avoid the MLCC's audible noise as shown in Table 4.

SSD Software Shutdown Enable
0 Software shutdown mode
1 Normal operation

PMS PWM Resolution
00 8-bit
01 10-bit
10 12-bit
11 16-bit

OSC Oscillator Clock Frequency Selection
000 16MHz
001 8MHz
010 1MHz
011 500kHz
100 250kHz
101 125kHz
110 62kHz
111 31kHz

Table 4 PWM Frequency

PWM Resolution	16M	8M	1M	500k	250k	125k	62k	31k
8-bit	62k	32k	4k	2k	1k	0.5k	244	122
10-bit	16k	8k	1k	0.5k	244	122	NA	NA
12-bit	4k	2k	244	122	NA	NA	NA	NA
16-bit	244	122	NA	NA	NA	NA	NA	NA

Table 5 01h~48h PWM Register

Reg	02h (04h, 06h…)	01h (03h, 05h…)
Bit	D7:D0	D7:D0
Name	PWMx_H	PWMx_L
Default	0000 0000	0000 0000

x=A or B, Each output has 2 bytes × 2, total 4 registers to modulate the PWM duty in 256/1024/4096/65536 steps. For example, OUT1 use 04h/03h (PWMB), 02h/01 (PWMA) to modulate the PWM, OUT2 use 08h/07h (PWMB), 06h/05 (PWMA) to modulate the PWM, etc., If using the 8 bit PWM resolution, only the PWM_L needs to be set.

The value of the SL (LED Scaling Register) decides the peak current of each LED noted I_{OUT}.

I_{OUT} and the value of the PWM Registers decide the average current of each LED noted I_{LED}.

I_{OUT} computed by Formula (1):

$$I_{OUT} = I_{OUT\,(MAX)} \times \frac{GCC}{256} \times \frac{SLB + SLA}{512} \quad (1)$$

I_{LED} computed by Formula (2):

$$I_{LED} = \frac{PWMB + PWMA}{2N} \times I_{OUT} \quad (2)$$

$$PWMA = \sum_{n=0}^{15} D[n] \cdot 2^n \quad (3)$$

$$PWMB = \sum_{n=0}^{15} D[n] \cdot 2^n \quad (4)$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (check R_{ISET} section for more information), GCC is the global current setting(6Eh), and SLB, SLA are the scaling of each output (4Ah~6Dh), N=256/1024/4096/65536(8/10/12/16 bit PWM resolution)

For example: R_{ISET}=6.8kΩ, GCC=0xFF, SL=0xFF, PMS= "11" (16 bit PWM resolution), PWMA_H=0xFF, PWMA_L=0xFF, PWMB_H=0xFF, PWMB_L=0xFF,

$I_{OUT(MAX)}$ = 23mA

$$I_{OUT} = I_{OUT(MAX)} \times \frac{255}{256} \times \frac{255+255}{512} = 23mA \quad (1)$$

$$PWMA = \sum_{n=0}^{15} D[n] \cdot 2^n = 65535 \quad (3)$$

$$PWMB = \sum_{n=0}^{15} D[n] \cdot 2^n = 65535 \quad (3)$$

N= 65536

$$I_{LED} = \frac{65535 + 65535}{2 \times 65536} \times 23\text{mA} = 23mA \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (check R_{ISET} section for more information)

The I_{OUT} of each channel is setting by the SL bits of LED Scaling Register (4Ah~6Dh). Please refer to the detail information in Table 7.

If R_{ISET}=6.8kΩ, GCC=0xFF, SL=0xFF, PMS= "00" (8 bit PWM resolution, only use the PWM_L, the PWM_H will be ignored), PWMA_H=0x77, PWMA_L=0xAA, PWMB_H=0x77, PWMB_L=0xAA,

$I_{OUT(MAX)}$ = 23mA

$$I_{OUT} = I_{OUT(MAX)} \times \frac{255}{256} \times \frac{255+255}{256 \times 2} = 23mA \quad (1)$$

$$PWMA = \sum_{n=0}^{8} D[n] \cdot 2^n = 170 \quad (3)$$

$$PWMB = \sum_{n=0}^{8} D[n] \cdot 2^n = 170 \quad (4)$$

N=256

$$I_{LED} = \frac{170 + 170}{256 \times 2} \times 23\text{mA} \quad (2)$$

Table 6 PWM and Scaling Register Map

OUT	PWM		SL
	PWM_H	PWM_L	
1	02h	01h	4Ah
	04h	03h	4Bh
2	06h	05h	4Ch
	08h	07h	4Dh
3	0Ah	09h	4Eh
	0Ch	0Bh	4Fh
4	0Eh	0Dh	50h
	10h	0Fh	51h
5	12h	11h	52h
	14h	13h	53h
6	16h	15h	54h
	18h	17h	55h
7	1Ah	19h	56h
	1Ch	1Bh	57h
8	1Eh	1Dh	58h
	20h	1Fh	59h
9	22h	21h	5Ah
	24h	23h	5Bh
10	26h	25h	5Ch
	28h	27h	5Dh
11	2Ah	29h	5Eh
	2Ch	2Bh	5Fh
12	2Eh	2Dh	60h
	30h	2Fh	61h
13	32h	31h	62h
	34h	33h	63h
14	36h	35h	64h
	38h	37h	65h
15	3Ah	39h	66h
	3Ch	3Bh	67h
16	3Eh	3Dh	68h
	40h	3Fh	69h
17	42h	41h	6Ah
	44h	43h	6Bh
18	46h	45h	6Ch
	48h	47h	6Dh

49h Update Register

When SDB= "H" and SSD= "1", a write of "0000 0000" to 49h is to update the PWM Registers (01h~48h) values.

Table 7 4Ah~6Dh LED Scaling Register

Bit	D7:D0
Name	SLx
Default	0000 0000

x=A or B, each output has 8 bits × 2 to modulate DC current in 256 steps, for example, OUT1 use 4Bh and 4Ah to set the DC output current, OUT2 use 4Dh and 4Ch to set the DC output current, etc.

The value of the SLB+SLA Registers decides the DC peak current of each LED noted I_{OUT}.

I_{OUT} computed by Formula (1):

$$I_{OUT} = I_{OUT\,(MAX)} \times \frac{GCC}{256} \times \frac{SLA + SLB}{256 \times 2} \qquad (1)$$

$$SLA = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (5)$$

$$SLB = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (5)$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET}, GCC is the global current setting(6Eh)

4Ah~6Dh don't need to update by 49h, each register will be updated immediately when it is written.

Table 8 6Eh Global Current Control Register

Bit	D7:D0
Name	GCC
Default	0000 0000

GCC and SL control the I_{OUT} as shown in Formula (1).

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (5)$$

If GCC=0xFF, SLA=0xFF, SLB=0xFF, I_{OUT}=$I_{OUT(MAX)}$

If GCC=0x01, SLA=0xFF, SLB=0x00,

$$I_{OUT} = I_{OUT\,(MAX)} \times \frac{1}{256} \times \frac{255 + 0}{256 \times 2}$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (check R_{ISET} section for more information).

Table 9 70h Phase Delay and Clock Phase Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PDE	-	PS	PS	PS	PS	PS	PS
Default	0	0	0	0	0	0	0	0

IS31FL3238 features the 6 phase delay function, when this bit enable, the phase delay function enable and otherwise it will be disabled

PDE	Phase Delay Enable
0	Phase delay disable
1	Phase delay enable

PS	Phase Select
0	Phase delay 0 Degree
1	Phase delay 180 Degree

Table 10 71h Open Short Detect Enable Register

Bit	D7:D2	D1:D0
Name	-	OSDE
Default	0000 00	00

OSDE enable the detect once and the result will store in 72h~76h, notice that the 72h~76h only store open or short information at the same time

OSDE	Open Detect Enable
00	Detect disable
01	Detect disable
10	Short detect enable
11	Open detect enable

Table 11-1 72h~75h LED Open/Short Register

72h	D7:D0
Name	OP/ST[8:1]
Default	x0x0 x0x0

Table 11-2 76h LED Open/Short Register

Bit	D7:D4	D3:D0
Name	-	OP/ST[18:17]
Default	0000	x0x0

Open or short status are stored in 72h to 76h.

OP[18:1]	Open Information of OUT18:OUT1
0	No open happens
1	The output opens

ST[18:1]	Short Information of OUT18:OUT1
0	No short happens
1	The output shorts

Table 12 77h Temperature Sensor Register

Bit	D7:D6	D5	D4	D3:D2	D1:D0
Name	TROF	-	T_Flag	-	TS
Default	00	0	0	00	00

TS stores the temperature/thermal roll-off point. TROF stores percentage of output current of the thermal rool-off function.

Read T_Flag=1 indicates die temperature exceeds the setting point (TS). Before each reading of 77h register, TROF and TS need to be re-written.

TROF	Thermal roll off percentage of output current
00	100%
01	75%
10	55%
11	30%

TS	Temperature Point, Thermal roll off start point
00	140°C
01	120°C
10	100°C
11	90°C

T_Flag	Temperature Flag
0	Temperature point not exceeded
1	Temperature point exceeded

Table 13 78h Spread Spectrum Register

Bit	D7:D5	D4	D3:D2	D1:D0
Name	DCPWM	SSP	RNG	CLT
Default	000	0	00	00

When DCPWM is set to “0”, the outputs PWM is decided by 01h~48h, and the PWM range is 0/256~255/256, still the 1/256 can’t be turned on. When the DCPWM is set to “1”, no matter what the values in 01h~48h register are, the output will be turned on 256/256, the output will open totally.

Spread spectrum register enable the spread spectrum function, adjust the cycle time and range.

DCPWM	Setting the output to work in DC mode
xx1	Channel1~6 PWM data set by register 01h~18h
xx0	Channel1~6 PWM data set to DC high
x1x	Channel7~12 PWM data set by register 19h~30h
x0x	Channel7~12 PWM data set to DC high
1xx	Channel13~18 PWM data set by register 31h~48h
0xx	Channel13~18 PWM data set to DC high

SSP	Spread Spectrum Enable
0	Disable
1	Enable

CLT	Spread Spectrum Cycle Time
00	1980μs
01	1200μs
10	820μs
11	660μs

RNG	Spread Spectrum Range
00	±5%
01	±15%
10	±24%
11	±34%

7Fh Reset Register

A write of “0000 0000” to 7Fh is to reset all registers to their default values.

APPLICATION INFORMATION

R_{ISET}

The maximum output current $I_{OUT(MAX)}$ of OUT1~OUT18 can be adjusted by the external resistor, R_{ISET}, as described in Formula (6).

$$I_{OUT\ (MAX\ )} = 2x \cdot \frac{V_{ISET}\left(R_{ISET}\left(k\Omega\right)+ 283\right)}{R_{ISET}\left(k\Omega\right)\cdot 283} \quad (6)$$

x = 81.28, V_{OUT} = 0.8V, V_{ISET} = 0.945V.

The recommended minimum value of R_{ISET} is 2kΩ.

When R_{ISET}=6.8kΩ, $I_{OUT(MAX)}$=23mA

When R_{ISET}=3.3kΩ, $I_{OUT(MAX)}$=47mA

When R_{ISET}=2kΩ, $I_{OUT(MAX)}$=78mA

CURRENT SETTING

The maximum output current is set by the external register R_{ISET}. The current of each output can also be set independently by the SLA or SLB 8 bits of LED Scaling Register (4Ah~6Dh).

Some applications the IOUT of each channel need to adjust independently.

For example, if OUT1 drive 1 LED and OUT2 drive 2 LED, the total 3 LED want to have same average current like 18mA, we can set the $I_{OUT(MAX)}$ to 36mA, and GCC=0xFF, 4Ah=0x80, 4Bh=0x80, 4Ch=0xFF, 4Dh=0xFF, the OUT1 sinks about 18mA and OUT2 sinks 36mA which can have two LEDs in parallel.

For another example, OUT1, OUT2 and OUT3 drive a RGB LED, OUT1 is Red LED, OUT2 is green LED and OUT 3 is blue LED, with same R_{ISET}, GCC and same SL bits, when OUT1 OUT2 and OUT3 have the same PWM value, the LED may looks a litter pink, or not so white, in this case, the SLx bits can be used to adjust the single IOUTx of some output and make it pure white color. We call this SL bits another name: white balance registers.

PWM CONTROL

The PWM Registers (01h~48h) can modulate LED brightness of 18 channels with 256/1024/4096/65536 steps. For example, if the data in PWM_H Register is “0000 0000” and in PWM_L Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

PWM FREQUENCY SELECT

The IS31FL3238 output channels operate with a default 8 bit PWM resolution and the PWM frequency of 62kHz (the oscillator frequency is 16MHz). Because all the OUTx channels are synchronized, the DC power supply will experience large instantaneous current surges when the OUTx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors. When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 300Hz to 18kHz, To avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3238’s output PWM frequency above/below the audible range. The Control Register (00h) can be used to set the switching frequency to 122Hz~62kHz as shown in Table 4, some combine setting of the OSC and PMS bits will get different output PWM frequency, and higher than 20kHz or lower than 300Hz is out of the audible range.

OPEN/SHORT DETECT FUNCTION

IS31FL3238 has open and short detect bit for each LED.

By setting the OSDE bit of Open Short Detect Enable Register (71h) from “00” to “10” (store short information) or “11” (store open information), the LED Open/Short Register will store the open/short information immediately the MCU can get the open/short information by reading the 72h~76h.

The Global Current Control Register (6Eh) needs to set to 0x01 in order to get the right open/short data.

SPREAD SPECTRUM FUNCTION

A switch mode controller can be particularly troublesome for application when the EMI is concerned. To optimize the EMI performance, the IS31FL3238 includes a spread spectrum function. By setting the RNG bit of Spread Spectrum Register (78h), Spread Spectrum range can be choose from ±5% /±15% /±24% /±34%. The spread spectrum can spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of EMI. With the spread spectrum, the EMI test can be easy to be passed with smaller size and lower cost filter circuit.

OPERATING MODE

PWM Mode

IS31FL3238 can only operate in PWM Mode. The brightness of each LED can be modulated with 256/1024/4096/65536 steps by PWM registers. For example, if the data in PWMA and PWMB Register are “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Control Register (00h) to “0”, the IS31FL3238 will operate in software shutdown mode. When the IS31FL3238 is in software shutdown, all current sources are switched off, so that the LEDs are blanked. All registers can be operated.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown.

The chip releases hardware shutdown when the SDB pin is pulled high. When set SDB high, the rising edge will reset the I2C module, but the register information retains. During hardware shutdown state Function Register can be operated.

If VCC has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

As described in external resistor (R_{ISET}), the chip consumes lots of power. Please consider below factors when layout the PCB.

1. The VCC capacitors need to close to the chip and the ground side should well connect to the GND of the chip.

2. R_{ISET} should be close to the chip and the ground side should well connect to the GND of the chip.

3. The thermal pad should connect to ground pins and the PCB should have the thermal pad too, usually this pad should have 16 or 25 via thru the PCB to other side’s ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of each package.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

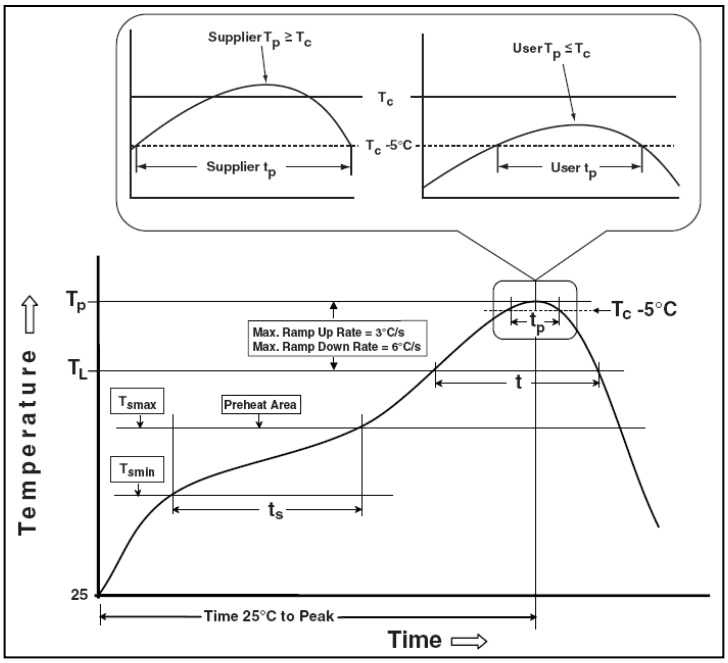
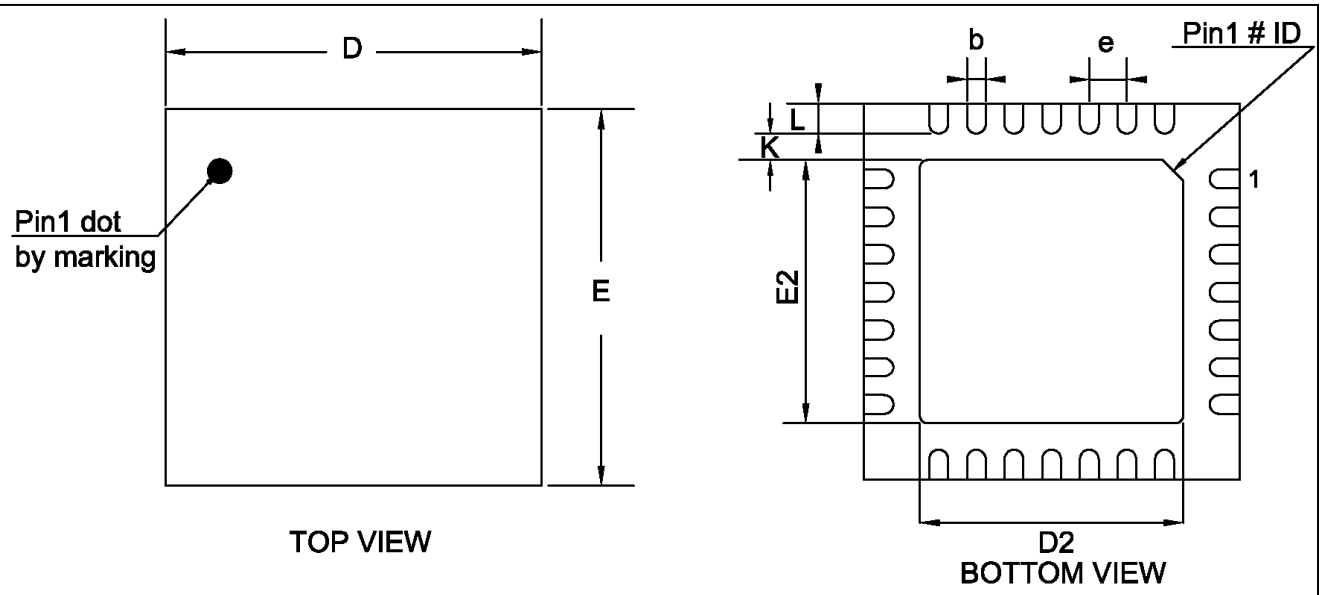


Figure 8 Classification Profile

PACKAGE INFORMATION

QFN-28



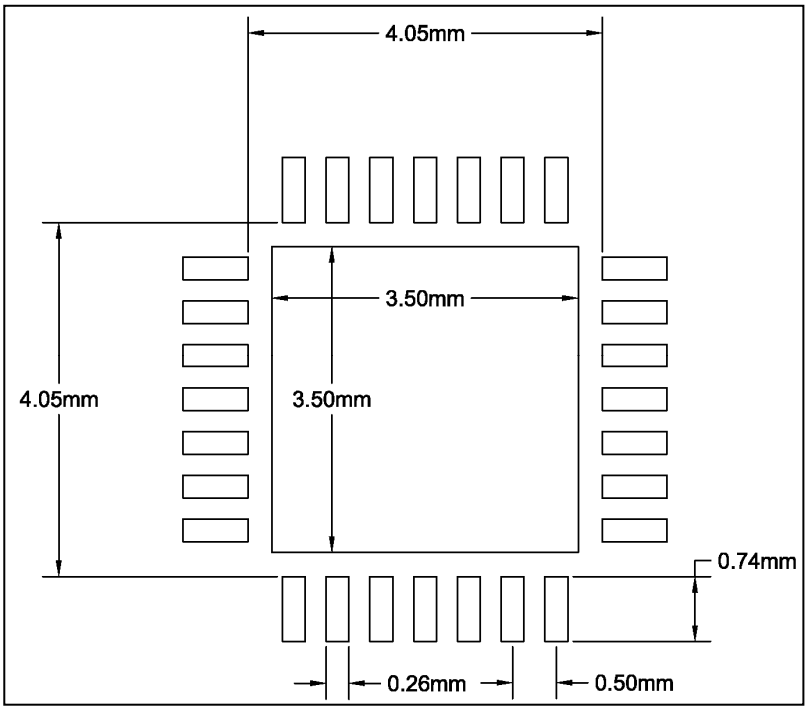
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.18	0.20	0.25
K	0.20	-	-
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
e	0.50BSC		

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

QFN-28



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release.	2018.04.02
0B	Update WFQFN to QFN package and remove eTSSOP package.	2018.12.06
0C	1. Update Table 4 and correct mistakes. 2. Update ISSI logo 3. Update Equation (6)	2019.02.14
A	1. Add pin no in typical circuit 2. Update EC test condition: VCC to 5V 3. Add Table 6	2019.06.24