74HC258

Quad 2-input multiplexer; 3-state; inverting

Rev. 04 — 14 April 2008 Product data sheet

1. General description

The 74HC258 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HC258 is specified in compliance with JEDEC standard no. 7A.

The 74HC258 has four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and is controlled by a common data select input (S).

The data inputs from source 0 (1I0 to 4I0) are selected when input S is LOW and the data inputs from source 1 (1I1 to 4I1) are selected when S is HIGH.

Data appears at the outputs ($1\overline{Y}$ to $4\overline{Y}$) in inverted form from the select inputs.

The 74HC258 is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S. The outputs are forced to a high-impedance OFF-state when $\overline{OE}$ is HIGH.

The logic equations for the outputs are:

$$1\overline{Y} = \overline{\overline{OE} \times (1I1 \times S + 1I0 \times \overline{S})}$$

$$2\overline{Y} = \overline{\overline{OE} \times (2I1 \times S + 2I0 \times \overline{S})}$$

$$3\overline{Y} = \overline{\overline{OE} \times (3I1 \times S + 3I0 \times \overline{S})}$$

$$4\overline{Y} = \overline{\overline{OE} \times (4I1 \times S + 4I0 \times \overline{S})}$$

The 74HC258 is identical to the 74HC257 but has inverting outputs.

2. Features

- 3-state outputs interface directly with system bus
- Low-power dissipation
- Inverting data path
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC258N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC258D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC258DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1

4. Functional diagram

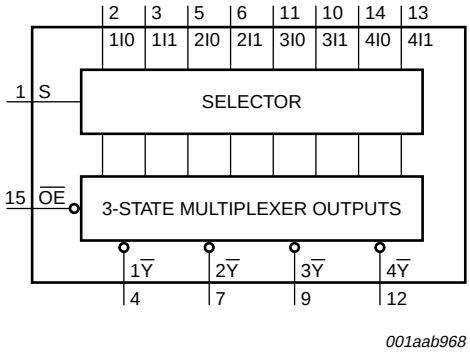


Fig 1. Functional diagram

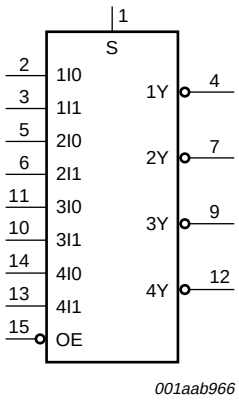


Fig 2. Logic symbol

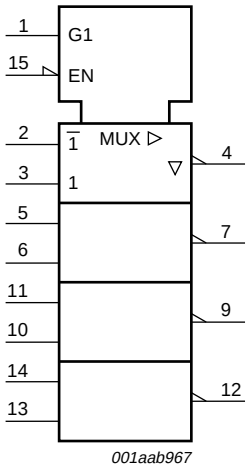


Fig 3. IEC logic symbol

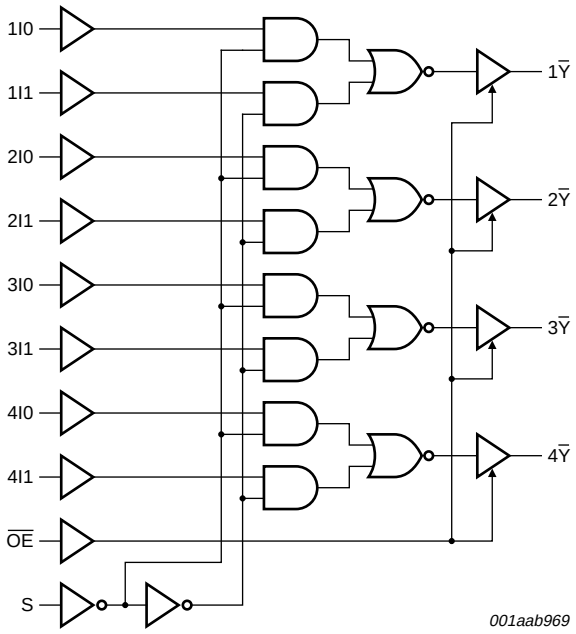


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

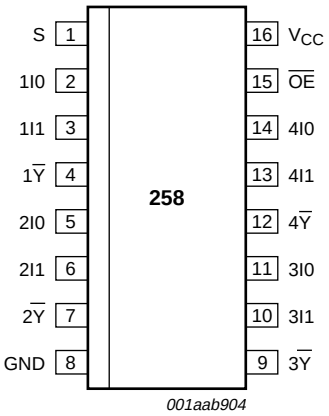


Fig 5. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	common data select input
1I0	2	data input 1 from source 0
1I1	3	data input 1 from source 1
$1\overline{Y}$	4	3-state multiplexer output 1; inverted
2I0	5	data input 2 from source 0
2I1	6	data input 2 from source 1
$2\overline{Y}$	7	3-state multiplexer output 2; inverted
GND	8	ground (0 V)
$3\overline{Y}$	9	3-state multiplexer output 3; inverted
3I1	10	data input 3 from source 1
3I0	11	data input 3 from source 0
$4\overline{Y}$	12	3-state multiplexer output 4; inverted
4I1	13	data input 4 from source 1
4I0	14	data input 4 from source 0
$\overline{OE}$	15	output enable input (active LOW)
V_{CC}	16	positive supply voltage

6. Functional description

Table 3. Function table[1]

Control		Input		Output
$\overline{OE}$	S	nI0	nI1	n$\overline{Y}$
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V		-	±35	mA
I_{CC}	supply current			-	70	mA
I_{GND}	ground current			–70	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C				
		DIP16 package	[2]	-	750	mW
		SO16 package	[3]	-	500	mW
		SSOP16 package	[4]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	ns
		V_{CC} = 4.5 V	-	1.67	139	ns
		V_{CC} = 6.0 V	-	-	83	ns

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –6 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_{CC} = 6.0 V; V_O = V_{CC} or GND; I_O = 0 A	-	-	±0.5	-	±5.0	-	±10	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit see Figure 8.

Symbol	Parameter	Conditions		25 °C			−40 °C to +125 °C		Unit
				Min	Typ	Max	Max (85 °C)	Max (125 °C)	
t_{pd}	propagation delay	nI0, nI1to n$\overline{Y}$; see Figure 6	[1]						
		V_{CC} = 2.0 V		-	30	95	120	145	ns
		V_{CC} = 4.5 V		-	11	19	24	29	ns
		V_{CC} = 6.0 V		-	9	16	20	25	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	9	-	-	-	ns
		S to n$\overline{Y}$; see Figure 6							
		V_{CC} = 2.0 V		-	47	140	175	210	ns
		V_{CC} = 4.5 V		-	17	28	35	42	ns
		V_{CC} = 6.0 V		-	14	24	30	36	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	14	-	-	-	ns
t_{en}	enable time	$\overline{OE}$ to n$\overline{Y}$; see Figure 7	[2]						
		V_{CC} = 2.0 V		-	39	140	175	210	ns
		V_{CC} = 4.5 V		-	14	28	35	42	ns
		V_{CC} = 6.0 V		-	11	24	30	36	ns
t_{dis}	disable time	$\overline{OE}$ to n$\overline{Y}$; see Figure 7	[3]						
		V_{CC} = 2.0 V		-	55	150	190	225	ns
		V_{CC} = 4.5 V		-	20	30	38	45	ns
		V_{CC} = 6.0 V		-	16	26	33	38	ns
t_t	transition time	see Figure 6	[4]						
		V_{CC} = 2.0 V		-	14	60	75	90	ns
		V_{CC} = 4.5 V		-	5	12	15	18	ns
		V_{CC} = 6.0 V		-	4	10	13	15	ns
C_{PD}	power dissipation capacitance	per multiplexer; V_I = GND to V_{CC}	[5]	-	55	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

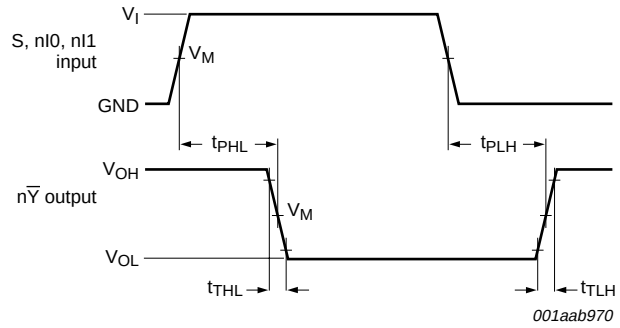
[2] t_{en} is the same as t_{PZH} and t_{PZL}.

[3] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[4] t_t is the same as t_{THL} and t_{TLH}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

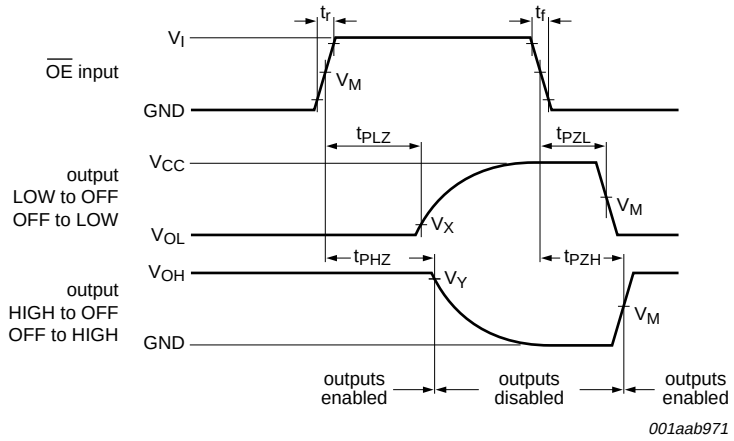
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. Input (nI0, nI1 and S) to output (nȲ) propagation delays and output transition times



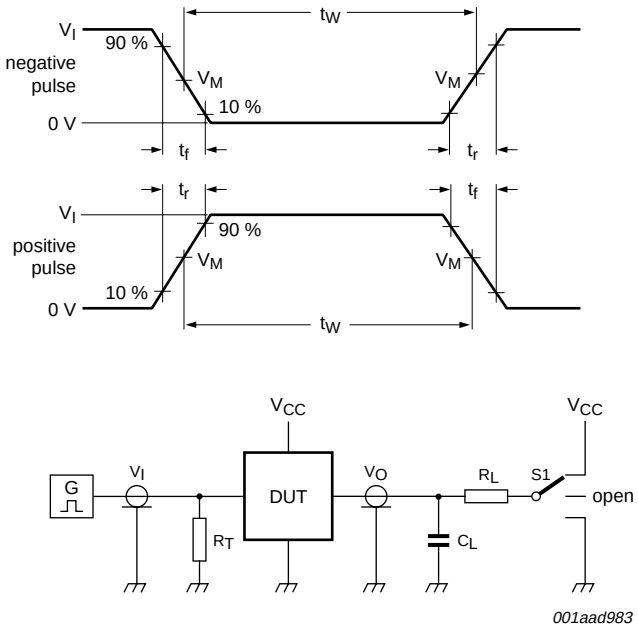
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. Enable and disable times

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

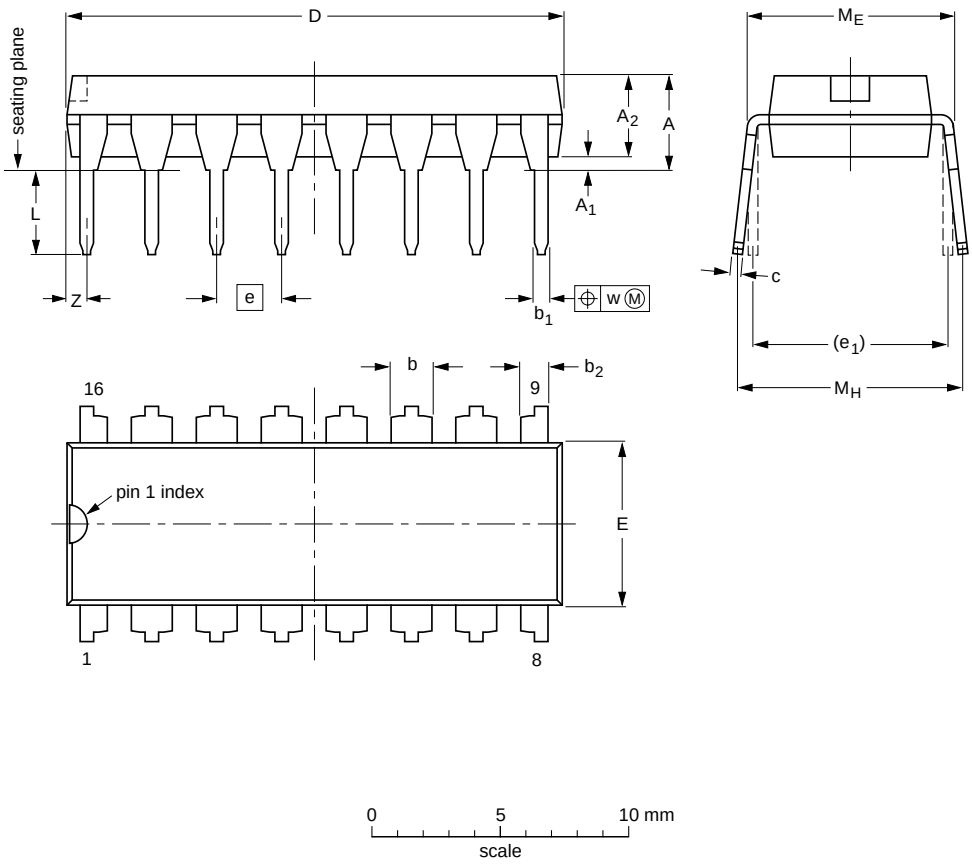
Fig 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		S1		
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PZL}, t_{PLZ}	t_{PZH}, t_{PHZ}	t_{PHL}, t_{PLH}
2.0 V	V_{CC}	6 ns	50 pF	1 kΩ	V_{CC}	GND	open
4.5 V	V_{CC}	6 ns	50 pF	1 kΩ	V_{CC}	GND	open
6.0 V	V_{CC}	6 ns	50 pF	1 kΩ	V_{CC}	GND	open
5.0 V	V_{CC}	6 ns	15 pF	1 kΩ	V_{CC}	GND	open

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

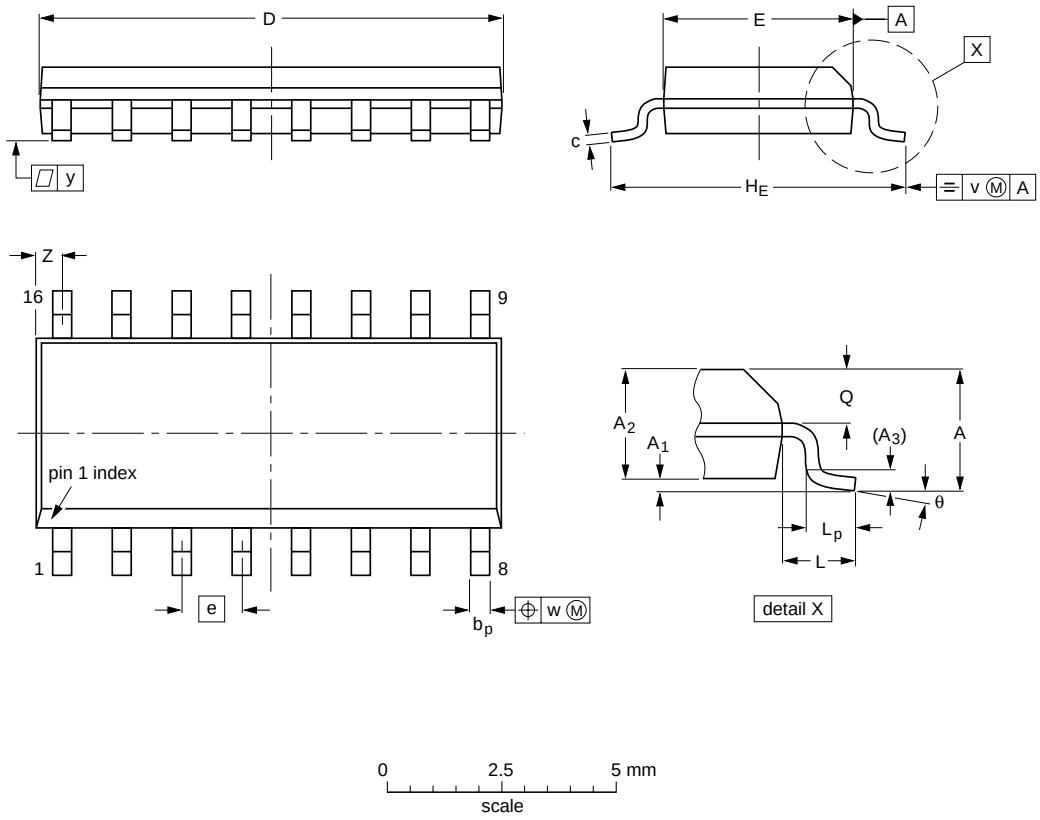
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 9. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

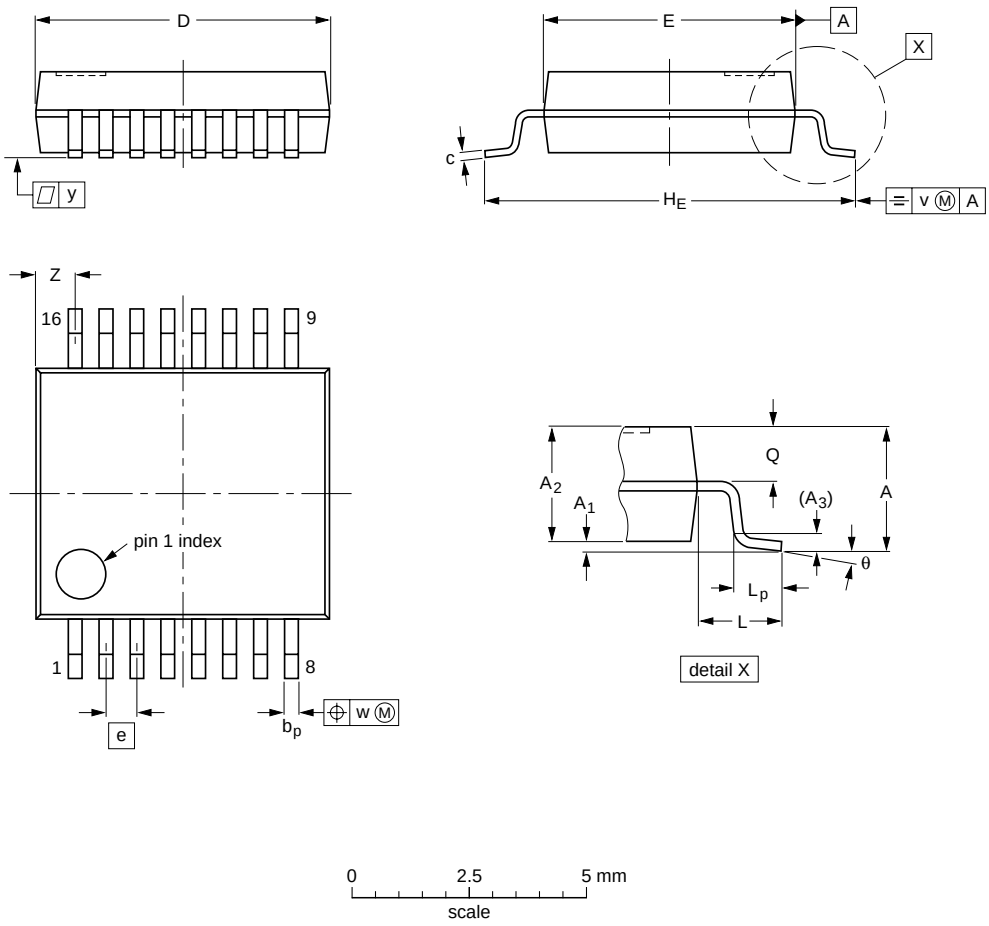
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT338-1 (SSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC258_4	20080414	Product data sheet	-	74HC258_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Pin assignment corrected for pins 10, 11, 13 and 14 in Figure 1, Figure 2, Figure 5 and Table 2.			
74HC258_3	20041112	Product data sheet	-	74HC_HCT258_CNV_2
74HC_HCT258_CNV_2	19990902	Product specification	-	74HC_HCT258_1
74HC_HCT258_1	19901201	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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