

# TLV2241, TLV2242, TLV2244 FAMILY OF 1- $\mu$ A/Ch RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS

SLOS329C – JULY 2000 REVISED - NOVEMBER 2000

- Micropower Operation . . . 1  $\mu$ A/Channel
- Rail-to-Rail Input/Output
- Gain Bandwidth Product . . . 5.5 kHz
- Supply Voltage Range . . . 2.5 V to 12 V
- Specified Temperature Range
  - $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  . . . Commercial Grade
  - $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  . . . Industrial Grade
- Ultrasmall Packaging
  - 5-Pin SOT-23 (TLV2241)
  - 8-Pin MSOP (TLV2242)
- Universal OpAmp EVM

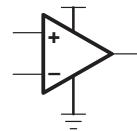
## description

The TLV224x family of single-supply operational amplifiers offers very low supply current of only 1  $\mu$ A per channel.

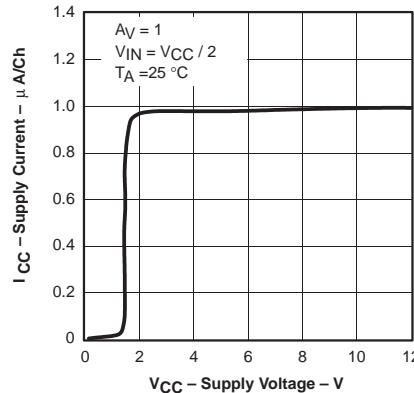
The low supply current is coupled with extremely low input bias currents enabling them to be used with mega- $\Omega$  resistors making them ideal for portable, long active life, applications. DC accuracy is ensured with a low typical offset voltage as low as 600  $\mu$ V, CMRR of 100 dB, and minimum open loop gain of 100 V/mV at 2.7 V.

The maximum recommended supply voltage is as high as 12 V and ensured operation down to 2.5 V, with electrical characteristics specified at 2.7 V, 5 V and 12 V. The 2.5-V operation makes it compatible with Li-Ion battery-powered systems and many micropower microcontrollers available today including TI's MSP430.

## Operational Amplifier



## SUPPLY CURRENT vs SUPPLY VOLTAGE



## FAMILY PACKAGE TABLE

DEVICE	NO. OF Ch	PACKAGE TYPES					UNIVERSAL EVM
		PDIP	SOIC	SOT-23	TSSOP	MSOP	
TLV2241	1	8	8	5	—	—	
TLV2242	2	8	8	—	—	8	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV2244	4	14	14	—	14	—	

## SELECTION OF SINGLE SUPPLY OPERATIONAL AMPLIFIER PRODUCTS†

DEVICE	V <sub>DD</sub> (V)	V <sub>IO</sub> (mV)	BW (MHz)	SLEW RATE (V/ $\mu$ s)	I <sub>DD</sub> (PER CHANNEL) ( $\mu$ A)	RAIL-TO-RAIL
TLV240x‡	2.5–16	0.390	0.005	0.002	0.880	I/O
TLV224x	2.5–12	0.600	0.005	0.002	1	I/O
TLV2211	2.7–10	0.450	0.065	0.025	13	O
TLV245x	2.7–6	0.020	0.22	0.110	23	I/O
TLV225x	2.7–8	0.200	0.2	0.12	35	O

† All specifications are typical values measured at 5 V.

‡ This device also offers 18-V reverse battery protection and 5-V over-the-rail operation on the inputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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## TLV2241 AVAILABLE OPTIONS

TA	$V_{IO}^{\max}$ AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE <sup>†</sup> (D)	SOT-23 <sup>‡</sup> (DBV)	SYMBOLS	PLASTIC DIP (P)
0°C to 70°C	3000 $\mu$ V	TLV2241CD	—	—	—
–40°C to 125°C		TLV2241ID	TLV2241IDBV	VBEI	TLV2241IP

<sup>†</sup>This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2241CDR).

<sup>‡</sup>This package is available in a 250 piece mini-reel. To order this package, add a T suffix to the part number (e.g., TLV2241DBVT). This package is also available in a 3000 piece reel, add a R suffix to the part number (e.g., TLV2241DBVR).

## TLV2242 AVAILABLE OPTIONS

TA	$V_{IO}^{\max}$ AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE <sup>†</sup> (D)	MSOP <sup>†</sup> (DGK)	SYMBOLS	PLASTIC DIP (P)
0°C to 70°C	3000 $\mu$ V	TLV2242CD	—	—	—
–40°C to 125°C		TLV2242ID	TLV2242IDGK	xxTIALE	TLV2242IP

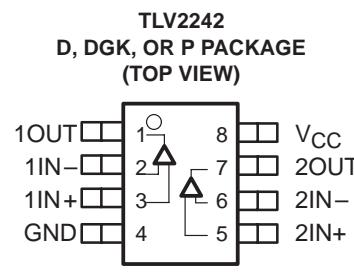
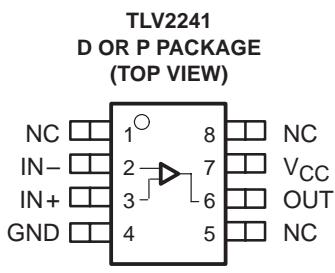
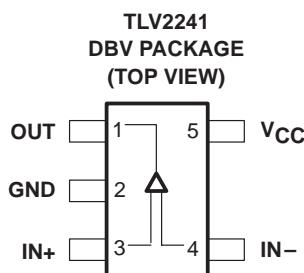
<sup>†</sup>This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2242CDR).

## TLV2244 AVAILABLE OPTIONS

TA	$V_{IO}^{\max}$ AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE <sup>†</sup> (D)	PLASTIC DIP (N)	TSSOP (PW)
0°C to 70°C	3000 $\mu$ V	TLV2244CD	—	—
–40°C to 125°C		TLV2244ID	TLV2244IN	TLV2244IPW

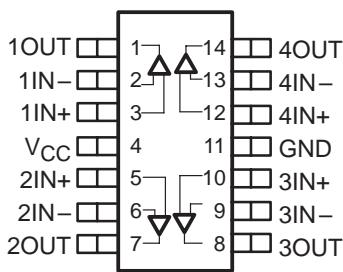
<sup>†</sup>This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2244CDR).

## TLV224x PACKAGE PINOUTS



NC – No internal connection

**TLV2244  
D, N, OR PW PACKAGE  
(TOP VIEW)**



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND.

## DISSIPATION RATING TABLE

PACKAGE	$\Theta_{JC}$ (°C/W)	$\Theta_{JA}$ (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.6	1022 mW	204.4 mW
DBV (5)	55	324.1	385 mW	77.1 mW
DGK (8)	54.2	259.9	481 mW	96.2 mW
N (14)	32	78	1600 mW	320.5 mW
P (8)	41	104	1200 mW	240.4 mW
PW (14)	29.3	173.6	720 mW	144 mW

### **recommended operating conditions**

		MIN	MAX	UNIT
Supply voltage, $V_{CC}$	Single supply	2.5	12	V
	Split supply	$\pm 1.25$	$\pm 6$	
Common-mode input voltage range, $V_{ICR}$		0	$V_{CC}$	V
Operating free-air temperature, $T_A$	C-suffix	0	70	°C
	I-suffix	-40	125	

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**electrical characteristics at recommended operating conditions,  $V_{CC} = 2.7, 5$  V, and 12 V (unless otherwise noted)†**

**dc performance**

PARAMETER	TEST CONDITIONS	$T_A$ †	MIN	TYP	MAX	UNIT
$V_{IO}$ Input offset voltage	$V_O = V_{CC}/2$ V, $V_{IC} = V_{CC}/2$ V, $R_S = 50$ $\Omega$	25°C	600	3000		$\mu$ V
$\alpha V_{IO}$ Offset voltage drift		Full range		4500		
		25°C		3		$\mu$ V/°C
CMRR Common-mode rejection ratio	$V_{IC} = 0$ to $V_{CC}$ , $R_S = 50$ $\Omega$	$V_{CC} = 2.7$ V	25°C	55	100	dB
			Full range	50		
		$V_{CC} = 5$ V	25°C	60	100	
			Full range	53		
		$V_{CC} = 12$ V	25°C	60	100	
			Full range	55		
AVD Large-signal differential voltage amplification	$V_{CC} = 2.7$ V, $V_O(pp) = 1$ V, $R_L = 500$ k $\Omega$ $V_{CC} = 5$ V, $V_O(pp) = 3$ V, $R_L = 500$ k $\Omega$ $V_{CC} = 12$ V, $V_O(pp) = 6$ V, $R_L = 500$ k $\Omega$	$V_{CC} = 2.7$ V	25°C	100	400	V/mV
			Full range	30		
		$V_{CC} = 5$ V	25°C	250	1000	
			Full range	100		
		$V_{CC} = 12$ V	25°C	700	1500	
			Full range	120		

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

**input characteristics**

PARAMETER	TEST CONDITIONS	$T_A$ †	MIN	TYP	MAX	UNIT
$I_{IO}$ Input offset current	$V_O = V_{CC}/2$ V, $V_{IC} = V_{CC}/2$ V, $R_S = 50$ $\Omega$	25°C	25	250		pA
		TLV224xC		300		
		TLV224xI		400		
$I_{IB}$ Input bias current	$V_O = V_{CC}/2$ V, $V_{IC} = V_{CC}/2$ V, $R_S = 50$ $\Omega$	25°C	100	500		pA
		TLV224xC		550		
		TLV224xI		1000		
$r_{i(d)}$ Differential input resistance		25°C		300		M $\Omega$
$C_{i(c)}$ Common-mode input capacitance	$f = 100$ kHz	25°C		3		pF

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

‡ Specifications at 5 V are ensured by design and device testing at 2.7 V and 12 V.

**TLV2241, TLV2242, TLV2244**  
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**electrical characteristics at recommended operating conditions,  $V_{CC} = 2.7, 5$  V, and 12 V (unless otherwise noted)† (continued)**

**output characteristics**

PARAMETER	TEST CONDITIONS	$T_A$ †	MIN	TYP	MAX	UNIT
$V_{OH}$ High-level output voltage	$V_{IC} = V_{CC}/2$ , $I_{OH} = -2 \mu A$	25°C	2.65	2.68		V
		Full range	2.63			
		25°C	4.95	4.98		
		Full range	4.93			
		25°C	11.95	11.98		
		Full range	11.93			
	$V_{IC} = V_{CC}/2$ , $I_{OH} = -50 \mu A$	25°C	2.62	2.65		
		Full range	2.6			
		25°C	4.92	4.95		
		Full range	4.9			
		25°C	11.92	11.95		
		Full range	11.9			
$V_{OL}$ Low-level output voltage	$V_{IC} = V_{CC}/2$ , $I_{OL} = 2 \mu A$	25°C	90	150		mV
		Full range		180		
	$V_{IC} = V_{CC}/2$ , $I_{OL} = 50 \mu A$	25°C	180	230		
		Full range		260		
$I_O$ Output current	$V_O = 0.5$ V from rail	25°C		±200		$\mu A$

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

**power supply**

PARAMETER	TEST CONDITIONS	$T_A$ †	MIN	TYP	MAX	UNIT
$I_{CC}$ Supply current (per channel)	$V_O = V_{CC}/2$	25°C	980	1200		nA
		Full range		1500		
	$V_{CC} = 12$ V	25°C	1000	1250		
		Full range		1550		
PSRR Power supply rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )	$V_{CC} = 2.7$ to 5 V, $V_{IC} = V_{CC}/2$ V, No load,	25°C	70	100		dB
		TLV224xC		65		
		TLV224xI		60		
	$V_{CC} = 5$ to 12 V, $V_{IC} = V_{CC}/2$ V, No load	25°C	70	100		dB
		Full range		70		

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

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**electrical characteristics at recommended operating conditions,  $V_{CC} = 2.7, 5$  V, and 12 V (unless otherwise noted)<sup>‡</sup> (continued)**

**dynamic performance**

PARAMETER	TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
UGBW Unity gain bandwidth	$R_L = 500$ k $\Omega$ , $C_L = 100$ pF	25°C	5.5			kHz
SR Slew rate at unity gain	$V_{O(pp)} = 0.8$ V, $R_L = 500$ k $\Omega$ , $C_L = 100$ pF	25°C	2			V/ms
$\phi M$ Phase margin	$R_L = 500$ k $\Omega$ , $C_L = 100$ pF	25°C	60			
Gain margin			15			dB
$t_s$ Settling time	$V_{CC} = 2.7$ or 5 V, $V_{(STEP)PP} = 1$ V, $C_L = 100$ pF, $A_V = -1$ , $R_L = 100$ k $\Omega$	0.1%		1.84		ms
	$V_{CC} = 12$ V, $V_{(STEP)PP} = 1$ V, $C_L = 100$ pF, $A_V = -1$ , $R_L = 100$ k $\Omega$	0.1%		6.1		
		0.01%		32		

**noise/distortion performance**

PARAMETER	TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
$V_n$ Equivalent input noise voltage	$f = 10$ Hz	25°C	800			nV/ $\sqrt{\text{Hz}}$
	$f = 100$ Hz		500			
$I_n$ Equivalent input noise current	$f = 100$ Hz		8			fA/ $\sqrt{\text{Hz}}$

<sup>‡</sup> Specifications at 5 V are ensured by design and device testing at 2.7 V and 12 V.

## TYPICAL CHARACTERISTICS

**Table of Graphs**

			<b>FIGURE</b>
$V_{IO}$	Input offset voltage	vs Common-mode input voltage	1, 2, 3
$I_{IB}$	Input bias current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
$I_{IO}$	Input offset current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
CMRR	Common-mode rejection ratio	vs Frequency	10
$V_{OH}$	High-level output voltage	vs High-level output current	11, 13, 15
$V_{OL}$	Low-level output voltage	vs Low-level output current	12, 14, 16
$V_{O(PP)}$	Output voltage peak-to-peak	vs Frequency	17
$Z_o$	Output impedance	vs Frequency	18
$I_{CC}$	Supply current	vs Supply voltage	19
PSRR	Power supply rejection ratio	vs Frequency	20
AVD	Differential voltage gain	vs Frequency	21
	Phase	vs Frequency	21
	Gain-bandwidth product	vs Supply voltage	22
SR	Slew rate	vs Free-air temperature	23
$\phi_m$	Phase margin	vs Capacitive load	24
	Gain margin	vs Capacitive load	25
Voltage noise over a 10 Second Period			26
Large-signal voltage follower			27, 28, 29
Small-signal voltage follower			30
Large-signal inverting pulse response			31, 32, 33
Small-signal inverting pulse response			34
Crosstalk		vs Frequency	35

# TLV2241, TLV2242, TLV2244

## FAMILY OF 1- $\mu$ A/Ch RAIL-TO-RAIL INPUT/OUTPUT

### OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS

### INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

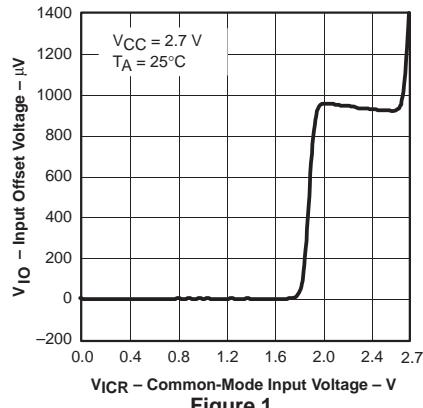


Figure 1

### INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

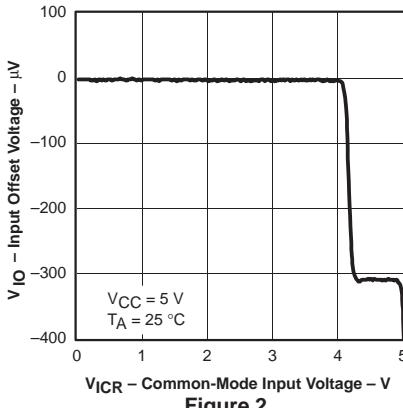


Figure 2

### INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

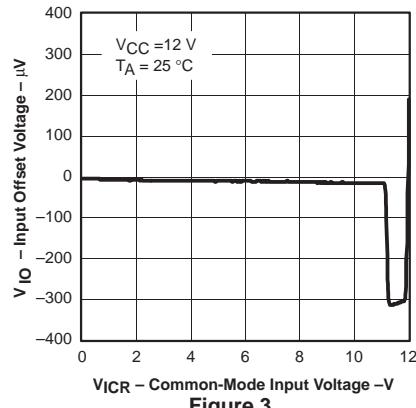


Figure 3

### INPUT BIAS / OFFSET CURRENT vs FREE-AIR TEMPERATURE

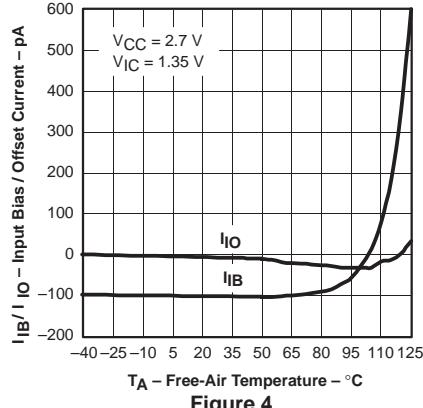


Figure 4

### INPUT BIAS / OFFSET CURRENT vs COMMON MODE INPUT VOLTAGE

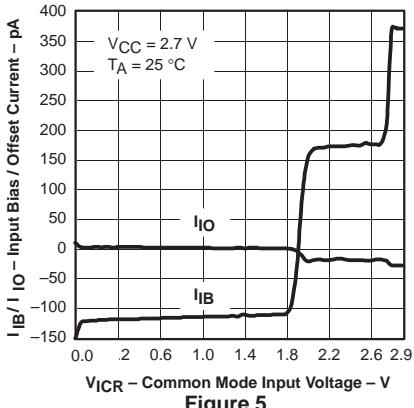


Figure 5

### INPUT BIAS / OFFSET CURRENT vs FREE-AIR TEMPERATURE

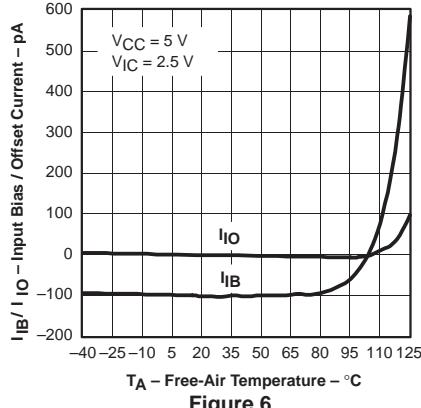


Figure 6

### INPUT BIAS / OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

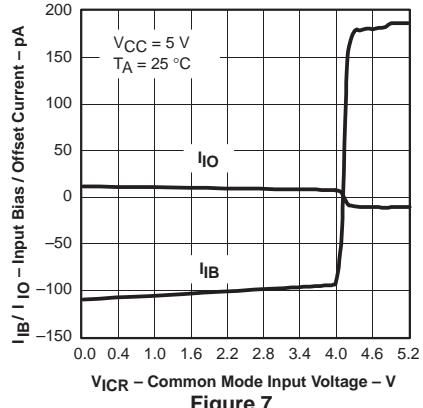


Figure 7

### INPUT BIAS / OFFSET CURRENT vs FREE-AIR TEMPERATURE

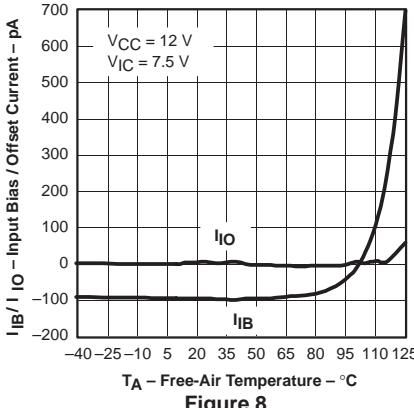


Figure 8

### INPUT BIAS / OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

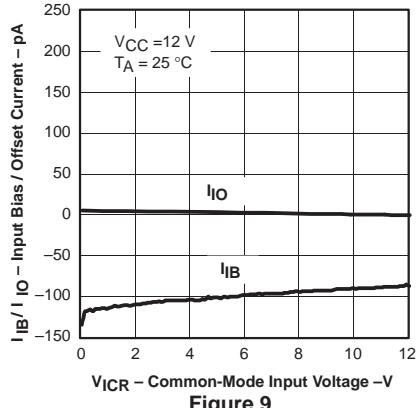
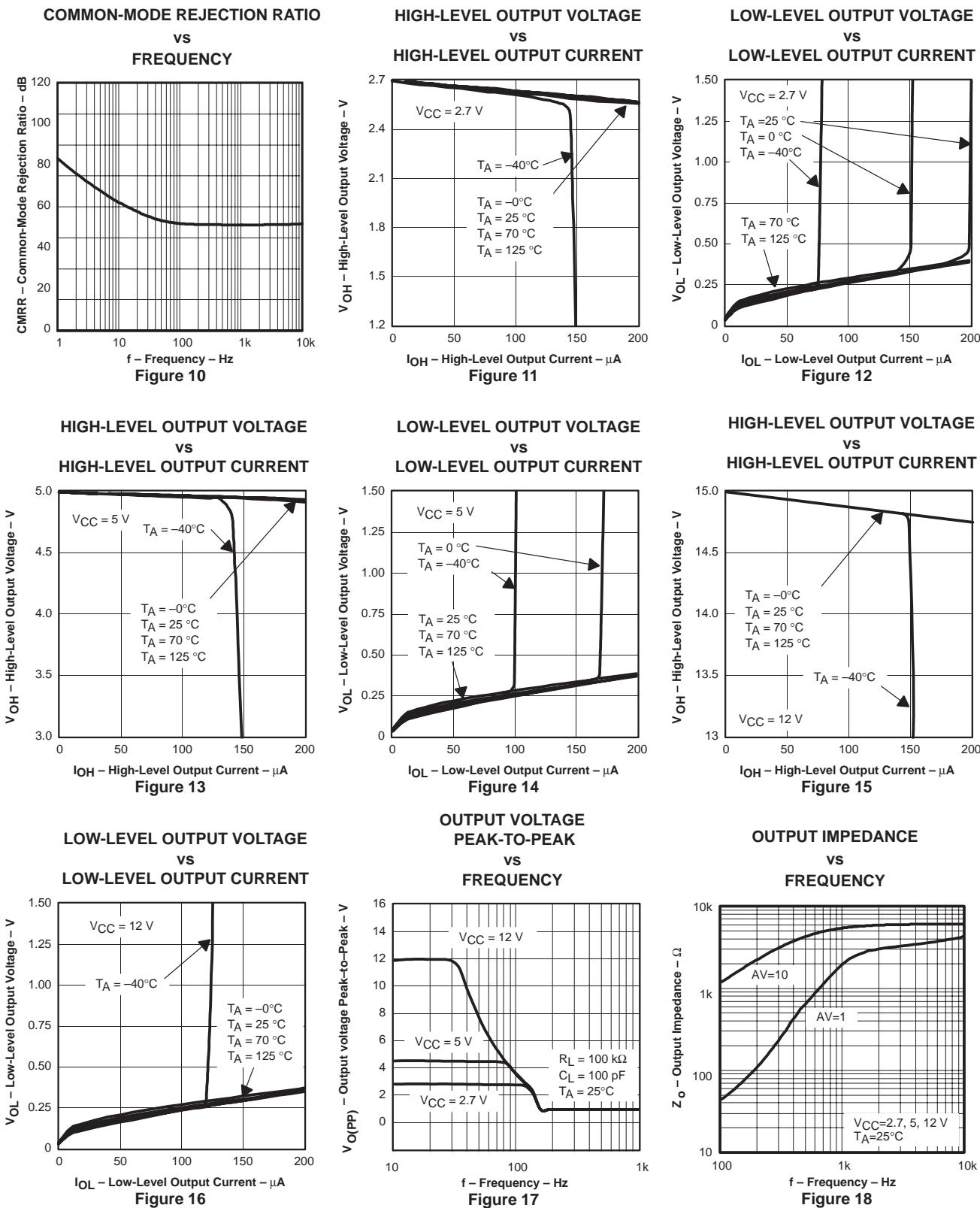


Figure 9

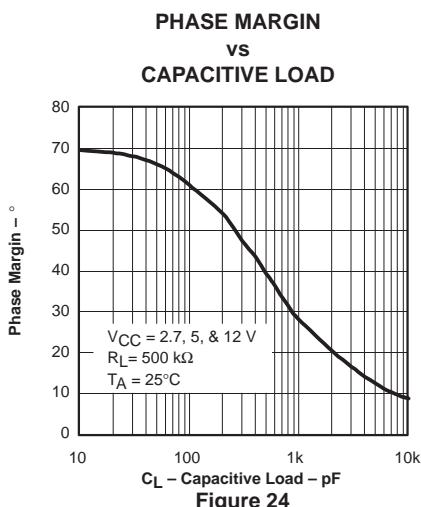
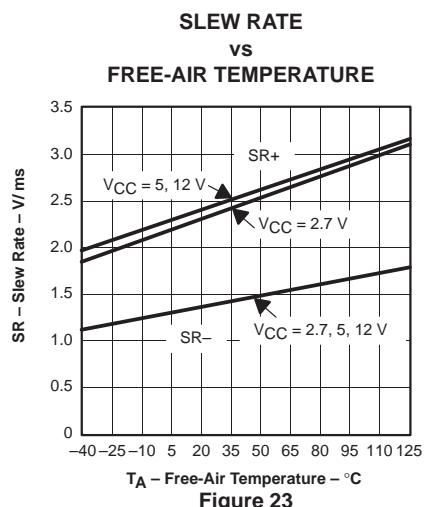
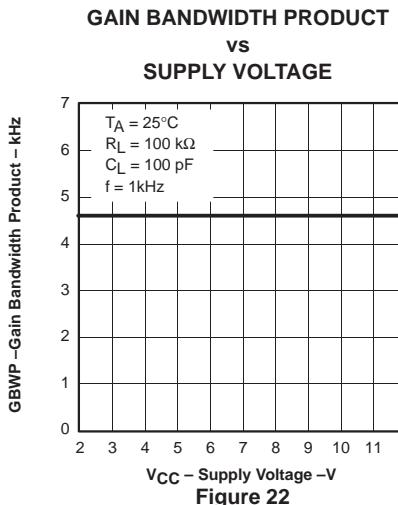
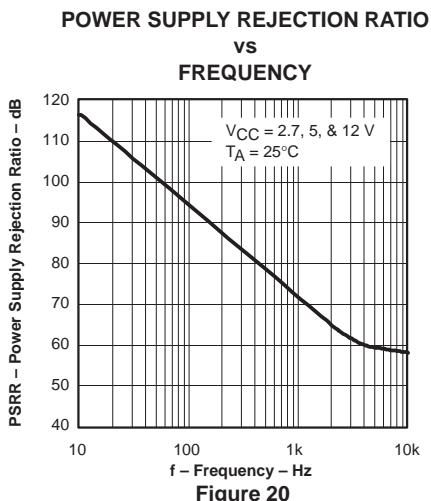
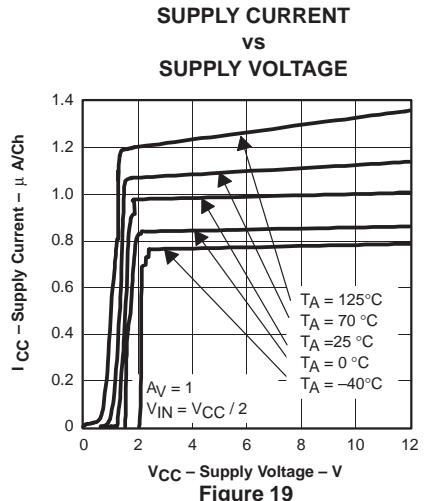
## TYPICAL CHARACTERISTICS



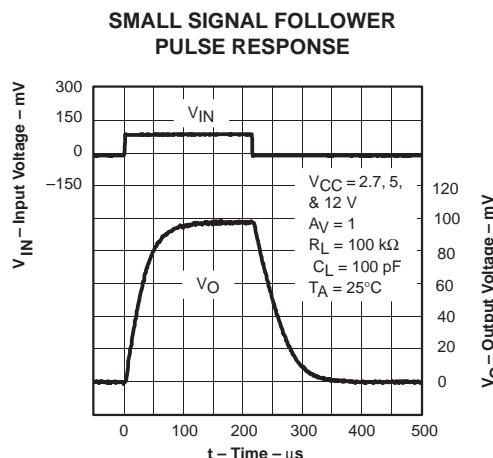
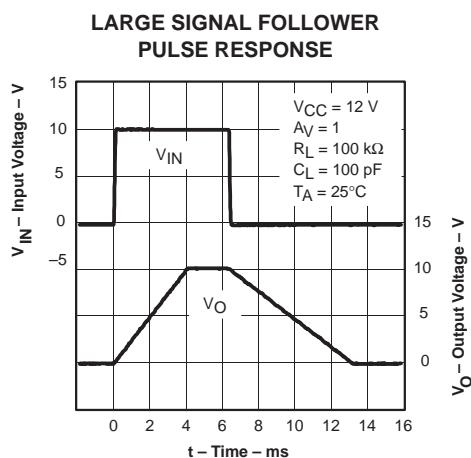
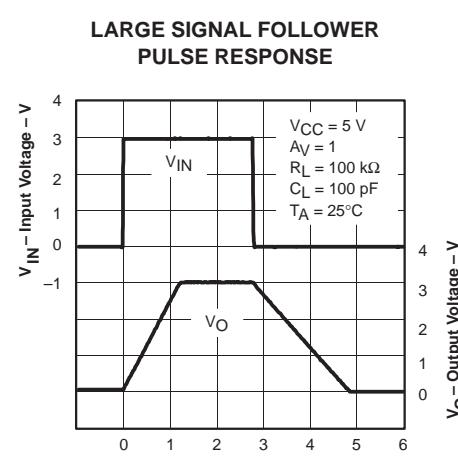
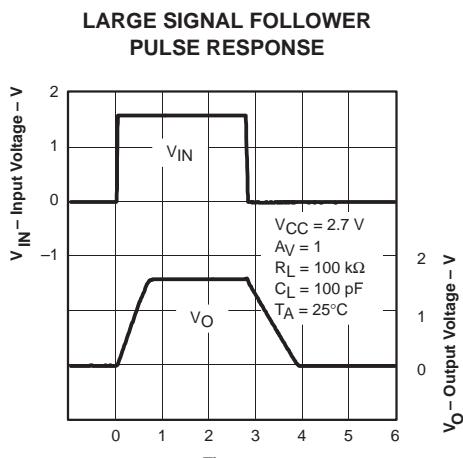
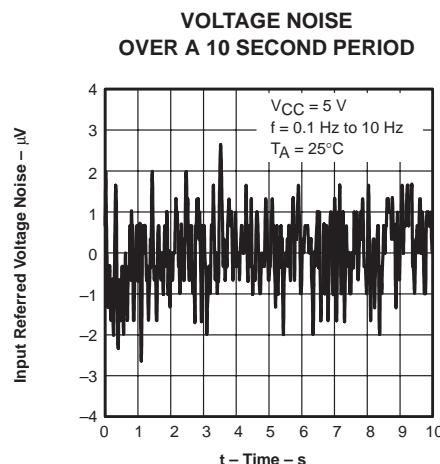
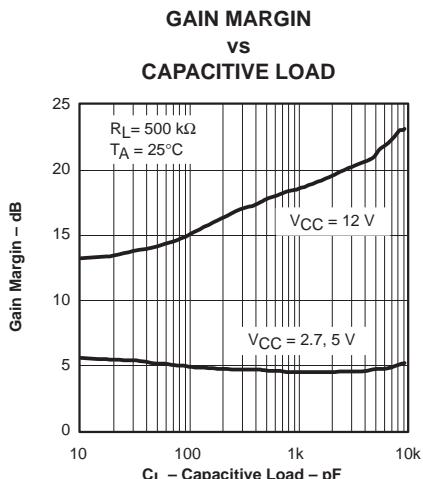
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**TYPICAL CHARACTERISTICS**



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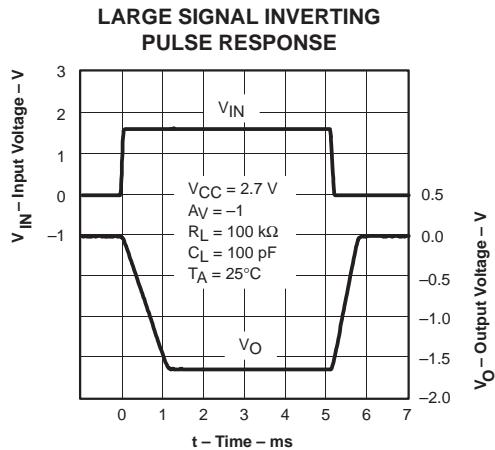


Figure 31

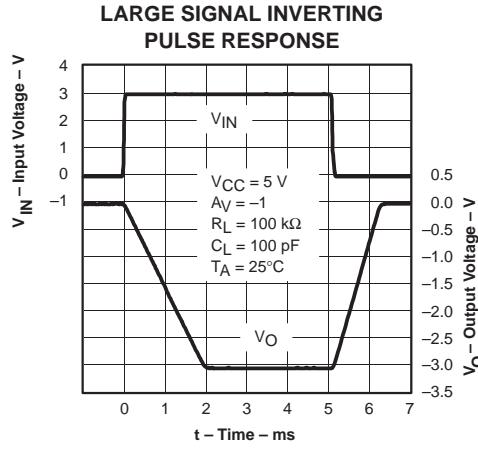


Figure 32

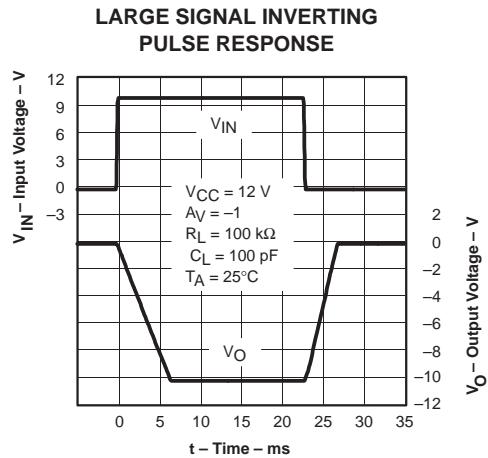


Figure 33

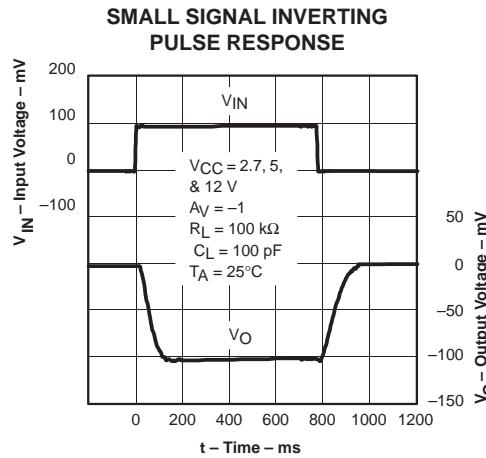


Figure 34

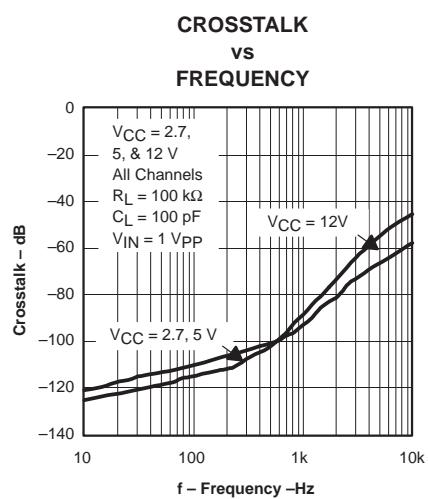
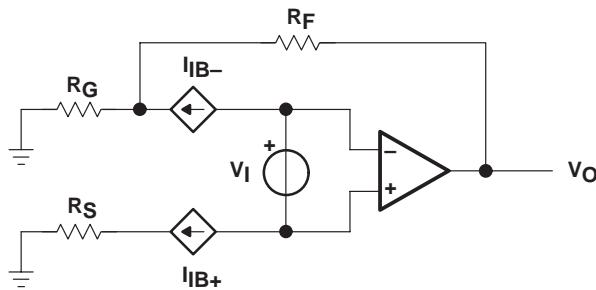


Figure 35

## APPLICATION INFORMATION

### offset voltage

The output offset voltage, ( $V_{OO}$ ) is the sum of the input offset voltage ( $V_{IO}$ ) and both input bias currents ( $I_{IB}$ ) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

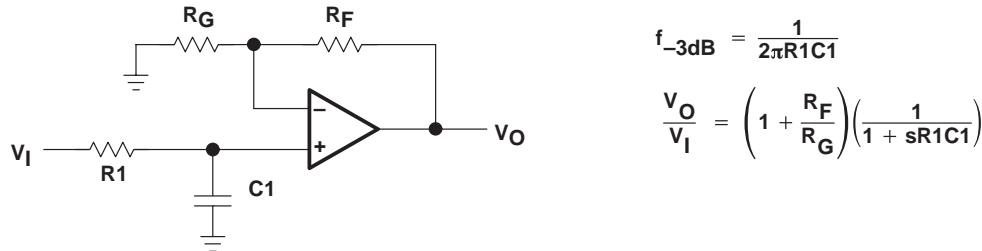


$$V_{OO} = V_{IO} \left( 1 + \left( \frac{R_F}{R_G} \right) \right) \pm I_{IB+} R_S \left( 1 + \left( \frac{R_F}{R_G} \right) \right) \pm I_{IB-} R_F$$

**Figure 36. Output Offset Voltage Model**

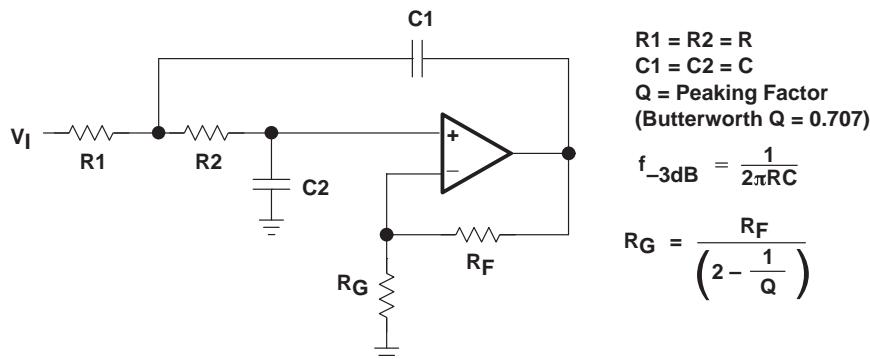
### general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 37).



**Figure 37. Single-Pole Low-Pass Filter**

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



$$R_1 = R_2 = R$$

$$C_1 = C_2 = C$$

$$Q = \text{Peaking Factor}$$

$$(\text{Butterworth } Q = 0.707)$$

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left( 2 - \frac{1}{Q} \right)}$$

**Figure 38. 2-Pole Low-Pass Sallen-Key Filter**

**TLV2241, TLV2242, TLV2244  
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## APPLICATION INFORMATION

### circuit layout considerations

To achieve the levels of high performance of the TLV224x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- **Ground planes**—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- **Proper power supply decoupling**—Use a 6.8- $\mu$ F tantalum capacitor in parallel with a 0.1- $\mu$ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- $\mu$ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- $\mu$ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- **Sockets**—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- **Short trace runs/compact part placements**—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- **Surface-mount passive components**—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.



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## APPLICATION INFORMATION

### general power dissipation considerations

For a given  $\theta_{JA}$ , the maximum power dissipation is shown in Figure 39 and is calculated by the following formula:

$$P_D = \left( \frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

$P_D$  = Maximum power dissipation of THS224x IC (watts)

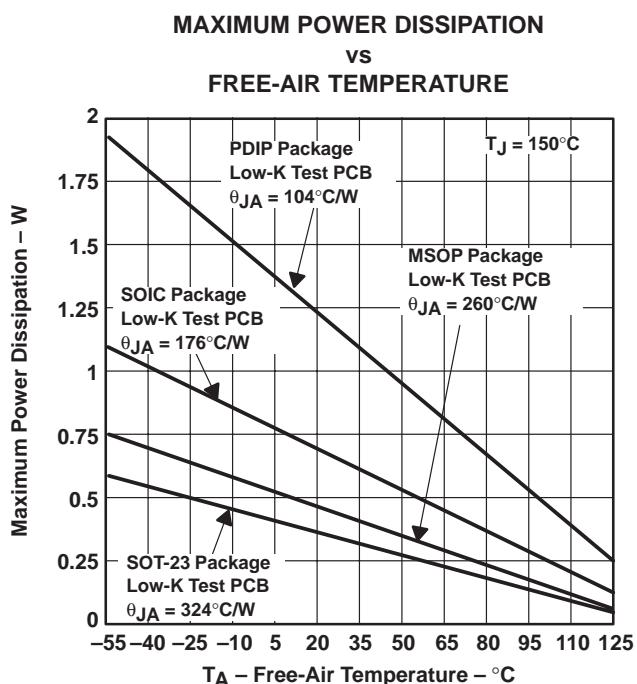
$T_{MAX}$  = Absolute maximum junction temperature (150°C)

$T_A$  = Free-ambient air temperature (°C)

$\theta_{JA}$  =  $\theta_{JC} + \theta_{CA}$

$\theta_{JC}$  = Thermal coefficient from junction to case

$\theta_{CA}$  = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

**Figure 39. Maximum Power Dissipation vs Free-Air Temperature**

# TLV2241, TLV2242, TLV2244 FAMILY OF 1- $\mu$ A/Ch RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS

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## APPLICATION INFORMATION

### macromodel information

Macromodel information provided was derived using Microsim *Parts*<sup>TM</sup> Release 8, the model generation software used with Microsim *PSpice*<sup>TM</sup>. The Boyle macromodel (see Note 2) and subcircuit in Figure 40 are generated using the TLV224x typical electrical and operating characteristics at  $T_A = 25^\circ\text{C}$ . Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

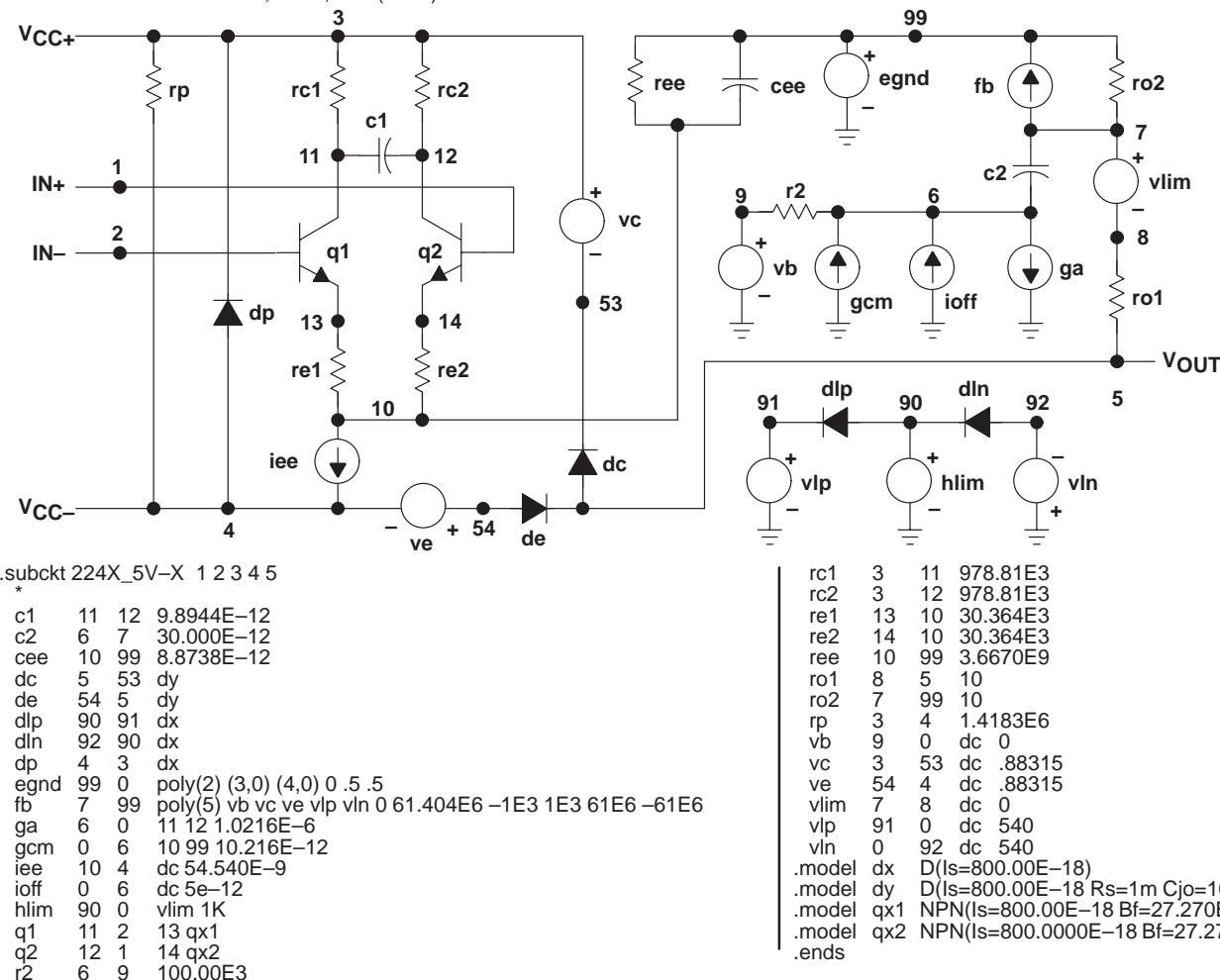


Figure 40. Boyle Macromodels and Subcircuit

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2241ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2241I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2241IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBEI	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2241IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBEI	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2241IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBEI	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2241IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBEI	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2241IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2241I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2241IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2241I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2241IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2241I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2242CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2242C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2242CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2242C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2242CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2242C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2242ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2242I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2242IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2242I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2242IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ALE	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2242IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ALE	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2242IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ALE	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2242IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2242I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2242IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2242I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2244CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2244C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2244ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2244I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2244IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2244I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2244IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2244I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2244IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2244I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2244IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2244I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2244IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2244I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2244IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2244I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TLV2244IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2244I	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

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**TBD:** The Pb-Free/Green conversion plan has not been defined.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

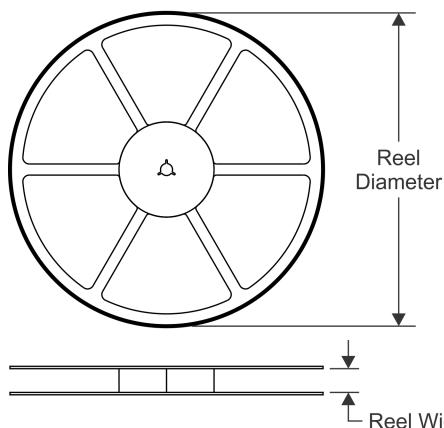
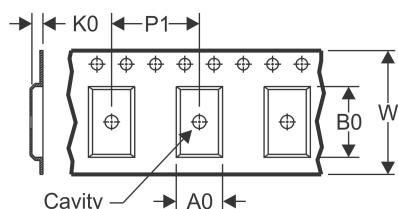
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

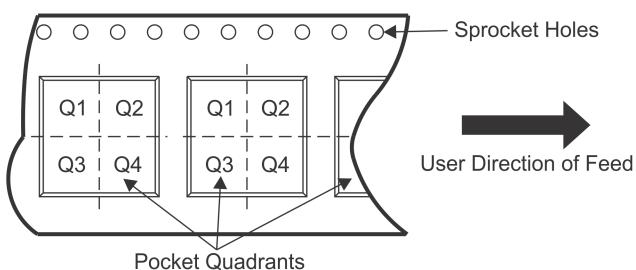
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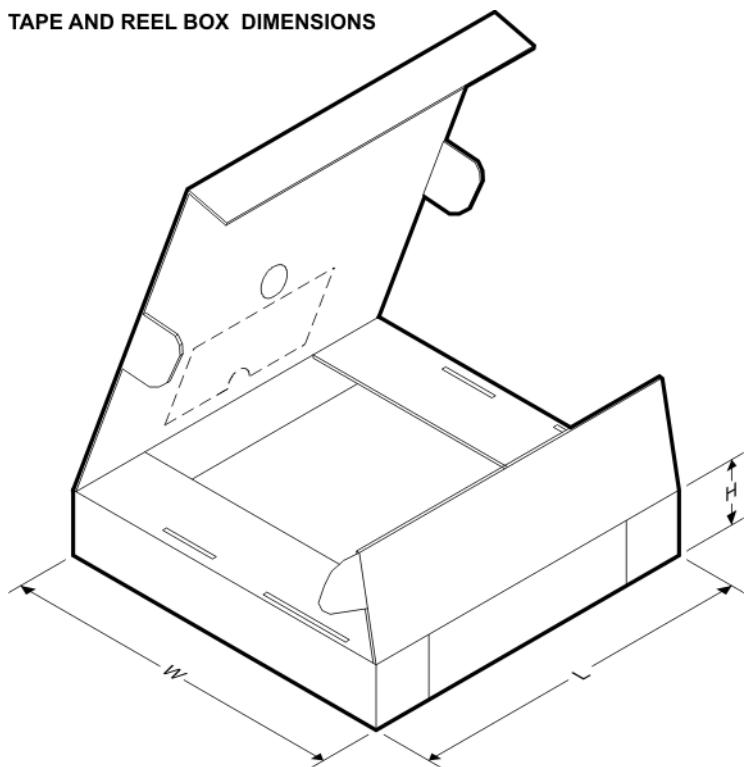
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2241IDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2241IDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2241IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2241IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2242CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2242IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2242IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2244IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2244IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2241IDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2241IDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV2241IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2241IDR	SOIC	D	8	2500	367.0	367.0	35.0
TLV2242CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2242IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2242IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2244IDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV2244IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
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