DATASHEET

ISL6526, ISL6526A

Single Synchronous Buck Pulse-Width Modulation (PWM) Controller

FN9055
Rev 12.00
Sep 30, 2015

The ISL6526, ISL6526A make simple work out of implementing a complete control and protection scheme for a DC/DC stepdown converter. Designed to drive N-Channel MOSFETs in a synchronous buck topology, the ISL6526, ISL6526A integrate the control, output adjustment, monitoring and protection functions into a single package.

The ISL6526, ISL6526A provide simple, single feedback loop, voltage-mode control with fast transient response. The output voltage can be precisely regulated to as low as 0.8V, with a maximum tolerance of ±1.5% over-temperature and line voltage variations. A fixed frequency oscillator reduces design complexity, while balancing typical application cost and efficiency.

The error amplifier features a 15MHz gain-bandwidth product and 6V/µs slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty cycles range from 0% to 100%.

Protection from overcurrent conditions is provided by monitoring the $r_{DS(ON)}$ of the upper MOSFET to inhibit PWM operation appropriately. This approach simplifies the implementation and improves efficiency by eliminating the need for a current sense resistor.

Features

- Operates from 3.3V to 5V Input
- 0.8V to V_{IN} Output Range
  - 0.8V Internal Reference
  - ±1.5% Over Load, Line Voltage and Temperature
- Drives N-Channel MOSFETs
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Fast Transient Response
  - High-Bandwidth Error Amplifier
  - Full 0% to 100% Duty Cycle
- Lossless, Programmable Overcurrent Protection
  - Uses Upper MOSFET's $r_{DS(on)}$
- Converter can Source and Sink Current
- Small Converter Size
  - Internal Fixed Frequency Oscillator
    - ISL6526: 300kHz
    - ISL6526A: 600kHz
- Internal Soft-Start
- 14 Ld SOIC or 16 Ld 5x5 QFN
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package Footprint, which Improves PCB Efficiency and has a Thinner Profile
- Pb-Free (RoHS Compliant)

Applications

- Power Supplies for Microprocessors
  - PCs
  - Embedded Controllers
- Subsystem Power Supplies
  - PCI/AGP/GTL+ Buses
  - ACPI Power Control
  - DDR SDRAM Bus Termination Supply
- Cable Modems, Set-Top Boxes, and DSL Modems
- DSP and Core Communications Processor Supplies
- Memory Supplies
- Personal Computer Peripherals
- Industrial Power Supplies
- 3.3V-Input DC/DC Regulators
- Low-Voltage Distributed Power Supplies

Ordering Information

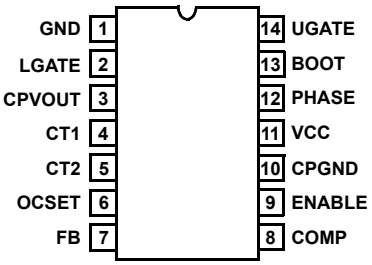
PART NUMBER (Notes 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG DWG. #
ISL6526CBZ	6526CBZ	0 to +70	14 Ld SOIC (Pb-free)	M14.15
ISL6526CBZ-T (Note 1)	6526CBZ	0 to +70	14 Ld SOIC (Pb-free)	M14.15
ISL6526ACBZ **(No longer available, recommended replacement: ISL6526AIRZ)**	6526ACBZ	0 to +70	14 Ld SOIC (Pb-free)	M14.15
ISL6526ACBZ-T (Note 1) **(No longer available, recommended replacement: ISL6526AIRZ-T)**	6526ACBZ	0 to +70	14 Ld SOIC (Pb-free)	M14.15
ISL6526CRZ **(No longer available, recommended replacement: ISL6526IRZ)**	ISL6526 CRZ	0 to +70	16 Ld 5x5 QFN (Pb-free)	L16.5x5B
ISL6526CRZ-T (Note 1) **(No longer available, recommended replacement: ISL6526IRZ-T)**	ISL6526 CRZ	0 to +70	16 Ld 5x5 QFN (Pb-free)	L16.5x5B
ISL6526IBZ	6526IBZ	-40 to +85	14 Ld SOIC (Pb-free)	M14.15
ISL6526IBZ-T (Note 1)	6526IBZ	-40 to +85	14 Ld SOIC (Pb-free)	M14.15
ISL6526IRZ	ISL 6526IRZ	-40 to +85	16 Ld 5x5 QFN (Pb-free)	L16.5x5B
ISL6526IRZ-T (Note 1)	ISL 6526IRZ	-40 to +85	16 Ld 5x5 QFN (Pb-free)	L16.5x5B
ISL6526IRZ-TK (Note 1)	ISL 6526IRZ	-40 to +85	16 Ld 5x5 QFN (Pb-free)	L16.5x5B
ISL6526AIRZ	ISL65 26AIRZ	-40 to +85	16 Ld 5x5 QFN (Pb-free)	L16.5x5B
ISL6526AIRZ-T (Note 1)	ISL65 26AIRZ	-40 to +85	16 Ld 5x5 QFN (Pb-free)	L16.5x5B
ISL6526AIRZ-TK (Note 1)	ISL65 26AIRZ	-40 to +85	16 Ld 5x5 QFN (Pb-free)	L16.5x5B
ISL6526EVAL1	ISL6526 SOIC Evaluation Board			
ISL6526EVAL2	ISL6526 QFN Evaluation Board			
ISL6526AEVAL1	ISL6526A SOIC Evaluation Board			
ISL6526AEVAL2	ISL6526A QFN Evaluation Board			

NOTES:

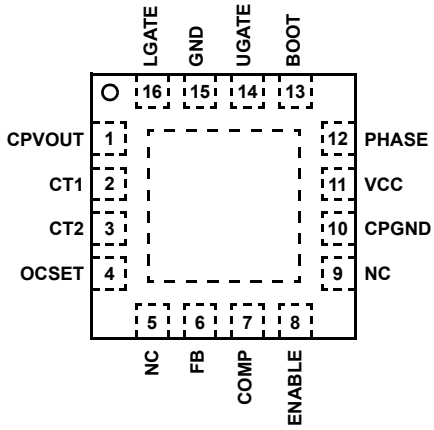
1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6526, ISL6526A. For more information on MSL please see tech brief TB363.

Pinouts

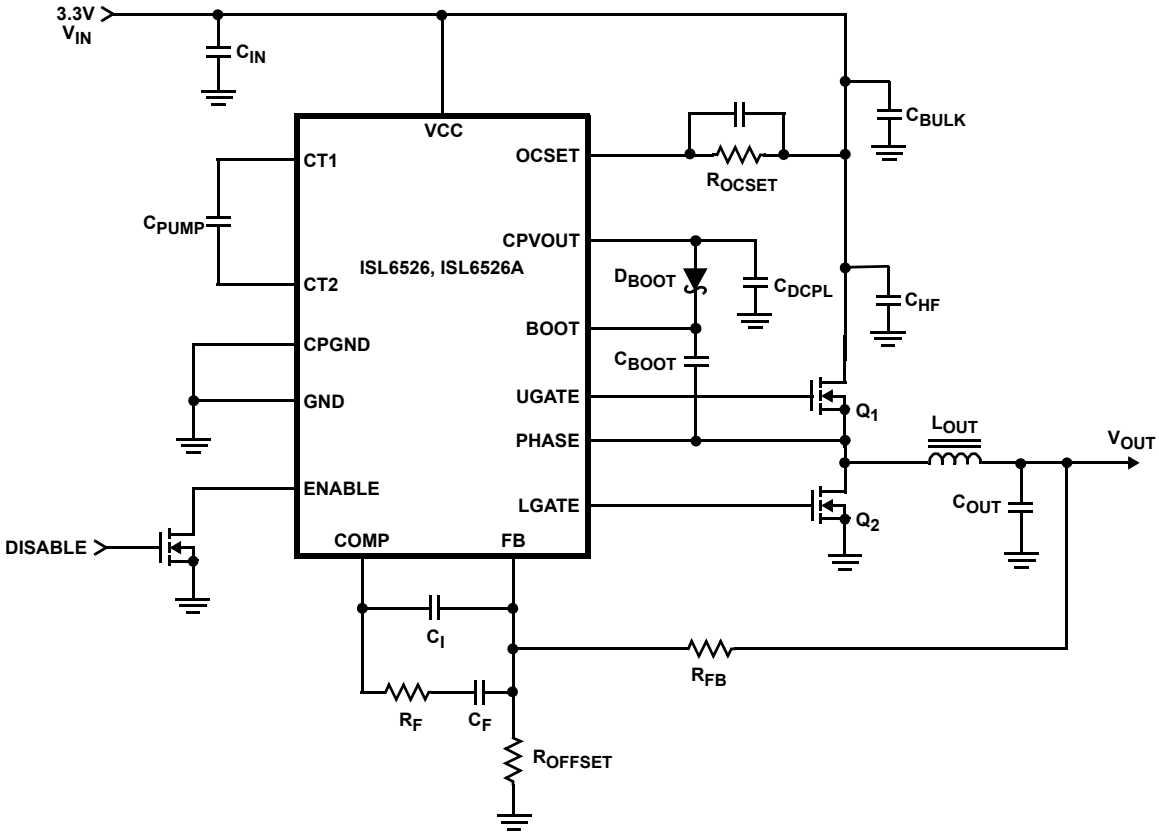
ISL6526, ISL6526A
(14 LD SOIC)
TOP VIEW



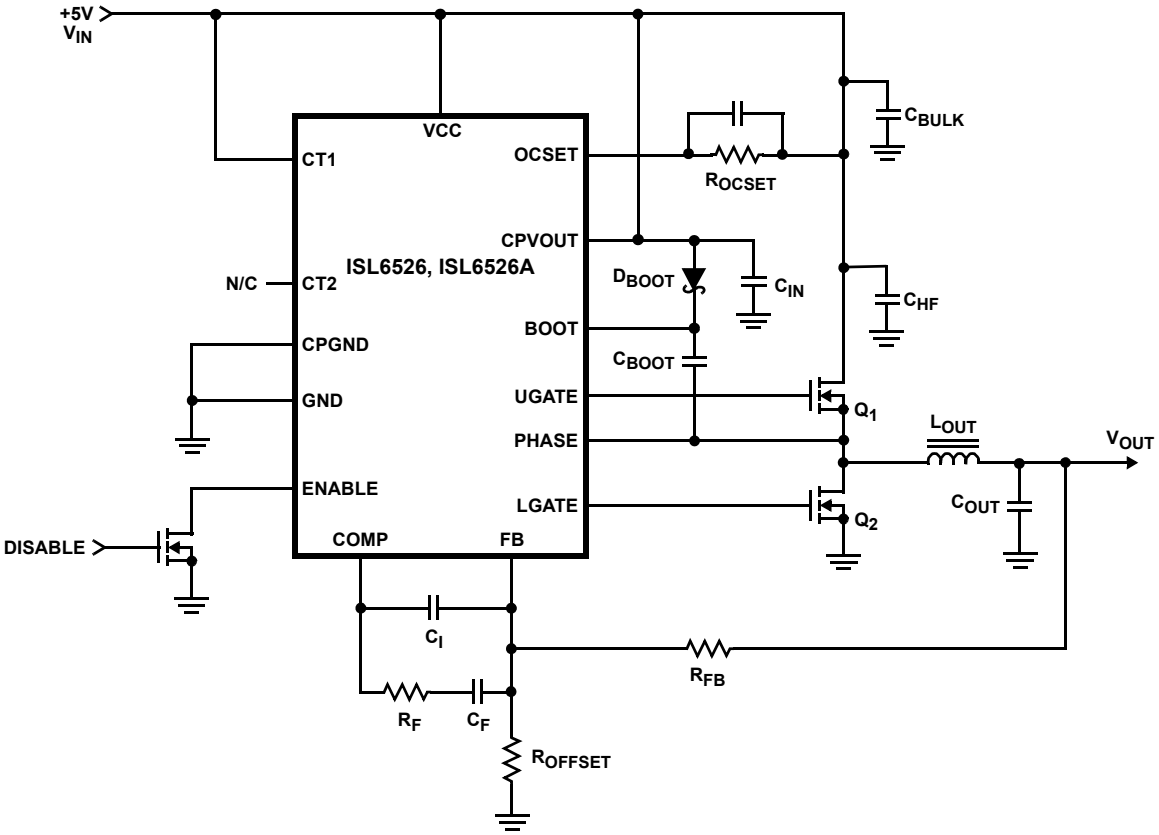
ISL6526, ISL6526A
(16 LD QFN)
TOP VIEW



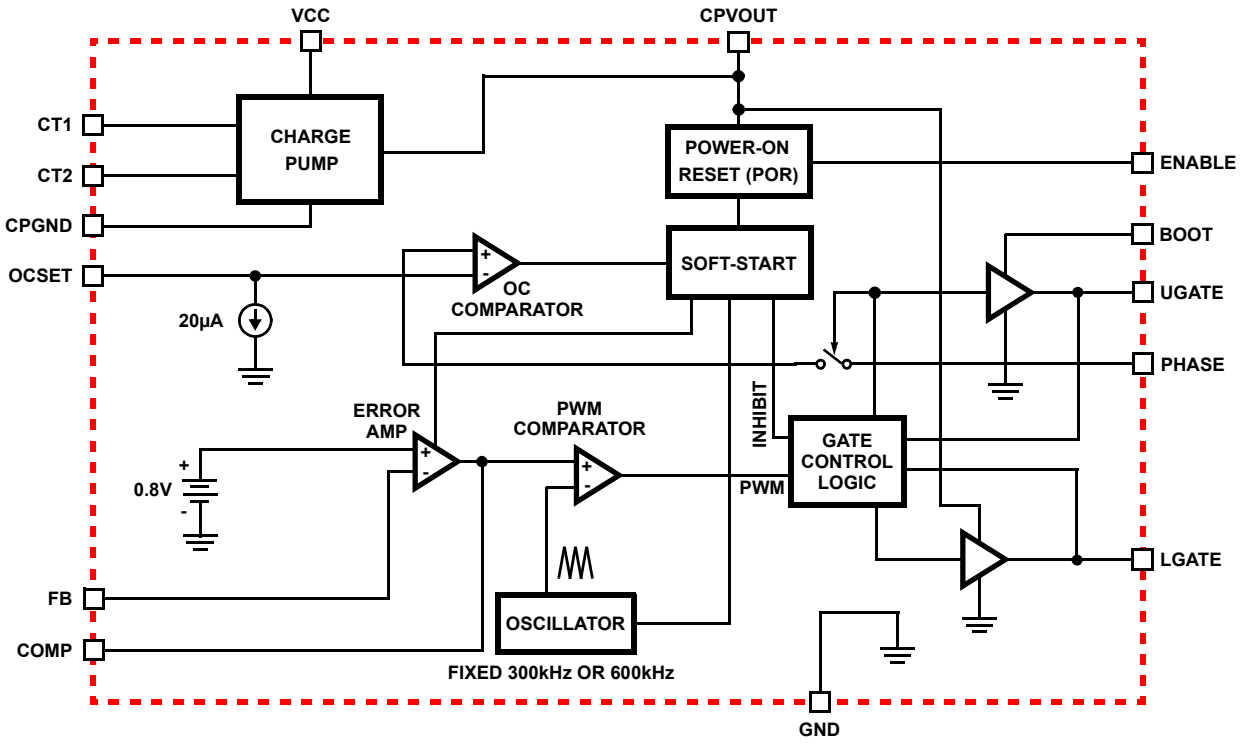
Typical Application - 3.3V Input



Typical Application - 5V Input



Block Diagram



Absolute Maximum Ratings

Supply Voltage, VCC . . . . . +7.0V
Absolute Boot Voltage, V_{BOOT} . . . . . +15.0V
Upper Driver Supply Voltage, V_{BOOT} - V_{PHASE} . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V

Operating Conditions

Supply Voltage, VCC . . . . . +3.3V ±10%
Ambient Temperature Range . . . . . -40°C to +85°C
Junction Temperature Range . . . . . -40°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 4)	67	N/A
QFN Package (Notes 5, 6)	35	5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, unless otherwise noted V_{CC} = 3.3V ±5% and T_A = +25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
VCC SUPPLY CURRENT						
Nominal Supply	I_{BIAS}		6.1	6.9	7.7	mA
POWER-ON RESET						
Rising CPVOUT POR Threshold	POR	Commercial	4.25	4.30	4.42	V
		Industrial	4.10	4.30	4.50	V
CPVOUT POR Threshold Hysteresis			0.3	0.6	0.9	V
OSCILLATOR						
Frequency	f_{OSC}	IC = ISL6526C, Commercial	275	300	325	kHz
		IC = ISL6526I, Industrial	250	300	340	kHz
		IC = ISL6526AC, Commercial	554	600	645	kHz
		IC = ISL6526AI, Industrial	524	600	650	kHz
Ramp Amplitude	ΔV_{OSC}		-	1.5	-	V_{P-P}
REFERENCE						
Reference Voltage Tolerance			-	-	1.5	%
Nominal Reference Voltage	V_{REF}		-	0.800	-	V
CHARGE PUMP						
Nominal Charge Pump Output	V_{CPVOUT}	V_{VCC} = 3.3V, No Load	-	5.1	-	V
Charge Pump Output Regulation			-	2	-	%
ERROR AMPLIFIER						
DC Gain		(Note 7)	-	88	-	dB
Gain-Bandwidth Product	GBWP		-	15	-	MHz
Slew Rate	SR		-	6	-	V/µs
SOFT-START						
Soft-Start Slew Rate		Commercial	6.2	-	7.3	ms
		Industrial	6.2	-	7.6	ms

Electrical Specifications Recommended Operating Conditions, unless otherwise noted V_{CC} = 3.3V ±5% and T_A = +25°C. **(Continued)**

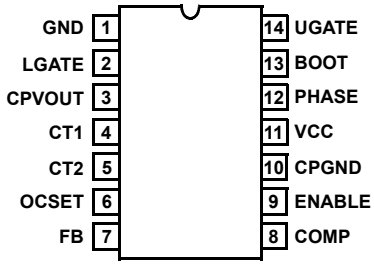
PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
GATE DRIVERS						
Upper Gate Source Current	$I_{UGATE-SRC}$	V_{BOOT} - V_{PHASE} = 5V, V_{UGATE} = 4V	-	-1	-	A
Upper Gate Sink Current	$I_{UGATE-SNK}$		-	1	-	A
Lower Gate Source Current	$I_{LGATE-SRC}$	V_{VCC} = 3.3V, V_{LGATE} = 4V	-	-1	-	A
Lower Gate Sink Current	$I_{LGATE-SNK}$		-	2	-	A
PROTECTION/DISABLE						
OCSET Current Source	I_{OCSET}	Commercial	18	20	22	µA
		Industrial	16	20	22	µA
Disable Threshold	$V_{DISABLE}$		-	-	0.8	V

NOTE:

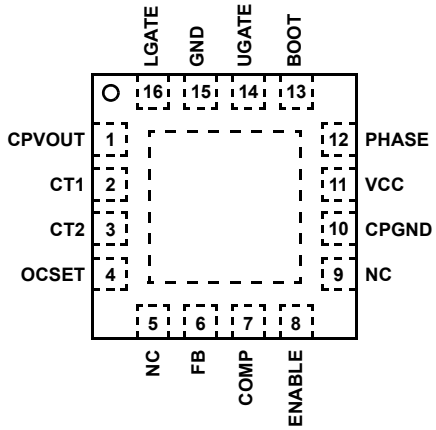
7. Limits should be considered typical and are not production tested.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Functional Pin Descriptions

14 LD SOIC
TOP VIEW



16 LD 5X5 QFN
TOP VIEW



VCC

This pin provides the bias supply for the ISL6526, ISL6526A. Connect a well-decoupled 3.3V supply to this pin.

COMP and FB

COMP and FB are the available external pins of the error amplifier. The FB pin is the inverting input of the internal error amplifier and the COMP pin is the error amplifier output. These pins are used to compensate the voltage control feedback loop of the converter.

GND

This pin represents the signal and power ground for the IC. Tie this pin to the ground island/plane through the lowest impedance connection available.

PHASE

Connect this pin to the upper MOSFET's source. This pin is used to monitor the voltage drop across the upper MOSFET for overcurrent protection.

UGATE

Connect this pin to the upper MOSFET's gate. This pin provides the PWM-controlled gate drive for the upper MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.

BOOT

This pin provides ground referenced bias voltage to the upper MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive a logic-level N-Channel MOSFET.

LGATE

Connect this pin to the lower MOSFET's gate. This pin provides the PWM-controlled gate drive for the lower MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.

OCSET

Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET (V_{IN}). R_{OCSET}, an internal 20µA current source (I_{OCSET}), and the upper MOSFET ON-resistance ($r_{DS(ON)}$) set the converter overcurrent (OC) trip point according Equation 1:

$$I_{PEAK} = \frac{I_{OCSET} x R_{OCSET}}{r_{DS(ON)}} \quad \text{(EQ. 1)}$$

An overcurrent trip cycles the soft-start function.

ENABLE

This pin is the open-collector enable pin. Pulling this pin to a level below 0.8V will disable the controller. Disabling the ISL6526, ISL6526A causes the oscillator to stop, the LGATE and UGATE outputs to be held low, and the soft-start circuitry to re-arm.

CT1 and CT2

These pins are the connections for the external charge pump capacitor. A minimum of a 0.1µF ceramic capacitor is recommended for proper operation of the IC.

CPVOUT

This pin represents the output of the charge pump. The voltage at this pin is the bias voltage for the IC. Connect a decoupling capacitor from this pin to ground. The value of the decoupling capacitor should be at least 10x the value of the charge pump capacitor. This pin may be tied to the bootstrap circuit as the source for creating the BOOT voltage.

CPGND

This pin represents the signal and power ground for the charge pump. Tie this pin to the ground island/plane through the lowest impedance connection available.

Functional Description

Initialization

The ISL6526, ISL6526A automatically initialize upon receipt of power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the output voltage of the charge pump. During POR, the charge pump operates on a free running oscillator. Once the POR level is reached, the charge pump oscillator is synched to the PWM oscillator. The POR function also initiates the soft-start operation after the charge pump output voltage exceeds its POR threshold.

Soft-Start

The POR function initiates the digital soft-start sequence. The PWM error amplifier reference is clamped to a level proportional to the soft-start voltage. As the soft-start voltage slews up, the PWM comparator generates PHASE pulses of increasing width that charge the output capacitor(s). This method provides a rapid and controlled output voltage rise. The soft-start sequence typically takes about 6.5ms.

Figure 1 shows the soft-start sequence for a typical application. At t0, the +3.3V VCC voltage starts to ramp-up. At time t1, the Charge Pump begins operation and the +5V CPVOUT IC bias voltage starts to ramp-up. Once the voltage on CPVOUT crosses the POR threshold at time t2, the output begins the soft-start sequence. The triangle waveform from the PWM oscillator is compared to the rising error amplifier output voltage. As the error amplifier voltage increases, the pulse width on the UGATE pin increases to reach the steady-state duty cycle at time t3.

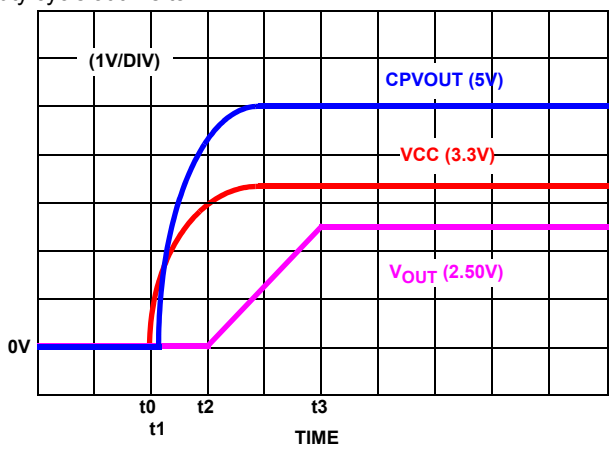


FIGURE 1. SOFT-START INTERVAL

Shoot-Through Protection

A shoot-through condition occurs when both the upper MOSFET and lower MOSFET are turned on simultaneously, effectively shorting the input voltage to ground. To protect the regulator from a shoot-through condition, the ISL6526, ISL6526A incorporate specialized circuitry which insures that the complementary MOSFETs are not ON simultaneously.

The adaptive shoot-through protection utilized by the ISL6526, ISL6526A look at the lower gate drive pin, LGATE, and the upper gate drive pin, UGATE, to determine whether a MOSFET is ON or OFF. If the voltage from UGATE or from LGATE to GND is less than 0.8V, then the respective MOSFET is defined as being OFF and the complementary MOSFET is turned ON. This method of shoot-through protection allows the regulator to sink or source current.

Since the voltage of the lower MOSFET gate and the upper MOSFET gate are being measured to determine the state of the MOSFET, the designer is encouraged to consider the repercussions of introducing external components between the gate drivers and their respective MOSFET gates before actually implementing such measures. Doing so may interfere with the shoot-through protection.

Output Voltage Selection

The output voltage can be programmed to any level between V_{IN} and the internal reference, 0.8V. An external resistor divider is used to scale the output voltage relative to the

reference voltage and feed it back to the inverting input of the error amplifier; see Figure 2. However, since the value of R1 affects the values of the rest of the compensation components, it is advisable to keep its value less than 5kΩ. R4 can be calculated based Equation 2:

$$R4 = \frac{R1 \times 0.8V}{V_{OUT1} - 0.8V} \quad \text{(EQ. 2)}$$

If the output voltage desired is 0.8V, simply route the output back to the FB pin through R1, but do not populate R4.

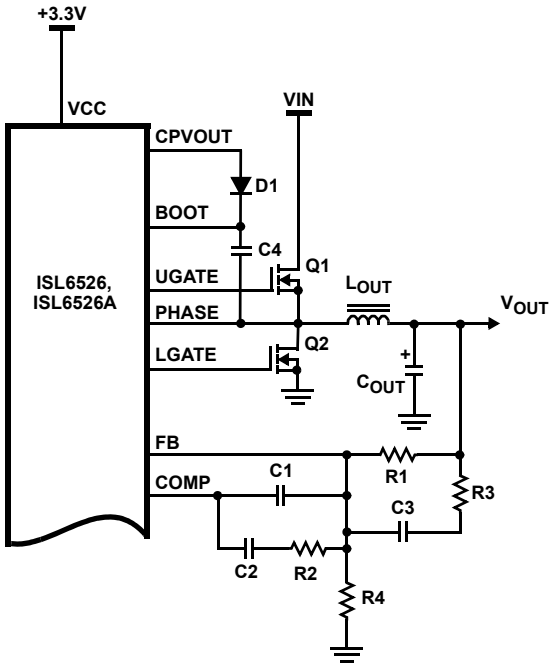


FIGURE 2. OUTPUT VOLTAGE SELECTION

Overcurrent Protection

The overcurrent function protects the converter from a shorted output by using the upper MOSFET ON-resistance, $r_{DS(ON)}$, to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

The overcurrent function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor (R_{OCSET}) programs the overcurrent trip level (see "Typical Application - 3.3V Input" on page 4 and "Typical Application - 5V Input" on page 4). An internal 20µA (typical) current sink develops a voltage across R_{OCSET} that is referenced to V_{IN}. When the voltage across the upper MOSFET (also referenced to V_{IN}) exceeds the voltage across R_{OCSET}, the overcurrent function initiates a soft-start sequence.

Figure 3 illustrates the protection feature responding to an overcurrent event. At time t0, an overcurrent condition is sensed across the upper MOSFET. As a result, the regulator is quickly shutdown and the internal soft-start function begins producing soft-start ramps. The delay interval seen by the output is equivalent to three soft-start cycles. The fourth internal soft-start cycle initiates a normal soft-start ramp of the output, at time t1. The output is brought back into regulation by time t2, as long as the overcurrent event has cleared.

Had the cause of the overcurrent still been present after the delay interval, the overcurrent condition would be sensed and the regulator would be shut down again for another delay interval of three soft-start cycles. The resulting hiccup mode style of protection would continue to repeat indefinitely.

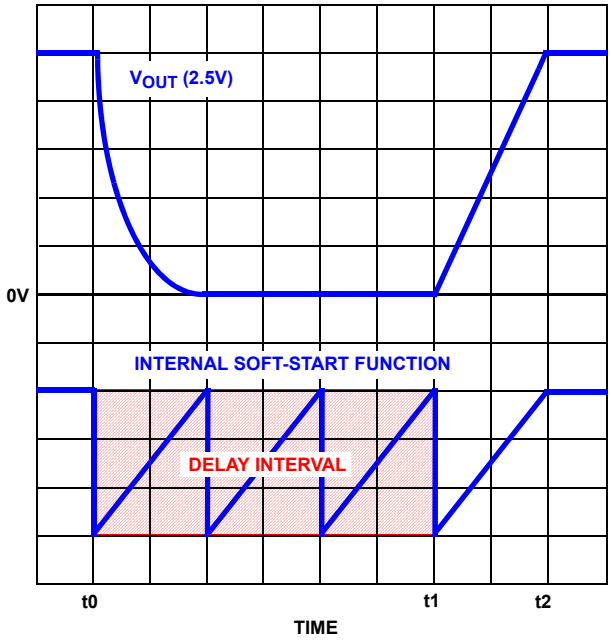


FIGURE 3. OVERCURRENT PROTECTION RESPONSE

The overcurrent function will trip at a peak inductor current (I_{PEAK}) determined by Equation 3:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}} \quad \text{(EQ. 3)}$$

where I_{OCSET} is the internal OCSET current source (20µA typical). The OC trip point varies mainly due to the MOSFET $r_{DS(ON)}$ variations. To avoid overcurrent tripping in the normal operating load range, find the R_{OCSET} resistor from Equation 3 with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature.
2. The minimum I_{OCSET} from the specification table.
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + \frac{(\Delta I)}{2}$, where ΔI is the output inductor ripple current.

For the ripple current, see Equation 11 in "Output Inductor Selection" on page 12.

A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage.

Current Sinking

The ISL6526, ISL6526A incorporate a MOSFET shoot-through protection method which allows a converter to sink current as well as source current. Care should be exercised when designing a converter with the ISL6526, ISL6526A when it is known that the converter may sink current.

When the converter is sinking current, it is behaving as a boost converter that is regulating its input voltage. This means that the converter is boosting current into the input rail of the regulator. If there is nowhere for this current to go, (such as to other distributed loads on the rail or through a voltage limiting protection device), the capacitance on this rail will absorb the current. This situation will allow the voltage level of the input rail to increase. If the voltage level of the rail is boosted to a level that exceeds the maximum voltage rating of any components attached to the input rail, then those components may experience an irreversible failure or experience stress that may shorten their lifespan. Ensuring that there is a path for the current to flow other than the capacitance on the rail will prevent this failure mode.

Application Guidelines

Layout Considerations

Layout is very important in high frequency switching converter design. With power devices switching efficiently at 300kHz or 600kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit board design minimize the voltage spikes in the converters.

As an example, consider the turn-off transition of the PWM MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is picked up by the lower MOSFET. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC/DC converter using the ISL6526, ISL6526A. The switching components are the most critical because they switch large amounts of energy, and therefore tend to generate large amounts of noise. Next are the small signal components which connect to sensitive nodes or supply critical bypass current and signal coupling.

A multi-layer printed circuit board is recommended. Figure 4 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer (usually a middle layer of the PC board) for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminals to the output inductor short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the GATE pins to the MOSFET gates should be kept short and wide enough to easily handle the 1A of drive current.

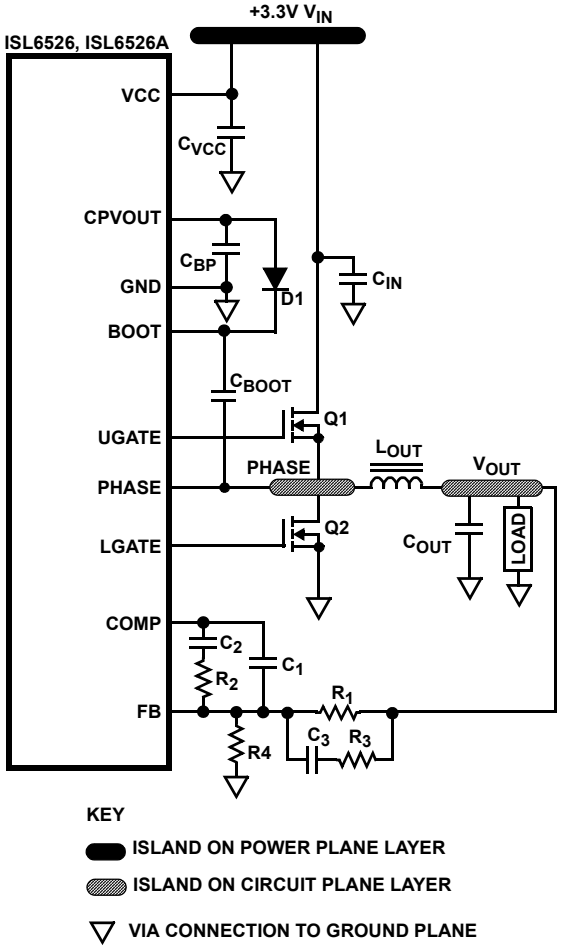


FIGURE 4. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

The switching components should be placed close to the ISL6526, ISL6526A first. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches by placing them nearby. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible. Position the output inductor and output capacitors between the upper MOSFET and lower MOSFET and the load.

The critical small signal components include any bypass capacitors, feedback components, and compensation components. Position the bypass capacitor, C_{BP}, close to the VCC pin with a via directly to the ground plane. Place the PWM converter compensation components close to the FB

and COMP pins. The feedback resistors for both regulators should also be located as close as possible to the relevant FB pin with vias tied straight to the ground plane as required.

Feedback Compensation

Figure 5 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at f_{LC} and a zero at f_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

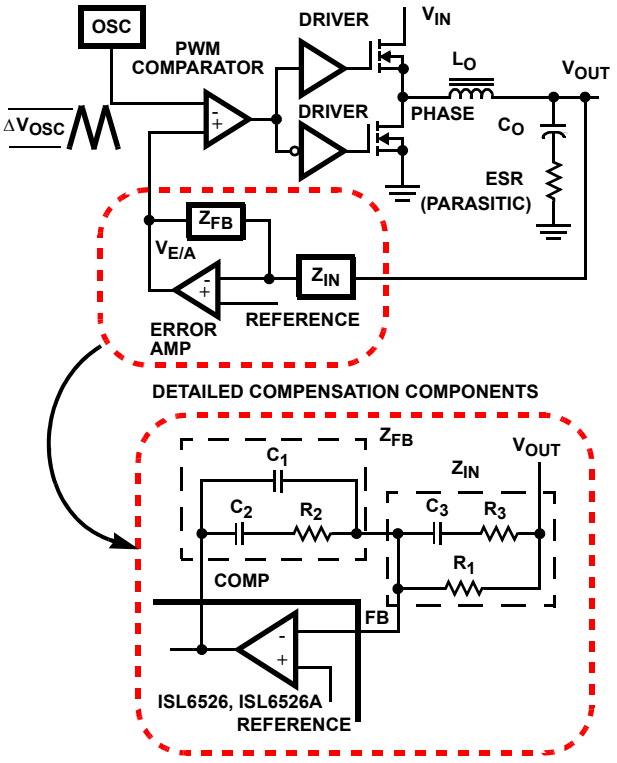


FIGURE 5. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

Modulator Break Frequency Equations

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \quad \text{(EQ. 4)}$$

$$f_{ESR} = \frac{1}{2\pi \times ESR \times C_O} \quad \text{(EQ. 5)}$$

The compensation network consists of the error amplifier (internal to the ISL6526, ISL6526A) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180°. Equations 6, 7, 8 and 9 relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 5. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick gain (R_2/R_1) for desired converter bandwidth.
2. Place first zero below filter's double pole (~75% f_{LC}).
3. Place second zero at filter's double pole.
4. Place first pole at the ESR zero.
5. Place second pole at half the switching frequency.
6. Check gain against error amplifier's open-loop gain.
7. Estimate phase margin - repeat if necessary.

Compensation Break Frequency Equations

$$f_{Z1} = \frac{1}{2\pi \times R_2 \times C_2} \quad \text{(EQ. 6)}$$

$$f_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \quad \text{(EQ. 7)}$$

$$f_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)} \quad \text{(EQ. 8)}$$

$$f_{P2} = \frac{1}{2\pi \times R_3 \times C_3} \quad \text{(EQ. 9)}$$

Figure 6 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 6. Using the previously mentioned guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at f_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the graph of Figure 6 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin.

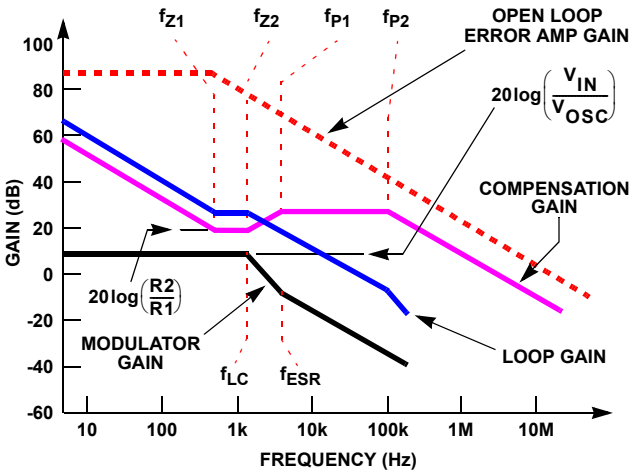


FIGURE 6. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Component Selection Guidelines

Charge Pump Capacitor Selection

A capacitor across pins CT1 and CT2 is required to create the proper bias voltage for the ISL6526, ISL6526A when operating the IC from 3.3V. Selecting the proper capacitance value is important so that the bias current draw and the current required by the MOSFET gates do not overburden the capacitor. A conservative approach is presented in Equation 10.

$$C_{PUMP} = \frac{I_{BiasAndGate}}{V_{CC} \times f_s} \times 1.5 \quad \text{(EQ. 10)}$$

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern digital ICs can produce high transient load slew rates. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by Equations 11 and 12:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{f_s \times L} \times \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 11)}$$

$$\Delta V_{OUT} = \Delta I \times ESR \quad \text{(EQ. 12)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6526, ISL6526A will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. Equations 13 and 14 give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \quad \text{(EQ. 13)}$$

$$t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}} \quad \text{(EQ. 14)}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q_1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q_1 and the source of Q_2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

The maximum RMS current required by the regulator may be closely approximated using Equation 15:

$$I_{RMS_{MAX}} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left({I_{OUT_{MAX}}}^2 + \frac{1}{12} \times \left(\frac{V_{IN} - V_{OUT}}{L \times f_s} \times \frac{V_{OUT}}{V_{IN}} \right)^2 \right)} \quad \text{(EQ. 15)}$$

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

MOSFET Selection/Considerations

The ISL6526, ISL6526A require two N-Channel power MOSFETs. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor. The switching losses seen when sourcing current will be different from the switching losses seen when sinking current. When sourcing current, the upper MOSFET realizes most of the switching losses. The lower switch realizes most of the switching losses when the converter is sinking current (see Equations 16 and 17). These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the upper and lower MOSFET's body diode. The gate-charge losses are dissipated by the ISL6526, ISL6526A and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

Losses while Sourcing Current

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times f_s$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D) \quad \text{(EQ. 16)}$$

Losses while Sinking Current

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D) + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times f_s$$

Where: D is the duty cycle = V_{OUT}/V_{IN},
t_{SW} is the combined switch ON and OFF time, and
f_s is the switching frequency.

(EQ. 17)

Given the reduced available gate bias voltage (5V), logic-level or sub-logic-level transistors should be used for both N-MOSFETs. Caution should be exercised with devices exhibiting very low $V_{GS(ON)}$ characteristics. The shoot-through protection present aboard the ISL6526, ISL6526A may be circumvented by these MOSFETs if they have large parasitic impedances and/or capacitances that would inhibit the gate of the MOSFET from being discharged below its threshold level before the complementary MOSFET is turned on.

Bootstrap Component Selection

External bootstrap components, a diode and capacitor, are required to provide sufficient gate enhancement to the upper MOSFET. The internal MOSFET gate driver is supplied by the external bootstrap circuitry, as shown in Figure 7. The boot capacitor, C_{BOOT}, develops a floating supply voltage referenced to the PHASE pin. This supply is refreshed each cycle, when D_{BOOT} conducts, to a voltage of CPVOUT less the boot diode drop, V_D, plus the voltage rise across Q_{LOWER}.

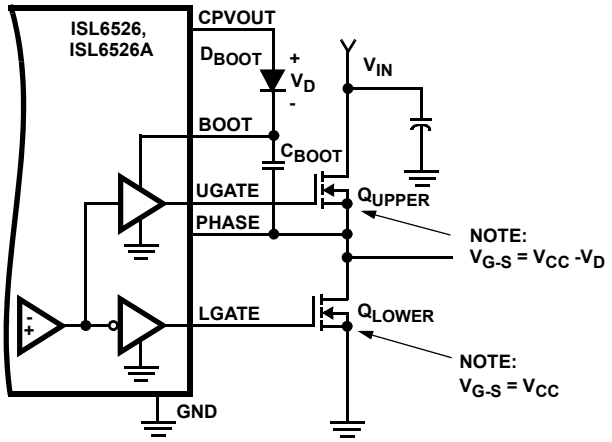


FIGURE 7. UPPER GATE DRIVE BOOTSTRAP

Just after the PWM switching cycle begins and the charge transfer from the bootstrap capacitor to the gate capacitance is complete, the voltage on the bootstrap capacitor is at its lowest point during the switching cycle. The charge lost on the bootstrap capacitor will be equal to the charge transferred to the equivalent gate-source capacitance of the upper MOSFET as shown in Equation 18:

$$Q_{GATE} = C_{BOOT} \times (V_{BOOT1} - V_{BOOT2}) \quad \text{(EQ. 18)}$$

where Q_{GATE} is the maximum total gate charge of the upper MOSFET, C_{BOOT} is the bootstrap capacitance, V_{BOOT1} is the bootstrap voltage immediately before turn-on, and V_{BOOT2} is the bootstrap voltage immediately after turn-on.

The bootstrap capacitor begins its refresh cycle when the gate drive begins to turn-off the upper MOSFET. A refresh cycle ends when the upper MOSFET is turned on again, which varies depending on the switching frequency and duty cycle.

The minimum bootstrap capacitance can be calculated by rearranging the previous equation and solving for C_{BOOT}.

$$C_{BOOT} = \frac{Q_{GATE}}{V_{BOOT1} - V_{BOOT2}} \quad \text{(EQ. 19)}$$

Typical gate charge values for MOSFETs considered in these types of applications range from 20 to 100nC. Since the voltage drop across Q_{LOWER} is negligible, V_{BOOT1} is simply V_{CPVOUT} - V_D. A Schottky diode is recommended to minimize the voltage drop across the bootstrap capacitor during the on-time of the upper MOSFET. Initial calculations with V_{BOOT2} no less than 4V will quickly help narrow the bootstrap capacitor range.

For example, consider an upper MOSFET is chosen with a maximum gate charge, Q_g, of 100nC. Limiting the voltage drop across the bootstrap capacitor to 1V results in a value of no less than 0.1µF. The tolerance of the ceramic capacitor should also be considered when selecting the final bootstrap capacitance value.

A fast recovery diode is recommended when selecting a bootstrap diode to reduce the impact of reverse recovery charge loss. Otherwise, the recovery charge, Q_{RR}, would have to be added to the gate charge of the MOSFET and taken into consideration when calculating the minimum bootstrap capacitance.

ISL6526, ISL6526A DC/DC Converter Application Circuit

Figure 8 shows an application circuit of a DC/DC Converter. Detailed information on the circuit, including a complete Bill of Materials and circuit board description, can be found in Application Note AN1021: http://www.intersil.com/data/an/an1021.pdf.

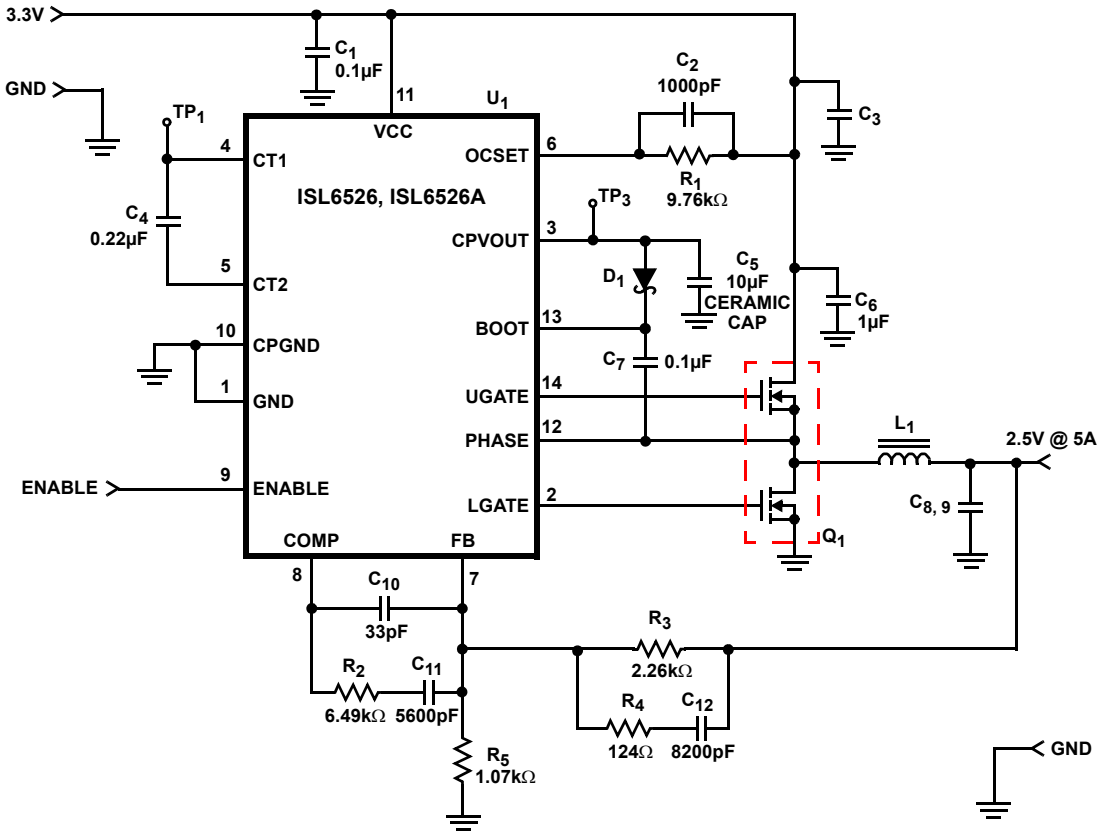


FIGURE 8. 3.3V TO 2.5V 5A DC/DC CONVERTER

Component Selection Notes:

C_3, C_8, C_9 - Each 150µF, Panasonic EEF-UE0J151R or Equivalent.

D1 - 30mA Schottky Diode, MA732 or Equivalent

L_1 - 1µH Inductor, Panasonic P/N ETQ-P6F1ROSFA or Equivalent.

Q_1 - Fairchild MOSFET; ITF86110DK8.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Sep 30, 2015	FN9055.12	Updated Ordering Information Table on page 2. Added Revision History.

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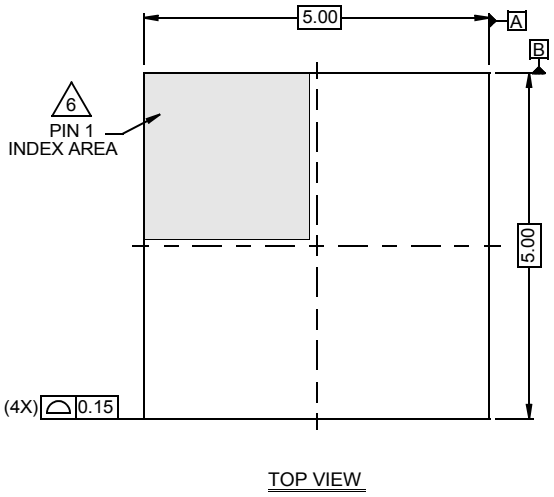
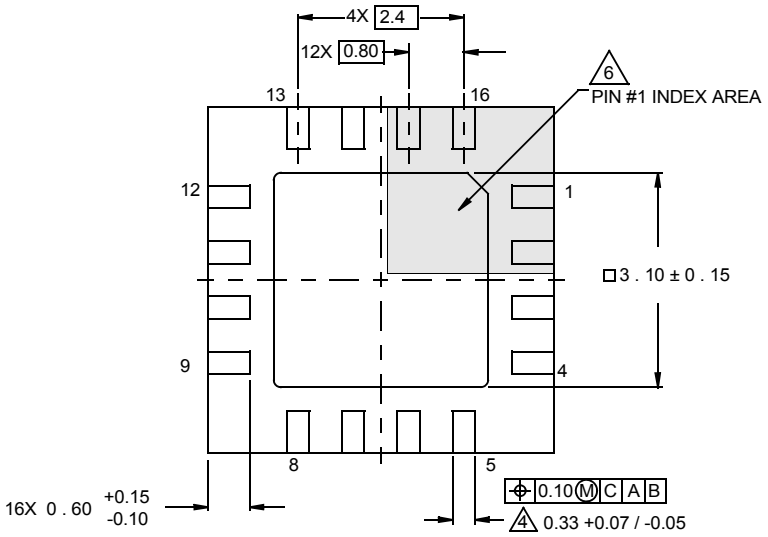
Package Outline Drawing

L16.5x5B

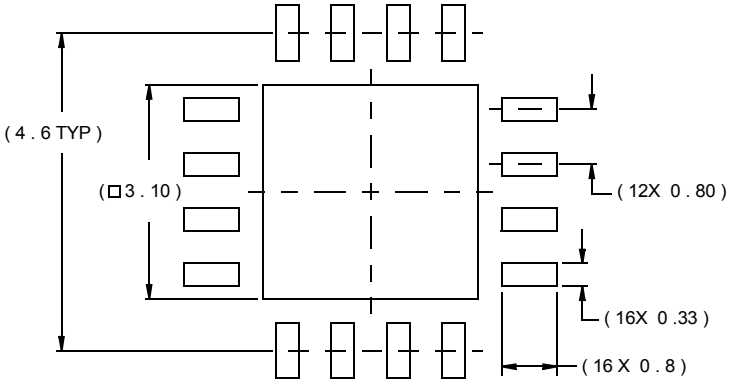
16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 02/08



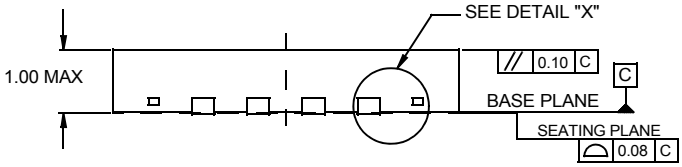
TOP VIEW



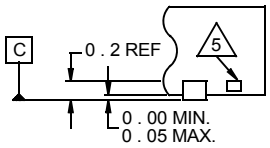
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

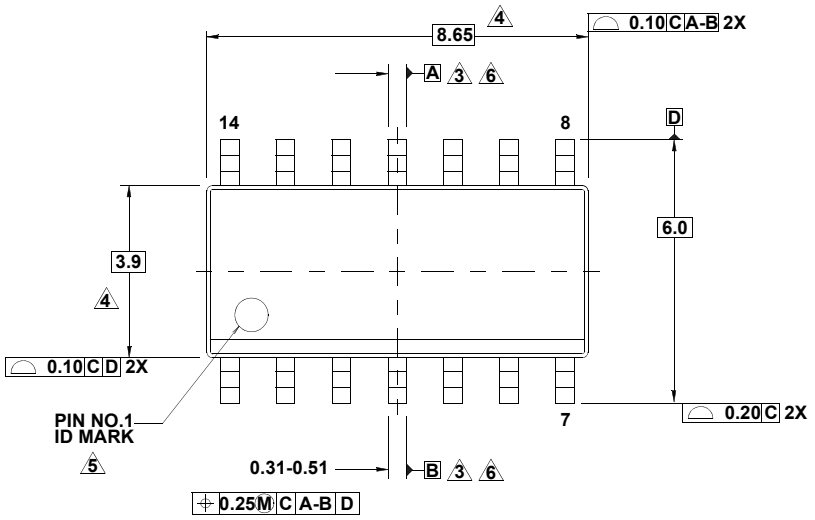
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

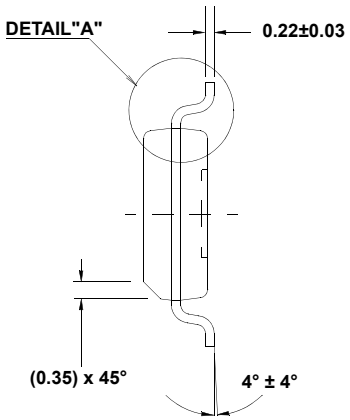
Package Outline Drawing

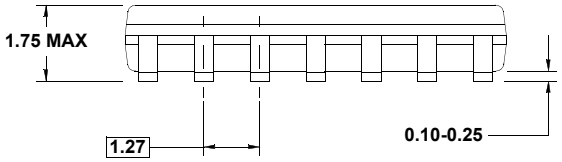
M14.15

14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 1, 10/09

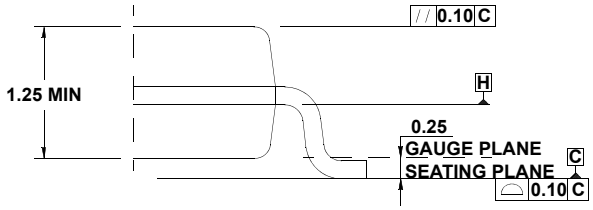


TOP VIEW

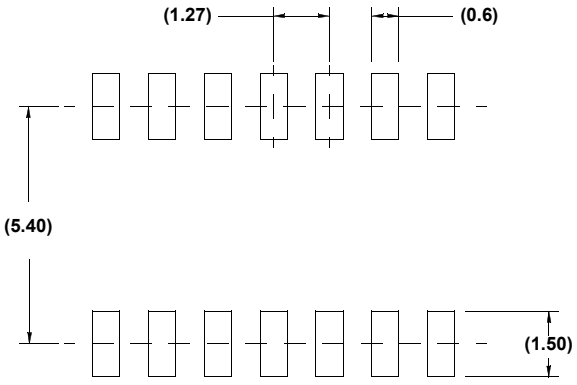




SIDE VIEW



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 indentifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.