# CMOS,
# 12-Bit, Monolithic Multiplying DAC

Data Sheet

# AD7541A

## FEATURES

**Improved version of the obsoleted product, AD7541**
**Full 4 quadrant multiplication**
**12-bit linearity (endpoint)**
**All parts guaranteed monotonic**
**TTL/CMOS compatible**
**Protection Schottky diodes not required**
**Low logic input leakage**

## APPLICATIONS

**Waveform generators**
**Analog processing**
**Instrumentation applications**
**Programmable amplifiers and attenuators**
**Digitally controlled calibration**
**Programmable filters and oscillators**
**Composite video**
**Ultrasound**
**Gain, offset, and voltage trimming**

## FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

LOGIC: A SWITCH IS CLOSED TO $I_{OUT\,1}$ FOR ITS DIGITAL INPUT IN A HIGH STATE.

*Figure 1.*

## GENERAL DESCRIPTION

The AD7541A is a high performance, 12-bit monolithic multiplying digital-to-analog converter (DAC). It is fabricated using advanced, low noise, thin film, complementary metal-oxide semiconductor (CMOS) technology. The AD7541A is available in 18-lead PDIP, 18-lead PLCC, and 18-lead SOIC packages.

The AD7541A is functionally and pin compatible with the industry standard AD7541, and it offers improved specifications and performance over the obsolete product, AD7541. The improved design ensures that the AD7541A is latch-up free; therefore, no output protection Schottky diodes are required.

The AD7541A uses laser wafer trimming to provide full 12-bit endpoint linearity with several high performance grades.
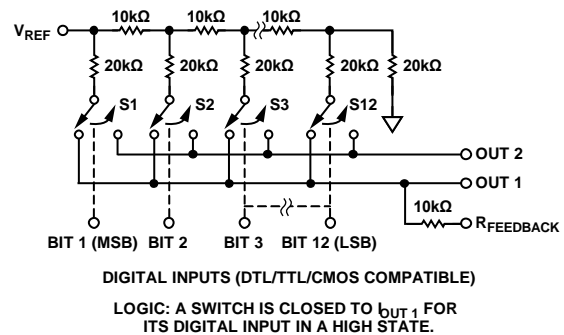
## PRODUCT HIGHLIGHTS

Compatibility—The AD7541A can be used as a direct replacement for any AD7541 type device. As with the AD7541, The digital inputs on the AD7541A are TTL/CMOS compatible. They have a ±1 µA maximum input current requirement so that they do not load the driving circuitry.

Improvements—The AD7541A offers the following improved specifications over the AD7541:

1. Gain error for all grades are reduced with premium grade versions having a maximum gain error of ±3 LSB.
2. Gain error temperature coefficient are reduced to 2 ppm/°C typical and 5 ppm/°C maximum.
3. Digital-to-analog charge injection energy for the AD7541A is typically 20% less than the standard AD7541.
4. Latch-up proof.
5. Laser wafer trimming provides 1/2 LSB maximum differential nonlinearity for top grade devices over the operating temperature range (vs. 1 LSB on previous AD7541 devices).
6. All grades are guaranteed monotonic to 12 bits over the operating temperature range.

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## REVISION HISTORY

**3/2017—Rev. B to Rev. C**

## SPECIFICATIONS

$V_{DD}$ = 15 V, $V_{REF}$ = 10 V, OUT 1 = OUT 2 = GND = 0 V, unless otherwise noted. Temperature range is as follows for the J version and the K version: 0°C to +70°C.

**Table 1.**

| Parameter | Version | $T_A$ = 25°C | $T_A$ = $T_{MIN}$, $T_{MAX}$ | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| ACCURACY | | | | | |
| Resolution | All | 12 | 12 | Bits | |
| Relative Accuracy | J | ±1 | ±1 | LSB max | ±1 LSB = ±0.024% of full scale |
| | K | ±1/2 | ±1/2 | LSB max | ±1/2 LSB = ±0.012% of full scale |
| Differential Nonlinearity | J | ±1 | ±1 | LSB max | All grades guaranteed monotonic to |
| | K | ±1/2 | ±1/2 | LSB max | 12 bits, $T_{MIN}$ to $T_{MAX}$. |
| Gain Error | J | ±6 | ±8 | LSB max | Measured using internal $R_{FEEDBACK}$ and |
| | K | ±3 | ±5 | LSB max | includes effect of leakage current and gain temperature coefficient (TC); gain error can be trimmed to zero |
| Gain TC[1] | | | | | |
| ΔGain/ΔTemperature | All | 5 | 5 | ppm/°C max | Typical value is 2 ppm/°C |
| Output Leakage Current | | | | | |
| OUT 1 (Pin 1) | J, K | ±5 | ±10 | nA max | All digital inputs = 0 V |
| OUT 2 (Pin 2) | J, K | ±5 | ±10 | nA max | All digital inputs = $V_{DD}$ |
| REFERENCE INPUT | | | | | |
| Input Resistance (Pin 17 to GND) | All | 7 to 18 | 7 to 18 | kΩ min/max | Typical input resistance = 11 kΩ; typical input resistance TC = −300 ppm/°C |
| DIGITAL INPUTS | | | | | |
| Input Voltage | | | | | |
| High, $V_{IH}$ | All | 2.4 | 2.4 | V min | |
| Low, $V_{IL}$ | All | 0.8 | 0.8 | V max | |
| Input Current, $I_{IN}$ | All | ±1 | ±1 | µA max | Logic inputs are MOS gates; $I_{IN}$ typical (25°C) = 1 nA |
| Input Capacitance, $C_{IN}$[1] | All | 8 | 8 | pF max | $V_{IN}$ = 0 V |
| POWER SUPPLY REJECTION | | | | | |
| ΔGain/Δ$V_{DD}$ | All | ±0.01 | ±0.02 | % per % max | Δ$V_{DD}$ = ±5% |
| POWER SUPPLY | | | | | |
| $V_{DD}$ Range | All | 5 to 16 | 5 to 16 | V min/V max | Accuracy is not guaranteed over this range |
| $I_{DD}$ | All | 2 | 2 | mA max | All digital inputs $V_{IL}$ or $V_{IH}$ |
| | | 100 | 500 | µA max | All digital inputs 0 V or $V_{DD}$ |

[1] Guaranteed by design but not production tested.

## AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test. $V_{DD}$ = 15 V, $V_{IN}$ = 10 V, and OUT 1 = OUT 2 = GND = 0 V, unless otherwise noted. Temperature range is as follows for the J version and the K version: 0°C to +70°C.

**Table 2.**

| Parameter | $T_A$ = 25°C | $T_A$ = $T_{MIN}$,$T_{MAX}$ | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| PROPAGATION DELAY (FROM DIGITAL INPUT CHANGE TO 90% OF FINAL ANALOG OUTPUT) | 100 | | ns typ | OUT 1 load = 100 Ω, $C_{EXT}$ = 13 pF; digital inputs = 0 V to $V_{DD}$ or $V_{DD}$ to 0 V |
| DIGITAL-TO-ANALOG GLITCH IMPULSE | 1000 | | nV-sec typ | $V_{REF}$ = 0 V; all digital inputs 0 V to $V_{DD}$ or $V_{DD}$ to 0 V; measured using Model 50K as output amplifier |
| MULTIPLYING FEEDTHROUGH ERROR ($V_{REF}$ to OUT 1) | 1.0 | | mV p-p typ | $V_{REF}$ = ±10 V, 10 kHz sine wave |
| OUTPUT CURRENT SETTLING TIME | 0.6 | | µs typ | To 0.01% of full-scale range; OUT 1 load = 100 Ω, $C_{EXT}$ = 13 pF; digital inputs = 0 V to $V_{DD}$ or $V_{DD}$ to 0 V |
| OUTPUT CAPACITANCE | | | | |
| $C_{OUT\,1}$ (Pin 1) | 200 | 200 | pF max | Digital inputs = $V_{IH}$ |
| | 70 | 70 | pF max | Digital inputs = $V_{IL}$ |
| $C_{OUT\,2}$ (Pin 2) | 70 | 70 | pF max | Digital inputs = $V_{IH}$ |
| | 200 | 200 | pF max | Digital inputs = $V_{IL}$ |

# ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$, unless otherwise noted.

**Table 3.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | 17 V |
| $V_{REF}$ to GND | ±25 V |
| $V_{RFEEDBACK}$ to GND | ±25 V |
| Digital Input Voltage to GND | −0.3 V, $V_{DD}$ + 0.3 V |
| OUT 1, OUT 2 to GND | −0.3 V, $V_{DD}$ + 0.3 V |
| Power Dissipation (Any Package) | |
| To 75°C | 450 mW |
| Derates Above 75°C | 6 mW/°C |
| Operating Temperature Range | |
| Commercial (J Version/K Version) | 0°C to 70°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 secs) | 300°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
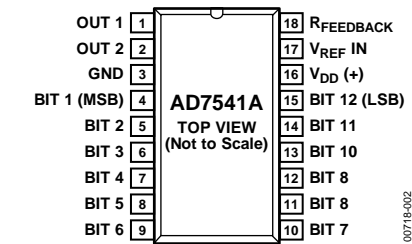
# PIN CONFIGURATIONS



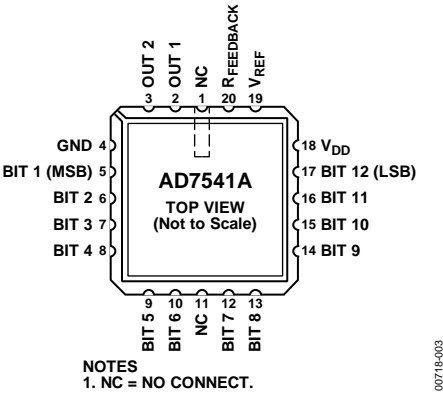*Figure 2. 18-Lead PDIP and 18-Lead SOIC Pin Configuration*



NOTES
1. NC = NO CONNECT.

*Figure 3. 20-Lead PLCC Pin Configuration*

# TERMINOLOGY

**Relative Accuracy**

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero scale and full scale, and it is expressed in % of full-scale range or (sub) multiples of 1 LSB.

**Differential Nonlinearity**

Differential nonlinearity is the difference between the measured change and the ideal l LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum over the operating temperature range ensures monotonicity.

**Gain Error**

Gain error is a measure of the output error between an ideal DAC and the actual device output. For the AD7541A, ideal maximum output is

$$-(4095/4096)(V_{REF})$$

Gain error is adjustable to zero using external trims, as shown in Figure 7, Figure 8, and Figure 9.

**Output Leakage Current**

Current that appears at OUT I with the DAC loaded to all 0s or at OUT 2 with the DAC loaded to all 1s.

**Multiplying Feedthrough Error**

AC error due to capacitive feedthrough from the $V_{REF}$ terminal to OUT 1 with the DAC loaded to all 0s.

**Output Current Settling Time**

Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, that is, 0 to full scale.

**Propagation Delay**

The propagation delay is a measure of the internal delay of the circuit, and it is measured from the time a digital input changes to the point at which the analog output at OUT 1 reaches 90% of its final value.

**Digital-to-Analog Glitch Impulse (QDA)**

The QDA is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nV-sec and is measured with $V_{REF}$ = GND and a Model 50K as the output op amp, C1 (phase compensation) = 0 pF.

# THEORY OF OPERATION

The simplified digital-to-analog circuit is shown in Figure 4. An inverted R-2R ladder structure was used, meaning the binarily weighted currents are switched between the OUT 1 and OUT 2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.
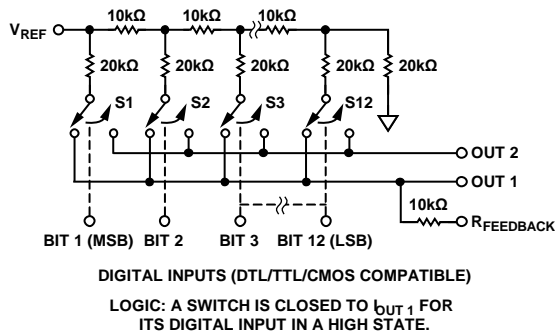


*Figure 4. Functional Diagram (Inputs High)*

The input resistance at $V_{REF}$ (see Figure 4) is always equal to $R_{LDR}$, which is the R-2R ladder characteristic resistance and is equal to value R. Because $R_{IN}$ at the $V_{REF}$ pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. If a current source is used, a low temperature coefficient external $R_{FEEDBACK}$ is recommended to define the scale factor.

## EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs low and all digital inputs high are shown in Figure 5 and Figure 6. In Figure 5 with all digital inputs low, the reference current is switched to OUT 2. The current source, $I_{LEAKAGE}$, is composed of surface and junction leakages to the substrate, while the $I/_{4096}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The on capacitance of the output N-channel switch is 200 pF, as shown on the OUT 2 terminal. The off switch capacitance is 70 pF, as shown on the OUT 1 terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 5, is similar to Figure 4; however, the on switches are now on the OUT 1 terminal; therefore, 200 pF at that terminal.
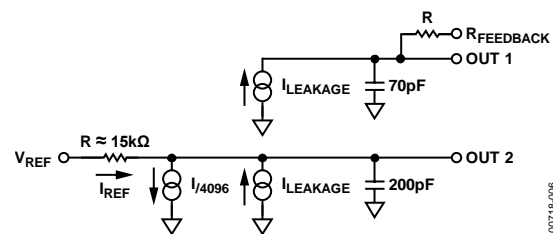


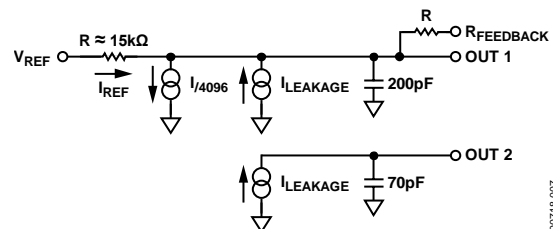*Figure 5. DAC Equivalent Circuit, All Digital Inputs Low*



*Figure 6. DAC Equivalent Circuit All Digital Inputs High*

# APPLICATIONS INFORMATION

## UNIPOLAR BINARY OPERATION (TWO QUADRANT MULTIPLICATION)

Figure 7 shows the analog circuit connections required for unipolar binary (two quadrant multiplication) operation. With a dc reference voltage or current (positive or negative polarity) applied at Pin 17, the circuit is a unipolar DAC. With an ac reference voltage or current, the circuit provides two quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table 5.
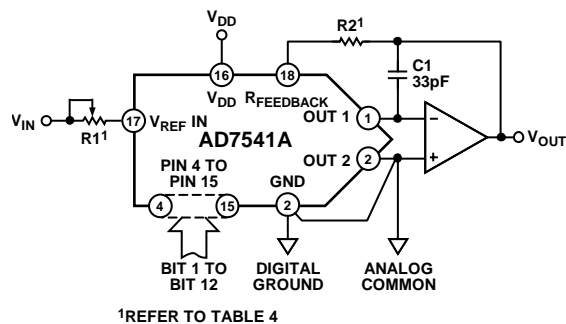


*Figure 7. Unipolar Binary Operation*

R1 provides full-scale trim capability (that is, load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)). Alternatively, full scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 pF to 25 pF) may be required for stability when using high speed amplifiers. C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT 1.

Amplifier A1 must be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at $V_{OUT}$. Additionally, the amplifier must exhibit a bias current that is low over the temperature range of interest (bias current causes output offset at $V_{OUT}$ equal to $I_B$ times the DAC feedback resistance, nominally 11 kΩ).

**Table 4. Recommended Trim Resistor Values vs. Grades**

| Trim Resistor | JN | KN |
|---|---|---|
| R1 | 100 Ω | 100 Ω |
| R2 | 47 Ω | 33 Ω |

**Table 5. Unipolar Binary Code Table for Circuit of Figure 7**

| Binary Number in DAC | | | Analog Output, $V_{OUT}$ |
|---|---|---|---|
| **MSB** | | **LSB** | |
| 1111 | 1111 | | $-V_{IN}(4095/4096)$ |
| 1000 | 0000 | 0000 | $-V_{IN}(2048/4096) = -1/2V_{IN}$ |
| 0000 | 0000 | 0001 | $-V_{IN}(1/4096)$ |
| 0000 | 0000 | 0000 | 0 V |

## BIPOLAR OPERATION (FOUR QUADRANT MULTIPLICATION)

Figure 8 and Table 6 illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity), the circuit provides offset binary operation. With an ac reference, the circuit provides full four quadrant multiplication.

With the DAC loaded to 1000 0000 0000, adjust R1 for $V_{OUT}$ = 0 V (alternatively, omit R1 and R2 and adjust the ratio of R3 to R4 for $V_{OUT}$ = 0 V). To accomplish, full-scale trimming, adjust the amplitude of $V_{REF}$ or vary the R5 value.

As in unipolar operation, A1 must be chosen for low $V_{OS}$ and low $I_B$. R3, R4, and R5 must be selected for matching and tracking. Mismatch of R3 to R4 causes both offset and full-scale error. Mismatch of R5 to R4 or R3 causes full-scale error. C1 phase compensation (10 pF to 50 pF) may be required for stability, depending on amplifier used.

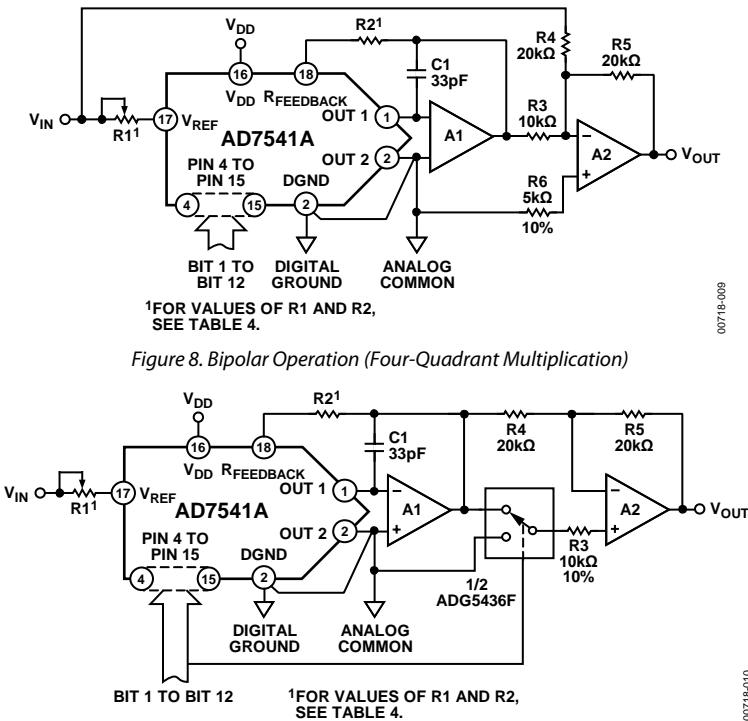**Table 6. Bipolar Code Table for Offset Binary Circuit of Figure 8**

| Binary Number in DAC | | | Analog Output, $V_{OUT}$ |
|---|---|---|---|
| **MSB** | | **LSB** | |
| 1 1 1 1 | 1 1 1 1 | 1 1 1 1 | $+V_{IN}(2047/2048)$ |
| 1 0 0 0 | 0 0 0 0 | 0 0 0 1 | $+V_{IN}(1/2048)$ |
| 1 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 V |
| 0 1 1 1 | 1 1 1 1 | 1 1 1 1 | $-V_{IN}(1/2048)$ |
| 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | $-V_{IN}(2048/2048)$ |

Figure 9 and Table 7 show an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage of giving 12-bit resolution in each quadrant, compared with 11-bit resolution per quadrant for the circuit of Figure 8. The ADG5436F is a dual SPDT, latch-up immune switch. R4 and R5 must match each other to 0.01% to maintain the accuracy of the DAC. Mismatch between R4 and R5 introduces a gain error.

**Table 7. 12-Bit Plus Sign Magnitude Code Table for Circuit of Figure 9**

| Sign Bit[1] | Binary Number in DAC | | | Analog Output, $V_{OUT}$ |
|---|---|---|---|---|
| | **MSB** | | **LSB** | |
| 0 | 1 1 1 1 | 1 1 1 1 | 1 1 1 1 | $+V_{IN} \times (4095/4096)$ |
| 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 V |
| 1 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 V |
| 1 | 1 1 1 1 | 1 1 1 1 | 1 1 1 1 | $-V_{IN} \times (4095/4096)$ |

[1] When the sign bit equals 0, it connects R3 to GND.



*Figure 8. Bipolar Operation (Four-Quadrant Multiplication)*



*Figure 9. 12-Bit Plus Sign Magnitude Operation*

## APPLICATIONS HINTS

### Output Offset

The CMOS DACs exhibit a code dependent, output resistance that can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the nonlinearity of the DAC, is 0.67 $V_{OS}$, where $V_{OS}$ is the amplifier input offset voltage. To maintain monotonic operation, it is recommended that $V_{OS}$ be no greater than $(25 \times 10^{-6}) \times V_{REF}$ over the temperature range of operation. Suitable op amps include the following: OP27, OP177, and OP777. The OP27 is best suited for fixed reference applications with low bandwidth requirements. The OP27 has extremely low offset (25 µV), and does not require an offset trim in most applications. The AD711 has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications that require fast settling.

### Digital Glitches

One cause of digital glitches is capacitive coupling from the digital lines to the OUT 1 and OUT 2 terminals. This coupling can be minimized by screening the analog pins of the AD7541A (Pin 1, Pin 2, Pin 17, and Pin 18) from the digital pins by a ground track run between Pin 2 and Pin 3 and between Pin 16 and Pin 17 of the AD7541A. Note how the analog pins are at one end of the package and are separated from the digital pins by $V_{DD}$ and GND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7541A, particularly in circuits with high currents and fast rise and fall times.

### Temperature Coefficients

The gain temperature coefficient of the AD7541A has a maximum value of 5 ppm/°C and a typical value of 2 ppm/°C. This coefficient corresponds to worst case gain shifts of 2 LSB and 0.8 LSB, respectively, over a 100°C temperature range. When trim resistors, R1 and R2, are used to adjust the full-scale range, the temperature coefficients of R1 and R2 must also be taken into account.

## SINGLE-SUPPLY OPERATION

Figure 10 shows the AD7541A connected in a voltage switching mode. OUT 1 is connected to the reference voltage, and OUT 2 is connected to GND. The output voltage of the DAC is available at the $V_{REF}$ pin (Pin 17) and has a constant output impedance equal to $R_{LDR}$. The feedback resistor, $R_{FEEDBACK}$, is not used in this circuit.



$V_{OUT} \pm V_{REF} D (1 + R2/R1)$ WHERE $0 \le D \le 1$, THAT IS, D IS A FRACTIONAL REPRESENTATION OF THE DIGITAL INPUT
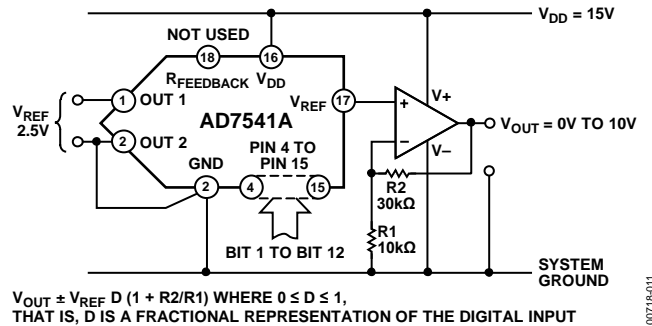
*Figure 10. Single Supply Operation Using Voltage Switching Mode*

The reference voltage must always be positive. If OUT 1 goes more than 0.3 V less than GND, an internal diode is turned on and a heavy current may flow, causing device damage (the AD7541A is protected from the SCR latch-up phenomenon prevalent in many CMOS devices). Suitable references include the ADR431, the ADR441, and the REF192.

The loading on the reference voltage source is code dependent, and the behavior of the reference voltage with changing load conditions often determines the response time of the circuit. To maintain linearity, the voltage at OUT 1 must remain within 2.5 V of GND for a $V_{DD}$ of 15 V. If $V_{DD}$ is reduced from 15 V, or if the reference voltage at OUT 1 is increased to more than 2.5 V, the differential nonlinearity of the DAC increases, and the linearity of the DAC degrades.
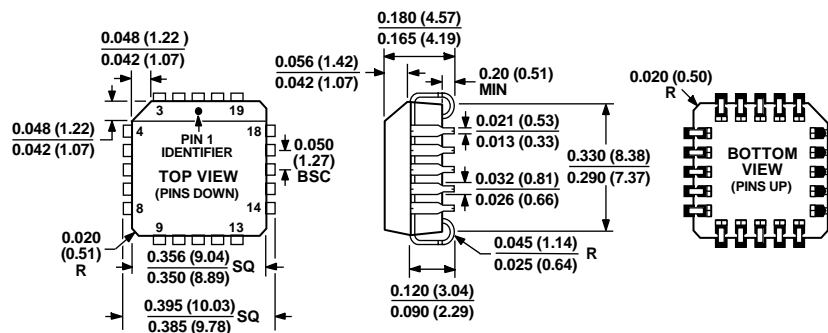
## SUPPLEMENTAL APPLICATION MATERIAL

For further information on CMOS multiplying DACs, refer to the following:

*Analog-Digital Conversion Handbook, 1972*, Analog Devices, Inc.

*CMOS DAC Application Guide, 1984*, Analog Devices

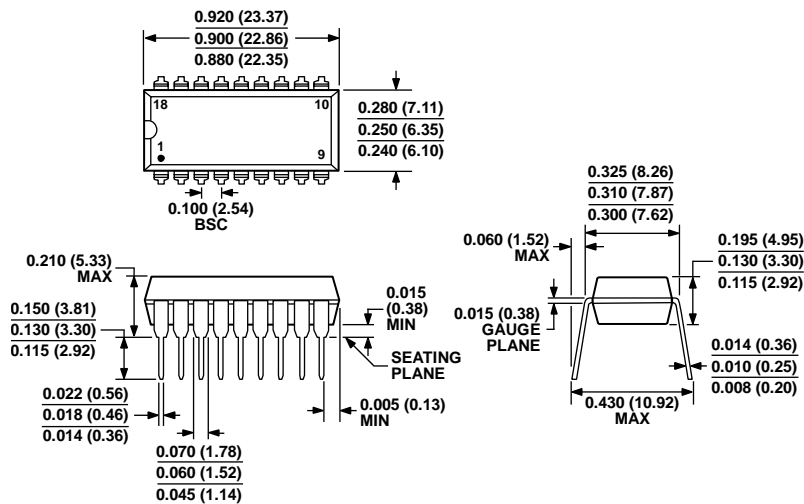*Analog-Digital Conversion Handbook, 1986*, Analog Devices

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-047-AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

*Figure 11. 20-Lead Plastic Leadless Chip Carrier [PLCC]*
*(P-20)*
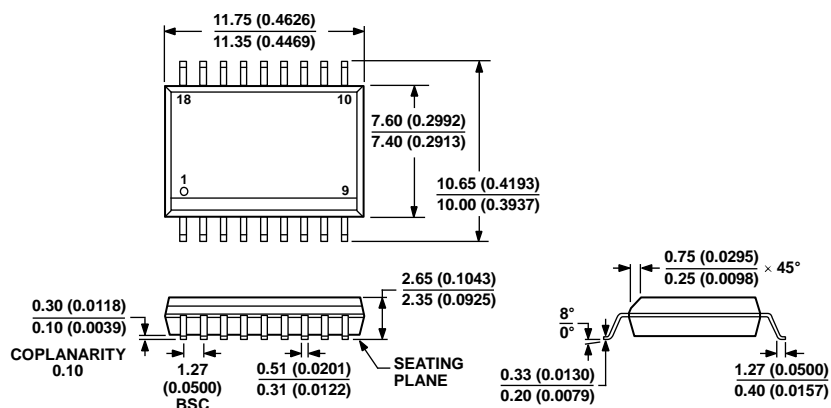*Dimensions shown in inches and (millimeters)*



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

*Figure 12. 18-Lead Plastic Dual In-Line Package [PDIP]*
*(N-18)*
*Dimensions shown in inches and (millimeters)*

COMPLIANT TO JEDEC STANDARDS MS-013-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

*Figure 13. 18-Lead Standard Small Outline Package [SOIC_W]*
*(RW-18)*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model[1] | Temperature Range | Relative Accuracy, $T_{MIN}$ to $T_{MAX}$ | Error, $T_A = 25°C$ | Package Description | Package Option |
|---|---|---|---|---|---|
| AD7541AJNZ | 0°C to +70°C | ±1 LSB | ±6 LSB | 18-Lead PDIP | N-18 |
| AD7541AKNZ | 0°C to +70°C | ±1/2 LSB | ±3 LSB | 18-Lead PDIP | N-18 |
| AD7541AJPZ-REEL | 0°C to +70°C | ±1 LSB | ±6 LSB | 20-Lead PLCC | P-20 |
| AD7541AKPZ-REEL | 0°C to +70°C | ±1/2 LSB | ±3 LSB | 20-Lead PLCC | P-20 |
| AD7541AKR | 0°C to +70°C | ±1/2 LSB | ±3 LSB | 18-Lead SOIC_W | RW-18 |
| AD7541AKRZ | 0°C to +70°C | ±1/2 LSB | ±3 LSB | 18-Lead SOIC_W | RW-18 |
| AD7541AKRZ-REEL | 0°C to +70°C | ±1/2 LSB | ±3 LSB | 18-Lead SOIC_W | RW-18 |
| AD7541AKRZ–REEL7 | 0°C to +70°C | ±1/2 LSB | ±3 LSB | 18-Lead SOIC_W | RW-18 |
| AD7541AACHIPS | | | | DIE | |

[1] Z = RoHS Compliant Part.

**ANALOG DEVICES**

www.analog.com