

74HC273-Q100; 74HCT273-Q100

Octal D-type flip-flop with reset; positive-edge trigger

Rev. 1 — 19 June 2013

Product data sheet

1. General description

The 74HC273-Q100; 74HCT273-Q100 is an octal positive-edge triggered D-type flip-flop. The device features clock (CP) and master reset (MR) inputs. The outputs Qn assume the state of their corresponding Dn inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A LOW on MR forces the outputs LOW independently of clock and data inputs. Inputs include clamp diodes which enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from -40°C to $+85^{\circ}\text{C}$ and from -40°C to $+125^{\circ}\text{C}$
- Input levels:
 - ◆ For 74HC273-Q100: CMOS level
 - ◆ For 74HCT273-Q100: TTL level
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V.
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74HC273D-Q100	-40°C to $+125^{\circ}\text{C}$	SO20	plastic small outline package; 20 leads; body width 7.5 mm		SOT163-1
74HCT273D-Q100					
74HC273PW-Q100	-40°C to $+125^{\circ}\text{C}$	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm		SOT360-1
74HCT273PW-Q100					
74HC273BQ-Q100	-40°C to $+125^{\circ}\text{C}$	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body $2.5 \times 4.5 \times 0.85$ mm		SOT764-1
74HCT273BQ-Q100					

nexperia

4. Functional diagram

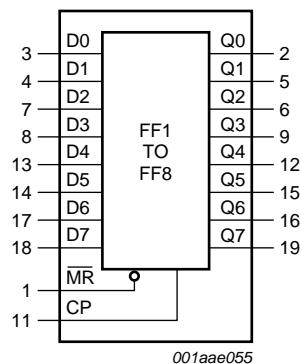


Fig 1. Functional diagram

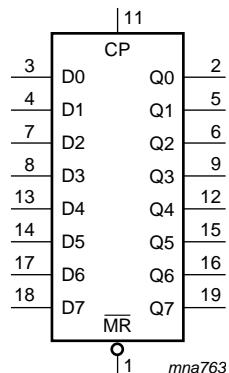


Fig 2. Logic symbol

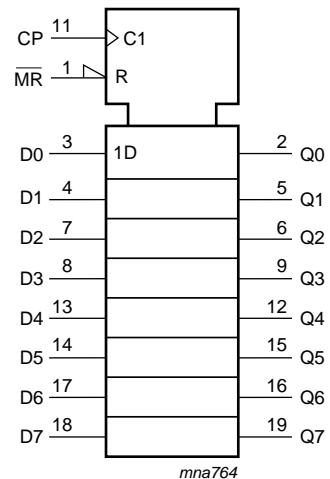


Fig 3. IEC logic symbol

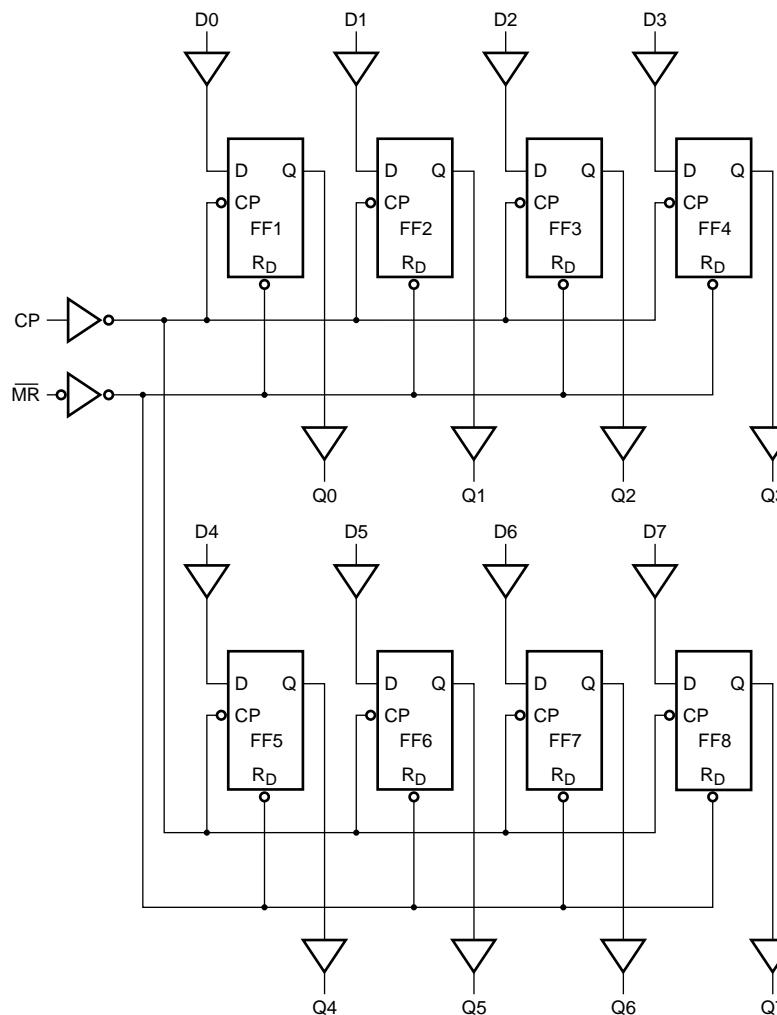


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

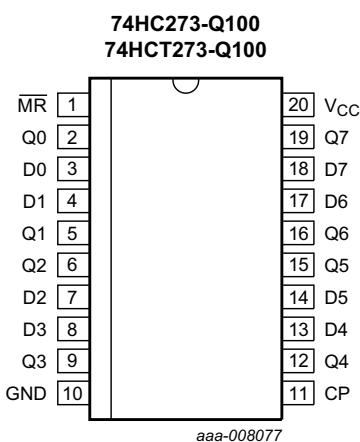


Fig 5. Pin configuration SO20 and TSSOP20

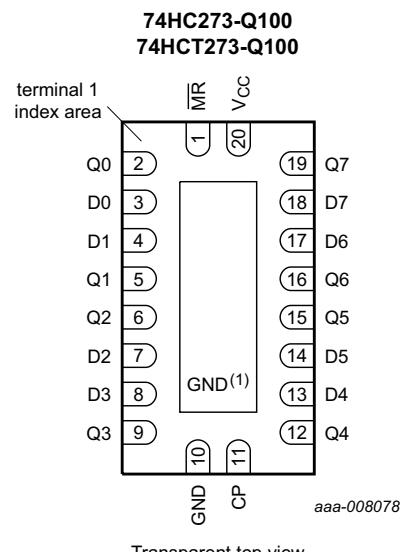


Fig 6. Pin configuration DHVQFN20

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
MR	1	master reset input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	flip-flop output
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data input
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge-triggered)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table^[1]

Operating modes	Inputs			Outputs
	MR	CP	Dn	
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	I	L

[1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 L = LOW voltage level;
 I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 X = don't care;
 ↑ = LOW-to-HIGH clock transition.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	^[1] -	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	^[1] -	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] For SO20 package: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For TSSOP20 package: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN20 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC273-Q100			74HCT273-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC273-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = −20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = −4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = −5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT273-Q100										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = -20 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
V_{OL}	LOW-level output voltage	$I_O = -4.0 \text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
		$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = 20 \mu\text{A}$; $V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
I_I	input leakage current	$I_O = 5.2 \text{ mA}$; $V_{CC} = 5.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	± 0.1	-	± 1	-	± 1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 5.5 \text{ V}$	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		MR input	-	100	360	-	450	-	490	μA
		CP input	-	175	630	-	787.5	-	857.5	μA
		Dn input	-	15	54	-	67.5	-	73.5	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit, see [Figure 10](#)

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC273-Q100										
t_{pd}	propagation delay	CP to Qn; see Figure 7 [1]								
		$V_{CC} = 2.0 \text{ V}$	-	41	150	-	185	-	225	ns
		$V_{CC} = 4.5 \text{ V}$	-	15	30	-	37	-	45	ns
		$V_{CC} = 5.0 \text{ V}$; $C_L = 15 \text{ pF}$	-	15	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	13	26	-	31	-	38	ns

Table 7. Dynamic characteristics ...continued

GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit, see [Figure 10](#)

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Figure 8								
		$V_{CC} = 2.0 \text{ V}$	-	44	150	-	185	-	225	ns
		$V_{CC} = 4.5 \text{ V}$	-	16	30	-	37	-	45	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	15	-	-	-	-	-	ns
t_t	transition time	Qn output; see Figure 7 [2]								
		$V_{CC} = 2.0 \text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0 \text{ V}$	-	6	13	-	15	-	19	ns
t_w	pulse width	CP input HIGH or LOW; see Figure 7								
		$V_{CC} = 2.0 \text{ V}$	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$	14	4	-	17	-	20	-	ns
		MR input LOW; see Figure 8								
		$V_{CC} = 2.0 \text{ V}$	60	17	-	75	-	90	-	ns
		$V_{CC} = 4.5 \text{ V}$	12	6	-	15	-	18	-	ns
		$V_{CC} = 6.0 \text{ V}$	10	5	-	13	-	15	-	ns
t_{rec}	recovery time	MR to CP; see Figure 8								
		$V_{CC} = 2.0 \text{ V}$	50	-6	-	65	-	75	-	ns
		$V_{CC} = 4.5 \text{ V}$	10	-2	-	13	-	15	-	ns
		$V_{CC} = 6.0 \text{ V}$	9	-2	-	11	-	13	-	ns
t_{su}	set-up time	Dn to CP; see Figure 9								
		$V_{CC} = 2.0 \text{ V}$	60	11	-	75	-	90	-	ns
		$V_{CC} = 4.5 \text{ V}$	12	4	-	15	-	18	-	ns
		$V_{CC} = 6.0 \text{ V}$	10	3	-	13	-	15	-	ns
t_h	hold time	Dn to CP; see Figure 9								
		$V_{CC} = 2.0 \text{ V}$	3	-6	-	3	-	3	-	ns
		$V_{CC} = 4.5 \text{ V}$	3	-2	-	3	-	3	-	ns
		$V_{CC} = 6.0 \text{ V}$	3	-2	-	3	-	3	-	ns
f_{max}	maximum frequency	CP input; see Figure 7								
		$V_{CC} = 2.0 \text{ V}$	6	20.6	-	4.8	-	4	-	MHz
		$V_{CC} = 4.5 \text{ V}$	30	103	-	24	-	20	-	MHz
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	66	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	per package; $V_I = \text{GND to } V_{CC}$	[3]	-	20	-	-	-	-	pF

Table 7. Dynamic characteristics ...continued

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see [Figure 10](#)

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT273-Q100										
t_{pd}	propagation delay	CP to Qn; see Figure 7 [1]								
		$V_{CC} = 4.5$ V	-	16	30	-	38	-	45	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Figure 8								
		$V_{CC} = 4.5$ V	-	23	34	-	43	-	51	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	20	-	-	-	-	-	ns
t_t	transition time	Qn output; see Figure 7 [2]								
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
t_w	pulse width	CP input; see Figure 7								
		$V_{CC} = 4.5$ V	16	9	-	20	-	24	-	ns
		MR input LOW; see Figure 8								
		$V_{CC} = 4.5$ V	16	8	-	20	-	24	-	ns
t_{rec}	recovery time	MR to CP; see Figure 8								
		$V_{CC} = 4.5$ V	10	−2	-	13	-	15	-	ns
t_{su}	set-up time	Dn to CP; see Figure 9								
		$V_{CC} = 4.5$ V	12	5	-	15	-	18	-	ns
t_h	hold time	Dn to CP; see Figure 9								
		$V_{CC} = 4.5$ V	3	−4	-	3	-	3	-	ns
f_{max}	maximum frequency	CP input; see Figure 7								
		$V_{CC} = 4.5$ V	30	56	-	24	-	20	-	MHz
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	36	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	per package; $V_I = \text{GND to } V_{CC} - 1.5$ V [3]	-	23	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .[2] t_t is the same as t_{THL} and t_{TLH} .[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

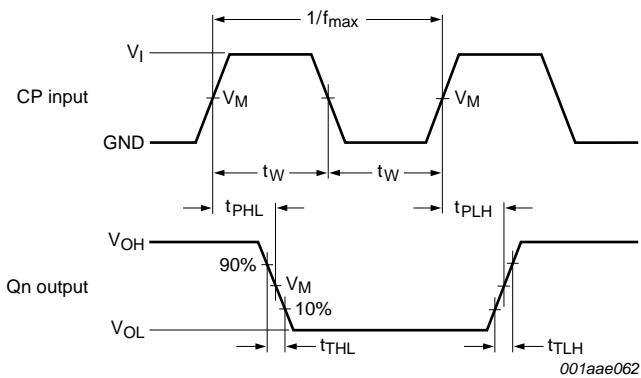
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 f_i = input frequency in MHz; f_o = output frequency in MHz;

$$\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs;}$$

 C_L = output load capacitance in pF; V_{CC} = supply voltage in V.

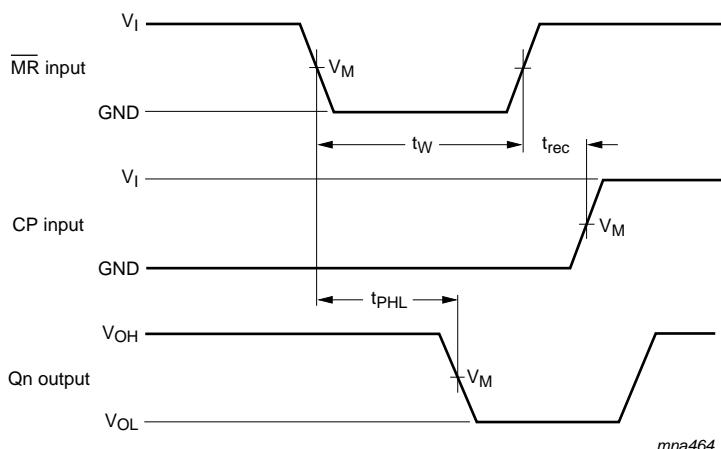
11. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

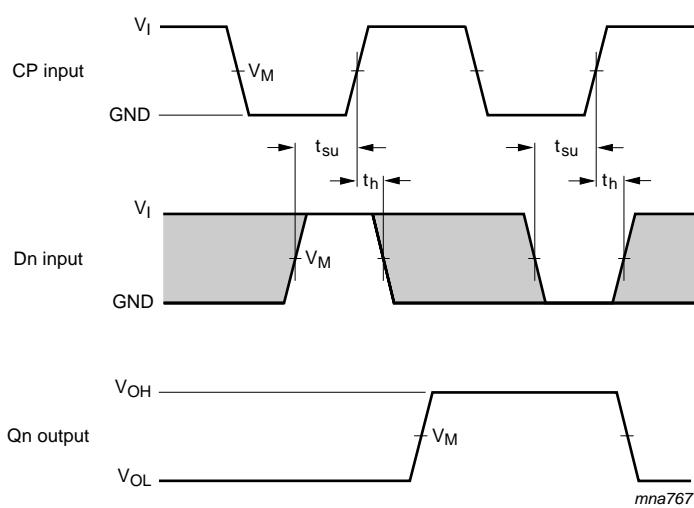
Fig 7. Propagation delay clock input (CP) to output (Qn), clock (CP) pulse width, output transition time and the maximum clock pulse frequency



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Propagation delay master reset (MR) to output (Qn), pulse width master reset (MR) and recovery time master reset (MR) to clock (CP)



Measurement points are given in [Table 8](#).

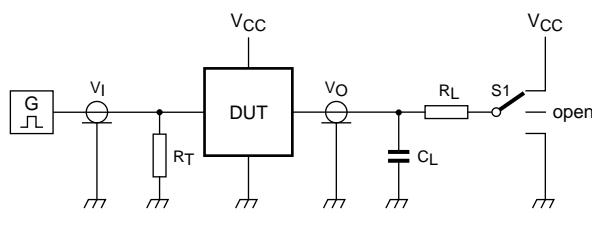
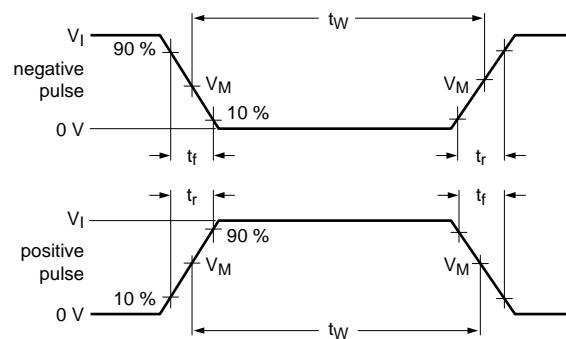
The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Data set-up and hold times data input (Dn)

Table 8. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC273-Q100	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
74HCT273-Q100	3 V	1.3 V	1.3 V



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Test data is given in [Table 9](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

$S1$ = Test selection switch

Fig 10. Test circuit for measuring switching times

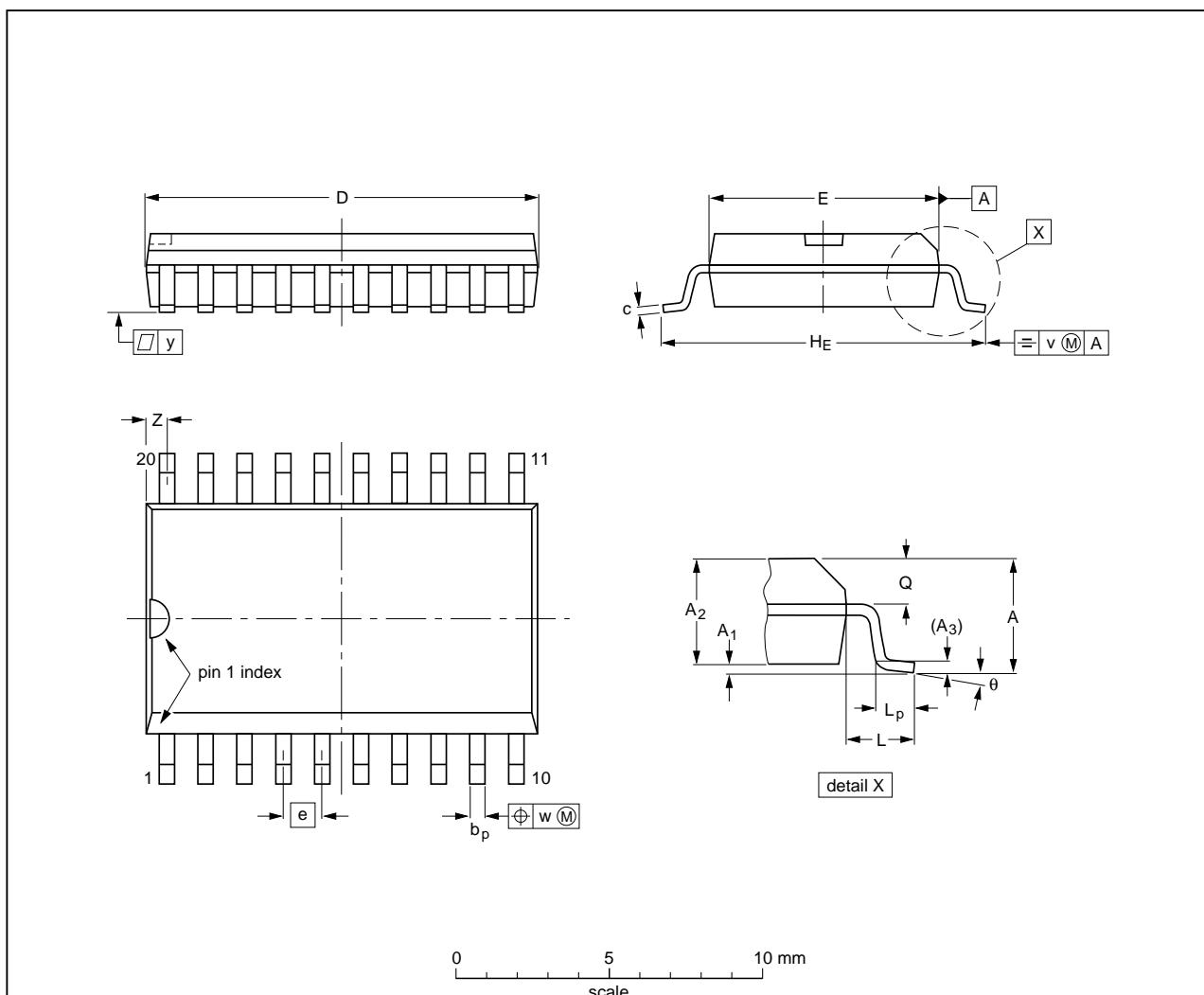
Table 9. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	
74HC273-Q100	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open
74HCT273-Q100	3 V	6 ns	15 pF, 50 pF	1 k Ω	open

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65 0.1	0.3 2.25	2.45	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0° 0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT163-1	075E04	MS-013			99-12-27 03-02-19

Fig 11. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

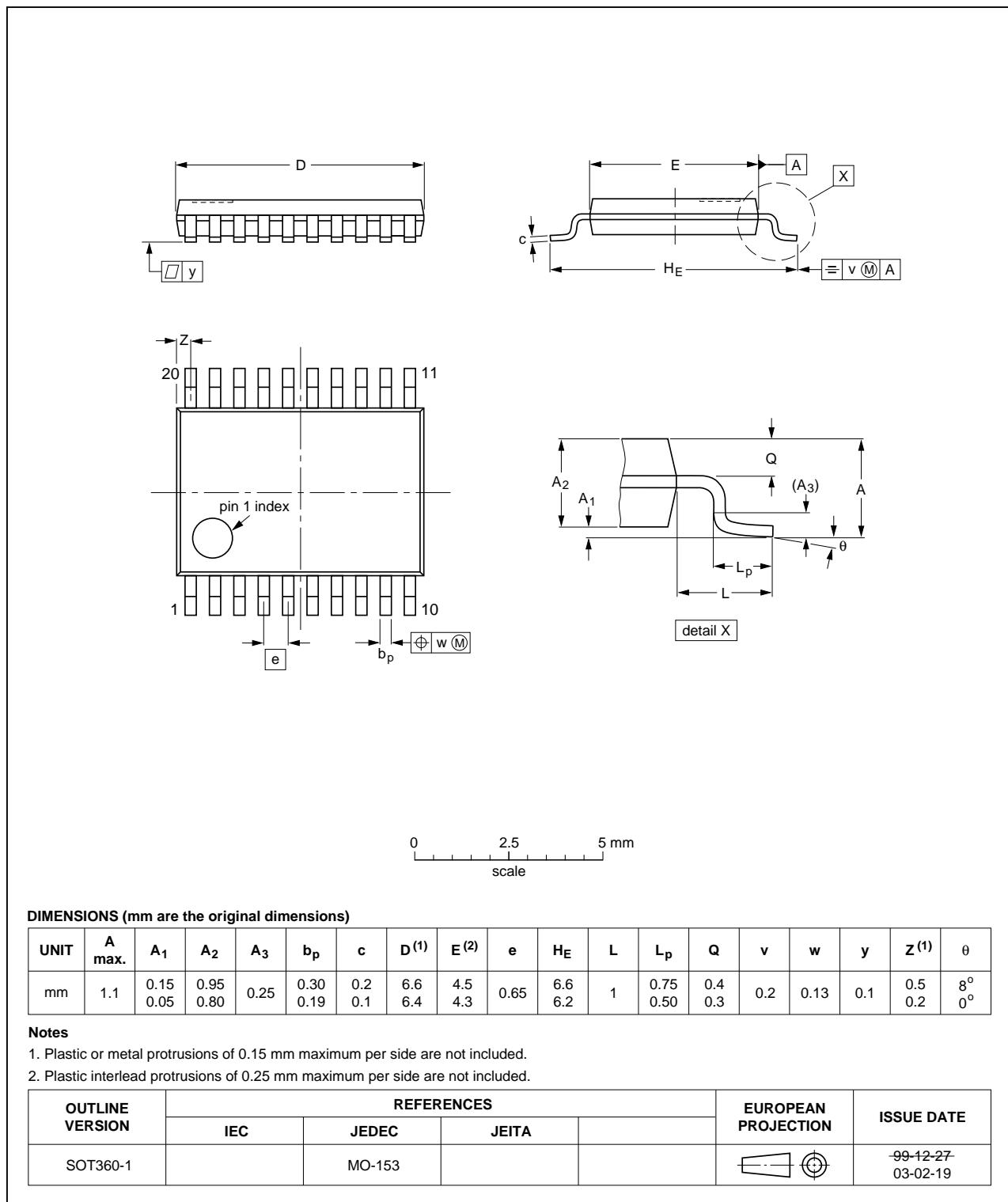


Fig 12. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

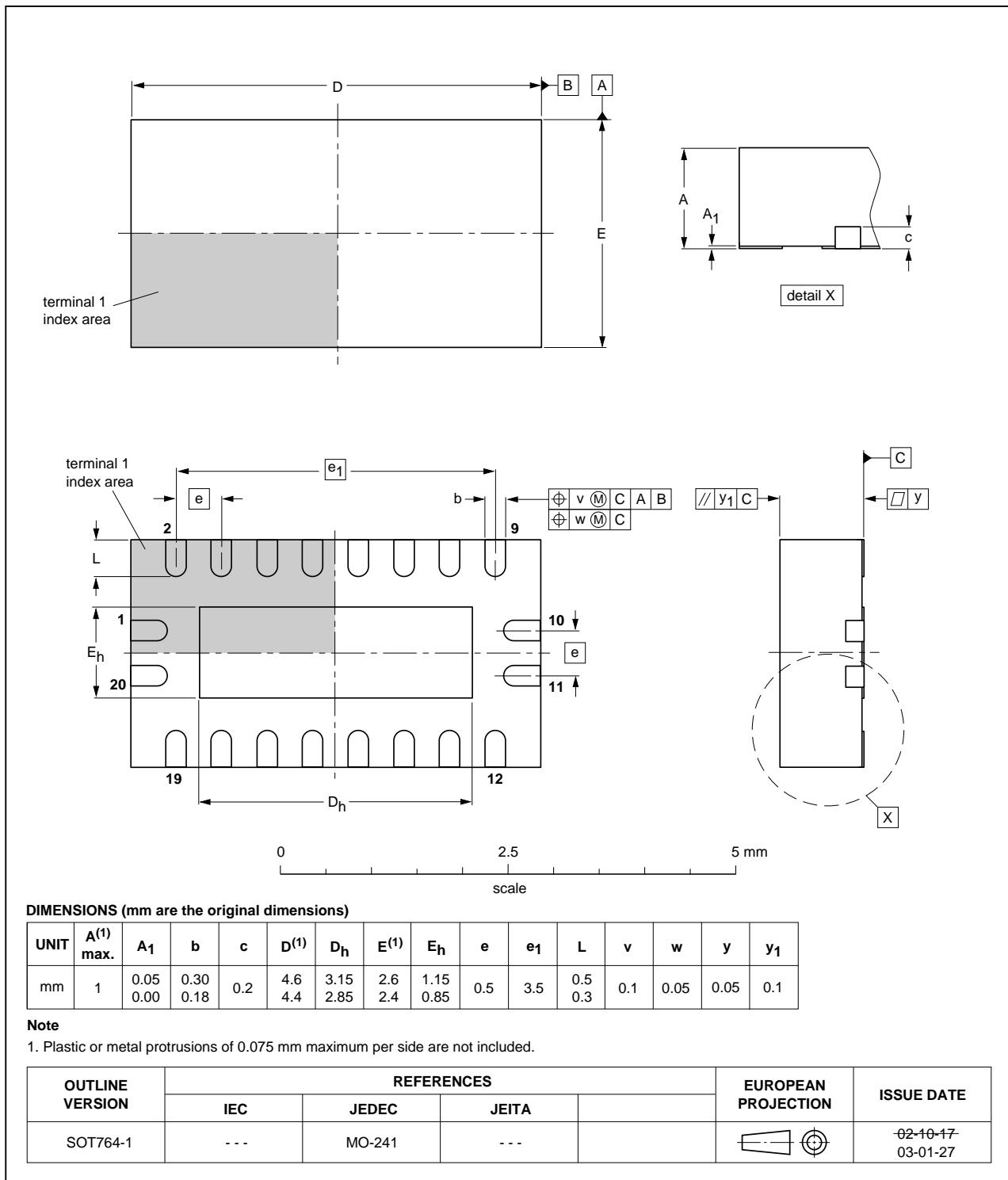


Fig 13. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT273_Q100 v.1	20130619	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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