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Renesas Electronics Corporation

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1. Overview

1.1 Features

The R8C/2H Group and R8C/2J Group of single-chip MCUs incorporate the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

1.1.1 Applications

Electric power meters, electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

1.1.2 Specifications

Table 1.1 outlines the Specifications for R8C/2H Group and Table 1.2 outlines the Specifications for R8C/2J Group.

Table 1.1 Specifications for R8C/2H Group

| Item | Function | Specification |
|------------------------------------|---------------------------|--|
| CPU | Central processing unit | R8C/Tiny series core <ul style="list-style-type: none"> • Number of fundamental instructions: 89 • Minimum instruction execution time: <ul style="list-style-type: none"> 125 ns (System clock = 8 MHz, VCC = 2.7 to 5.5 V) 250 ns (System clock = 4 MHz, VCC = 2.2 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM | Refer to Table 1.3 Product List for R8C/2H Group . |
| Power Supply Voltage Detection | Voltage detection circuit | <ul style="list-style-type: none"> • Power-on reset • Voltage detection 3 |
| Comparator | | <ul style="list-style-type: none"> • 2 circuits (shared with voltage monitor 1 and voltage monitor 2) • External reference voltage input is available |
| I/O Ports | | <ul style="list-style-type: none"> • Output-only: 1 • CMOS I/O ports: 15, selectable pull-up resistor |
| Clock | Clock generation circuits | <ul style="list-style-type: none"> • 2 circuits: On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function), XCIN clock oscillation circuit (32 kHz) • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: <ul style="list-style-type: none"> Standard operating mode (low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| | | Real-time clock (timer RE) |
| Interrupts | | <ul style="list-style-type: none"> • External: 3 sources, Internal: 17 sources, Software: 4 sources • Priority levels: 7 levels |
| Watchdog Timer | | 15 bits × 1 (with prescaler), reset start selectable |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RE | 8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode |
| | Timer RF | 16 bits × 1 (with capture/compare register pin and compare register pin) Input capture mode, output compare mode |
| Serial Interface | UART0, UART2 | Clock synchronous serial I/O/UART × 2 |
| LIN Module | | Hardware LIN: 1 (timer RA, UART0) |
| Flash Memory | | <ul style="list-style-type: none"> • Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function |
| Operating Frequency/Supply Voltage | | System clock = 8 MHz (VCC = 2.7 to 5.5 V) System clock = 4 MHz (VCC = 2.2 to 5.5 V) |
| Current consumption | | 5 mA (VCC = 5 V, system clock = 8 MHz) 23 μA (VCC = 3 V, wait mode (low-speed on-chip oscillator on)) 0.7 μA (VCC = 3 V, stop mode, BGR trimming circuit disabled) |
| Operating Ambient Temperature | | -20 to 85°C (N version) -40 to 85°C (D version) ⁽¹⁾ |
| Package | | 20-pin LSSOP Package code: PLSP0020JB-A (previous code: 20P2F-A) |

NOTE:

1. Specify the D version if D version functions are to be used.

Table 1.2 Specifications for R8C/2J Group

| Item | Function | Specification |
|------------------------------------|---------------------------|--|
| CPU | Central processing unit | R8C/Tiny series core <ul style="list-style-type: none"> • Number of fundamental instructions: 89 • Minimum instruction execution time: <ul style="list-style-type: none"> 125 ns (System clock = 8 MHz, VCC = 2.7 to 5.5 V) 250 ns (System clock = 4 MHz, VCC = 2.2 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM | Refer to Table 1.4 Product List for R8C/2J Group . |
| Power Supply Voltage Detection | Voltage detection circuit | <ul style="list-style-type: none"> • Power-on reset • Voltage detection 3 |
| Comparator | | <ul style="list-style-type: none"> • 2 circuits (shared with voltage monitor 1 and voltage monitor 2) • External reference voltage input is available |
| I/O Ports | | CMOS I/O ports: 12, selectable pull-up resistor |
| Clock | Clock generation circuits | <ul style="list-style-type: none"> • 1 circuits: On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function), • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: <ul style="list-style-type: none"> Standard operating mode (high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | <ul style="list-style-type: none"> • External: 3 sources, Internal: 14 sources, Software: 4 sources • Priority levels: 7 levels |
| Watchdog Timer | | 15 bits × 1 (with prescaler), reset start selectable |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RE | Not implemented |
| | Timer RF | 16 bits × 1 (with capture/compare register pin and compare register pin) Input capture mode, output compare mode |
| Serial Interface | UART0 | Clock synchronous serial I/O/UART × 1 |
| LIN Module | | Hardware LIN: 1 (timer RA, UART0) |
| Flash Memory | | <ul style="list-style-type: none"> • Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function |
| Operating Frequency/Supply Voltage | | System clock = 8 MHz (VCC = 2.7 to 5.5 V) System clock = 4 MHz (VCC = 2.2 to 5.5 V) |
| Current consumption | | 5 mA (VCC = 5 V, system clock = 8 MHz) 23 μA (VCC = 3 V, wait mode (low-speed on-chip oscillator on)) 0.7 μA (VCC = 3 V, stop mode, BGR trimming circuit disabled) |
| Operating Ambient Temperature | | -20 to 85°C (N version) -40 to 85°C (D version) ⁽¹⁾ |
| Package | | 20-pin LSSOP Package code: PLSP0020JB-A (previous code: 20P2F-A) |

NOTE:

1. Specify the D version if D version functions are to be used.

1.2 Product List

Table 1.3 lists Product List for R8C/2H Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2H Group. Table 1.4 lists Product List for R8C/2J Group, Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2J Group.

Table 1.3 Product List for R8C/2H Group

Current of Mar. 2008

| Part No. | ROM Capacity | RAM Capacity | Package Type | Remarks |
|--------------|--------------|--------------|--------------|-----------|
| R5F212H1SNSP | 4 Kbytes | 256 bytes | PLSP0020JB-A | N version |
| R5F212H2SNSP | 8 Kbytes | 384 bytes | PLSP0020JB-A | |
| R5F212H1SDSP | 4 Kbytes | 256 bytes | PLSP0020JB-A | D version |
| R5F212H2SDSP | 8 Kbytes | 384 bytes | PLSP0020JB-A | |

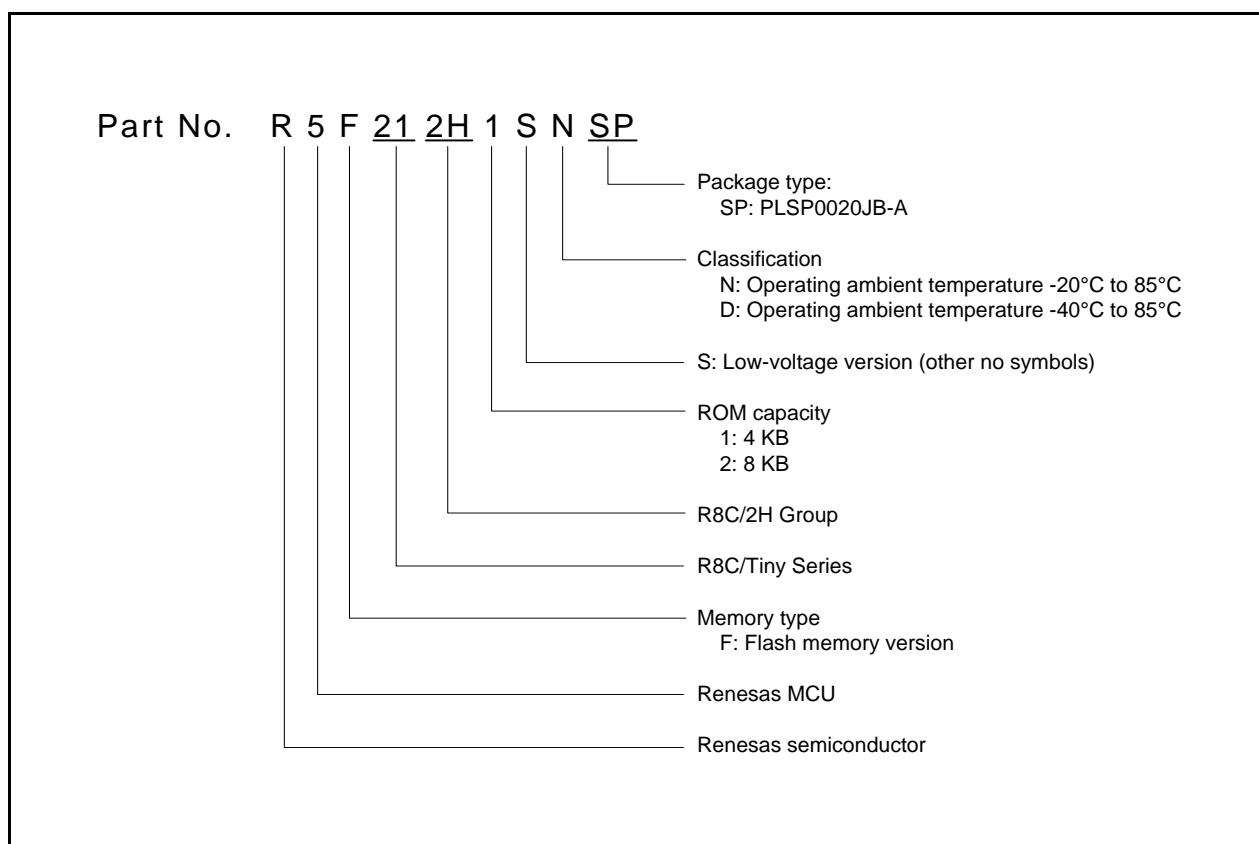
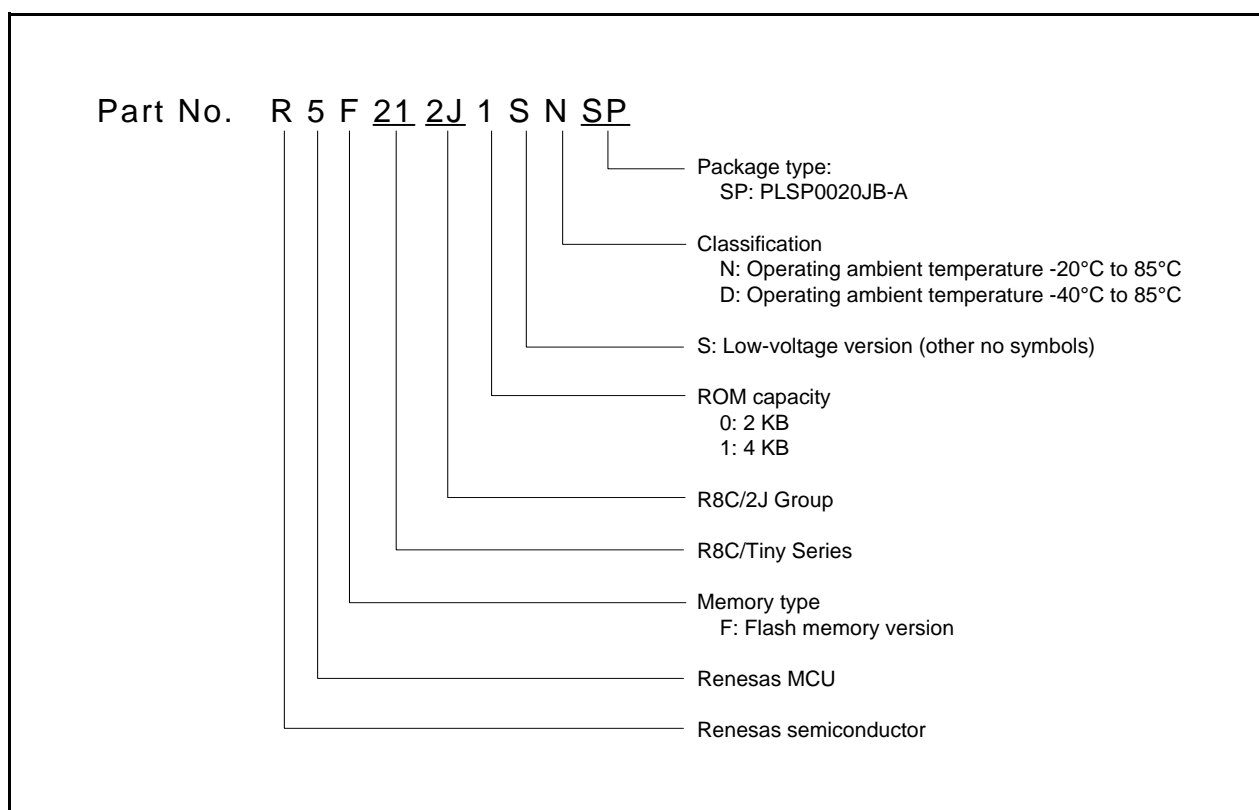


Figure 1.1 Part Number, Memory Size, and Package of R8C/2H Group

Table 1.4 Product List for R8C/2J Group**Current of Mar. 2008**

| Part No. | ROM Capacity | RAM Capacity | Package Type | Remarks |
|--------------|--------------|--------------|--------------|-----------|
| R5F212J0SNSP | 2 Kbytes | 256 bytes | PLSP0020JB-A | N version |
| R5F212J1SNSP | 4 Kbytes | 384 bytes | PLSP0020JB-A | |
| R5F212J0SDSP | 2 Kbytes | 256 bytes | PLSP0020JB-A | D version |
| R5F212J1SDSP | 4 Kbytes | 384 bytes | PLSP0020JB-A | |

**Figure 1.2 Part Number, Memory Size, and Package of R8C/2J Group**

1.3 Block Diagram

Figure 1.3 shows a Block Diagram of R8C/2H Group and Figure 1.4 shows a Block Diagram of R8C/2J Group.

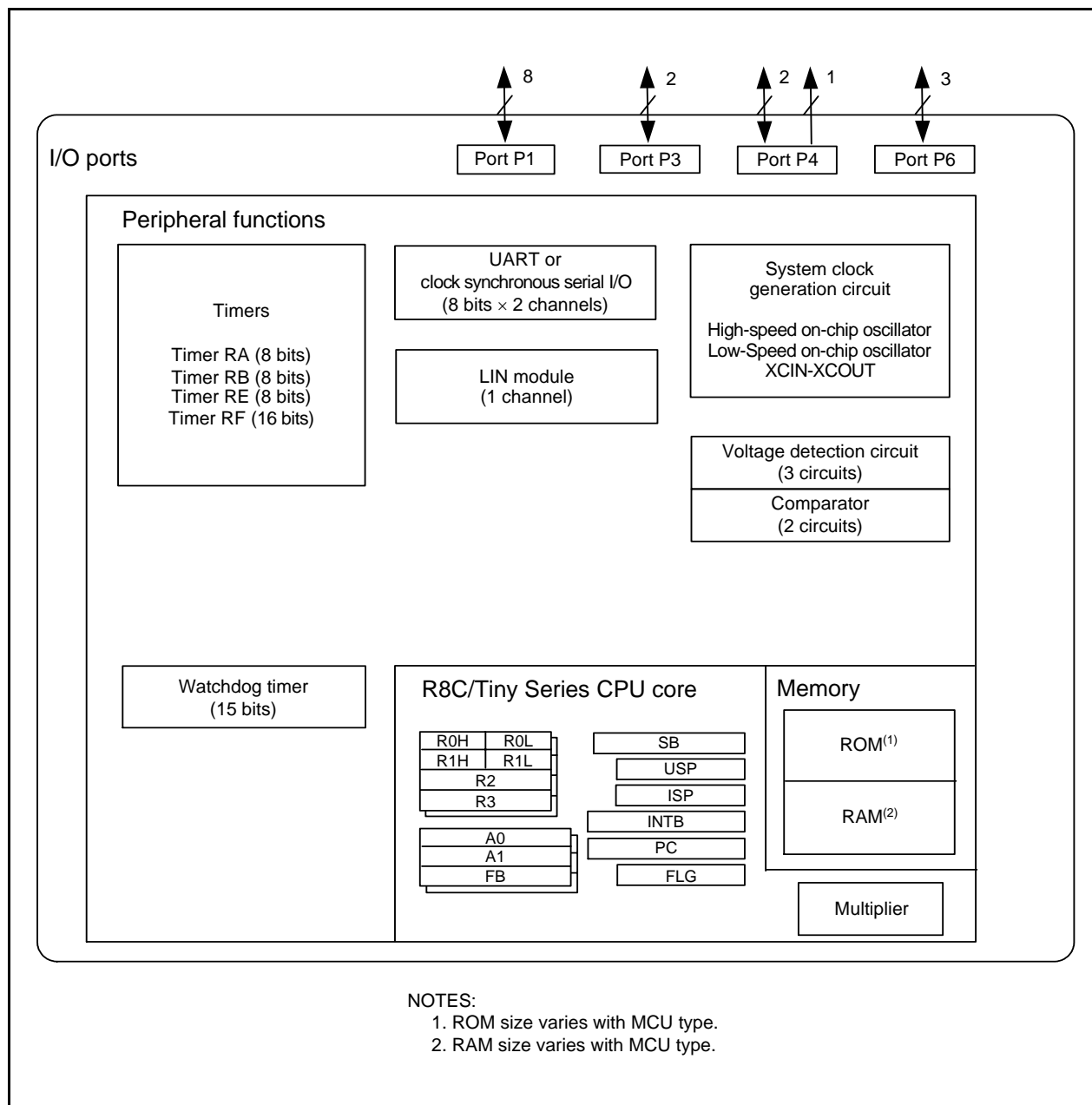


Figure 1.3 Block Diagram of R8C/2H Group

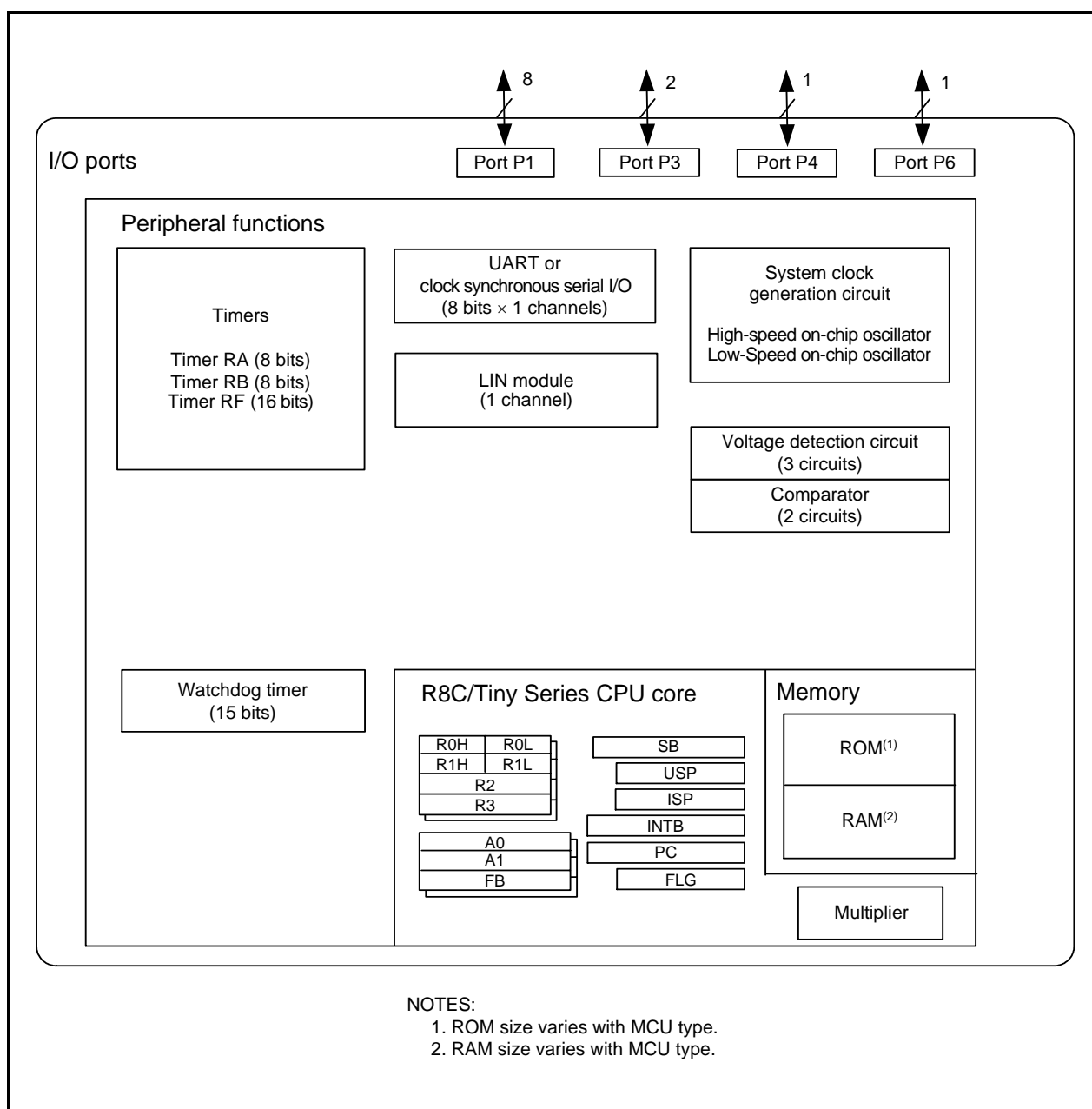


Figure 1.4 Block Diagram of R8C/2J Group

1.4 Pin Assignment

Figure 1.5 shows Pin Assignment (Top View) of R8C/2H Group. Table 1.5 outlines the Pin Name Information by Pin Number of R8C/2H Group.

Figure 1.6 shows Pin Assignment (Top View) of R8C/2J Group. Table 1.6 outlines the Pin Name Information by Pin Number of R8C/2J Group.

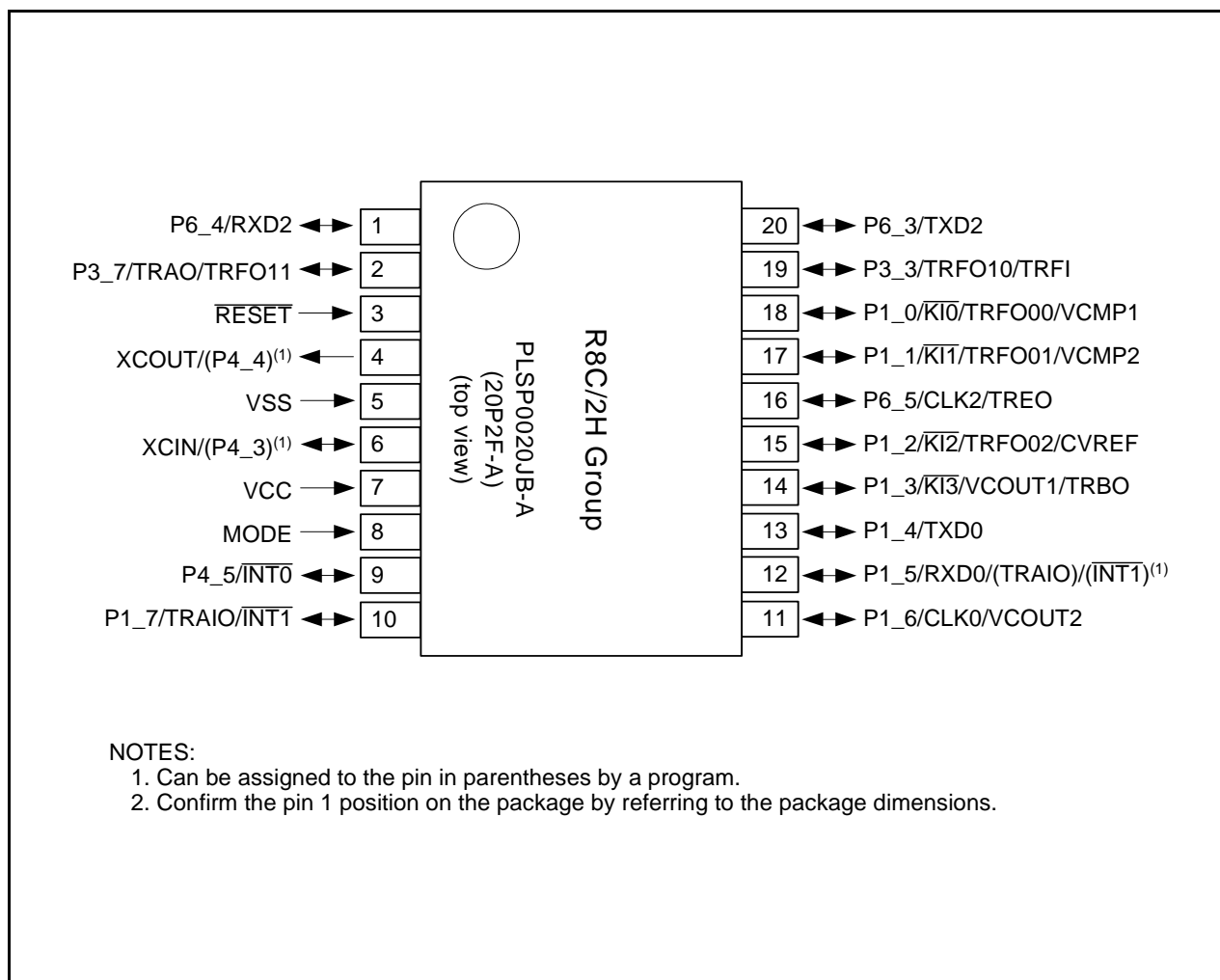


Figure 1.5 Pin Assignment (Top View) of R8C/2H Group

Table 1.5 Pin Name Information by Pin Number of R8C/2H Group

| Pin Number | Control Pin | Port | I/O Pin Functions for of Peripheral Modules | | | |
|------------|-------------|--------|---|------------------------|------------------|------------|
| | | | Interrupt | Timer | Serial Interface | Comparator |
| 1 | | P6_4 | | | RXD2 | |
| 2 | | P3_7 | | TRAO/TRFO11 | | |
| 3 | RESET | | | | | |
| 4 | XCOUT | (P4_4) | | | | |
| 5 | VSS | | | | | |
| 6 | XCIN | (P4_3) | | | | |
| 7 | VCC | | | | | |
| 8 | MODE | | | | | |
| 9 | | P4_5 | INT0 | | | |
| 10 | | P1_7 | INT1 | TRAIO | | |
| 11 | | P1_6 | | | CLK0 | VCOUT2 |
| 12 | | P1_5 | (INT1) ⁽¹⁾ | (TRAIO) ⁽¹⁾ | RXD0 | |
| 13 | | P1_4 | | | TXD0 | |
| 14 | | P1_3 | KI3 | TRBO | | VCOUT1 |
| 15 | | P1_2 | KI2 | TRFO02 | | CVREF |
| 16 | | P6_5 | | TREO | CLK2 | |
| 17 | | P1_1 | KI1 | TRFO01 | | VCMP2 |
| 18 | | P1_0 | KI0 | TRFO00 | | VCMP1 |
| 19 | | P3_3 | | TRFO10/TRFI | | |
| 20 | | P6_3 | | | TXD2 | |

NOTE:

1. Can be assigned to the pin in parentheses by a program.

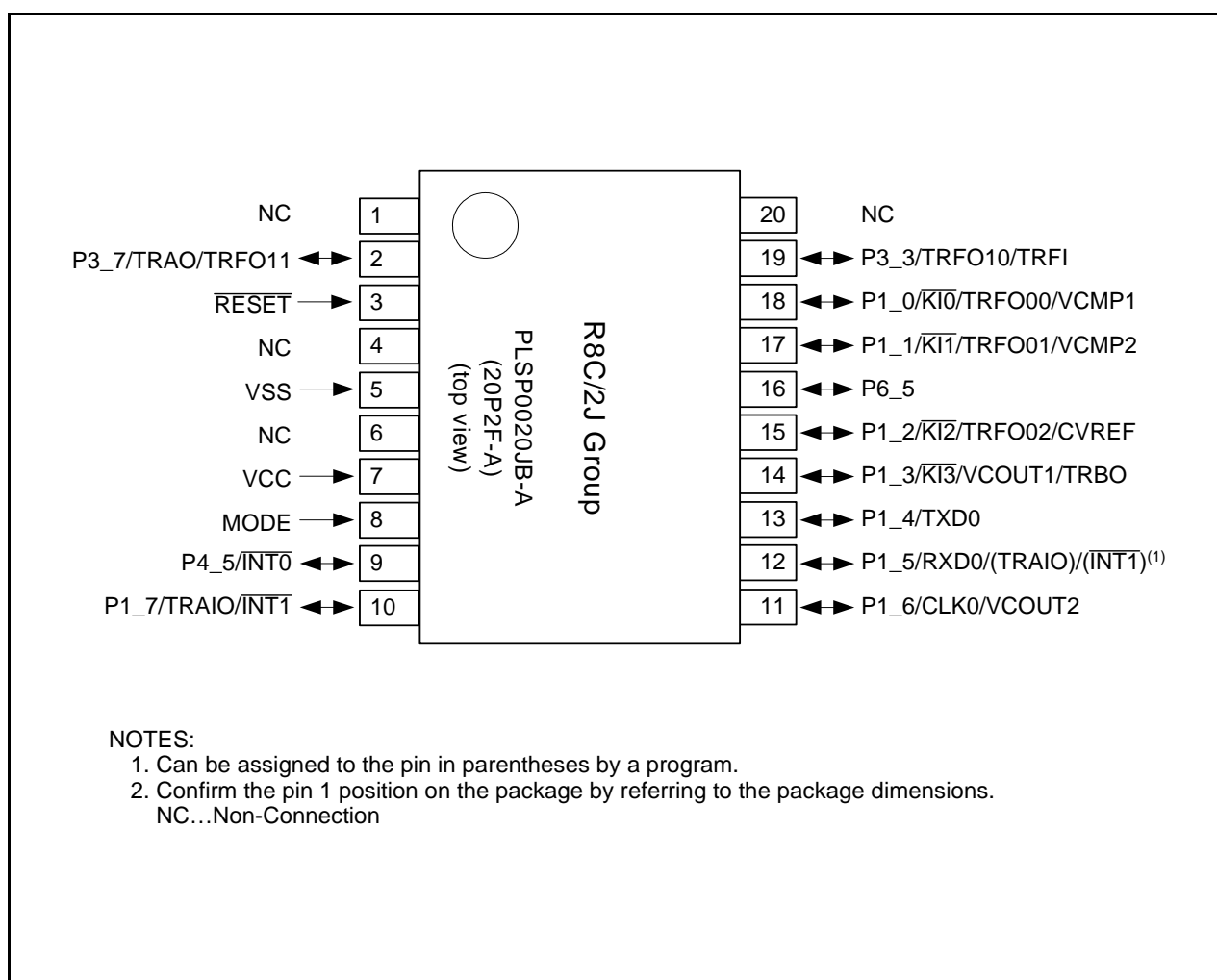


Figure 1.6 Pin Assignment (Top View) of R8C/2J Group

Table 1.6 Pin Name Information by Pin Number of R8C/2J Group

| Pin Number | Control Pin | Port | I/O Pin Functions for of Peripheral Modules | | | |
|------------|-------------------|------|---|------------------------|------------------|------------|
| | | | Interrupt | Timer | Serial Interface | Comparator |
| 1 | NC ⁽²⁾ | | | | | |
| 2 | | P3_7 | | TRAO/TRFO11 | | |
| 3 | RESET | | | | | |
| 4 | NC ⁽²⁾ | | | | | |
| 5 | VSS | | | | | |
| 6 | NC ⁽²⁾ | | | | | |
| 7 | VCC | | | | | |
| 8 | MODE | | | | | |
| 9 | | P4_5 | INT0 | | | |
| 10 | | P1_7 | INT1 | TRAIO | | |
| 11 | | P1_6 | | | CLK0 | VCOUT2 |
| 12 | | P1_5 | (INT1) ⁽¹⁾ | (TRAIO) ⁽¹⁾ | RXD0 | |
| 13 | | P1_4 | | | TXD0 | |
| 14 | | P1_3 | KI3 | TRBO | | VCOUT1 |
| 15 | | P1_2 | KI2 | TRFO02 | | CVREF |
| 16 | | P6_5 | | | | |
| 17 | | P1_1 | KI1 | TRFO01 | | VCMP2 |
| 18 | | P1_0 | KI0 | TRFO00 | | VCMP1 |
| 19 | | P3_3 | | TRFO10/TRFI | | |
| 20 | NC ⁽²⁾ | | | | | |

NOTES:

1. Can be assigned to the pin in parentheses by a program.
2. NC(Non-Connection)

1.5 Pin Functions

Table 1.7 lists Pin Functions of R8C/2H Group and Table 1.8 lists Pin Functions of R8C/2J Group.

Table 1.7 Pin Functions of R8C/2H Group

| Type | Symbol | I/O Type | Description |
|---|---|----------|---|
| Power supply input | VCC, VSS | — | Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin. |
| Reset input | $\overline{\text{RESET}}$ | I | Input "L" on this pin resets the MCU. |
| MODE | MODE | I | Connect this pin to VCC via a resistor. |
| XCIN clock input | XCIN | I | These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins. ⁽¹⁾ To use an external clock, input it to the XCIN pin and leave the XCOUT pin open. |
| XCIN clock output | XCOUT | O | |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}, \overline{\text{INT1}}$ | I | $\overline{\text{INT}}$ interrupt input pins |
| Key input interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Key input interrupt input pins |
| Timer RA | TRAIO | I/O | Timer RA I/O pin |
| | TRA0 | O | Timer RA output pin |
| Timer RB | TRBO | O | Timer RB output pin |
| Timer RE | TREO | O | Divided clock output pin |
| Timer RF | TRFI | I | Timer RF input pin |
| | TRFO00 to TRFO02, TRFO10 to TRFO11 | O | Timer RF output pins |
| Serial interface | CLK0, CLK2 | I/O | Clock I/O pin |
| | RXD0, RXD2 | I | Serial data input pin |
| | TXD0, TXD2 | O | Serial data output pin |
| Comparator | VCMP1, VCMP2 | I | Analog input pins to comparator |
| | CVREF | I | Reference voltage input pin to comparator |
| | VCOUT1, VCOUT2 | O | Comparator output pins |
| I/O port | P1_0 to P1_7, P3_3, P3_7, P4_3, P4_5, P6_3 to P6_5 | I/O | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. |
| Output port | P4_4 | O | Output-only port |

I: Input O: Output I/O: Input and output

NOTE:

1. Refer to the oscillator manufacturer for oscillation characteristics.

Table 1.8 Pin Functions of R8C/2J Group

| Type | Symbol | I/O Type | Description |
|---|--|----------|---|
| Power supply input | VCC, VSS | — | Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin. |
| Reset input | $\overline{\text{RESET}}$ | I | Input “L” on this pin resets the MCU. |
| MODE | MODE | I | Connect this pin to VCC via a resistor. |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}, \overline{\text{INT1}}$ | I | $\overline{\text{INT}}$ interrupt input pins |
| Key input interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Key input interrupt input pins |
| Timer RA | TRAIO | I/O | Timer RA I/O pin |
| | TRA0 | O | Timer RA output pin |
| Timer RB | TRBO | O | Timer RB output pin |
| Timer RF | TRFI | I | Timer RF input pin |
| | TRFO00 to TRFO02, TRFO10 to TRFO11 | O | Timer RF output pins |
| Serial interface | CLK0 | I/O | Clock I/O pin |
| | RXD0 | I | Serial data input pin |
| | TXD0 | O | Serial data output pin |
| Comparator | VCMP1, VCMP2 | I | Analog input pins to comparator |
| | CVREF | I | Reference voltage input pin to comparator |
| | VCOUT1, VCOUT2 | O | Comparator output pins |
| I/O port | P1_0 to P1_7, P3_3, P3_7, P4_5, P6_5 | I/O | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. |

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

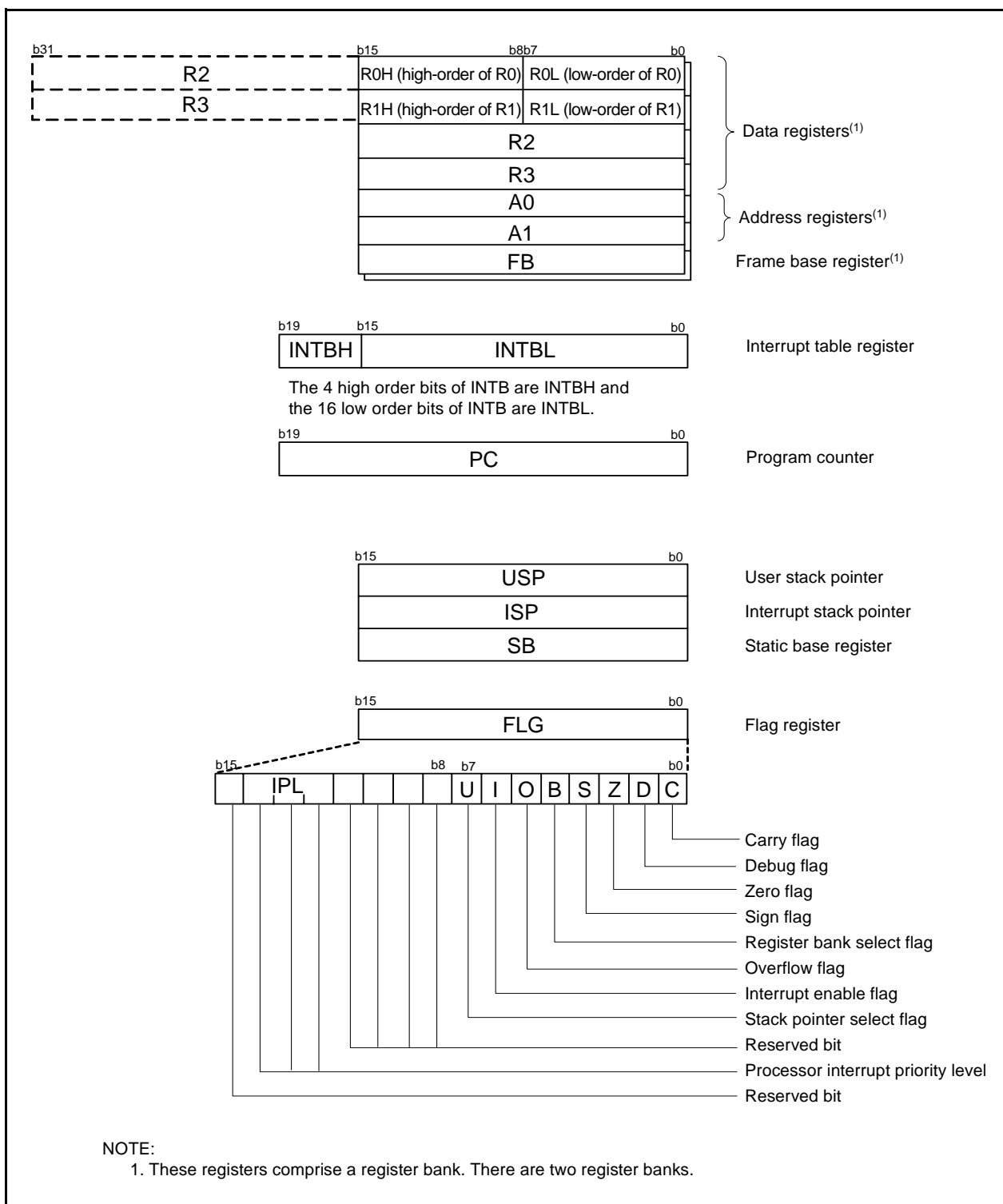


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

Figure 3.1 is a Memory Map of R8C/2H Group and Figure 3.2 is a Memory Map of R8C/2J Group. The R8C/2H group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 4-Kbyte internal ROM area is allocated addresses 0F000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 256-bytes internal RAM area is allocated addresses 00400h to 004FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

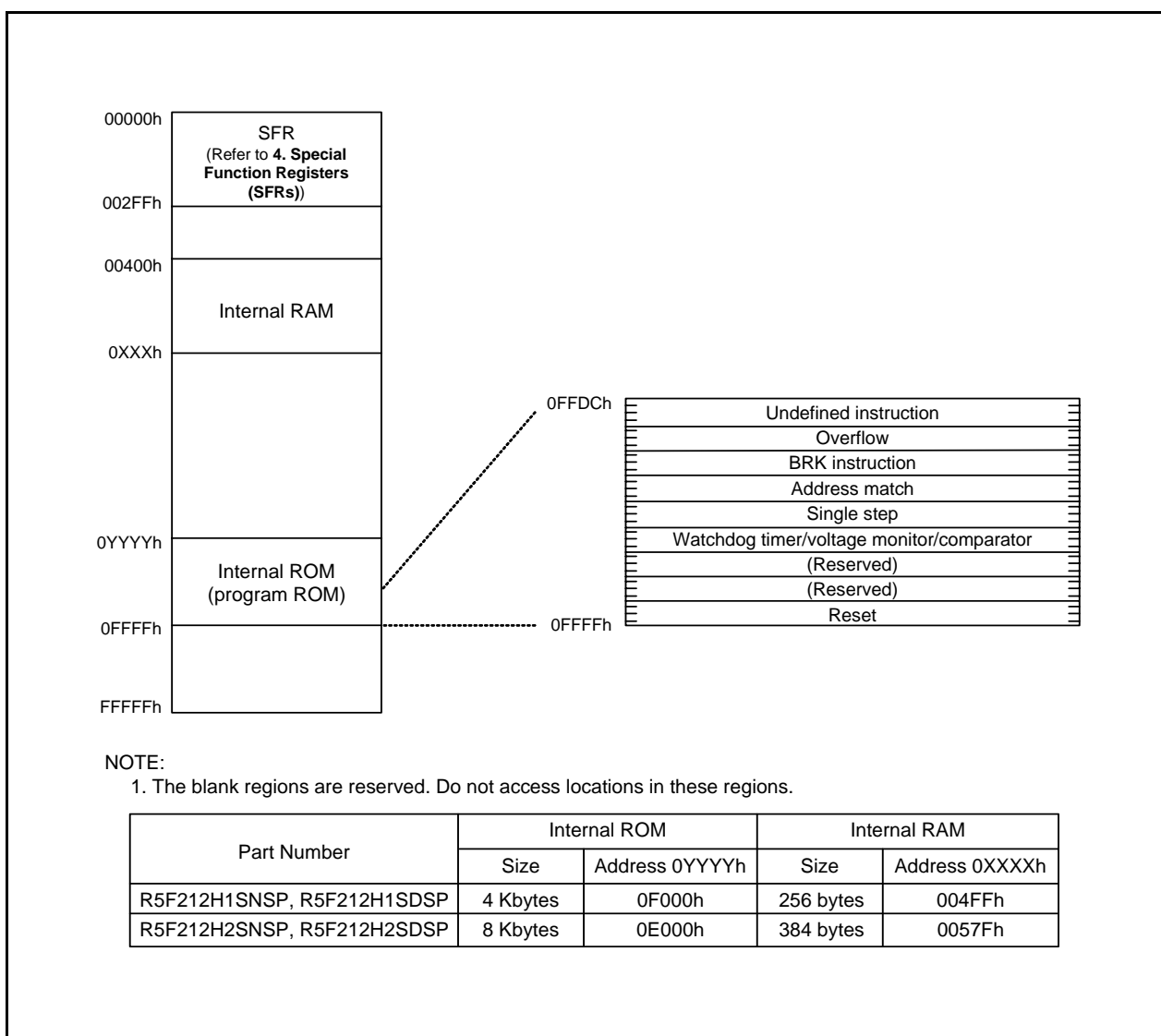


Figure 3.1 Memory Map of R8C/2H Group

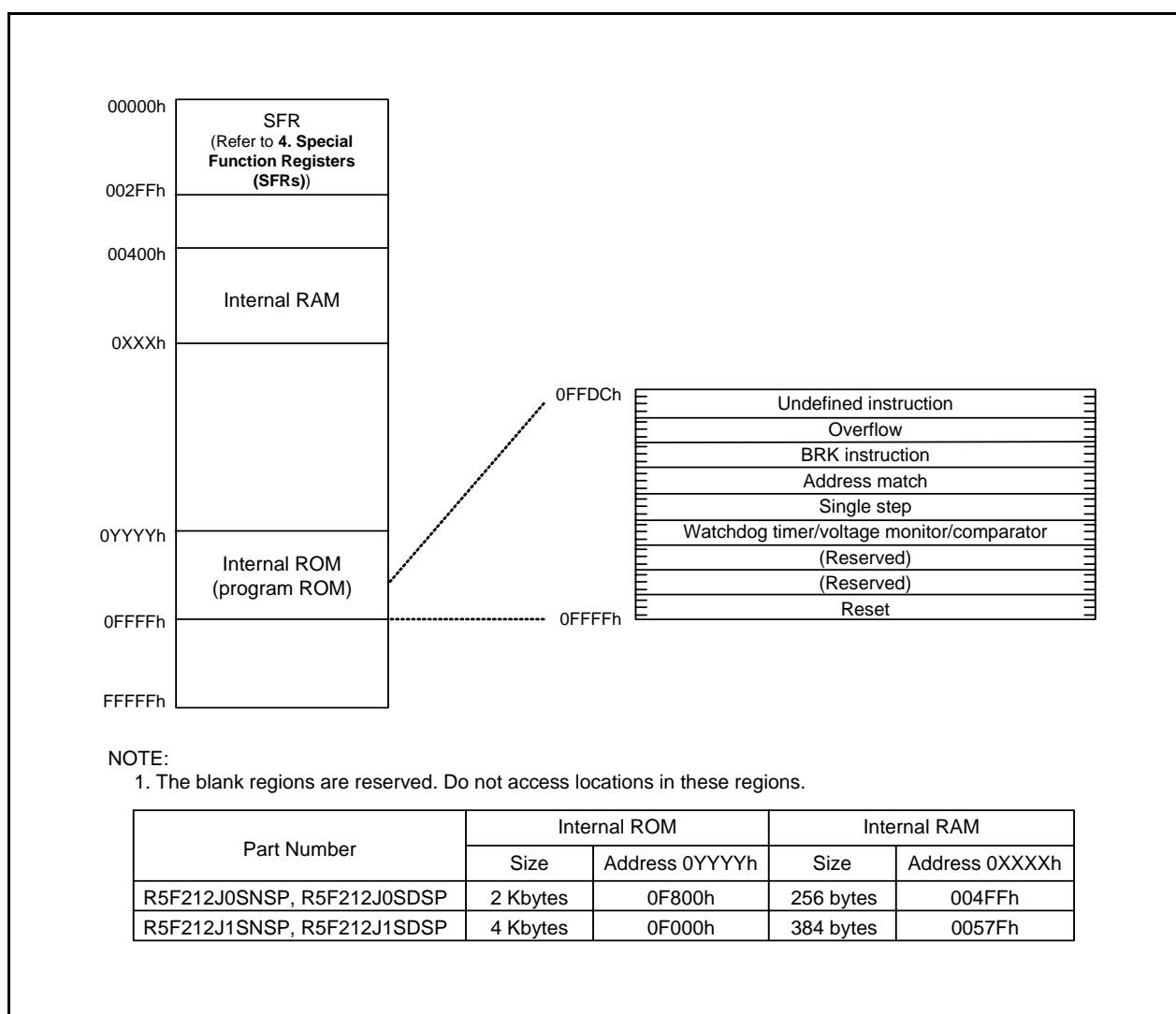


Figure 3.2 Memory Map of R8C/2J Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers.

Table 4.1 SFR Information (1)(1)

| Address | Register | Symbol | After reset |
|---------|--|---------|---------------------|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 | PM0 | 00h |
| 0005h | Processor Mode Register 1 | PM1 | 00h |
| 0006h | System Clock Control Register 0 | CM0 | 01011000b |
| 0007h | System Clock Control Register 1 | CM1 | 00h |
| 0008h | | | |
| 0009h | | | |
| 000Ah | Protect Register | PRCR | 00h |
| 000Bh | | | |
| 000Ch | System Clock Select Register(3) | OCD | 00000100b |
| 000Dh | Watchdog Timer Reset Register | WDTR | XXh |
| 000Eh | Watchdog Timer Start Register | WDTS | XXh |
| 000Fh | Watchdog Timer Control Register | WDC | 00X11111b |
| 0010h | Address Match Interrupt Register 0 | RMAD0 | 00h |
| 0011h | | | 00h |
| 0012h | | | 00h |
| 0013h | Address Match Interrupt Enable Register | AIER | 00h |
| 0014h | Address Match Interrupt Register 1 | RMAD1 | 00h |
| 0015h | | | 00h |
| 0016h | | | 00h |
| 0017h | | | 00h |
| 0018h | | | |
| 0019h | | | |
| 001Ah | | | |
| 001Bh | | | |
| 001Ch | Count Source Protection Mode Register | CSPR | 00h 10000000b(2) |
| 001Dh | | | |
| 001Eh | | | |
| 001Fh | | | |
| 0020h | High-Speed On-Chip Oscillator Control Register 0 | HRA0 | 00h |
| 0021h | High-Speed On-Chip Oscillator Control Register 1 | HRA1 | When Shipping |
| 0022h | High-Speed On-Chip Oscillator Control Register 2 | HRA2 | 00h |
| 0023h | | | |
| 0024h | | | |
| 0025h | | | |
| 0026h | | | |
| 0027h | | | |
| 0028h | Clock Prescaler Reset Flag(3) | CPSRF | 00h |
| 0029h | High-Speed On-Chip Oscillator Control Register 4 | FRA4 | When Shipping |
| 002Ah | | | |
| 002Bh | High-Speed On-Chip Oscillator Control Register 6 | FRA6 | When Shipping |
| 002Ch | | | |
| 002Dh | | | |
| 002Eh | BGR Trimming Auxiliary Register A | BGRTRMA | When Shipping |
| 002Fh | BGR Trimming Auxiliary Register B | BGRTRMB | When Shipping |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The CSPROINI bit in the OFS register is set to 0.
3. This register is not implemented in the R8C/2J Group.

Table 4.2 SFR Information (2)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|---|---------|--|
| 0030h | | | |
| 0031h | Voltage Detection Register 1 ⁽²⁾ | VCA1 | 00001000b |
| 0032h | Voltage Detection Register 2 ⁽²⁾ | VCA2 | 00h ⁽³⁾ 00100000b ⁽⁴⁾ |
| 0033h | | | |
| 0034h | | | |
| 0035h | | | |
| 0036h | Voltage Monitor 1 Circuit Control Register ⁽⁵⁾ | VW1C | 00001010b |
| 0037h | Voltage Monitor 2 Circuit Control Register ⁽⁵⁾ | VW2C | 00000010b |
| 0038h | Voltage Monitor 0 Circuit Control Register ⁽²⁾ | VW0C | 1000X010b ⁽³⁾ 1100X011b ⁽⁴⁾ |
| 0039h | | | |
| 003Ah | | | |
| 003Bh | Voltage Detection Circuit External Input Control Register | VCAB | 00h |
| 003Ch | Comparator Mode Register | ALCMR | 00h |
| 003Dh | Voltage Monitor Circuit Edge Select Register | VCAC | 00h |
| 003Eh | BGR Control Register | BGRCR | 00h |
| 003Fh | BGR Trimming Register | BGRTRM | When Shipping |
| 0040h | | | |
| 0041h | Comparator 1 Interrupt Control Register | VCMP1IC | XXXXX000b |
| 0042h | Comparator 2 Interrupt Control Register | VCMP2IC | XXXXX000b |
| 0043h | | | |
| 0044h | | | |
| 0045h | | | |
| 0046h | | | |
| 0047h | | | |
| 0048h | | | |
| 0049h | | | |
| 004Ah | Timer RE Interrupt Control Register ⁽⁶⁾ | TREIC | XXXXX000b |
| 004Bh | UART2 Transmit Interrupt Control Register ⁽⁶⁾ | S2TIC | XXXXX000b |
| 004Ch | UART2 Receive Interrupt Control Register ⁽⁶⁾ | S2RIC | XXXXX000b |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXXX000b |
| 004Eh | | | |
| 004Fh | | | |
| 0050h | Compare 1 Interrupt Control Register | CMP1IC | XXXXX000b |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | | | |
| 0054h | | | |
| 0055h | | | |
| 0056h | Timer RA Interrupt Control Register | TRAIC | XXXXX000b |
| 0057h | | | |
| 0058h | Timer RB Interrupt Control Register | TRBIC | XXXXX000b |
| 0059h | INT1 Interrupt Control Register | INT1IC | XX00X000b |
| 005Ah | | | |
| 005Bh | Timer RF Interrupt Control Register | TRFIC | XXXXX000b |
| 005Ch | Compare 0 Interrupt Control Register | CMP0IC | XXXXX000b |
| 005Dh | INT0 Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | | | |
| 005Fh | Capture Interrupt Control Register | CAPIC | XXXXX000b |
| 0060h | | | |
| 0061h | | | |
| 0062h | | | |
| 0063h | | | |
| 0064h | | | |
| 0065h | | | |
| 0066h | | | |
| 0067h | | | |
| 0068h | | | |
| 0069h | | | |
| 006Ah | | | |
| 006Bh | | | |
| 006Ch | | | |
| 006Dh | | | |
| 006Eh | | | |
| 006Fh | | | |

X: Undefined

NOTES:

- The blank regions are reserved. Do not access locations in these regions.
- Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
- The LVD0ON bit in the OFS register is set to 1 and hardware reset.
- Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset.
- Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
- This register is not implemented in the R8C/2J Group.

Table 4.3 SFR Information (3)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|---|--------|-------------|
| 0070h | | | |
| 0071h | | | |
| 0072h | | | |
| 0073h | | | |
| 0074h | | | |
| 0075h | | | |
| 0076h | | | |
| 0077h | | | |
| 0078h | | | |
| 0079h | | | |
| 007Ah | | | |
| 007Bh | | | |
| 007Ch | | | |
| 007Dh | | | |
| 007Eh | | | |
| 007Fh | | | |
| 0080h | | | |
| 0081h | | | |
| 0082h | | | |
| 0083h | | | |
| 0084h | | | |
| 0085h | | | |
| 0086h | | | |
| 0087h | | | |
| 0088h | | | |
| 0089h | | | |
| 008Ah | | | |
| 008Bh | | | |
| 008Ch | | | |
| 008Dh | | | |
| 008Eh | | | |
| 008Fh | | | |
| 0090h | | | |
| 0091h | | | |
| 0092h | | | |
| 0093h | | | |
| 0094h | | | |
| 0095h | | | |
| 0096h | | | |
| 0097h | | | |
| 0098h | | | |
| 0099h | | | |
| 009Ah | | | |
| 009Bh | | | |
| 009Ch | | | |
| 009Dh | | | |
| 009Eh | | | |
| 009Fh | | | |
| 00A0h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 00A1h | UART0 Bit Rate Register | U0BRG | XXh |
| 00A2h | UART0 Transmit Buffer Register | U0TB | XXh |
| 00A3h | | | XXh |
| 00A4h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 00A5h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00000010b |
| 00A6h | UART0 Receive Buffer Register | U0RB | XXh |
| 00A7h | | | XXh |
| 00A8h | | | |
| 00A9h | | | |
| 00AAh | | | |
| 00ABh | | | |
| 00ACh | | | |
| 00ADh | | | |
| 00AEh | | | |
| 00AFh | | | |

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.4 SFR Information (4)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|----------------------------|--------|-------------|
| 00B0h | | | |
| 00B1h | | | |
| 00B2h | | | |
| 00B3h | | | |
| 00B4h | | | |
| 00B5h | | | |
| 00B6h | | | |
| 00B7h | | | |
| 00B8h | | | |
| 00B9h | | | |
| 00BAh | | | |
| 00BBh | | | |
| 00BCh | | | |
| 00BDh | | | |
| 00BEh | | | |
| 00BFh | | | |
| 00C0h | | | |
| 00C1h | | | |
| 00C2h | | | |
| 00C3h | | | |
| 00C4h | | | |
| 00C5h | | | |
| 00C6h | | | |
| 00C7h | | | |
| 00C8h | | | |
| 00C9h | | | |
| 00CAh | | | |
| 00CBh | | | |
| 00CCh | | | |
| 00CDh | | | |
| 00CEh | | | |
| 00CFh | | | |
| 00D0h | | | |
| 00D1h | | | |
| 00D2h | | | |
| 00D3h | | | |
| 00D4h | | | |
| 00D5h | | | |
| 00D6h | | | |
| 00D7h | | | |
| 00D8h | | | |
| 00D9h | | | |
| 00DAh | | | |
| 00DBh | | | |
| 00DCh | | | |
| 00DDh | | | |
| 00DEh | | | |
| 00DFh | | | |
| 00E0h | | | |
| 00E1h | Port P1 Register | P1 | 00h |
| 00E2h | | | |
| 00E3h | Port P1 Direction Register | PD1 | 00h |
| 00E4h | | | |
| 00E5h | Port P3 Register | P3 | 00h |
| 00E6h | | | |
| 00E7h | Port P3 Direction Register | PD3 | 00h |
| 00E8h | Port P4 Register | P4 | 00h |
| 00E9h | | | |
| 00EAh | Port P4 Direction Register | PD4 | 00h |
| 00EBh | | | |
| 00ECh | Port P6 Register | P6 | 00h |
| 00EDh | | | |
| 00EEh | Port P6 Direction Register | PD6 | 00h |
| 00EFh | | | |

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.5 SFR Information (5)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|--|--------|-------------|
| 00F0h | | | |
| 00F1h | | | |
| 00F2h | | | |
| 00F3h | | | |
| 00F4h | | | |
| 00F5h | | | |
| 00F6h | Pin Select Register 2 | PINSR2 | 00h |
| 00F7h | | | |
| 00F8h | Port Mode Register | PMR | 00h |
| 00F9h | External Input Enable Register | INTEN | 00h |
| 00FAh | INT Input Filter Select Register | INTF | 00h |
| 00FBh | Key Input Enable Register | KIEN | 00h |
| 00FCh | Pull-Up Control Register 0 | PUR0 | 00h |
| 00FDh | Pull-Up Control Register 1 | PUR1 | 00h |
| 00FEh | | | |
| 00FFh | | | |
| 0100h | Timer RA Control Register | TRACR | 00h |
| 0101h | Timer RA I/O Control Register | TRAIOC | 00h |
| 0102h | Timer RA Mode Register | TRAMR | 00h |
| 0103h | Timer RA Prescaler Register | TRAPRE | FFh |
| 0104h | Timer RA Register | TRA | FFh |
| 0105h | | | |
| 0106h | LIN Control Register | LINCR | 00h |
| 0107h | LIN Status Register | LINST | 00h |
| 0108h | Timer RB Control Register | TRBCR | 00h |
| 0109h | Timer RB One-Shot Control Register | TRBOCR | 00h |
| 010Ah | Timer RB I/O Control Register | TRBIOC | 00h |
| 010Bh | Timer RB Mode Register | TRBMR | 00h |
| 010Ch | Timer RB Prescaler Register | TRBPRE | FFh |
| 010Dh | Timer RB Secondary Register | TRBSC | FFh |
| 010Eh | Timer RB Primary Register | TRBPR | FFh |
| 010Fh | | | |
| 0110h | | | |
| 0111h | | | |
| 0112h | | | |
| 0113h | | | |
| 0114h | | | |
| 0115h | | | |
| 0116h | | | |
| 0117h | | | |
| 0118h | Timer RE Second Data Register / Counter Data Register ⁽²⁾ | TRESEC | XXh |
| 0119h | Timer RE Minute Data Register / Compare Data Register ⁽²⁾ | TREMIN | XXh |
| 011Ah | Timer RE Hour Data Register ⁽²⁾ | TREHR | X0XXXXXXb |
| 011Bh | Timer RE Day of Week Data Register ⁽²⁾ | TREWK | X0000XXXb |
| 011Ch | Timer RE Control Register 1 ⁽²⁾ | TRECR1 | XXX0X0X0b |
| 011Dh | Timer RE Control Register 2 ⁽²⁾ | TRECR2 | 00XXXXXXb |
| 011Eh | Timer RE Count Source Select Register ⁽²⁾ | TRECSR | 00001000b |
| 011Fh | Timer RE Real-Time Clock Precision Adjust Register ⁽²⁾ | TREOPR | 00h |
| 0120h | | | |
| 0121h | | | |
| 0122h | | | |
| 0123h | | | |
| 0124h | | | |
| 0125h | | | |
| 0126h | | | |
| 0127h | | | |
| 0128h | | | |
| 0129h | | | |
| 012Ah | | | |
| 012Bh | | | |
| 012Ch | | | |
| 012Dh | | | |
| 012Eh | | | |
| 012Fh | | | |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions
2. This register is not implemented in the R8C/2J Group.

Table 4.6 SFR Information (6)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|--|--------|-------------|
| 0130h | | | |
| 0131h | | | |
| 0132h | | | |
| 0133h | | | |
| 0134h | | | |
| 0135h | | | |
| 0136h | | | |
| 0137h | | | |
| 0138h | | | |
| 0139h | | | |
| 013Ah | | | |
| 013Bh | | | |
| 013Ch | | | |
| 013Dh | | | |
| 013Eh | | | |
| 013Fh | | | |
| 0140h | | | |
| 0141h | | | |
| 0142h | | | |
| 0143h | | | |
| 0144h | | | |
| 0145h | | | |
| 0146h | | | |
| 0147h | | | |
| 0148h | | | |
| 0149h | | | |
| 014Ah | | | |
| 014Bh | | | |
| 014Ch | | | |
| 014Dh | | | |
| 014Eh | | | |
| 014Fh | | | |
| 0150h | | | |
| 0151h | | | |
| 0152h | | | |
| 0153h | | | |
| 0154h | | | |
| 0155h | | | |
| 0156h | | | |
| 0157h | | | |
| 0158h | | | |
| 0159h | | | |
| 015Ah | | | |
| 015Bh | | | |
| 015Ch | | | |
| 015Dh | | | |
| 015Eh | | | |
| 015Fh | | | |
| 0160h | UART2 Transmit/Receive Mode Register ⁽²⁾ | U2MR | 00h |
| 0161h | UART2 Bit Rate Register ⁽²⁾ | U2BRG | XXh |
| 0162h | UART2 Transmit Buffer Register ⁽²⁾ | U2TB | XXh |
| 0163h | | | XXh |
| 0164h | UART2 Transmit/Receive Control Register 0 ⁽²⁾ | U2C0 | 00001000b |
| 0165h | UART2 Transmit/Receive Control Register 1 ⁽²⁾ | U2C1 | 00000010b |
| 0166h | UART2 Receive Buffer Register ⁽²⁾ | U2RB | XXh |
| 0167h | | | XXh |
| 0168h | | | |
| 0169h | | | |
| 016Ah | | | |
| 016Bh | | | |
| 016Ch | | | |
| 016Dh | | | |
| 016Eh | | | |
| 016Fh | | | |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. This register is not implemented in the R8C/2J Group.

Table 4.7 SFR Information (7)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|----------|--------|-------------|
| 0170h | | | |
| 0171h | | | |
| 0172h | | | |
| 0173h | | | |
| 0174h | | | |
| 0175h | | | |
| 0176h | | | |
| 0177h | | | |
| 0178h | | | |
| 0179h | | | |
| 017Ah | | | |
| 017Bh | | | |
| 017Ch | | | |
| 017Dh | | | |
| 017Eh | | | |
| 017Fh | | | |
| 0180h | | | |
| 0181h | | | |
| 0182h | | | |
| 0183h | | | |
| 0184h | | | |
| 0185h | | | |
| 0186h | | | |
| 0187h | | | |
| 0188h | | | |
| 0189h | | | |
| 018Ah | | | |
| 018Bh | | | |
| 018Ch | | | |
| 018Dh | | | |
| 018Eh | | | |
| 018Fh | | | |
| 0190h | | | |
| 0191h | | | |
| 0192h | | | |
| 0193h | | | |
| 0194h | | | |
| 0195h | | | |
| 0196h | | | |
| 0197h | | | |
| 0198h | | | |
| 0199h | | | |
| 019Ah | | | |
| 019Bh | | | |
| 019Ch | | | |
| 019Dh | | | |
| 019Eh | | | |
| 019Fh | | | |
| 01A0h | | | |
| 01A1h | | | |
| 01A2h | | | |
| 01A3h | | | |
| 01A4h | | | |
| 01A5h | | | |
| 01A6h | | | |
| 01A7h | | | |
| 01A8h | | | |
| 01A9h | | | |
| 01AAh | | | |
| 01ABh | | | |
| 01ACh | | | |
| 01ADh | | | |
| 01AEh | | | |
| 01AFh | | | |

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.8 SFR Information (8)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|---------------------------------|--------|-------------|
| 01B0h | | | |
| 01B1h | | | |
| 01B2h | | | |
| 01B3h | Flash Memory Control Register 4 | FMR4 | 01000000b |
| 01B4h | | | |
| 01B5h | Flash Memory Control Register 1 | FMR1 | 1000000Xb |
| 01B6h | | | |
| 01B7h | Flash Memory Control Register 0 | FMR0 | 00000001b |
| 01B8h | | | |
| 01B9h | | | |
| 01BAh | | | |
| 01BBh | | | |
| 01BCh | | | |
| 01BDh | | | |
| 01BEh | | | |
| 01BFh | | | |
| 01C0h | | | |
| 01C1h | | | |
| 01C2h | | | |
| 01C3h | | | |
| 01C4h | | | |
| 01C5h | | | |
| 01C6h | | | |
| 01C7h | | | |
| 01C8h | | | |
| 01C9h | | | |
| 01CAh | | | |
| 01CBh | | | |
| 01CCh | | | |
| 01CDh | | | |
| 01CEh | | | |
| 01CFh | | | |
| 01D0h | | | |
| 01D1h | | | |
| 01D2h | | | |
| 01D3h | | | |
| 01D4h | | | |
| 01D5h | | | |
| 01D6h | | | |
| 01D7h | | | |
| 01D8h | | | |
| 01D9h | | | |
| 01DAh | | | |
| 01DBh | | | |
| 01DCh | | | |
| 01DDh | | | |
| 01DEh | | | |
| 01DFh | | | |
| 01E0h | | | |
| 01E1h | | | |
| 01E2h | | | |
| 01E3h | | | |
| 01E4h | | | |
| 01E5h | | | |
| 01E6h | | | |
| 01E7h | | | |
| 01E8h | | | |
| 01E9h | | | |
| 01EAh | | | |
| 01EBh | | | |
| 01ECh | | | |
| 01EDh | | | |
| 01EEh | | | |
| 01EFh | | | |

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|----------|--------|-------------|
| 01F0h | | | |
| 01F1h | | | |
| 01F2h | | | |
| 01F3h | | | |
| 01F4h | | | |
| 01F5h | | | |
| 01F6h | | | |
| 01F7h | | | |
| 01F8h | | | |
| 01F9h | | | |
| 01FAh | | | |
| 01FBh | | | |
| 01FCh | | | |
| 01FDh | | | |
| 01FEh | | | |
| 01FFh | | | |
| 0200h | | | |
| 0201h | | | |
| 0202h | | | |
| 0203h | | | |
| 0204h | | | |
| 0205h | | | |
| 0206h | | | |
| 0207h | | | |
| 0208h | | | |
| 0209h | | | |
| 020Ah | | | |
| 020Bh | | | |
| 020Ch | | | |
| 020Dh | | | |
| 020Eh | | | |
| 020Fh | | | |
| 0210h | | | |
| 0211h | | | |
| 0212h | | | |
| 0213h | | | |
| 0214h | | | |
| 0215h | | | |
| 0216h | | | |
| 0217h | | | |
| 0218h | | | |
| 0219h | | | |
| 021Ah | | | |
| 021Bh | | | |
| 021Ch | | | |
| 021Dh | | | |
| 021Eh | | | |
| 021Fh | | | |
| 0220h | | | |
| 0221h | | | |
| 0222h | | | |
| 0223h | | | |
| 0224h | | | |
| 0225h | | | |
| 0226h | | | |
| 0227h | | | |
| 0228h | | | |
| 0229h | | | |
| 022Ah | | | |
| 022Bh | | | |
| 022Ch | | | |
| 022Dh | | | |
| 022Eh | | | |
| 022Fh | | | |

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.10 SFR Information (10)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|----------|--------|-------------|
| 0230h | | | |
| 0231h | | | |
| 0232h | | | |
| 0233h | | | |
| 0234h | | | |
| 0235h | | | |
| 0236h | | | |
| 0237h | | | |
| 0238h | | | |
| 0239h | | | |
| 023Ah | | | |
| 023Bh | | | |
| 023Ch | | | |
| 023Dh | | | |
| 023Eh | | | |
| 023Fh | | | |
| 0240h | | | |
| 0241h | | | |
| 0242h | | | |
| 0243h | | | |
| 0244h | | | |
| 0245h | | | |
| 0246h | | | |
| 0247h | | | |
| 0248h | | | |
| 0249h | | | |
| 024Ah | | | |
| 024Bh | | | |
| 024Ch | | | |
| 024Dh | | | |
| 024Eh | | | |
| 024Fh | | | |
| 0250h | | | |
| 0251h | | | |
| 0252h | | | |
| 0253h | | | |
| 0254h | | | |
| 0255h | | | |
| 0256h | | | |
| 0257h | | | |
| 0258h | | | |
| 0259h | | | |
| 025Ah | | | |
| 025Bh | | | |
| 025Ch | | | |
| 025Dh | | | |
| 025Eh | | | |
| 025Fh | | | |
| 0260h | | | |
| 0261h | | | |
| 0262h | | | |
| 0263h | | | |
| 0264h | | | |
| 0265h | | | |
| 0266h | | | |
| 0267h | | | |
| 0268h | | | |
| 0269h | | | |
| 026Ah | | | |
| 026Bh | | | |
| 026Ch | | | |
| 026Dh | | | |
| 026Eh | | | |
| 026Fh | | | |

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.11 SFR Information (11)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|--|--------|----------------------|
| 0270h | | | |
| 0271h | | | |
| 0272h | | | |
| 0273h | | | |
| 0274h | | | |
| 0275h | | | |
| 0276h | | | |
| 0277h | | | |
| 0278h | | | |
| 0279h | | | |
| 027Ah | | | |
| 027Bh | | | |
| 027Ch | | | |
| 027Dh | | | |
| 027Eh | | | |
| 027Fh | | | |
| 0280h | | | |
| 0281h | | | |
| 0282h | | | |
| 0283h | | | |
| 0284h | | | |
| 0285h | | | |
| 0286h | | | |
| 0287h | | | |
| 0288h | | | |
| 0289h | | | |
| 028Ah | | | |
| 028Bh | | | |
| 028Ch | | | |
| 028Dh | | | |
| 028Eh | | | |
| 028Fh | | | |
| 0290h | Timer RF Register | TRF | 00h |
| 0291h | | | 00h |
| 0292h | | | |
| 0293h | | | |
| 0294h | | | |
| 0295h | | | |
| 0296h | | | |
| 0297h | | | |
| 0298h | | | |
| 0299h | Timer RF Control Register 2 ⁽⁴⁾ | TRFCR2 | 00h |
| 029Ah | Timer RF Control Register 0 | TRFCR0 | 00h |
| 029Bh | Timer RF Control Register 1 | TRFCR1 | 00h |
| 029Ch | Capture and Compare 0 Register | TRFM0 | 0000h ⁽²⁾ |
| 029Dh | | | FFFFh ⁽³⁾ |
| 029Eh | Compare 1 Register | TRFM1 | FFh |
| 029Fh | | | FFh |
| 02A0h | | | |
| 02A1h | | | |
| 02A2h | | | |
| 02A3h | | | |
| 02A4h | | | |
| 02A5h | | | |
| 02A6h | | | |
| 02A7h | | | |
| 02A8h | | | |
| 02A9h | | | |
| 02AAh | | | |
| 02ABh | | | |
| 02ACh | | | |
| 02ADh | | | |
| 02AEh | | | |
| 02AFh | | | |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. After input capture mode.
3. After output compare mode.
4. This register is not implemented in the R8C/2J Group.

Table 4.12 SFR Information (12)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|----------------------------------|--------|-------------|
| 02B0h | | | |
| 02B1h | | | |
| 02B2h | | | |
| 02B3h | | | |
| 02B4h | | | |
| 02B5h | | | |
| 02B6h | | | |
| 02B7h | | | |
| 02B8h | | | |
| 02B9h | | | |
| 02BAh | | | |
| 02BBh | | | |
| 02BCh | | | |
| 02BDh | | | |
| 02BEh | | | |
| 02BFh | | | |
| 02C0h | | | |
| 02C1h | | | |
| 02C2h | | | |
| 02C3h | | | |
| 02C4h | | | |
| 02C5h | | | |
| 02C6h | | | |
| 02C7h | | | |
| 02C8h | | | |
| 02C9h | | | |
| 02CAh | | | |
| 02CBh | | | |
| 02CCh | | | |
| 02CDh | | | |
| 02CEh | | | |
| 02CFh | | | |
| 02D0h | | | |
| 02D1h | | | |
| 02D2h | | | |
| 02D3h | | | |
| 02D4h | | | |
| 02D5h | | | |
| 02D6h | | | |
| 02D7h | | | |
| 02D8h | | | |
| 02D9h | | | |
| 02DAh | | | |
| 02DBh | | | |
| 02DCh | | | |
| 02DDh | | | |
| 02DEh | | | |
| 02DFh | | | |
| 02E0h | | | |
| 02EFh | | | |
| 02F0h | | | |
| 02F1h | | | |
| 02F2h | | | |
| 02F3h | | | |
| 02F4h | | | |
| 02F5h | | | |
| 02F6h | | | |
| 02F7h | | | |
| 02F8h | | | |
| 02F9h | | | |
| 02FAh | | | |
| 02FBh | Pin Select Register 4 | PINSR4 | 00h |
| 02FCh | | | |
| 02FDh | | | |
| 02FEh | | | |
| 02FFh | Timer RF Output Control Register | TRFOUT | 00h |
| FFFFh | Option Function Select Register | OFS | (Note 2) |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Electrical Characteristics

5.1 R8C/2H Group

Table 5.1 Absolute Maximum Ratings

| Symbol | Parameter | Condition | Rated Value | Unit |
|------------------|-------------------------------|-------------------------|--|------|
| V _{CC} | Supply voltage | | –0.3 to 6.5 | V |
| V _I | Input voltage | | –0.3 to V _{CC} + 0.3 | V |
| V _O | Output voltage | | –0.3 to V _{CC} + 0.3 | V |
| P _d | Power dissipation | T _{opr} = 25°C | 500 | mW |
| T _{opr} | Operating ambient temperature | | –20 to 85 (N version) / –40 to 85 (D version) | °C |
| T _{stg} | Storage temperature | | –65 to 150 | °C |

Table 5.2 Recommended Operating Conditions

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|-----------------------|--|---|--|---------------------|------|---------------------|------|
| | | | | Min. | Typ. | Max. | |
| V _{CC} | Supply voltage | | | 2.2 | – | 5.5 | V |
| V _{SS} | Supply voltage | | | – | 0 | – | V |
| V _{IH} | Input “H” voltage | | | 0.8 V _{CC} | – | V _{CC} | V |
| V _{IL} | Input “L” voltage | | | 0 | – | 0.2 V _{CC} | V |
| I _{OH(sum)} | Peak sum output “H” current | Sum of all pins I _{OH(peak)} | | – | – | –160 | mA |
| I _{OH(sum)} | Average sum output “H” current | Sum of all pins I _{OH(avg)} | | – | – | –80 | mA |
| I _{OH(peak)} | Peak output “H” current | All pins | | – | – | –10 | mA |
| I _{OH(avg)} | Average output “H” current | All pins | | – | – | –5 | mA |
| I _{OL(sum)} | Peak sum output “L” currents | Sum of all pins I _{OL(peak)} | | – | – | 160 | mA |
| I _{OL(sum)} | Average sum output “L” currents | Sum of all pins I _{OL(avg)} | | – | – | 80 | mA |
| I _{OL(peak)} | Peak output “L” currents | All pins | | – | – | 10 | mA |
| I _{OL(avg)} | Average output “L” current | All pins | | – | – | 5 | mA |
| f _(XCIN) | XCIN clock input oscillation frequency | | 2.2 V ≤ V _{CC} ≤ 5.5 V | 0 | – | 70 | kHz |
| – | System clock | OCD2 = 0 XCIN clock selected | 2.2 V ≤ V _{CC} ≤ 5.5 V | 0 | – | 70 | kHz |
| | | OCD2 = 1 On-chip oscillator clock selected | HRA01 = 0 Low-speed on-chip oscillator selected | – | 125 | – | kHz |
| | | | HRA01 = 1 High-speed on-chip oscillator selected 2.7 V ≤ V _{CC} ≤ 5.5 V | – | – | 8 | MHz |
| | | | HRA01 = 1 High-speed on-chip oscillator selected 2.2 V ≤ V _{CC} ≤ 5.5 V | – | – | 4 | MHz |

NOTES:

- V_{CC} = 2.2 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
- The average output current indicates the average value of current measured during 100 ms.

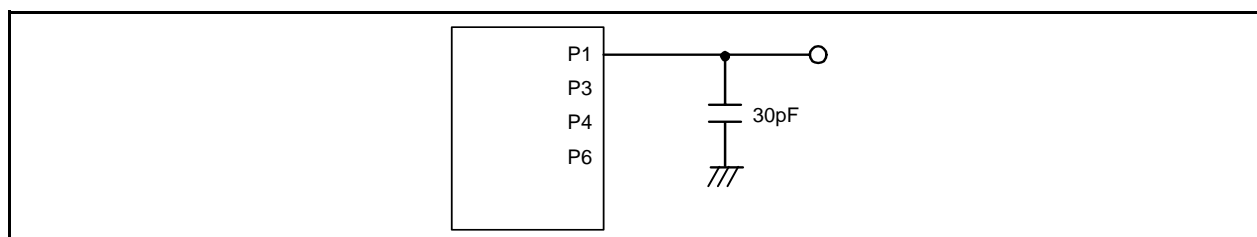


Figure 5.1 Ports P1, P3, P4, and P6 Timing Measurement Circuit

Table 5.3 Flash Memory (Program ROM) Electrical Characteristics

| Symbol | Parameter | Conditions | Standard | | | Unit |
|--------|--|----------------------------|--------------------|------|------|-------|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance ⁽²⁾ | | 100 ⁽³⁾ | – | – | times |
| – | Byte program time | | – | 50 | 400 | μs |
| – | Block erase time | | – | 0.4 | 9 | s |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.2 | – | 5.5 | V |
| – | Program, erase temperature | | 0 | – | 60 | °C |
| – | Data hold time ⁽⁷⁾ | Ambient temperature = 55°C | 20 | – | – | year |

NOTES:

1. VCC = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.4 Voltage Detection 0 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det0} | Voltage detection level | | 2.2 | 2.3 | 2.4 | V |
| — | Voltage detection circuit self power consumption | VCA25 = 1, V _{CC} = 5.0 V | — | 0.9 | — | μA |
| t _{d(E-A)} | Waiting time until voltage detection circuit operation starts ⁽²⁾ | | — | — | 300 | μs |
| V _{ccmin} | MCU operating voltage minimum value | | 2.2 | — | — | V |

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.5 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det1} | Voltage detection level ⁽⁴⁾ | | 2.70 | 2.85 | 3.00 | V |
| — | Voltage monitor 1 interrupt request generation time ⁽²⁾ | | — | 40 | — | μs |
| — | Voltage detection circuit self power consumption | VCA26 = 1, V _{CC} = 5.0 V | — | 0.6 | — | μA |
| t _{d(E-A)} | Waiting time until voltage detection circuit operation starts ⁽³⁾ | | — | — | 100 | μs |

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.6 Voltage Detection 2 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det2} | Voltage detection level | | 3.3 | 3.6 | 3.9 | V |
| — | Voltage monitor 2 interrupt request generation time ⁽²⁾ | | — | 40 | — | μs |
| — | Voltage detection circuit self power consumption | VCA27 = 1, V _{CC} = 5.0 V | — | 0.6 | — | μA |
| t _{d(E-A)} | Waiting time until voltage detection circuit operation starts ⁽³⁾ | | — | — | 100 | μs |

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.7 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics⁽³⁾

| Symbol | Parameter | Condition | Standard | | | Unit |
|-------------------|---|-----------|----------|------|-------------------|---------|
| | | | Min. | Typ. | Max. | |
| V _{por1} | Power-on reset valid voltage ⁽⁴⁾ | | – | – | 0.1 | V |
| V _{por2} | Power-on reset or voltage monitor 0 reset valid voltage | | 0 | – | V _{det0} | V |
| tr _{th} | External power V _{CC} rise gradient ⁽²⁾ | | 20 | – | – | mV/msec |

NOTES:

1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if V_{CC} ≥ 1.0 V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. t_{w(por1)} indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain t_{w(por1)} for 30 s or more if –20°C ≤ T_{opr} ≤ 85°C, maintain t_{w(por1)} for 3,000 s or more if –40°C ≤ T_{opr} < –20°C.

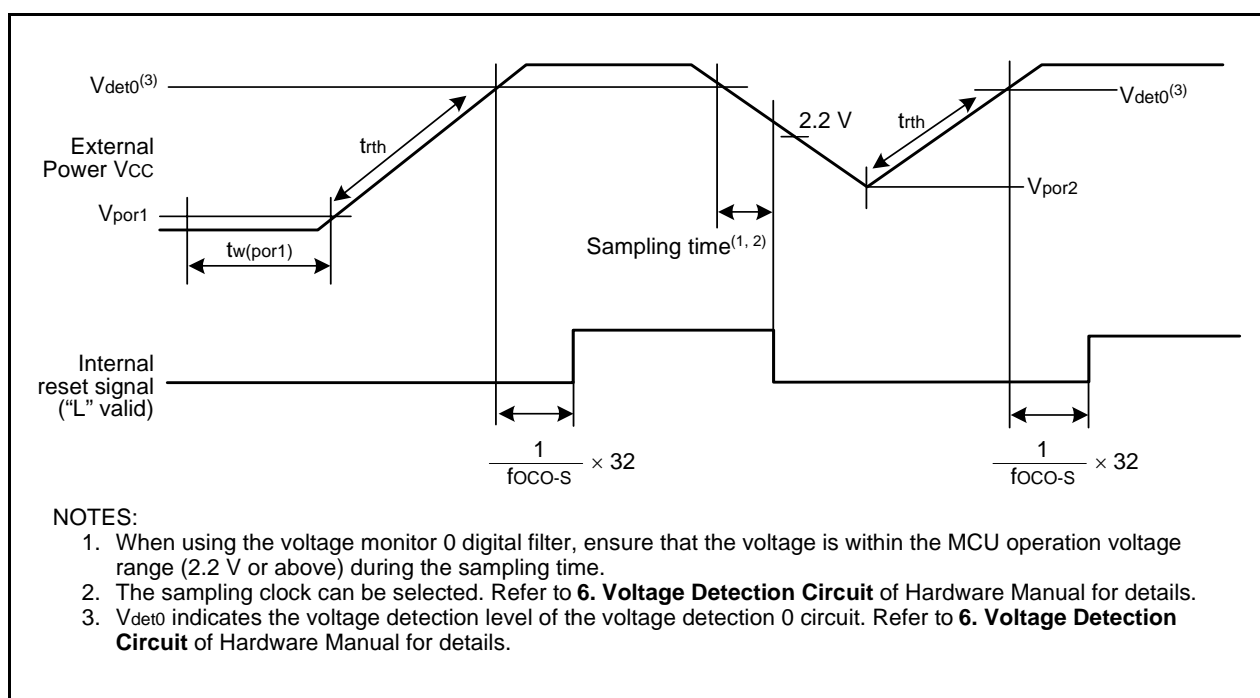
**Figure 5.2 Reset Circuit Electrical Characteristics**

Table 5.8 Comparator Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|---|---|----------|------|-----------|------|
| | | | Min. | Typ. | Max. | |
| Vref | Internal reference voltage | VCC = 2.2 V to 5.5 V, T _{opr} = 25°C | 1.15 | 1.25 | 1.35 | V |
| | | VCC = 2.2 V to 5.5 V, T _{opr} = -40 to 85°C | — | 1.25 | — | V |
| Vcref | External input reference voltage | VCC = 2.2 V to 4.0 V | 0.5 | — | VCC - 1.1 | V |
| | | VCC = 4.0 V to 5.5 V | 0.5 | — | VCC - 1.5 | V |
| Vcin | External comparison voltage input range | | -0.3 | — | VCC + 0.3 | V |
| Vofs | Input offset voltage | | — | 20 | 120 | mV |
| Tcrsp | Response time | | — | 4 | — | μs |

NOTE:

1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.9 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|--|---|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| fOCO-F | High-speed on-chip oscillator frequency temperature • supply voltage dependence | VCC = 4.75 V to 5.25 V T _{opr} = 0 to 60°C ⁽²⁾ | 7.76 | 8 | 8.24 | MHz |
| | | VCC = 2.7 V to 5.5 V T _{opr} = -20 to 85°C ⁽²⁾ | 7.68 | 8 | 8.32 | MHz |
| | | VCC = 2.7 V to 5.5 V T _{opr} = -40 to 85°C ⁽²⁾ | 7.44 | 8 | 8.32 | MHz |
| | | VCC = 2.2 V to 5.5 V T _{opr} = -20 to 85°C ⁽³⁾ | 7.04 | 8 | 8.96 | MHz |
| | | VCC = 2.2 V to 5.5 V T _{opr} = -40 to 85°C ⁽³⁾ | 6.8 | 8 | 9.2 | MHz |

NOTES:

1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the HRA1 register is set to the value before shipment and the HRA2 register is set to 00h.
3. These standard values show when the correction value in the FRA6 register is written into the HRA1 register.

Table 5.10 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|--|--------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 30 | 125 | 250 | kHz |
| — | Oscillation stability time | | — | 10 | 100 | μs |
| — | Self power consumption at oscillation | VCC = 5.0 V, T _{opr} = 25°C | — | 15 | — | μA |

NOTE:

1. VCC = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.11 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|----------------------|---|-----------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| t _d (P-R) | Time for internal power supply stabilization during power-on ⁽²⁾ | | 1 | — | 2000 | μs |
| t _d (R-S) | STOP exit time ⁽³⁾ | | — | — | 150 | μs |

NOTES:

1. The measurement condition is VCC = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.12 Electrical Characteristics (1) [V_{CC} = 5 V]

| Symbol | Parameter | | Condition | Standard | | | Unit |
|----------------------------------|---------------------|---|---|-----------------------|------|-----------------|------|
| | | | | Min. | Typ. | Max. | |
| V _{OH} | Output "H" voltage | | I _{OH} = -5 mA | V _{CC} - 2.0 | — | V _{CC} | V |
| | | | I _{OH} = -200 μA | V _{CC} - 0.5 | — | V _{CC} | V |
| V _{OL} | Output "L" voltage | | I _{OL} = 5 mA | — | — | 2.0 | V |
| | | | I _{OL} = 200 μA | — | — | 0.45 | V |
| V _{T+} -V _{T-} | Hysteresis | INT0, INT1, KI0, KI1, KI2, KI3, RXD0, RXD2, CLK0, CLK2 | | 0.1 | 0.5 | — | V |
| | | RESET | | 0.1 | 1.0 | — | V |
| I _{IH} | Input "H" current | | V _I = 5 V, V _{CC} = 5 V | — | — | 5.0 | μA |
| I _{IL} | Input "L" current | | V _I = 0 V, V _{CC} = 5 V | — | — | -5.0 | μA |
| R _{PULLUP} | Pull-up resistance | | V _I = 0 V, V _{CC} = 5 V | 30 | 50 | 167 | kΩ |
| R _{FXCIN} | Feedback resistance | XCIN | | — | 18 | — | MΩ |
| V _{RAM} | RAM hold voltage | | During stop mode | 2.0 | — | — | V |

NOTE:

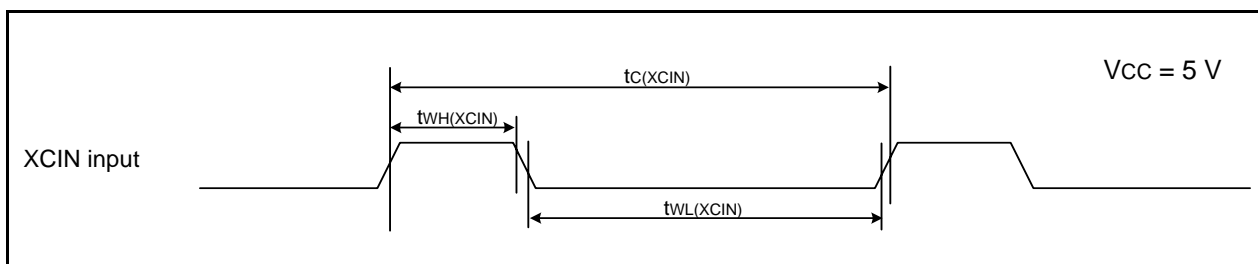
- V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.13 Electrical Characteristics (2) [V_{CC} = 5 V]
(T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

| Symbol | Parameter | Condition | Standard | | | Unit |
|-----------------|--|--|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| I _{CC} | Power supply current (V _{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V _{SS} | High-speed on-chip oscillator mode | – | 5 | 8 | mA |
| | | | | | | |
| | | High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division | – | 2 | – | mA |
| | | | | | | |
| | | High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 130 | 300 | μA |
| | | | | | | |
| | | Low-speed on-chip oscillator mode | – | 130 | 300 | μA |
| | | | | | | |
| | | Low-speed clock mode | – | 30 | – | μA |
| | | | | | | |
| | | Wait mode | – | 25 | 75 | μA |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | Stop mode | – | 0.8 | 3 | μA |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 5\text{ V}$]****Table 5.14 XCIN Input**

| Symbol | Parameter | Standard | | Unit |
|----------------|-----------------------|----------|------|---------------|
| | | Min. | Max. | |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | – | μs |
| $t_{WH(XCIN)}$ | XCIN input "H" width | 7 | – | μs |
| $t_{WL(XCIN)}$ | XCIN input "L" width | 7 | – | μs |

**Figure 5.3 XCIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.15 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|-----------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 100 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input "H" width | 40 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input "L" width | 40 | – | ns |

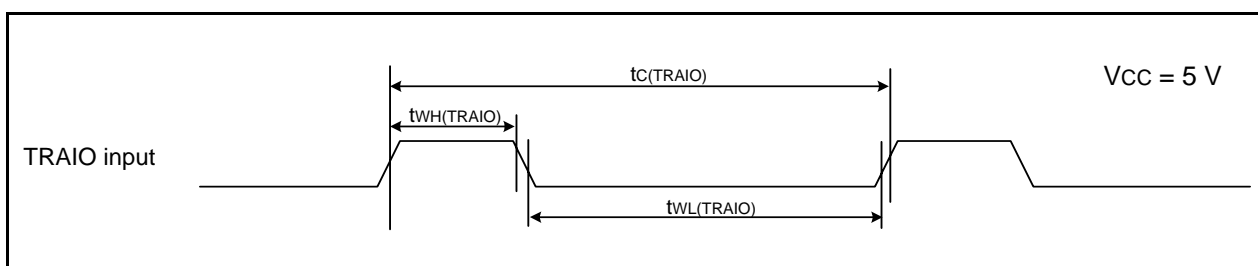
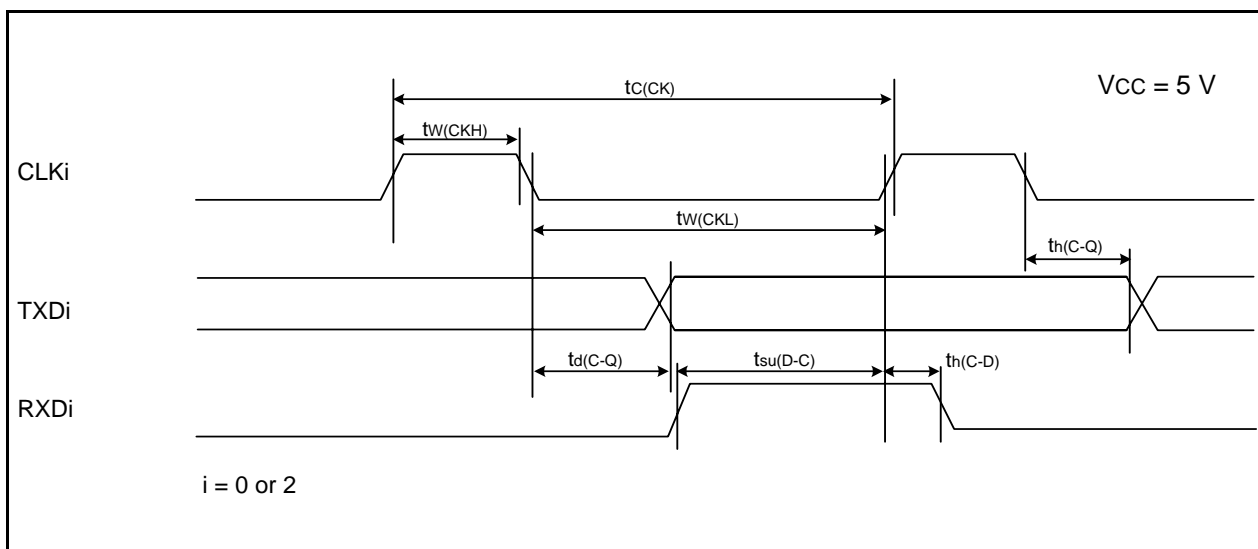
**Figure 5.4 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.16 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 200 | — | ns |
| $t_{w(CKH)}$ | CLKi input "H" width | 100 | — | ns |
| $t_{w(CKL)}$ | CLKi input "L" width | 100 | — | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | — | 50 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | — | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 50 | — | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | — | ns |

i = 0 or 2

**Figure 5.5 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.17 External Interrupt \overline{INTi} (i = 0 or 1) Input**

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|--------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | \overline{INTi} input "H" width | 250 ⁽¹⁾ | — | ns |
| $t_{w(INL)}$ | \overline{INTi} input "L" width | 250 ⁽²⁾ | — | ns |

NOTES:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

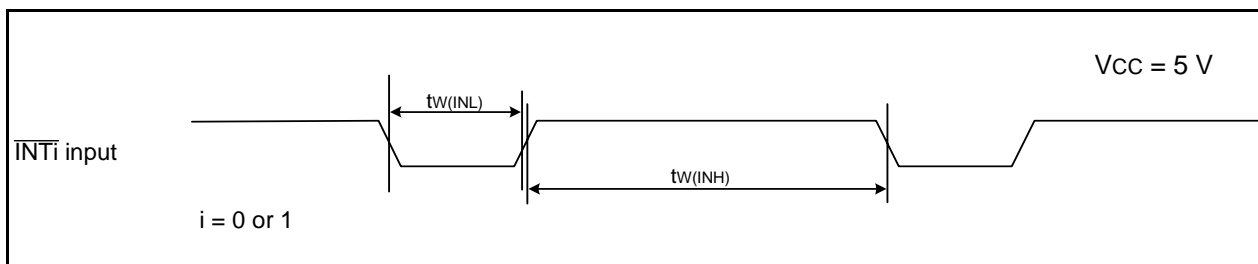
**Figure 5.6 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 5 V**

Table 5.18 Electrical Characteristics (3) [V_{CC} = 3 V]

| Symbol | Parameter | | Condition | Standard | | | Unit |
|----------------------------------|---------------------|---|---|-----------------------|------|-----------------|------|
| | | | | Min. | Typ. | Max. | |
| V _{OH} | Output "H" voltage | | I _{OH} = -1 mA | V _{CC} - 0.5 | — | V _{CC} | V |
| V _{OL} | Output "L" voltage | | I _{OL} = 1 mA | — | — | 0.5 | V |
| V _{T+} -V _{T-} | Hysteresis | $\overline{\text{INT0}}, \overline{\text{INT1}},$ $\overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}},$ $\overline{\text{RXD0}}, \overline{\text{RXD2}},$ $\overline{\text{CLK0}}, \overline{\text{CLK2}}$ | | 0.1 | 0.3 | — | V |
| | | $\overline{\text{RESET}}$ | | 0.1 | 0.4 | — | V |
| I _{IH} | Input "H" current | | V _I = 3 V, V _{CC} = 3 V | — | — | 4.0 | μA |
| I _{IL} | Input "L" current | | V _I = 0 V, V _{CC} = 3 V | — | — | -4.0 | μA |
| R _{PULLUP} | Pull-up resistance | | V _I = 0 V, V _{CC} = 3 V | 66 | 160 | 500 | kΩ |
| R _{FXCIN} | Feedback resistance | XCIN | | — | 18 | — | MΩ |
| V _{RAM} | RAM hold voltage | | During stop mode | 1.8 | — | — | V |

NOTE:

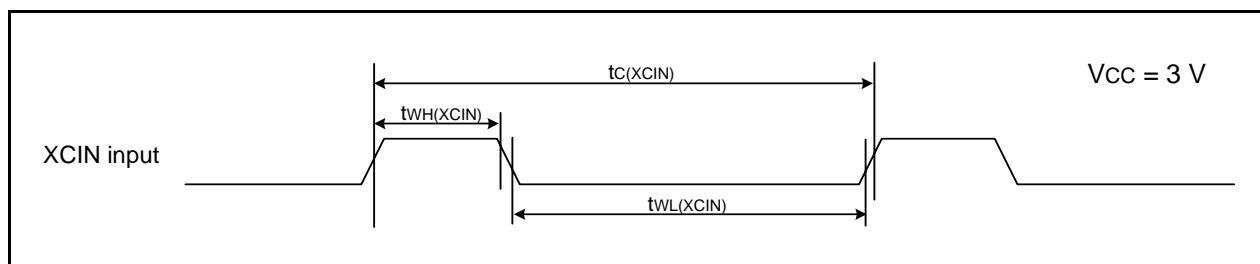
- V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.19 Electrical Characteristics (4) [V_{CC} = 3 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

| Symbol | Parameter | Condition | Standard | | | Unit |
|-----------------|--|--|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| I _{CC} | Power supply current (V _{CC} = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V _{SS} | High-speed on-chip oscillator mode | — | 5 | — | mA |
| | | | | | | |
| | | High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division | — | 2 | — | mA |
| | | | | | | |
| | | High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | — | 2 | — | mA |
| | | | | | | |
| | | Low-speed on-chip oscillator mode | — | 130 | 300 | μA |
| | | | | | | |
| | | Low-speed clock mode | — | 130 | 300 | μA |
| | | | | | | |
| | | Low-speed clock mode | — | 30 | — | μA |
| | | | | | | |
| | | Wait mode | — | 25 | 70 | μA |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | Stop mode | — | 0.7 | 3 | μA |
| | | | | | | |
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Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.20 XCIN Input**

| Symbol | Parameter | Standard | | Unit |
|-----------------------|-----------------------|----------|------|---------------|
| | | Min. | Max. | |
| $t_c(\text{XCIN})$ | XCIN input cycle time | 14 | – | μs |
| $t_{WH}(\text{XCIN})$ | XCIN input "H" width | 7 | – | μs |
| $t_{WL}(\text{XCIN})$ | XCIN input "L" width | 7 | – | μs |

**Figure 5.7 XCIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.21 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|------------------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_c(\text{TRAIO})$ | TRAIO input cycle time | 300 | – | ns |
| $t_{WH}(\text{TRAIO})$ | TRAIO input "H" width | 120 | – | ns |
| $t_{WL}(\text{TRAIO})$ | TRAIO input "L" width | 120 | – | ns |

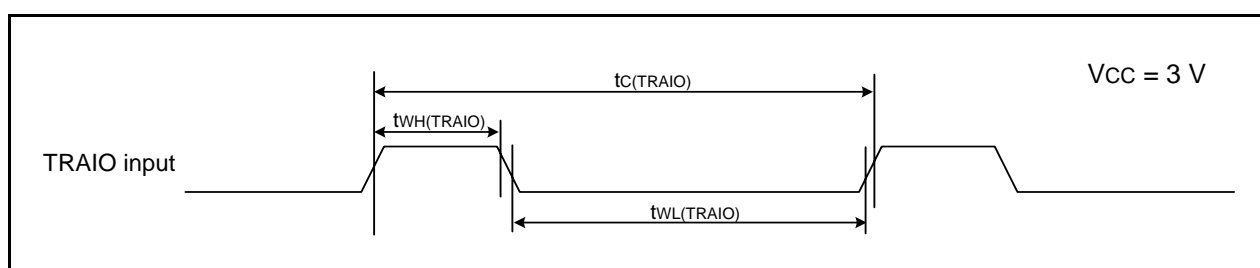
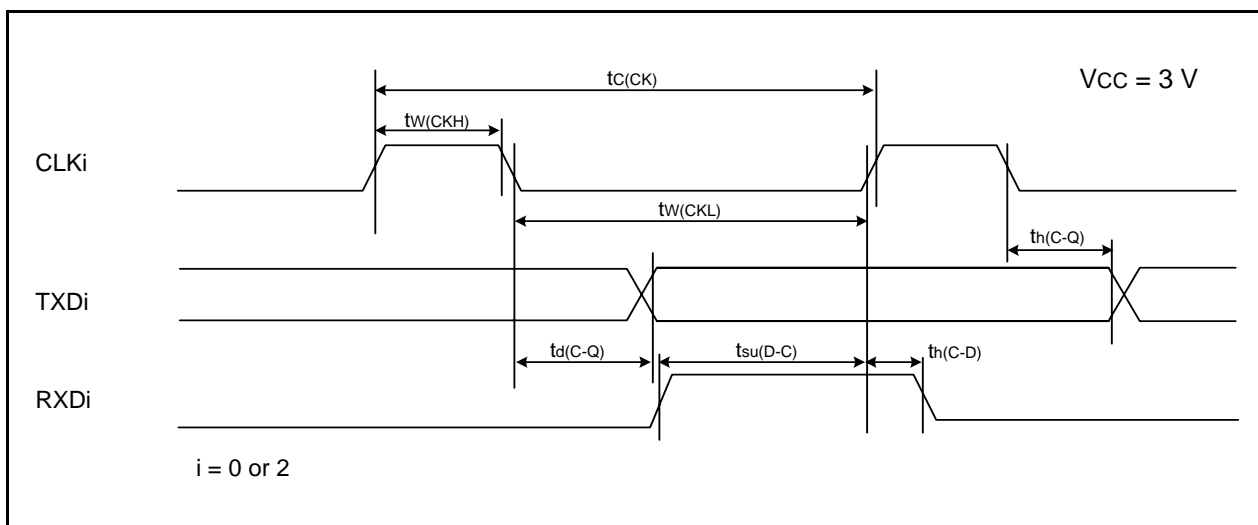
**Figure 5.8 TRAIO Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.22 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 300 | — | ns |
| $t_{w(CKH)}$ | CLKi input "H" width | 150 | — | ns |
| $t_{w(CKL)}$ | CLKi Input "L" width | 150 | — | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | — | 80 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | — | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | — | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | — | ns |

i = 0 or 2

**Figure 5.9 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.23 External Interrupt \overline{INTi} (i = 0 or 1) Input**

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|--------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | \overline{INTi} input "H" width | 380 ⁽¹⁾ | — | ns |
| $t_{w(INL)}$ | \overline{INTi} input "L" width | 380 ⁽²⁾ | — | ns |

NOTES:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

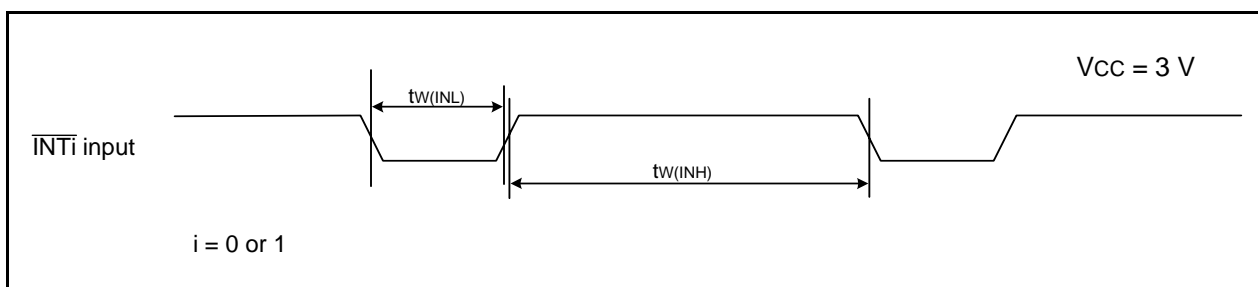
**Figure 5.10 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 3 V**

Table 5.24 Electrical Characteristics (5) [V_{CC} = 2.2 V]

| Symbol | Parameter | | Condition | Standard | | | Unit |
|----------------------------------|---------------------|---|-------------------------|-----------------------|------|-----------------|------|
| | | | | Min. | Typ. | Max. | |
| V _{OH} | Output "H" voltage | | I _{OH} = -1 mA | V _{CC} - 0.5 | — | V _{CC} | V |
| V _{OL} | Output "L" voltage | | I _{OL} = 1 mA | — | — | 0.5 | V |
| V _{T+} -V _{T-} | Hysteresis | $\overline{\text{INT0}}, \overline{\text{INT1}},$ $\overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}},$ $\overline{\text{RXD0}}, \overline{\text{RXD2}},$ $\overline{\text{CLK0}}, \overline{\text{CLK2}}$ | | 0.05 | 0.3 | — | V |
| | | $\overline{\text{RESET}}$ | | 0.05 | 0.15 | — | V |
| I _{IH} | Input "H" current | | V _I = 2.2 V | — | — | 4.0 | μA |
| I _{IL} | Input "L" current | | V _I = 0 V | — | — | -4.0 | μA |
| R _{PULLUP} | Pull-up resistance | | V _I = 0 V | 100 | 200 | 600 | kΩ |
| R _{FXCIN} | Feedback resistance | XCIN | | — | 35 | — | MΩ |
| V _{RAM} | RAM hold voltage | | During stop mode | 1.8 | — | — | V |

NOTE:

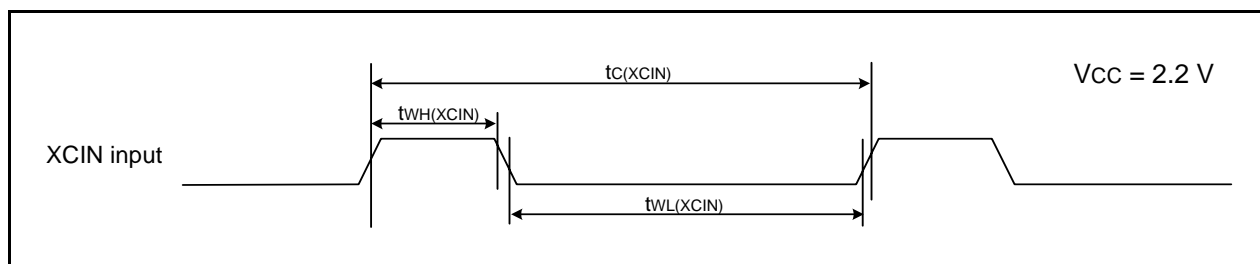
- V_{CC} = 2.2 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.25 Electrical Characteristics (6) [V_{CC} = 2.2 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

| Symbol | Parameter | Condition | Standard | | | Unit |
|-----------------|--|--|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| I _{CC} | Power supply current (V _{CC} = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are V _{SS} | High-speed on-chip oscillator mode | — | 3.5 | — | mA |
| | | | | | | |
| | | High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz No division | — | 1.5 | — | mA |
| | | | | | | |
| | | High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | — | 100 | 230 | μA |
| | | | | | | |
| | | Low-speed on-chip oscillator mode | — | 100 | 230 | μA |
| | | | | | | |
| | | Low-speed clock mode | — | 25 | — | μA |
| | | | | | | |
| | | Wait mode | — | 22 | 60 | μA |
| | | | | | | |
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| | | | | | | |
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| | | | | | | |
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| | | Stop mode | — | 0.7 | 3 | μA |
| | | | | | | |
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Timing requirements**(Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 2.2\text{ V}$]****Table 5.26 XCIN Input**

| Symbol | Parameter | Standard | | Unit |
|-----------------------|-----------------------|----------|------|---------------|
| | | Min. | Max. | |
| $t_c(\text{XCIN})$ | XCIN input cycle time | 14 | – | μs |
| $t_{WH}(\text{XCIN})$ | XCIN input "H" width | 7 | – | μs |
| $t_{WL}(\text{XCIN})$ | XCIN input "L" width | 7 | – | μs |

**Figure 5.11 XCIN Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.27 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|------------------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_c(\text{TRAIO})$ | TRAIO input cycle time | 500 | – | ns |
| $t_{WH}(\text{TRAIO})$ | TRAIO input "H" width | 200 | – | ns |
| $t_{WL}(\text{TRAIO})$ | TRAIO input "L" width | 200 | – | ns |

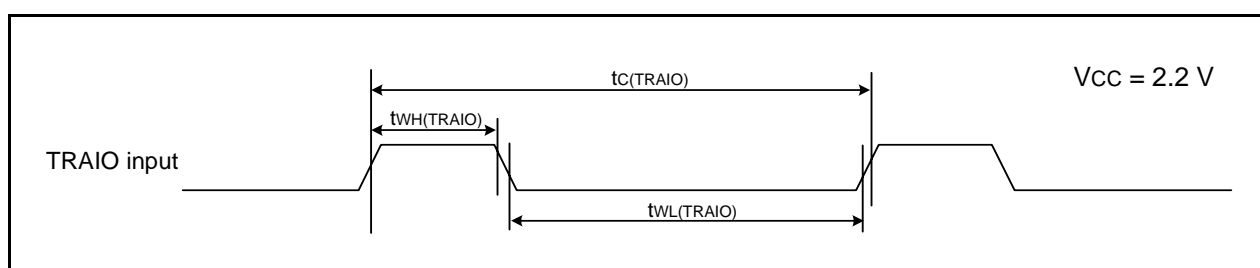
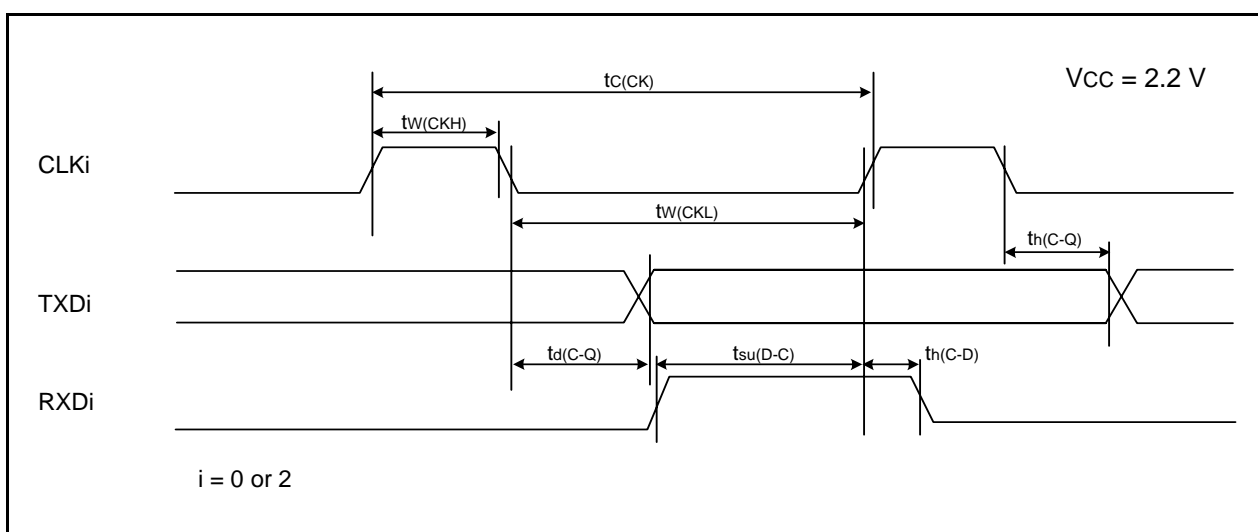
**Figure 5.12 TRAIO Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

Table 5.28 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 800 | — | ns |
| $t_{w(CKH)}$ | CLKi input "H" width | 400 | — | ns |
| $t_{w(CKL)}$ | CLKi input "L" width | 400 | — | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | — | 200 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | — | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 150 | — | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | — | ns |

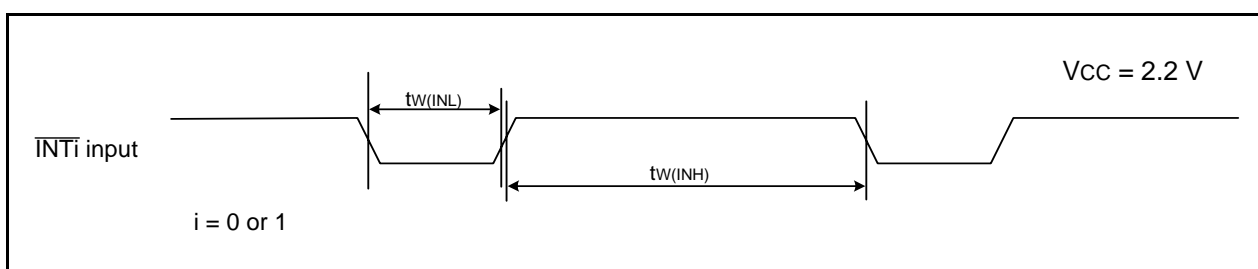
i = 0 or 2

**Figure 5.13 Serial Interface Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.29 External Interrupt \overline{INTi} (i = 0 or 1) Input**

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|---------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | \overline{INTi} input "H" width | 1000 ⁽¹⁾ | — | ns |
| $t_{w(INL)}$ | \overline{INTi} input "L" width | 1000 ⁽²⁾ | — | ns |

NOTES:

- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.

**Figure 5.14 External Interrupt \overline{INTi} Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

5.2 R8C/2J Group

Table 5.30 Absolute Maximum Ratings

| Symbol | Parameter | Condition | Rated Value | Unit |
|------------------|-------------------------------|-------------------------|--|------|
| V _{CC} | Supply voltage | | –0.3 to 6.5 | V |
| V _I | Input voltage | | –0.3 to V _{CC} + 0.3 | V |
| V _O | Output voltage | | –0.3 to V _{CC} + 0.3 | V |
| P _d | Power dissipation | T _{opr} = 25°C | 500 | mW |
| T _{opr} | Operating ambient temperature | | –20 to 85 (N version) / –40 to 85 (D version) | °C |
| T _{stg} | Storage temperature | | –65 to 150 | °C |

Table 5.31 Recommended Operating Conditions

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|-----------------------|---------------------------------|---------------------------------------|--|---------------------|------|---------------------|------|
| | | | | Min. | Typ. | Max. | |
| V _{CC} | Supply voltage | | | 2.2 | – | 5.5 | V |
| V _{SS} | Supply voltage | | | – | 0 | – | V |
| V _{IH} | Input “H” voltage | | | 0.8 V _{CC} | – | V _{CC} | V |
| V _{IL} | Input “L” voltage | | | 0 | – | 0.2 V _{CC} | V |
| I _{OH(sum)} | Peak sum output “H” current | Sum of all pins I _{OH(peak)} | | – | – | –160 | mA |
| I _{OH(sum)} | Average sum output “H” current | Sum of all pins I _{OH(avg)} | | – | – | –80 | mA |
| I _{OH(peak)} | Peak output “H” current | All pins | | – | – | –10 | mA |
| I _{OH(avg)} | Average output “H” current | All pins | | – | – | –5 | mA |
| I _{OL(sum)} | Peak sum output “L” currents | Sum of all pins I _{OL(peak)} | | – | – | 160 | mA |
| I _{OL(sum)} | Average sum output “L” currents | Sum of all pins I _{OL(avg)} | | – | – | 80 | mA |
| I _{OL(peak)} | Peak output “L” currents | All pins | | – | – | 10 | mA |
| I _{OL(avg)} | Average output “L” current | All pins | | – | – | 5 | mA |
| – | System clock | | HRA01 = 0 Low-speed on-chip oscillator selected | – | 125 | – | kHz |
| | | | HRA01 = 1 High-speed on-chip oscillator selected 2.7 V ≤ V _{CC} ≤ 5.5 V | – | – | 8 | MHz |
| | | | HRA01 = 1 High-speed on-chip oscillator selected 2.2 V ≤ V _{CC} ≤ 5.5 V | – | – | 4 | MHz |

NOTES:

- V_{CC} = 2.2 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
- The average output current indicates the average value of current measured during 100 ms.

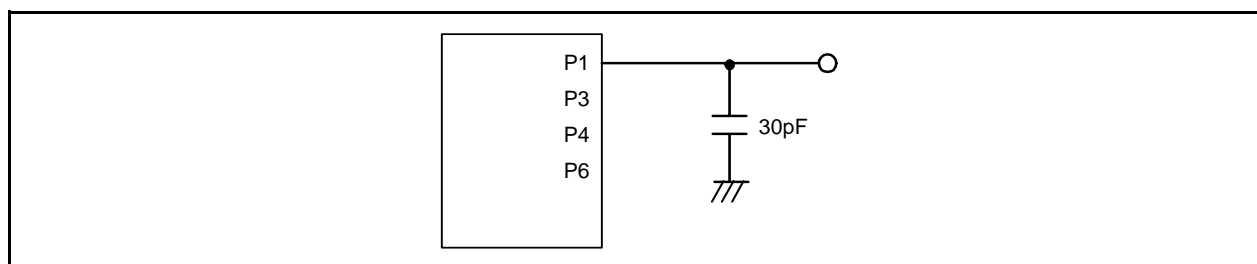

Figure 5.15 Ports P1, P3, P4, and P6 Timing Measurement Circuit

Table 5.32 Flash Memory (Program ROM) Electrical Characteristics

| Symbol | Parameter | Conditions | Standard | | | Unit |
|--------|--|----------------------------|--------------------|------|------|-------|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance ⁽²⁾ | | 100 ⁽³⁾ | – | – | times |
| – | Byte program time | | – | 50 | 400 | μs |
| – | Block erase time | | – | 0.4 | 9 | s |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.2 | – | 5.5 | V |
| – | Program, erase temperature | | 0 | – | 60 | °C |
| – | Data hold time ⁽⁷⁾ | Ambient temperature = 55°C | 20 | – | – | year |

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.33 Voltage Detection 0 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det0} | Voltage detection level | | 2.2 | 2.3 | 2.4 | V |
| — | Voltage detection circuit self power consumption | VCA25 = 1, V _{CC} = 5.0 V | — | 0.9 | — | μA |
| t _{d(E-A)} | Waiting time until voltage detection circuit operation starts ⁽²⁾ | | — | — | 300 | μs |
| V _{ccmin} | MCU operating voltage minimum value | | 2.2 | — | — | V |

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.34 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det1} | Voltage detection level ⁽⁴⁾ | | 2.70 | 2.85 | 3.00 | V |
| — | Voltage monitor 1 interrupt request generation time ⁽²⁾ | | — | 40 | — | μs |
| — | Voltage detection circuit self power consumption | VCA26 = 1, V _{CC} = 5.0 V | — | 0.6 | — | μA |
| t _{d(E-A)} | Waiting time until voltage detection circuit operation starts ⁽³⁾ | | — | — | 100 | μs |

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.35 Voltage Detection 2 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det2} | Voltage detection level | | 3.3 | 3.6 | 3.9 | V |
| — | Voltage monitor 2 interrupt request generation time ⁽²⁾ | | — | 40 | — | μs |
| — | Voltage detection circuit self power consumption | VCA27 = 1, V _{CC} = 5.0 V | — | 0.6 | — | μA |
| t _{d(E-A)} | Waiting time until voltage detection circuit operation starts ⁽³⁾ | | — | — | 100 | μs |

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.36 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics⁽³⁾

| Symbol | Parameter | Condition | Standard | | | Unit |
|-------------------|---|-----------|----------|------|-------------------|---------|
| | | | Min. | Typ. | Max. | |
| V _{por1} | Power-on reset valid voltage ⁽⁴⁾ | | – | – | 0.1 | V |
| V _{por2} | Power-on reset or voltage monitor 0 reset valid voltage | | 0 | – | V _{det0} | V |
| tr _{th} | External power V _{CC} rise gradient ⁽²⁾ | | 20 | – | – | mV/msec |

NOTES:

1. The measurement condition is $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. $t_{w(port)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{port}) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(port)}$ for 30 s or more if $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$, maintain $t_{w(port)}$ for 3,000 s or more if $-40^{\circ}\text{C} \leq T_{opr} < -20^{\circ}\text{C}$.

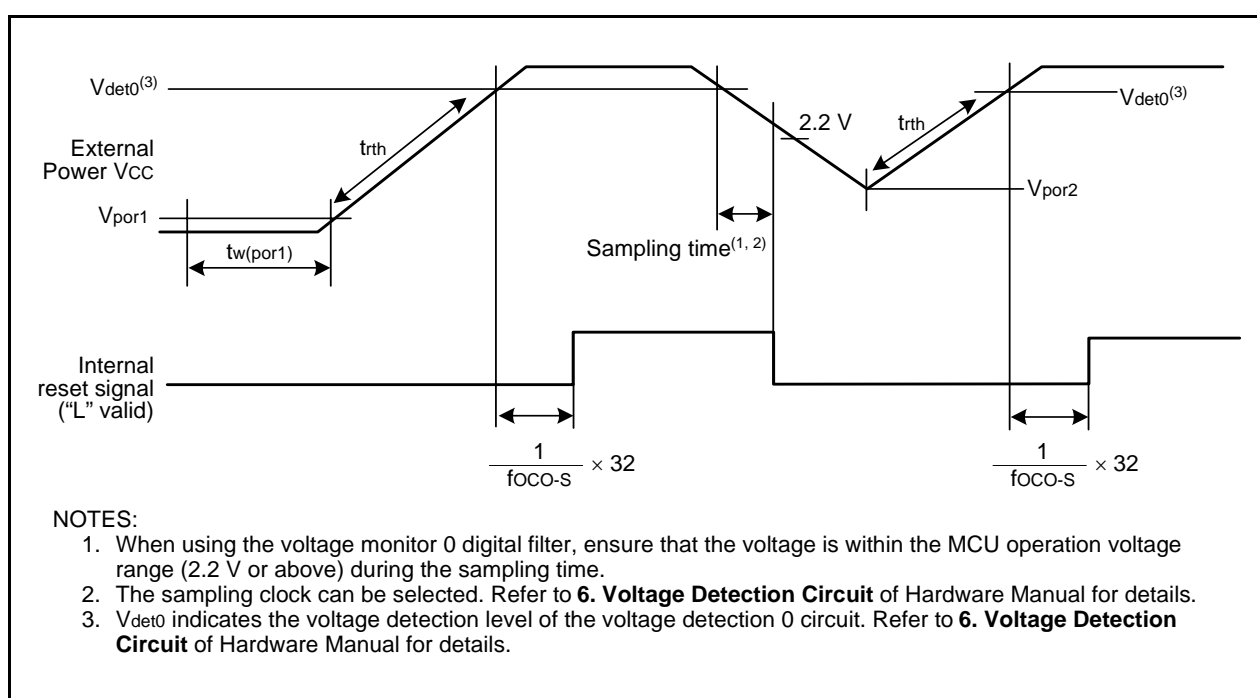


Figure 5.16 Reset Circuit Electrical Characteristics

Table 5.37 Comparator Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|---|---|----------|------|-----------|------|
| | | | Min. | Typ. | Max. | |
| Vref | Internal reference voltage | VCC = 2.2 V to 5.5 V, T _{opr} = 25°C | 1.15 | 1.25 | 1.35 | V |
| | | VCC = 2.2 V to 5.5 V, T _{opr} = -40 to 85°C | — | 1.25 | — | V |
| Vcref | External input reference voltage | VCC = 2.2 V to 4.0 V | 0.5 | — | VCC - 1.1 | V |
| | | VCC = 4.0 V to 5.5 V | 0.5 | — | VCC - 1.5 | V |
| Vcin | External comparison voltage input range | | -0.3 | — | VCC + 0.3 | V |
| Vofs | Input offset voltage | | — | 20 | 120 | mV |
| Tcrsp | Response time | | — | 4 | — | μs |

NOTE:

1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.38 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|--|---|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| fOCO-F | High-speed on-chip oscillator frequency temperature • supply voltage dependence | VCC = 4.75 V to 5.25 V T _{opr} = 0 to 60°C ⁽²⁾ | 7.76 | 8 | 8.24 | MHz |
| | | VCC = 2.7 V to 5.5 V T _{opr} = -20 to 85°C ⁽²⁾ | 7.68 | 8 | 8.32 | MHz |
| | | VCC = 2.7 V to 5.5 V T _{opr} = -40 to 85°C ⁽²⁾ | 7.44 | 8 | 8.32 | MHz |
| | | VCC = 2.2 V to 5.5 V T _{opr} = -20 to 85°C ⁽³⁾ | 7.04 | 8 | 8.96 | MHz |
| | | VCC = 2.2 V to 5.5 V T _{opr} = -40 to 85°C ⁽³⁾ | 6.8 | 8 | 9.2 | MHz |

NOTES:

1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the HRA1 register is set to the value before shipment and the HRA2 register is set to 00h.
3. These standard values show when the correction value in the FRA6 register is written into the HRA1 register.

Table 5.39 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|--|--------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 30 | 125 | 250 | kHz |
| — | Oscillation stability time | | — | 10 | 100 | μs |
| — | Self power consumption at oscillation | VCC = 5.0 V, T _{opr} = 25°C | — | 15 | — | μA |

NOTE:

1. VCC = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.40 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|----------------------|---|-----------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| t _d (P-R) | Time for internal power supply stabilization during power-on ⁽²⁾ | | 1 | — | 2000 | μs |
| t _d (R-S) | STOP exit time ⁽³⁾ | | — | — | 150 | μs |

NOTES:

1. The measurement condition is VCC = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.41 Electrical Characteristics (1) [V_{CC} = 5 V]

| Symbol | Parameter | | Condition | Standard | | | Unit |
|----------------------------------|--------------------|--|---|-----------------------|------|-----------------|------|
| | | | | Min. | Typ. | Max. | |
| V _{OH} | Output "H" voltage | | I _{OH} = -5 mA | V _{CC} - 2.0 | — | V _{CC} | V |
| | | | I _{OH} = -200 μA | V _{CC} - 0.5 | — | V _{CC} | V |
| V _{OL} | Output "L" voltage | | I _{OL} = 5 mA | — | — | 2.0 | V |
| | | | I _{OL} = 200 μA | — | — | 0.45 | V |
| V _{T+} -V _{T-} | Hysteresis | $\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}}, \overline{\text{RXD0}}, \overline{\text{CLK0}}$ | | 0.1 | 0.5 | — | V |
| | | $\overline{\text{RESET}}$ | | 0.1 | 1.0 | — | V |
| I _{IH} | Input "H" current | | V _I = 5 V, V _{CC} = 5 V | — | — | 5.0 | μA |
| I _{IL} | Input "L" current | | V _I = 0 V, V _{CC} = 5 V | — | — | -5.0 | μA |
| R _{PULLUP} | Pull-up resistance | | V _I = 0 V, V _{CC} = 5 V | 30 | 50 | 167 | kΩ |
| V _{RAM} | RAM hold voltage | | During stop mode | 2.0 | — | — | V |

NOTE:

- V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.42 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

| Symbol | Parameter | Condition | | Standard | | | Unit |
|--------|--|--|---|----------|------|------|------|
| | | | | Min. | Typ. | Max. | |
| Icc | Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss | High-speed on-chip oscillator mode | High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division | – | 5 | 8 | mA |
| | | | High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 2 | – | mA |
| | | Low-speed on-chip oscillator mode | High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1 | – | 130 | 300 | μA |
| | | Wait mode | High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 25 | 75 | μA |
| | | | High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 23 | 60 | μA |
| | | Stop mode | Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1) | – | 0.8 | 3 | μA |
| | | | Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1) | – | 1.2 | – | μA |
| | | | Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0) | – | 5 | 8 | μA |
| | | | Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0) | – | 5.5 | – | μA |

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 5\text{ V}$]****Table 5.43 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|------------------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_c(\text{TRAIO})$ | TRAIO input cycle time | 100 | – | ns |
| $t_{WH}(\text{TRAIO})$ | TRAIO input "H" width | 40 | – | ns |
| $t_{WL}(\text{TRAIO})$ | TRAIO input "L" width | 40 | – | ns |

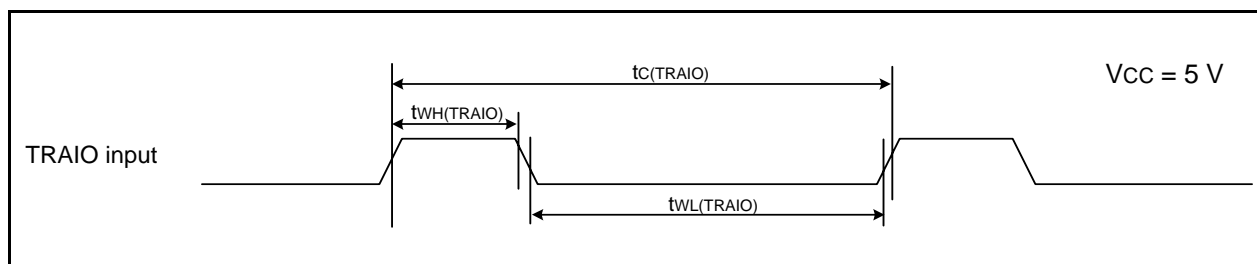
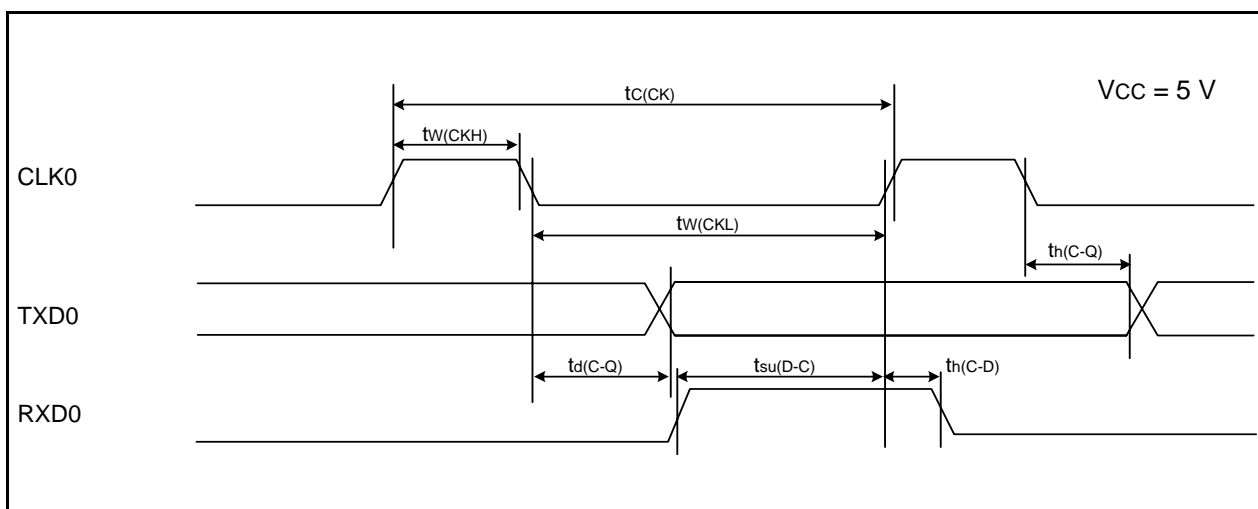
**Figure 5.17 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.44 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLK0 input cycle time | 200 | — | ns |
| $t_{w(CKH)}$ | CLK0 input “H” width | 100 | — | ns |
| $t_{w(CKL)}$ | CLK0 input “L” width | 100 | — | ns |
| $t_{d(C-Q)}$ | TXD0 output delay time | — | 50 | ns |
| $t_{h(C-Q)}$ | TXD0 hold time | 0 | — | ns |
| $t_{su(D-C)}$ | RXD0 input setup time | 50 | — | ns |
| $t_{h(C-D)}$ | RXD0 input hold time | 90 | — | ns |

**Figure 5.18 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.45 External Interrupt \overline{INTi} ($i = 0$ or 1) Input**

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|--------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | \overline{INTi} input “H” width | 250 ⁽¹⁾ | — | ns |
| $t_{w(INL)}$ | \overline{INTi} input “L” width | 250 ⁽²⁾ | — | ns |

NOTES:

- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

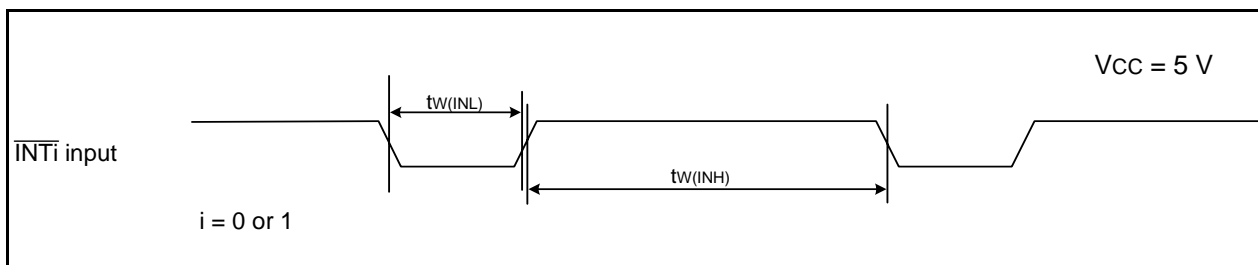
**Figure 5.19 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 5 V**

Table 5.46 Electrical Characteristics (3) [V_{CC} = 3 V]

| Symbol | Parameter | | Condition | Standard | | | Unit |
|----------------------------------|--------------------|--|---|-----------------------|------|-----------------|------|
| | | | | Min. | Typ. | Max. | |
| V _{OH} | Output "H" voltage | | I _{OH} = -1 mA | V _{CC} - 0.5 | — | V _{CC} | V |
| V _{OL} | Output "L" voltage | | I _{OL} = 1 mA | — | — | 0.5 | V |
| V _{T+} -V _{T-} | Hysteresis | $\overline{\text{INT0}}, \overline{\text{INT1}},$ $\overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}},$ $\overline{\text{RXD0}}, \overline{\text{CLK0}}$ | | 0.1 | 0.3 | — | V |
| | | $\overline{\text{RESET}}$ | | 0.1 | 0.4 | — | V |
| I _{IH} | Input "H" current | | V _I = 3 V, V _{CC} = 3 V | — | — | 4.0 | μA |
| I _{IL} | Input "L" current | | V _I = 0 V, V _{CC} = 3 V | — | — | -4.0 | μA |
| R _{PULLUP} | Pull-up resistance | | V _I = 0 V, V _{CC} = 3 V | 66 | 160 | 500 | kΩ |
| V _{RAM} | RAM hold voltage | | During stop mode | 1.8 | — | — | V |

NOTE:

- V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.47 Electrical Characteristics (4) [V_{CC} = 3 V]
(T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

| Symbol | Parameter | Condition | Standard | | | Unit | |
|--------|---|--|---|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| Icc | Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss | High-speed on-chip oscillator mode | High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division | – | 5 | – | mA |
| | | | High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 2 | – | mA |
| | | Low-speed on-chip oscillator mode | High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1 | – | 130 | 300 | μA |
| | | Wait mode | High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 25 | 70 | μA |
| | | | High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 23 | 55 | μA |
| | | Stop mode | Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1) | – | 0.7 | 3 | μA |
| | | | Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1) | – | 1.1 | – | μA |
| | | | Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0) | – | 5 | 7 | μA |
| | | Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0) | – | 5.5 | – | μA | |

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.48 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|------------------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_c(\text{TRAIO})$ | TRAIO input cycle time | 300 | – | ns |
| $t_{WH}(\text{TRAIO})$ | TRAIO input "H" width | 120 | – | ns |
| $t_{WL}(\text{TRAIO})$ | TRAIO input "L" width | 120 | – | ns |

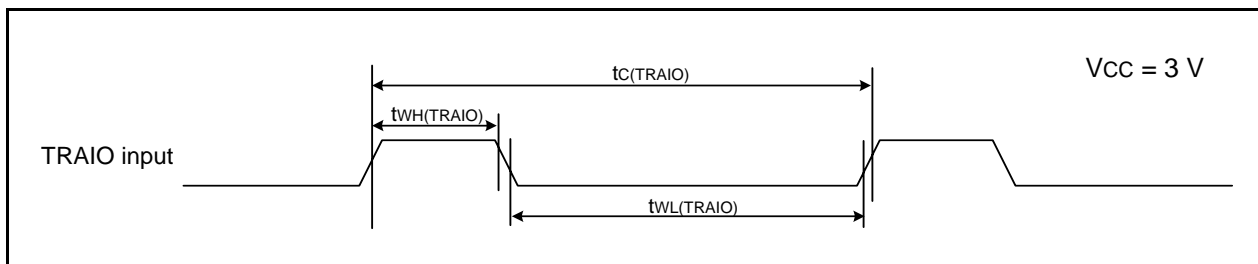
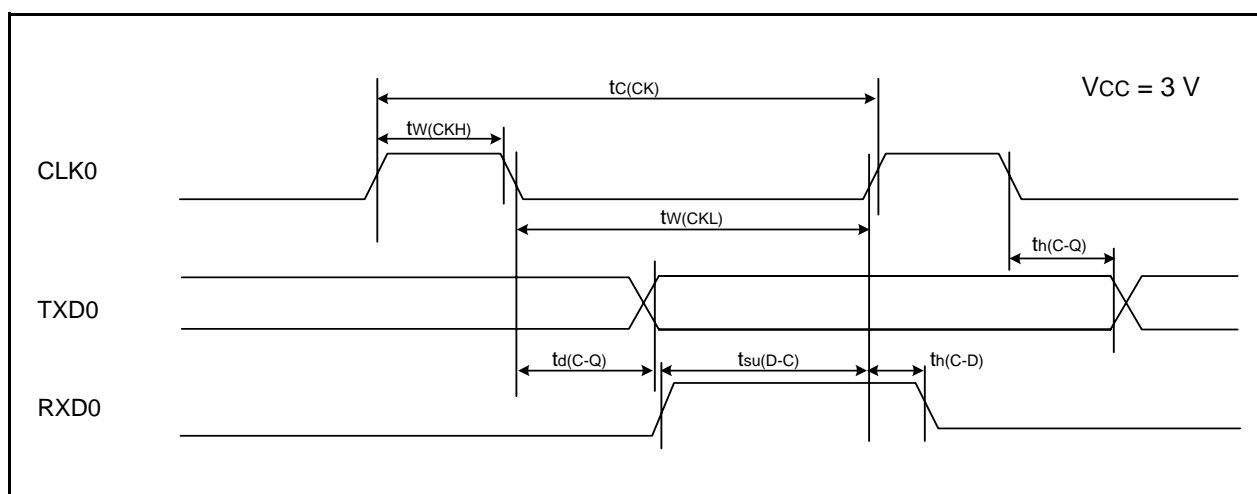
**Figure 5.20 TRAIO Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.49 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLK0 input cycle time | 300 | — | ns |
| $t_{w(CKH)}$ | CLK0 input "H" width | 150 | — | ns |
| $t_{w(CKL)}$ | CLK0 Input "L" width | 150 | — | ns |
| $t_{d(C-Q)}$ | TXD0 output delay time | — | 80 | ns |
| $t_{h(C-Q)}$ | TXD0 hold time | 0 | — | ns |
| $t_{su(D-C)}$ | RXD0 input setup time | 70 | — | ns |
| $t_{h(C-D)}$ | RXD0 input hold time | 90 | — | ns |

**Figure 5.21 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.50 External Interrupt \overline{INTi} (i = 0 or 1) Input**

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|--------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | \overline{INTi} input "H" width | 380 ⁽¹⁾ | — | ns |
| $t_{w(INL)}$ | \overline{INTi} input "L" width | 380 ⁽²⁾ | — | ns |

NOTES:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

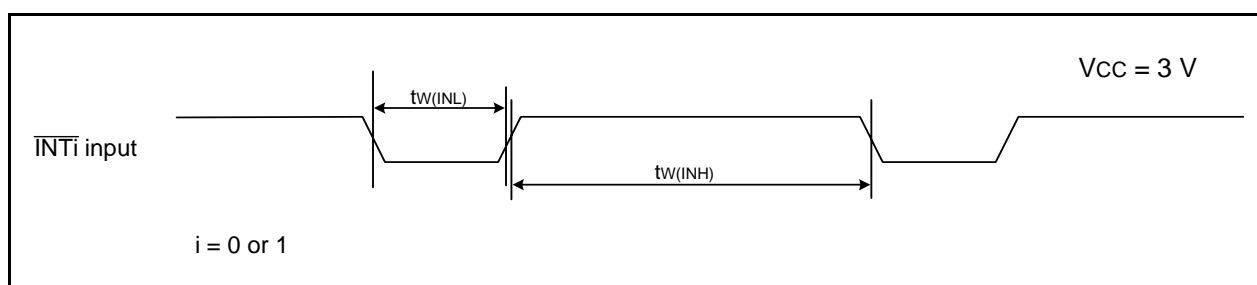
**Figure 5.22 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 3 V**

Table 5.51 Electrical Characteristics (5) [V_{CC} = 2.2 V]

| Symbol | Parameter | | Condition | Standard | | | Unit |
|----------------------------------|---------------------|--|-------------------------|-----------------------|------|-----------------|------|
| | | | | Min. | Typ. | Max. | |
| V _{OH} | Output "H" voltage | | I _{OH} = -1 mA | V _{CC} - 0.5 | — | V _{CC} | V |
| V _{OL} | Output "L" voltage | | I _{OL} = 1 mA | — | — | 0.5 | V |
| V _{T+} -V _{T-} | Hysteresis | $\overline{\text{INT0}}, \overline{\text{INT1}},$ $\overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}},$ $\overline{\text{RXD0}}, \overline{\text{CLK0}}$ | | 0.05 | 0.3 | — | V |
| | | $\overline{\text{RESET}}$ | | 0.05 | 0.15 | — | V |
| I _{IH} | Input "H" current | | V _I = 2.2 V | — | — | 4.0 | μA |
| I _{IL} | Input "L" current | | V _I = 0 V | — | — | -4.0 | μA |
| R _{PULLUP} | Pull-up resistance | | V _I = 0 V | 100 | 200 | 600 | kΩ |
| R _{XCIN} | Feedback resistance | XCIN | | — | 35 | — | MΩ |
| V _{RAM} | RAM hold voltage | | During stop mode | 1.8 | — | — | V |

NOTE:

- V_{CC} = 2.2 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.52 Electrical Characteristics (6) [$V_{CC} = 2.2\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version) / $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

| Symbol | Parameter | Condition | Standard | | | Unit | |
|--------|---|------------------------------------|---|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| Icc | Power supply current (Vcc = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss | High-speed on-chip oscillator mode | High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz No division | – | 3.5 | – | mA |
| | | | High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 1.5 | – | mA |
| | | Low-speed on-chip oscillator mode | High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1 | – | 100 | 230 | μA |
| | | Wait mode | High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 22 | 60 | μA |
| | | | High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 20 | 55 | μA |
| | | Stop mode | Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1) | – | 0.7 | 3 | μA |
| | | | Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1) | – | 1.1 | – | μA |
| | | | Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0) | – | 5 | 7 | μA |
| | | | Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0) | – | 5.5 | – | μA |

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 2.2\text{ V}$]****Table 5.53 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|------------------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_c(\text{TRAIO})$ | TRAIO input cycle time | 500 | – | ns |
| $t_{WH}(\text{TRAIO})$ | TRAIO input "H" width | 200 | – | ns |
| $t_{WL}(\text{TRAIO})$ | TRAIO input "L" width | 200 | – | ns |

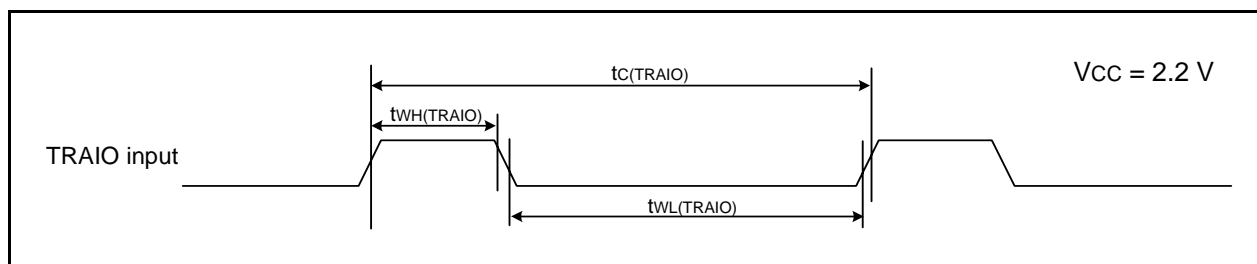
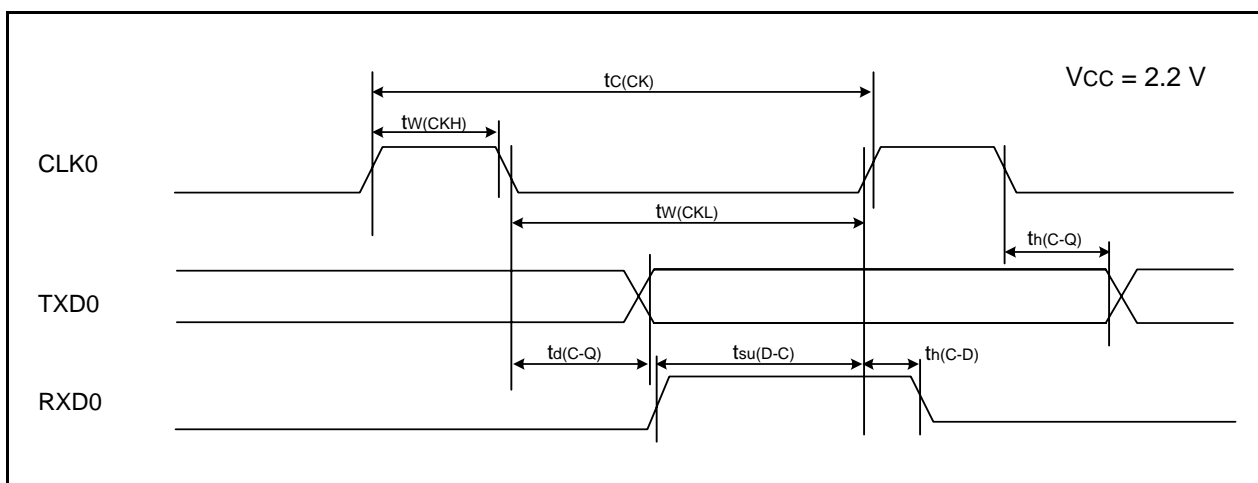
**Figure 5.23 TRAIO Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

Table 5.54 Serial Interface

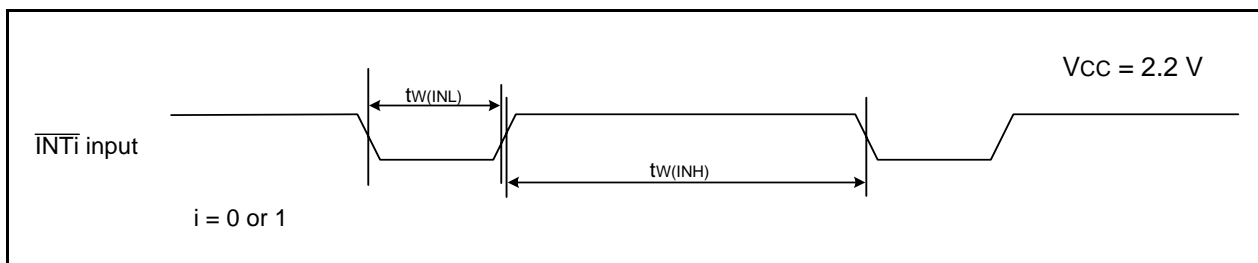
| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLK0 input cycle time | 800 | — | ns |
| $t_{w(CKH)}$ | CLK0 input "H" width | 400 | — | ns |
| $t_{w(CKL)}$ | CLK0 input "L" width | 400 | — | ns |
| $t_{d(C-Q)}$ | TXD0 output delay time | — | 200 | ns |
| $t_{h(C-Q)}$ | TXD0 hold time | 0 | — | ns |
| $t_{su(D-C)}$ | RXD0 input setup time | 150 | — | ns |
| $t_{h(C-D)}$ | RXD0 input hold time | 90 | — | ns |

**Figure 5.24 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.55 External Interrupt \overline{INTi} ($i = 0$ or 1) Input**

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|---------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | \overline{INTi} input "H" width | 1000 ⁽¹⁾ | — | ns |
| $t_{w(INL)}$ | \overline{INTi} input "L" width | 1000 ⁽²⁾ | — | ns |

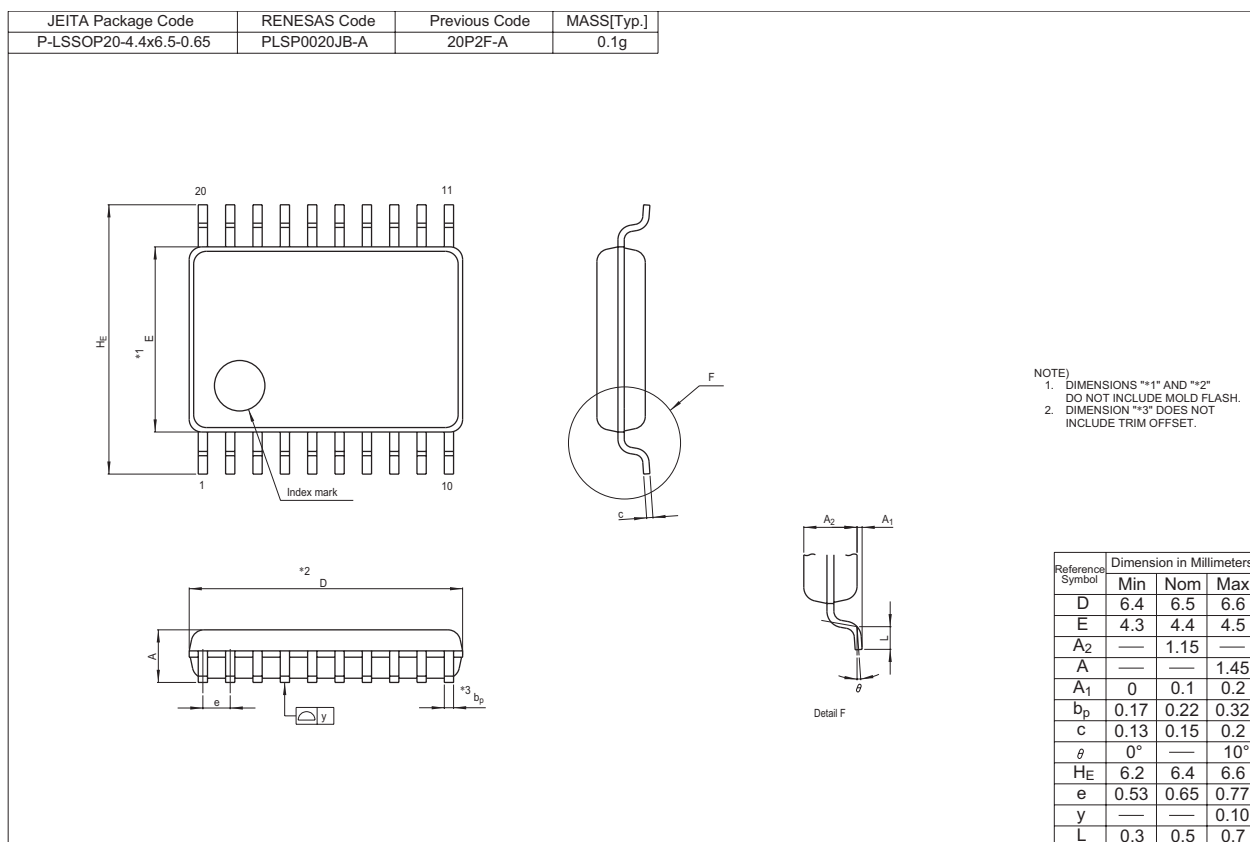
NOTES:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.

**Figure 5.25 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 2.2 V**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.



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| REVISION HISTORY | R8C/2H Group, R8C/2J Group Datasheet |
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| Rev. | Date | Description | |
|------|--------------|-------------|--|
| | | Page | Summary |
| 0.01 | Jun 18, 2007 | – | First Edition issued |
| 0.10 | Jul 20, 2007 | 20 | Table 4.2: 0038h After reset; “0000X010b” → “1000X010b”, “0100X011b” → “1100X011b” |
| | | 31 to 64 | 5. Electrical Characteristics added |
| 0.20 | Nov 12, 2007 | 2 | Table 1.1 I/O Ports: “• Output-only: 1” added |
| | | | “• CMOS I/O ports: 16” → “• CMOS I/O ports: 15” |
| | | 6 | Figure 1.3 revised |
| | | 8 | Figure 1.5 revised |
| | | 9 | Table 1.5 Pin Number: 4, 6, 16 revised |
| | | 12 | Table 1.7 I/O port: “P4_3 to P4_5” → “P4_3, P4_5” |
| | | | Timer RE, Output port added |
| | | 19 | Table 4.1 0006h “01001000b” → “01011000b” |
| | | 23 | Table 4.5 0118h to 011Dh: After reset revised 011Fh “Timer RE Real-Time Clock Precision Adjust Register” added |
| | | 31, 48 | Table 5.2, Table 5.31 NOTE2 revised |
| 1.00 | Mar 28, 2008 | 54, 58 | Table 5.42, Table 5.47 revised |
| | | 62 | Table 5.52 revised |
| | | All pages | “Under development” deleted |
| | | 2, 3 | Table 1.1, Table 1.2 revised |
| | | 4, 5 | Table 1.3, Table 1.4; “(D): Under development” deleted |
| | | 17, 18 | Figure 3.1, Figure 3.2; “Expanded area” deleted |
| | | 19 | Table 4.1 “002Eh” “002Fh” revised |
| | | 20 | Table 4.2 “003Eh” “003Fh” revised |
| | | 32 | Table 5.3 revised Old Figure 5.2 deleted |
| | | 35 | Table 5.8, Table 5.11 revised Table 5.9 revised, NOTE3 added |
| | | 37 | Table 5.13 revised |
| | | 41 | Table 5.19 revised |
| | | 45 | Table 5.25 revised |
| | | 49 | Table 5.32 revised Old Figure 5.17 deleted |
| | | 52 | Table 5.37, Table 5.40 revised Table 5.38 revised, NOTE3 added |
| | | 54 | Table 5.42 revised |
| | | 58 | Table 5.47 revised |

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| REVISION HISTORY | R8C/2H Group, R8C/2J Group Datasheet |
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| Rev. | Date | Description | |
|------|--------------|-------------|--------------------|
| | | Page | Summary |
| 1.00 | Mar 28, 2008 | 62 | Table 5.52 revised |
| | | | |

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Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
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Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
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1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
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Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510