TS1108 Data Sheet

TS1108 Coulomb Counter: Bidirectional Current Sense Amplifier with Integrator + Comparator

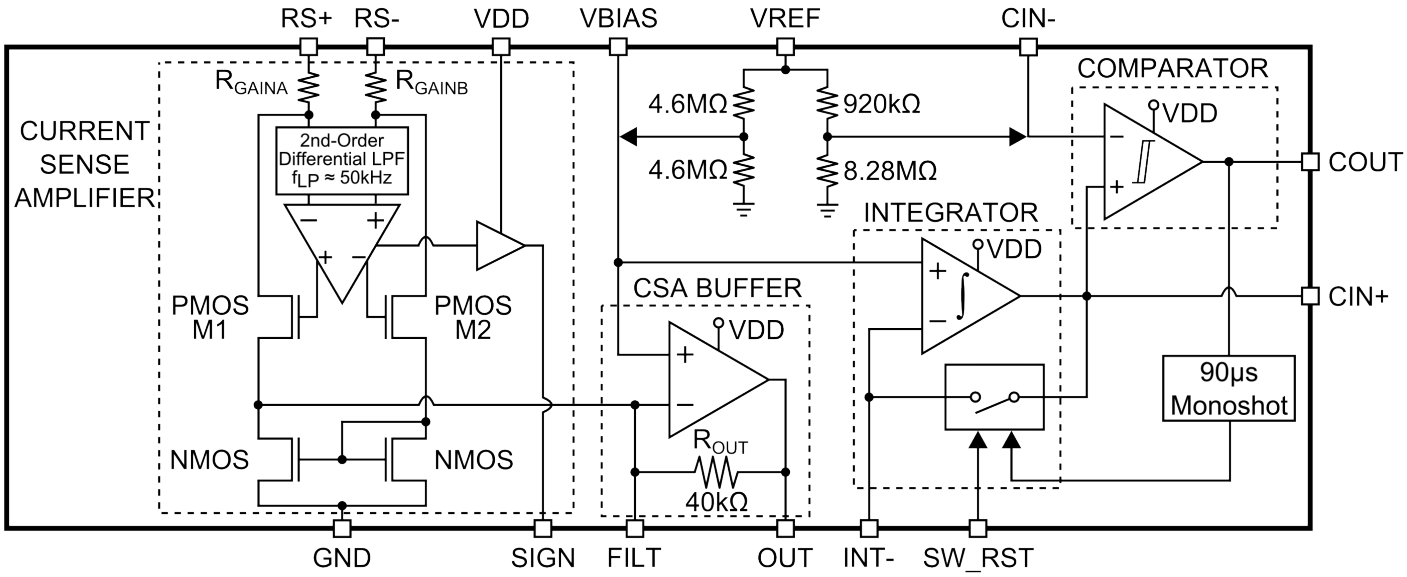
The TS1108 coulomb counter accurately measures battery depletion while also indicating the battery charging polarity. The battery discharge current is monitored by a current-sense amplifier through an external sense resistor. Utilizing an Integrator and a Comparator plus a Monoshot, the TS1108 voltage-to-frequency converter provides a series of 90 µs output pulses at COUT which represents an accumulation of coulombs flowing out of the battery. The charge count frequency is adjustable by the integration resistor and capacitor.

Applications

- Power Management Systems
- Portable/Battery-Powered Systems
- Smart Chargers

KEY FEATURES

- Coulomb Counting plus Charge Polarity
- Adjustable Charge Count Frequency
- External Crystal Oscillator Not Required
- Low Supply Current
  - Current Sense Amplifier: 0.68 µA
  - I_{VDD}: 1.93 µA
- High Side Bidirectional Current Sense Amplifier
- Wide CSA Input Common Mode Range: +2 V to +27 V
- Low CSA Input Offset Voltage: 150 µV(max)
- Low Gain Error: 1%(max)
- Two Gain Options Available:
  - Gain = 20 V/V : TS1108-20
  - Gain = 200 V/V : TS1108-200
- 16-Pin TQFN Packaging (3 mm x 3 mm)



1. Ordering Information

Table 1.1. Ordering Part Numbers

Ordering Part Number	Description	Gain V/V
TS1108-20ITQ1633	Coulomb counter: Bidirectional current sense amplifier with integrator and comparator	20
TS1108-200ITQ1633	Coulomb counter: Bidirectional current sense amplifier with integrator and comparator	200
Note: Adding the suffix “T” to the part number (e.g. TS1108-200ITQ1633T) denotes tape and reel.		

2. System Overview

2.1 Functional Block Diagram

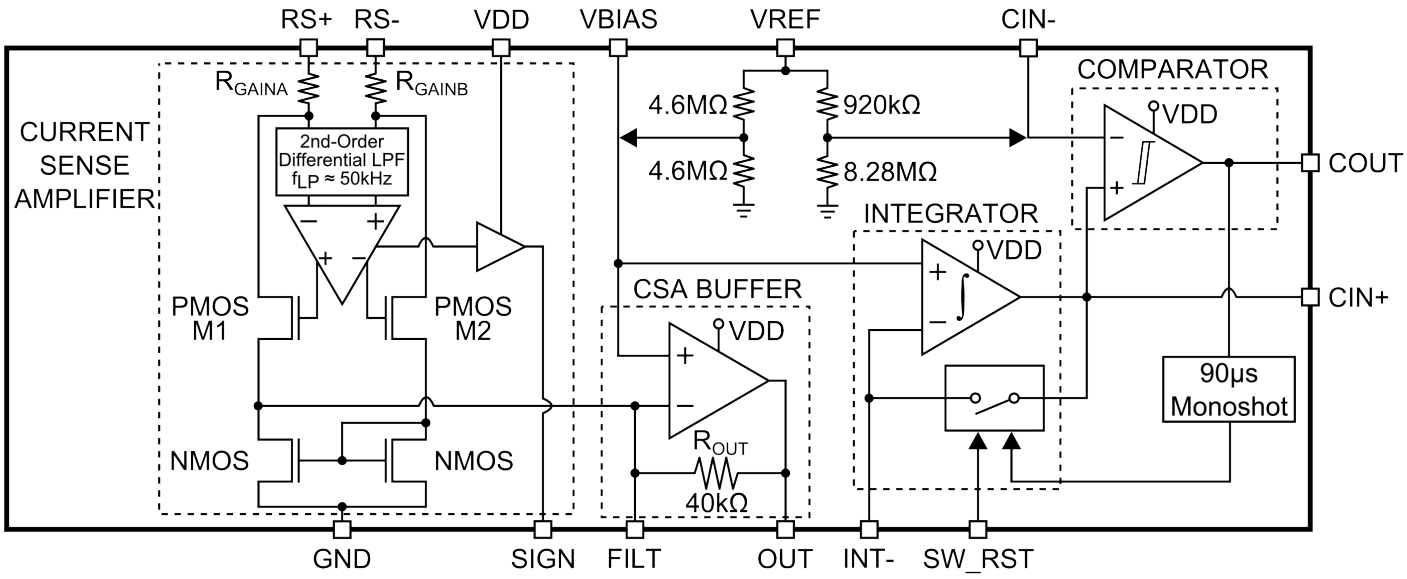


Figure 2.1. TS1108 Coulomb Counter Block Diagram

2.2 Current Sense Amplifier + Output Buffer

The internal configuration of the TS1108 bidirectional current-sense amplifier is a variation of the TS1101 bidirectional current-sense amplifier. The TS1108 current-sense amplifier is configured for fully differential input/output operation.

Referring to the block diagram, the inputs of the TS1108's differential input/output amplifier are connected to RS+ and RS– across an external R_{SENSE} resistor that is used to measure current. At the non-inverting input of the current-sense amplifier, the applied voltage difference in voltage between RS+ and RS– is I_{LOAD} x R_{SENSE}. Since the RS– terminal is the non-inverting input of the internal op-amp, the current-sense op-amp action drives PMOS[1/2] to drive current across $R_{GAIN[A/B]}$ to equalize voltage at its inputs.

Thus, since the M1 PMOS source is connected to the inverting input of the internal op-amp and since the voltage drop across R_{GAINA} is the same as the external V_{SENSE}, the M1 PMOS drain-source current is equal to:

$$I_{DS(M1)} = \frac{V_{SENSE}}{R_{GAINA}}$$

$$I_{DS(M1)} = \frac{I_{LOAD} \times R_{SENSE}}{R_{GAINA}}$$

The drain terminal of the M1 PMOS is connected to the transimpedance amplifier's gain resistor, ROUT, via the inverting terminal. The non-inverting terminal of the transimpedance amplifier is internally connected to VBIAS, therefore the output voltage of the TS1108 at the OUT terminal is:

$$V_{OUT} = V_{BIAS} - I_{LOAD} \times R_{SENSE} \times \frac{R_{OUT}}{R_{GAINA}}$$

When the voltage at the RS– terminal is greater than the voltage at the RS+ terminal, the external VSENSE voltage drop is impressed upon R_{GAINB}. The voltage drop across R_{GAINB} is then converted into a current by the M2 PMOS. The M2 PMOS' drain-source current is the input current for the NMOS current mirror which is matched with a 1-to-1 ratio. The transimpedance amplifier sources the M2 PMOS drain-source current for the NMOS current mirror. Therefore the output voltage of the TS1108 at the OUT terminal is:

$$V_{OUT} = V_{BIAS} + I_{LOAD} \times R_{SENSE} \times \frac{R_{OUT}}{R_{GAINB}}$$

When M1 is conducting current ($V_{RS+} > V_{RS-}$), the TS1108's internal amplifier holds M2 OFF. When M2 is conducting current ($V_{RS-} > V_{RS+}$), the internal amplifier holds M1 OFF. In either case, the disabled PMOS does not contribute to the resultant output voltage.

The current-sense amplifier's gain accuracy is therefore the ratio match of R_{OUT} to $R_{GAIN[A/B]}$. For each of the two gain options available, The following table lists the values for $R_{GAIN[A/B]}$.

Table 2.1. Internal Gain Setting Resistors (Typical Values)

GAIN (V/V)	$R_{GAIN[A/B]}$ (Ω)	R_{OUT} (Ω)	Part Number
20	2 k	40 k	TS1108-20
200	200	40 k	TS1108-200

The TS1108 allows access to the inverting terminal of the transimpedance amplifier by the FILT pin, whereby a series RC filter may be connected to reduce noise at the OUT terminal. The recommended RC filter is 4 kΩ and 0.47 µF connected in series from FILT to GND to suppress the noise. Any capacitance at the OUT terminal should be minimized for stable operation of the buffer.

2.3 Sign Output

The TS1108 SIGN output indicates the load current's direction. The SIGN output is a logic HIGH when M1 is conducting current (V_{RS+} > $V_{RS–}$). Alternatively, the SIGN output is a logic LOW when M2 is conducting current ($V_{RS–}$ > V_{RS+}). The SIGN comparator's transfer characteristic is illustrated in Figure 1. Unlike other current-sense amplifiers that implement an OUT/SIGN arrangement, the TS1108 exhibits no "dead zone" at I_{LOAD} switchover.

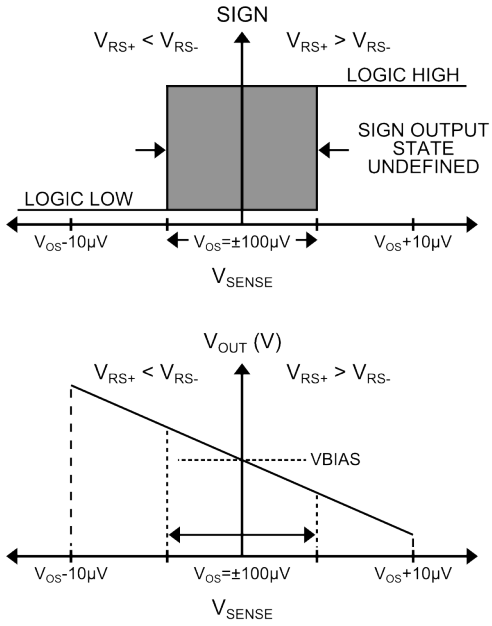


Figure 2.2. TS1108 Sign Output Transfer Characteristic

2.4 Integrator + Comparator

The TS1108 Coulomb Counter function utilizes an Integrator and a Comparator plus a 90 µs Monoshot. The CSA's buffered output is applied to the integrator's input. This signal is integrated by the comparator until it reaches a level that trips the comparator. The comparator's trip level is determined by the voltage applied to the comparator's non-inverting terminal, CIN+. The Monoshot produces a 90 µs output pulse at COUT and the integrator is reset. Therefore, each COUT 90 µs pulse represents an accumulation of coulombs (Please refer to the equations in 2.6 Coulomb Counter). The TS1108 Integrator works best when the 90 µs Monoshot represents less than 2% of the total integration period. Therefore, the minimum integration time for a full-scale V_{SENSE} should be limited to 4.7 ms. To guarantee stable operation of the OUT buffer, an integration capacitance of 0.1 µF should be used for integration capacitor, C_{INT} . The maximum integration period can be very long, limited by the leakage current and offset.

A reset switch is configured internally to discharge the external integration capacitor, C_{INT}. To enable the Coulomb Counting feature, SW_RST should be tied to either GND or COUT, allowing the 90 µs Monoshot Pulse to control the discharge of C_{INT}. To close the reset switch and short out C_{INT}, SW_RST may be tied high.

TS1108's Coulomb Counting interrupt is provided by the internal comparator with a push-pull output configuration. As shown in the block diagram, the integrator's output is applied internally to the non-inverting terminal of the comparator, CIN+. Therefore the comparator's output will latch high for 90 µs once the integrator's output is charged to the voltage supplied to the comparator's inverting terminal, CIN–. The inverting terminal of the comparator, CIN–, must be at a higher potential than the voltage supplied to VBIAS for proper operation. The capacitive load at COUT should be minimized for minimal output delays.

2.5 VREF Divider

The TS1108 provides an internal voltage divider network to set VBIAS and CIN–, eliminating the need for externally setting the required voltages. The VREF Divider is activated once the voltage applied to VREF is 0.9 V or greater. The VREF divider connects to VBIAS and CIN–, where the VBIAS voltage is equal to 50% of VREF while the CIN– voltage is equal to 90% of VREF . The VREF Divider exhibits a typical total series resistance of 4.6 MΩ from VREF to GND when activated.

2.6 Coulomb Counter

The amount of charge, or coulombs, over time is measured by the integration of current. The TS1108 Coulomb Counter measures the charge consumed by the load by integrating the voltage output of the Current Sense Amplifier, thereby converting the sensed current at the CSA's applied input into a measurement of coulombs. The comparator's output represents a measurement of coulombs per output pulse. The period of the comparator's output pulses is defined by:

$$t_{COUT} = \frac{R_{INT} C_{INT} (V_{CIN-} - V_{VBIAS})}{GAIN \times V_{SENSE}}$$

Since a coulomb is defined as the multiplication of current and time, the quantity of coulombs per comparator output pulse can be defined as:

$$One\,Comparator\,Output\,Pulse = \frac{R_{INT} C_{INT} (V_{CIN-} - V_{VBIAS})}{GAIN \times R_{SENSE}} Coulombs$$

The comparator's output pulse can also quantify the ampere-hours (Ah) of battery charge, as most battery manufacturers specify a battery's capacity in ampere-hours.

$$One\,Comparator\,Output\,Pulse = \frac{R_{INT} C_{INT} (V_{CIN-} - V_{VBIAS})}{3600 \times GAIN \times R_{SENSE}} Ah$$

It should be noted that the sense resistor value, R_{SENSE}, should not be used to adjust the relationship between coulombs and the applied sense current to the CSA's input. The integration resistor, R_{INT}, and the comparator's upper limit voltage, $V_{CIN–}$, should be used to adjust the integration time, and therefore the comparator's output period.

2.7 Selecting a Sense Resistor

Selecting the optimal value for the external R_{SENSE} is based on the following criteria and for each commentary follows:

1. R_{SENSE} Voltage Loss
2. V_{OUT} Swing vs. Desired V_{SENSE} and Applied Supply Voltage at VDD
3. Total I_{LOAD} Accuracy
4. Circuit Efficiency and Power Dissipation
5. R_{SENSE} Kelvin Connections

2.7.1 RSENSE Voltage Loss

For lowest IR power dissipation in R_{SENSE}, the smallest usable resistor value for R_{SENSE} should be selected.

2.7.2 VOUT Swing vs. Desired VSENSE and Applied Supply Voltage at VDD

Although the Current Sense Amplifier draws its power from the voltage at its RS+ and RS– terminals, the signal voltage at the OUT terminal is provided by a buffer, and is therefore bounded by the buffer's output range. As shown in the Electrical Characteristics table, the CSA Buffer has a maximum and minimum output voltage of:

$$V_{OUT(\max)} = VDD_{(\min)} - 0.2V$$

$$V_{OUT(\min)} = 0.2V$$

Therefore, the full-scale sense voltage should be chosen so that the OUT voltage is neither greater nor less than the maximum and minimum output voltage defined above. To satisfy this requirement, the positive full-scale sense voltage, $V_{SENSE(pos\_max)}$, should be chosen so that:

$$V_{SENSE(pos\_\max)} < \frac{VBIAS - V_{OUT(\min)}}{GAIN}$$

Likewise, the negative full-scale sense voltage, $V_{SENSE(neg\_min)}$, should be chosen so that:

$$V_{SENSE(neg\_\min)} < \frac{V_{OUT(\max)} - VBIAS}{GAIN}$$

For best performance, R_{SENSE} should be chosen so that the full-scale V_{SENSE} is less than ±75 mV.

2.7.3 Total Load Current Accuracy

In the TS1108's linear region where $V_{OUT(min)} < V_{OUT} < V_{OUT(max)}$, there are two specifications related to the circuit's accuracy: a) the TS1108 CSA's input offset voltage ($V_{OS(max)}$ = 150 µV), b) the TS1108 CSA's gain error ($GE_{(max)}$ = 1%). An expression for the TS1108's total error is given by:

$$V_{OUT} = VBIAS - \left[GAIN \times \left(1 \pm GE\right) \times V_{SENSE}\right] \pm \left(GAIN \times V_{OS}\right)$$

A large value for R_{SENSE} permits the use of smaller load currents to be measured more accurately because the effects of offset voltages are less significant when compared to larger V_{SENSE} voltages. Due care though should be exercised as previously mentioned with large values of R_{SENSE}.

2.7.4 Circuit Efficiency and Power Dissipation

IR loses in R_{SENSE} can be large especially at high load currents. It is important to select the smallest, usable R_{SENSE} value to minimize power dissipation and to keep the physical size of R_{SENSE} small. If the external R_{SENSE} is allowed to dissipate significant power, then its inherent temperature coefficient may alter its design center value, thereby reducing load current measurement accuracy. Precisely because the TS1108 CSA's input stage was designed to exhibit a very low input offset voltage, small R_{SENSE} values can be used to reduce power dissipation and minimize local hot spots on the pcb.

2.7.5 RSENSE Kelvin Connections

For optimal V_{SENSE} accuracy in the presence of large load currents, parasitic pcb track resistance should be minimized. Kelvin-sense pcb connections between R_{SENSE} and the TS1108's RS+ and RS– terminals are strongly recommended. The drawing below illustrates the connections between the current-sense amplifier and the current-sense resistor. The pcb layout should be balanced and symmetrical to minimize wiring-induced errors. In addition, the pcb layout for R_{SENSE} should include good thermal management techniques for optimal R_{SENSE} power dissipation.

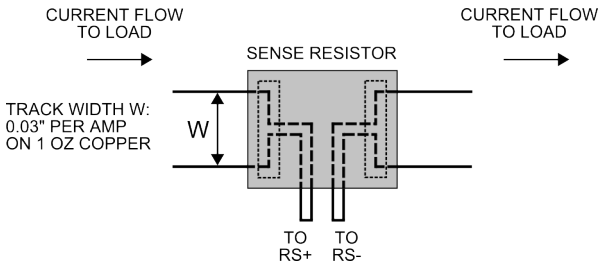


Figure 2.3. Making PCB Connections to R_{SENSE}

2.7.6 RSENSE Composition

Current-shunt resistors are available in metal film, metal strip, and wire-wound constructions. Wire-wound current-shunt resistors are constructed with wire spirally wound onto a core. As a result, these types of current shunt resistors exhibit the largest self-inductance. In applications where the load current contains high-frequency transients, metal film or metal strip current sense resistors are recommended.

2.7.7 Internal Noise Filter

In power management and motor control applications, current-sense amplifiers are required to measure load currents accurately in the presence of both externally-generated differential and common-mode noise. An example of differential-mode noise that can appear at the inputs of a current-sense amplifier is high-frequency ripple. High-frequency ripple (whether injected into the circuit inductively or capacitively) can produce a differential-mode voltage drop across the external current-shunt resistor, R_{SENSE}. An example of externally-generated, common-mode noise is the high-frequency output ripple of a switching regulator that can result in common-mode noise injection into both inputs of a current-sense amplifier.

Even though the load current signal bandwidth is dc, the input stage of any current-sense amplifier can rectify unwanted out-of-band noise that can result in an apparent error voltage at its output. Against common-mode injection noise, the current-sense amplifier's internal common-mode rejection ratio is 130 dB (typ).

To counter the effects of externally-injected noise, the TS1108 incorporates a 50 kHz (typ), 2nd-order differential low-pass filter as shown in the TS1108's block diagram, thereby eliminating the need for an external low-pass filter, which can generate errors in the offset voltage and the gain error.

2.7.8 PC Board Layout and Power-Supply Bypassing

For optimal circuit performance, the TS1108 should be in very close proximity to the external current-sense resistor and the pcb tracks from R_{SENSE} to the RS+ and the RS– input terminals of the TS1108 should be short and symmetric. Also recommended are surface mount resistors and capacitors, as well as a ground plane.

3. Electrical Characteristics

Table 3.1. Recommended Operating Conditions[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
System Specifications						
Operating Voltage Range	VDD		1.7	—	5.25	V
Common-Mode Input Range	V_{CM}	V_{RS+}, Guaranteed by CMRR	2	—	27	V

Note:
1. All devices 100% production tested at TA = +25 °C. Limits over Temperature are guaranteed by design and characterization.

Table 3.2. DC Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
System Specifications						
No Load Input Supply Current	$I_{RS+} + I_{RS-}$	See Note 2	—	0.68	1.2	µA
	I_{VDD}		—	1.93	2.88	µA
Current Sense Amplifier						
Common Mode Rejection Ratio	CMRR	2 V < V_{RS+} < 27 V	120	130	—	dB
Input Offset Voltage[3]	V_{OS}	T_A = +25 °C	—	±100	±150	µV
		–40 °C < T_A < +85 °C	—	—	±200	µV
V_{OS} Hysteresis[4]	V_{HYS}	T_A = +25 °C	—	10	—	µV
Gain	G	TS1108-20	—	20	—	V/V
		TS1108-200	—	200	—	V/V
Positive Gain Error[5]	GE+	T_A = +25 °C	—	±0.1	±0.6	%
		–40 °C < T_A < +85 °C	—	—	±1	%
Negative Gain Error[5]	GE–	T_A = +25 °C	—	±0.6	±1	%
		–40 °C < T_A < +85 °C	—	—	±1.4	%
Gain Match[5]	GM	T_A = +25 °C	—	±0.6	±1	%
		–40 °C < T_A < +85 °C	—	—	±1.4	%
Transfer Resistance	R_{OUT}	From FILT to OUT	28	40	52	kΩ
CSA Buffer						
Input Bias Current	I_{Buffer_BIAS}		—	—	0.5	nA
Input referred DC Offset	V_{Buffer_OS}		—	—	±2.5	mV
Offset Drift	TCV_{Buffer_OS}	–40 °C < T_A < +85 °C	—	0.6	—	µV/°C
Input Common Mode Range	V_{Buffer_CM}		0.2	—	VDD – 0.2	V
CSA Sign Comparator						

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Low Voltage	V_{SIGN_OL}	V_{DD} = 1.7 V, I_{SINK} = 35 µA	—	—	0.2	V
Output High Voltage	V_{SIGN_OH}	V_{DD} = 1.7 V, I_{SOURCE} = 35 µA	VDD – 0.2	—	—	V
Comparator						
Input Bias Current	I_{CIN-_BIAS}	CIN–	—	—	0.5	nA
Input Bias Current	I_{CIN+_BIAS}	CIN+	—	0.3	—	nA
Input referred DC offse	V_{C_OS}		—	—	±4	mV
Input Common Mode Range	V_{C_CM}		0.4	—	VDD – 0.4	V
COUT Output Range	$V_{COUT(min,max)}$	I_{COUT} = ±500 µA; VDD = 1.7 V	0.4	—	VDD – 0.4	V
Output Range	$V_{OUT(min,max)}$	I_{OUT} = ±150 µA; VDD = 1.7 V	0.2	—	VDD – 0.2	V
Integrator						
Input Referred DC Offset	V_{INT_OS}		—	—	±2.5	mV
Offset Drift	TCV_{INT_OS}	–40 C < T_A < +85 C	—	0.6	—	µV/C
Input Common-Mode Range	V_{INT_CM}		0.2	—	VDD – 0.2	V
Output Low Voltage	I_{INT_OL}	$I_{CIN+(SINK)}$ = 150 µA; VDD = 1.7 V	—	—	0.2	V
Output High Voltage	I_{INT_OH}	$I_{CIN+(SOURCE)}$ = 150 µA; VDD = 1.7 V	VDD – 0.2	—	—	V
VREF Divider						
VREF Activation voltage	$V_{REF(min)}$	VREF Rising edge	—	—	0.9	V
Resistor on VREF	R_{VREF}		—	4.6	—	MΩ
VBIAS	V_{VBIAS}	VREF = 1 V	0.495	0.5	0.505	V
CIN–	V_{CIN-}	VREF = 1 V	0.895	0.9	0.505	V

Note:

1. RS+ = RS– = 3.6 V; V_{SENSE} =(V_{RS+} – V_{RS-}) = 0 V; VDD = 3 V; VBIAS = 1.5 V; CIN+ = 0.75 V; VREF = GND; CLATCH = GND; R_{FET} = 1 MΩ; FILT connected to 4 kΩ and 470 nF in series to GND. T_A = T_J = –40 °C to +85 °C unless otherwise noted. Typical values are at T_A=+25 °C.
2. Extrapolated to V_{OUT} = V_{FILT}; I_{RS+} + I_{RS-} is the total current into the RS+ and the RS– pins.
3. Input offset voltage V_{OS} is extrapolated from a $V_{OUT(+)}$ measurement with V_{SENSE} set to +1 mV and a $V_{OUT(-)}$ measurement with V_{SENSE} set to –1 mV; average V_{OS} = ($V_{OUT(-)}$ – $V_{OUT(+)}$)/(2 x GAIN).
4. Amplitude of V_{SENSE} lower or higher than V_{OS} required to cause the comparator to switch output states.
5. Gain error is calculated by applying two values for V_{SENSE} and then calculating the error of the actual slope vs. the ideal transfer characteristic. For GAIN = 20 V/V, the applied V_{SENSE} for GE± is ±25 mV and ±60 mV. For GAIN = 200 V/V, the applied V_{SENSE} for GE± is ±2.5 mV and ±6 mV

Table 3.3. AC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CSA Buffer						
Output Settling time	t_{OUT_s}	1% Final value, V_{OUT} = 1.3 V	—	1.35	—	msec
Sign Comparator Parameters						
Propagation Delay	t_{SIGN_PD}	V_{SENSE} = ±1 mV	—	3	—	msec
		V_{SENSE} = ±10 mV	—	0.4	—	msec
Reset Switch						
Capacitor Discharge Time	t_{RESET}	C_{INT} = 0.1 µF; After comparator trigger	—	—	60	µsec
Comparator						
Rising Propagation Delay	t_{C_PDR}	Overdrive = +10 mV, C_{COUT} = 15 pF	—	9	—	µsec
Comparator Hysteresis	V_{C_HYS}	CIN+ Rising	—	20	—	mV
Monoshot						
Monoshot Time	t_{MONO}	1.7 ≤ VDD ≤ 5.25	75.5	90	126	µsec

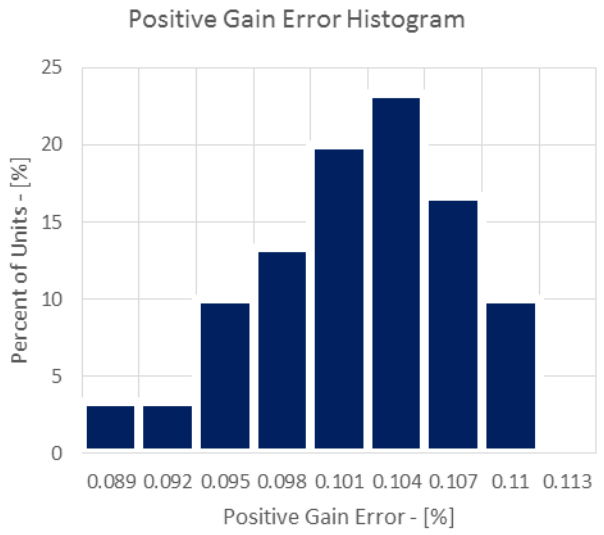
Table 3.4. Thermal Conditions

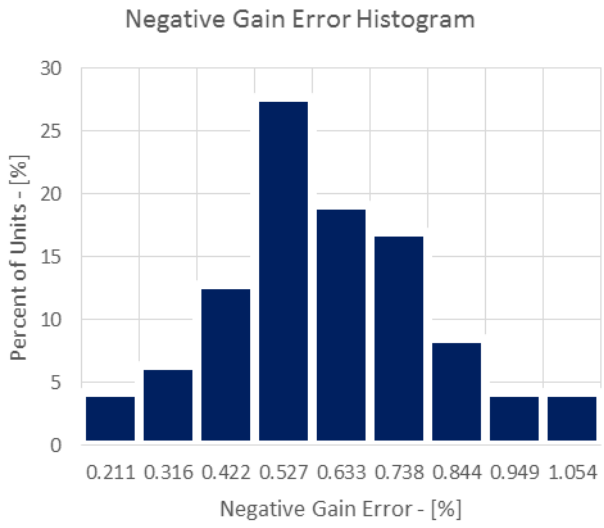
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Temperature Range	T_{OP}		-40	—	+85	°C

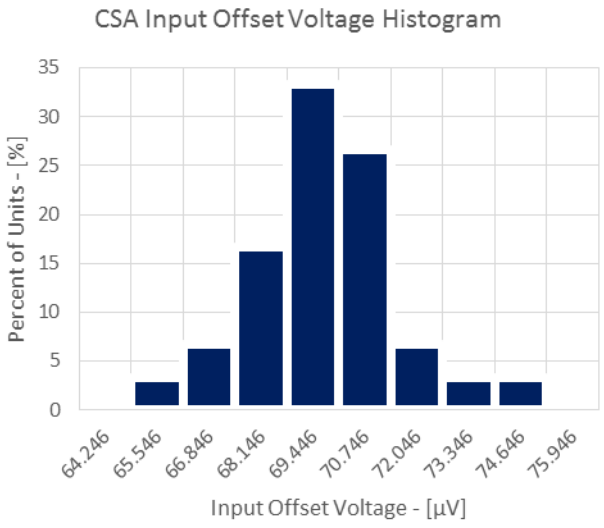
Table 3.5. Absolute Maximum Limits

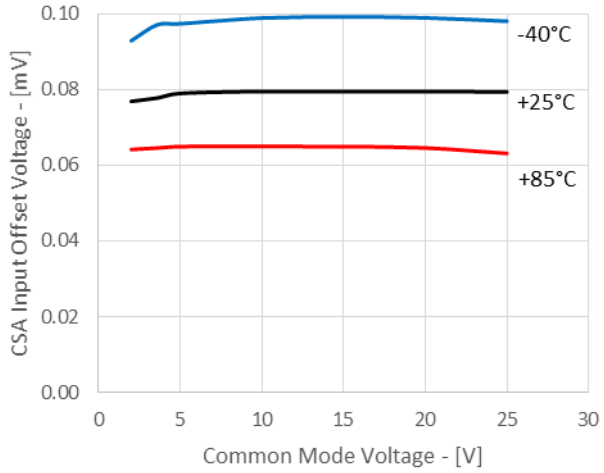
Parameter	Symbol	Conditions	Min	Typ	Max	Units
RS+ Voltage	V_{RS+}		–0.3	—	27	V
RS– Voltage	$V_{RS–}$		–0.3	—	27	V
Supply Voltage	VDD		–0.3	—	6	V
OUT Voltage	V_{OUT}		–0.3	—	6	V
SIGN Voltage	V_{SIGN}		–0.3	—	6	V
FILT Voltage	V_{FILT}		–0.3	—	6	V
SW_RST Voltage	V_{SW_RST}		–0.3	—	6	V
COUT Voltage	V_{COUT}		–0.3	—	6	V
VREF Voltage	V_{VREF}		–0.3	—	6	V
CIN+ Voltage	V_{CIN+}		–0.3	—	VDD + 0.3	V
CIN– Voltage	$V_{CIN–}$		–0.3	—	VDD + 0.3	V
INT– Voltage	$V_{INT–}$		–0.3	—	VDD + 0.3	V
VBIAS Voltage	V_{VBIAS}		–0.3	—	VDD + 0.3	V
RS+ to RS– Voltage	$V_{RS+} – V_{RS–}$		—	—	27	V
Short Circuit Duration: OUT to GND			—	—	Continuous	
Continuous Input Current (Any Pin)			–20	—	20	mA
Junction Temperature			—	—	150	°C
Storage Temperature Range			–65	—	150	°C
Lead Temperature (Soldering, 10 s)			—	—	300	°C
Soldering Temperature (Reflow)			—	—	260	°C
ESD Tolerance						
Human Body Model			—	—	2000	V
Machine Model			—	—	200	V

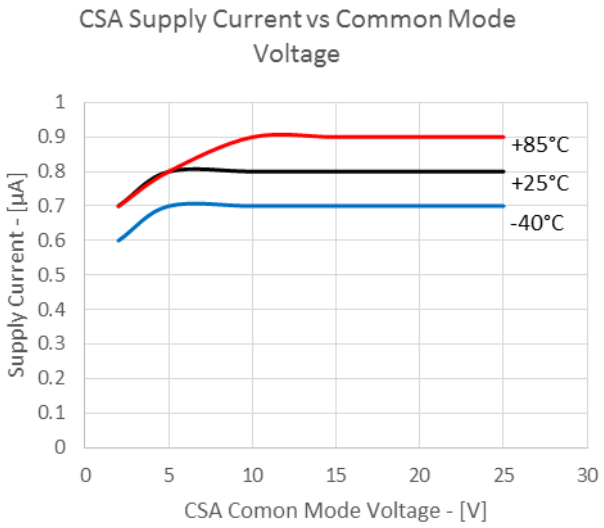
For the following graphs, V_{RS+} = V_{RS-} = 3.6 V; VDD = 3 V; VREF = GND; VBIAS = 1.5 V, CIN– = 2.5 V, SW_RST = COUT; R_{INT} = 47 kΩ; C_{INT} = 0.1 µF, and T_A = +25 C unless otherwise noted.

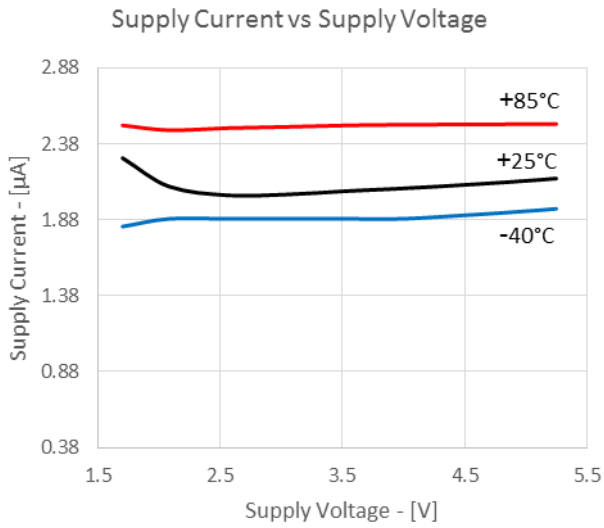


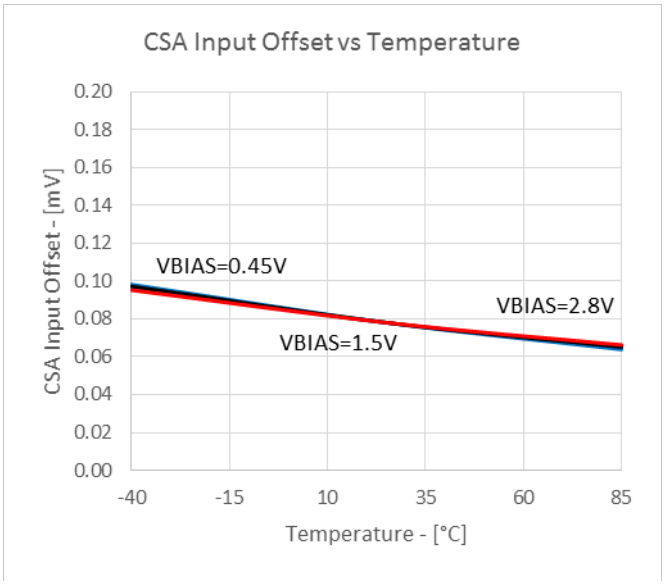


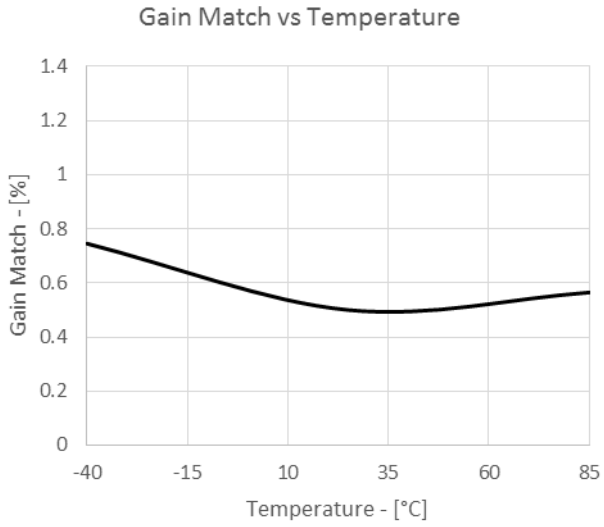


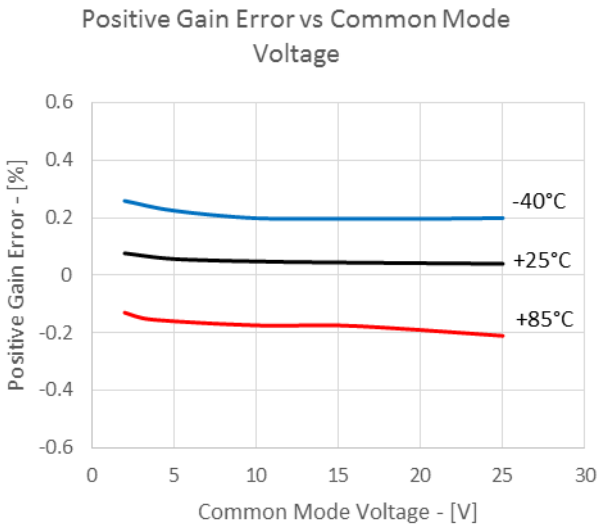


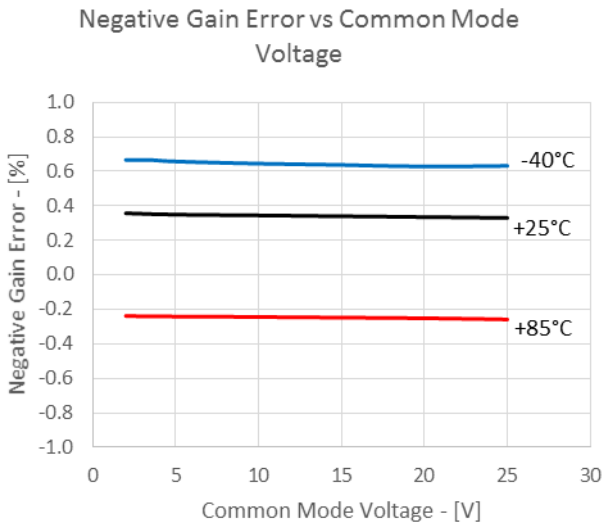


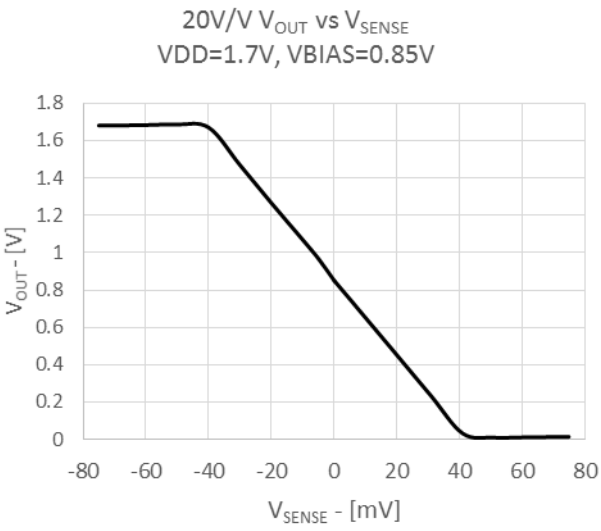


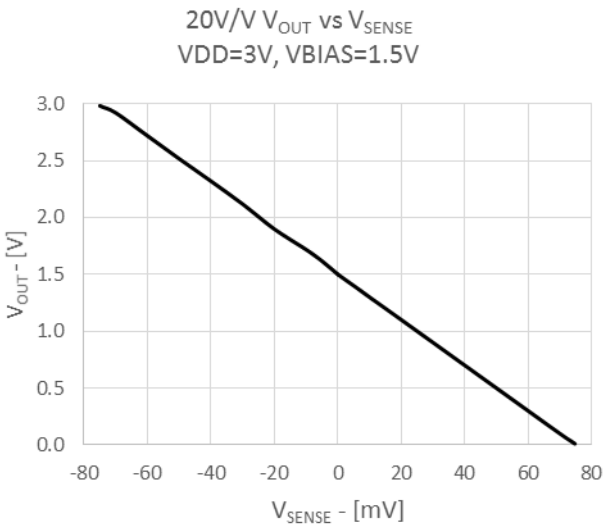

CSA Input Offset vs Temperature
CSA Input Offset - [mV]
0.20
0.18
0.16
0.14
0.12
0.10
0.08
0.06
0.04
0.02
0.00
VBIAS=0.45V
VBIAS=2.8V
VBIAS=1.5V
-40
-15
10
35
60
85
Temperature - [°C]

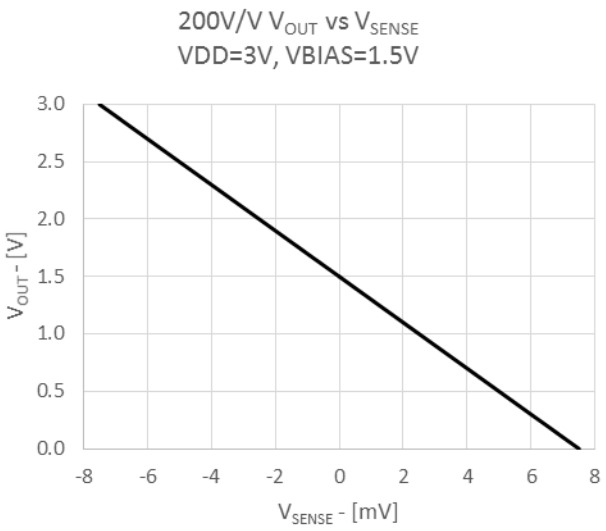

Gain Match vs Temperature
Gain Match - [%]
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-40
-15
10
35
60
85
Temperature - [°C]

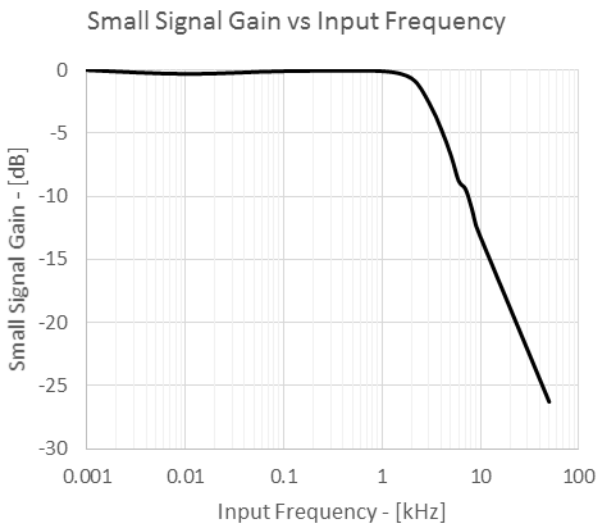

Positive Gain Error vs Common Mode Voltage
Positive Gain Error - [%]
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-40°C
+25°C
+85°C
0
5
10
15
20
25
30
Common Mode Voltage - [V]

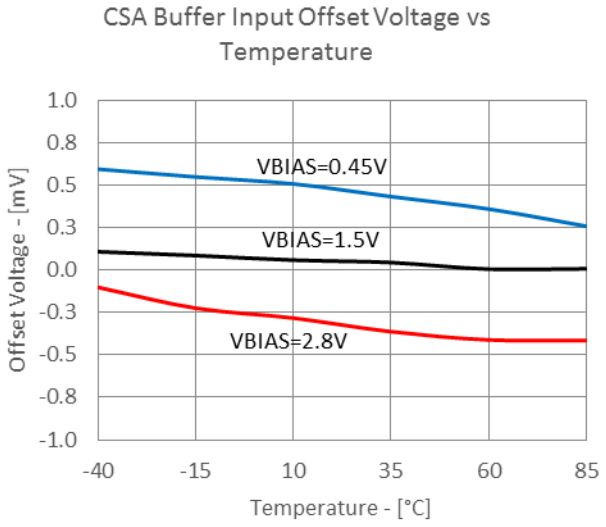

Negative Gain Error vs Common Mode Voltage
Negative Gain Error - [%]
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
-40°C
+25°C
+85°C
0
5
10
15
20
25
30
Common Mode Voltage - [V]

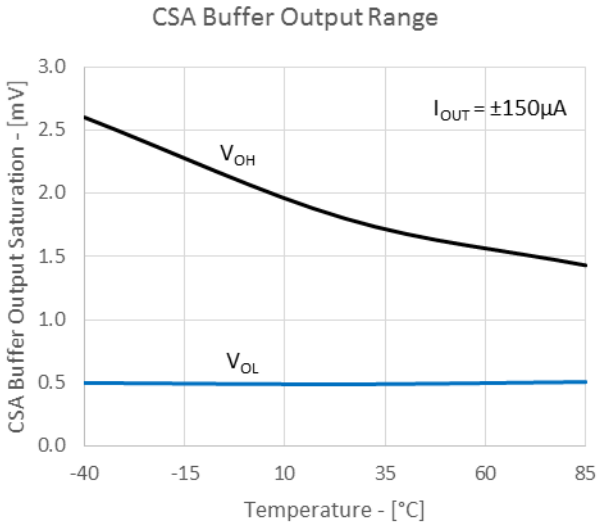

20V/V VOUT vs VSENSE
VDD=1.7V, VBIAS=0.85V
VOUT - [V]
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-80
-60
-40
-20
0
20
40
60
80
VSENSE - [mV]

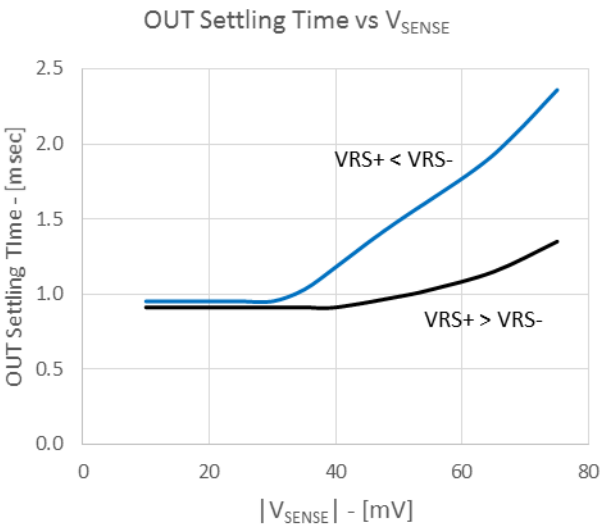

20V/V VOUT vs VSENSE
VDD=3V, VBIAS=1.5V
VOUT - [V]
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-80
-60
-40
-20
0
20
40
60
80
VSENSE - [mV]

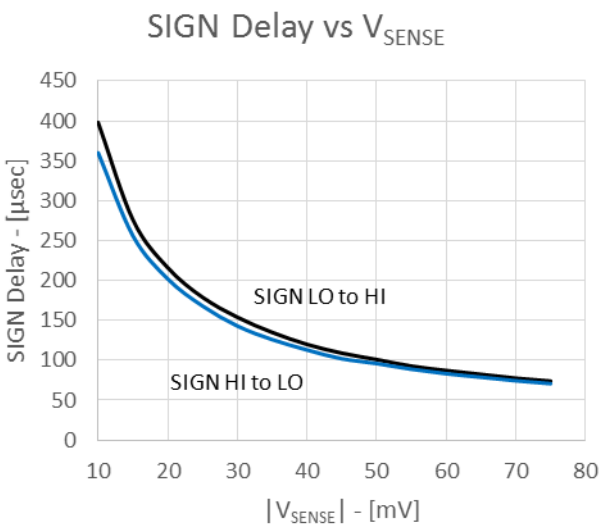

200V/V V_{OUT} vs V_{SENSE}
VDD=3V, VBIAS=1.5V
V_{OUT} - [V]
V_{SENSE} - [mV]

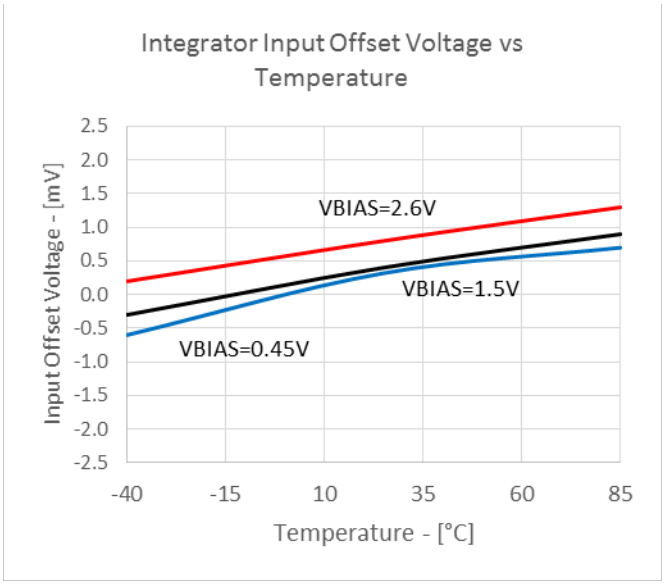

Small Signal Gain vs Input Frequency
Small Signal Gain - [dB]
Input Frequency - [kHz]

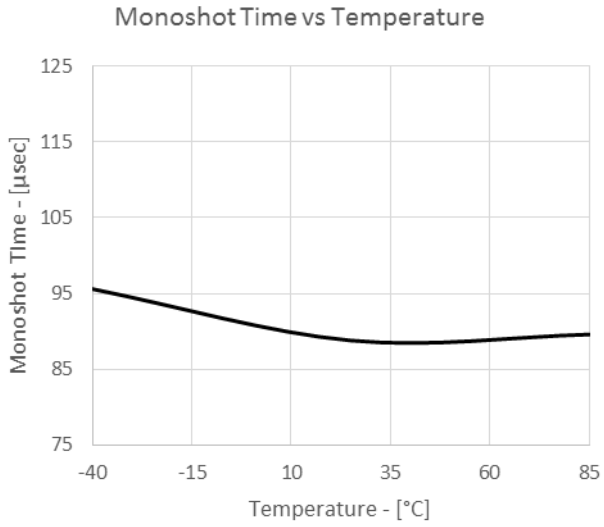

CSA Buffer Input Offset Voltage vs Temperature
VBIAS=0.45V
VBIAS=1.5V
VBIAS=2.8V
Offset Voltage - [mV]
Temperature - [°C]

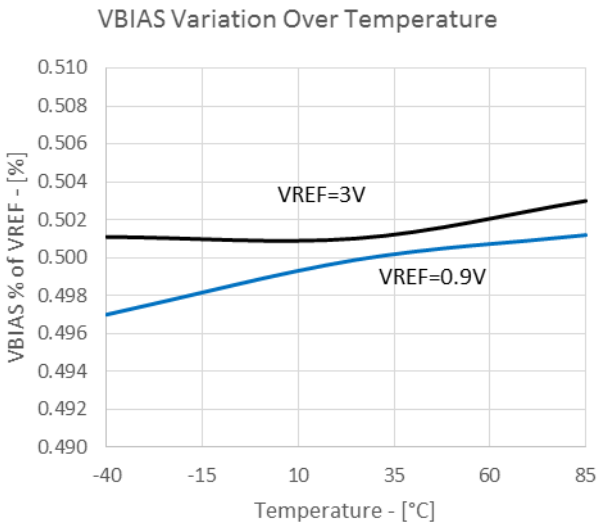

CSA Buffer Output Range
I_{OUT} = ±150µA
V_{OH}
V_{OL}
CSA Buffer Output Saturation - [mV]
Temperature - [°C]

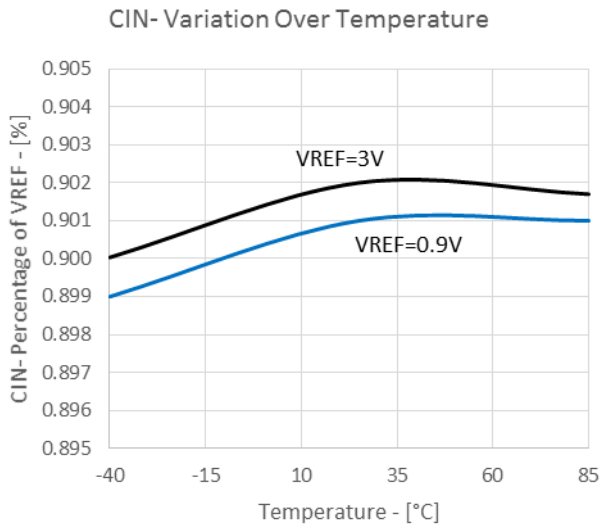

OUT Settling Time vs V_{SENSE}
VRS+ < VRS-
VRS+ > VRS-
OUT Settling Time - [msec]
$|V_{SENSE}|$ - [mV]

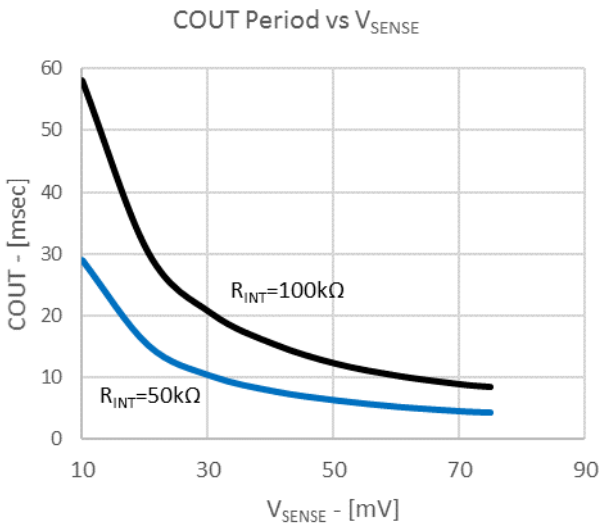

SIGN Delay vs V_{SENSE}
SIGN LO to HI
SIGN HI to LO
SIGN Delay - [µsec]
$|V_{SENSE}|$ - [mV]

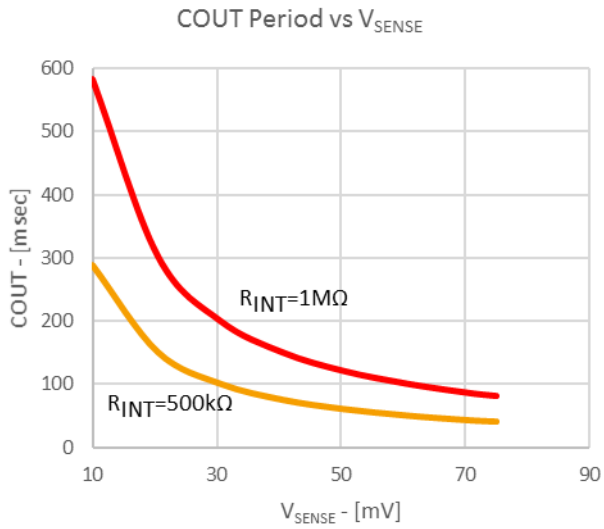

Integrator Input Offset Voltage vs Temperature
Input Offset Voltage - [mV]
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
VBIAS=2.6V
VBIAS=1.5V
VBIAS=0.45V
-40
-15
10
35
60
85
Temperature - [°C]


Monoshot Time vs Temperature
Monoshot Time - [µsec]
125
115
105
95
85
75
-40
-15
10
35
60
85
Temperature - [°C]

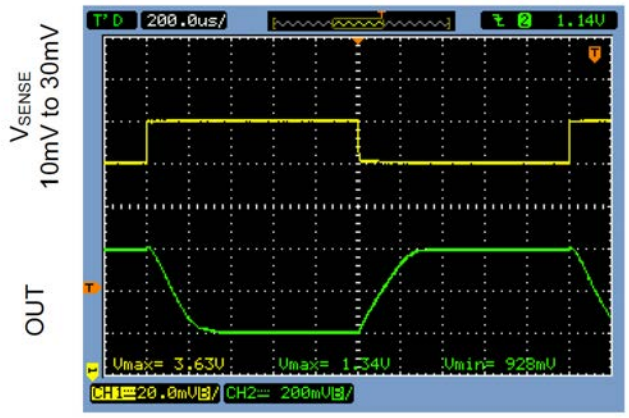

VBIAS Variation Over Temperature
VBIAS % of VREF - [%]
0.510
0.508
0.506
0.504
0.502
0.500
0.498
0.496
0.494
0.492
0.490
VREF=3V
VREF=0.9V
-40
-15
10
35
60
85
Temperature - [°C]


CIN- Variation Over Temperature
CIN- Percentage of VREF - [%]
0.905
0.904
0.903
0.902
0.901
0.900
0.899
0.898
0.897
0.896
0.895
VREF=3V
VREF=0.9V
-40
-15
10
35
60
85
Temperature - [°C]

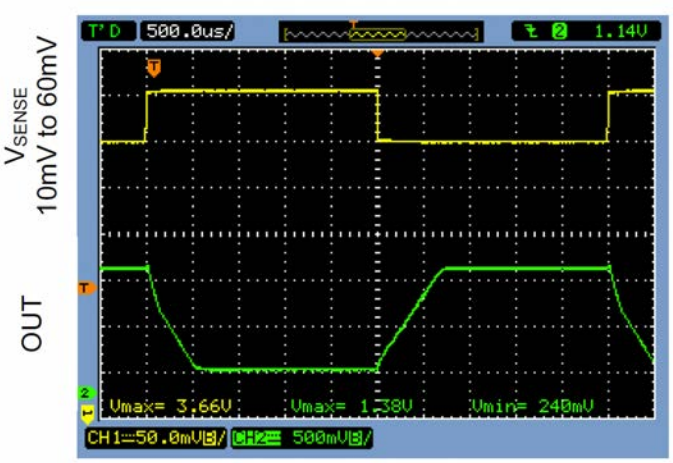

COUT Period vs VSENSE
COUT - [msec]
60
50
40
30
20
10
0
RINT=100kΩ
RINT=50kΩ
10
30
50
70
90
VSENSE - [mV]


COUT Period vs VSENSE
COUT - [msec]
600
500
400
300
200
100
0
RINT=1MΩ
RINT=500kΩ
10
30
50
70
90
VSENSE - [mV]

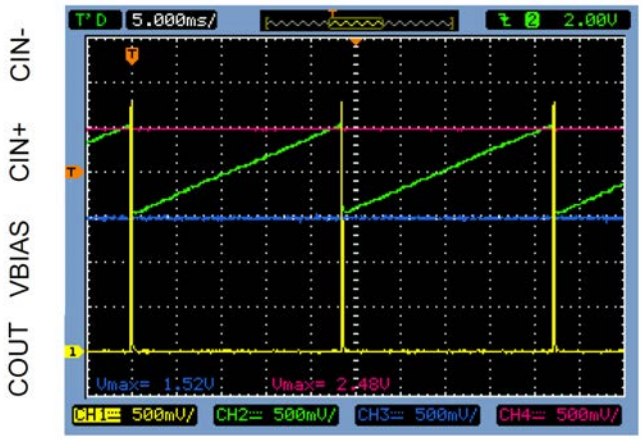
Small Signal Pulse Response
TS1108-20



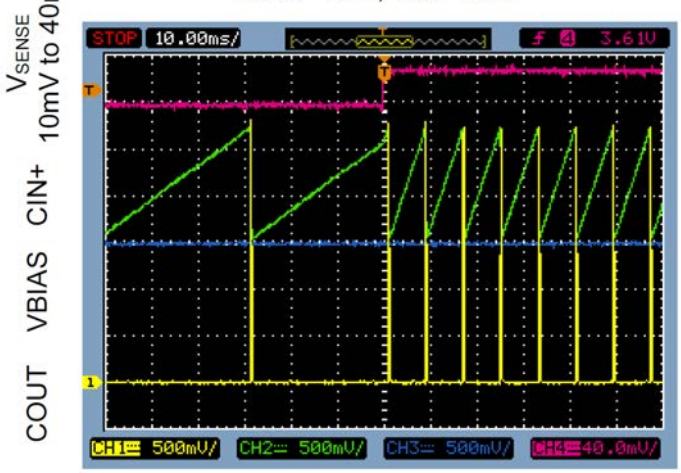
Large Signal Pulse Response
TS1108-20



TS1108-20 Coulomb Counting
V_{SENSE}=10mV, V_{VBIAS}=1.5V, V_{CIN-}=2.5V



TS1108-20 Coulomb Counting
V_{VBIAS}=1.5V, V_{CIN-}=2.5V



4. Typical Application Circuit

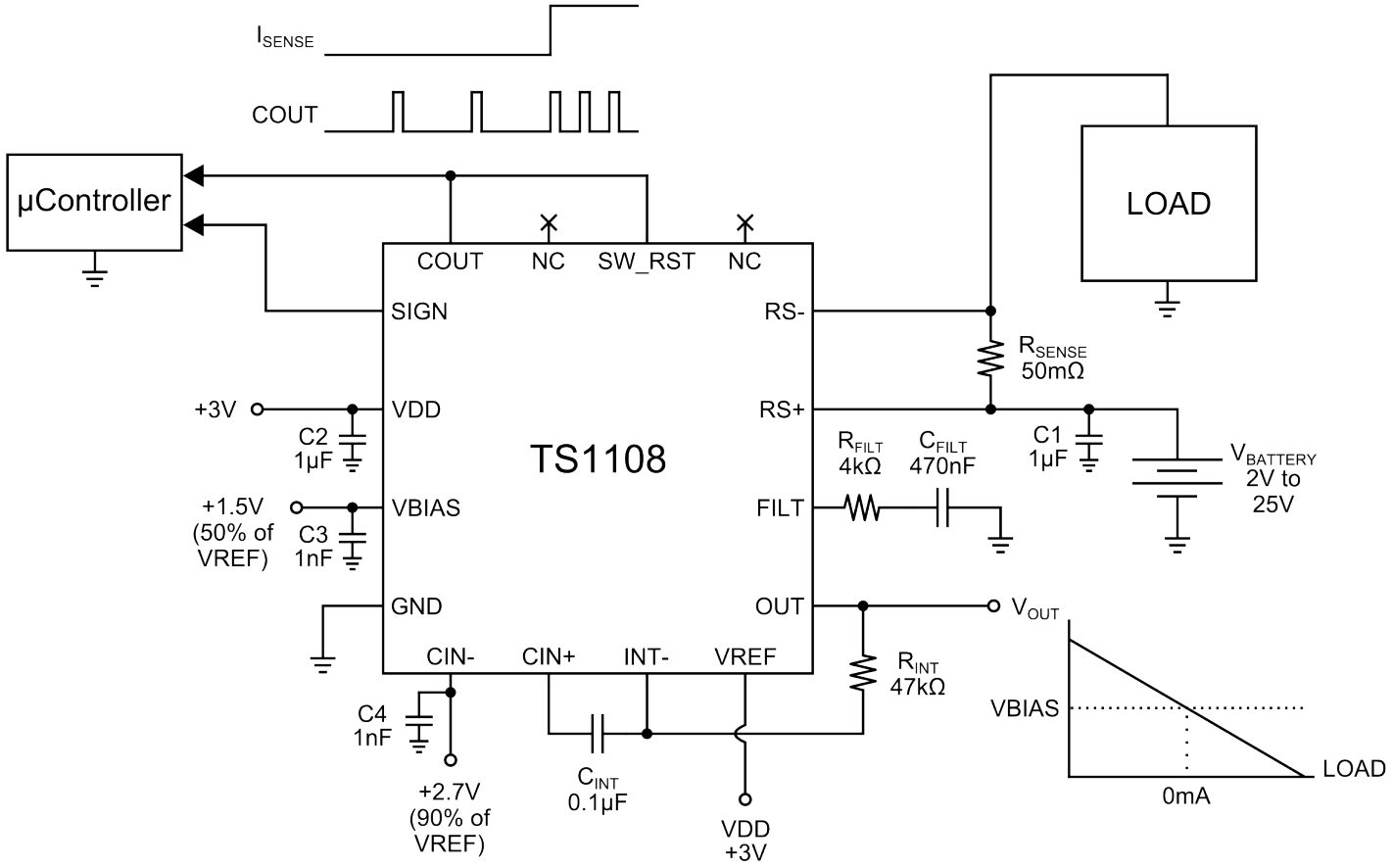


Figure 4.1. TS1108 Typical Application Circuit

5. Pin Descriptions

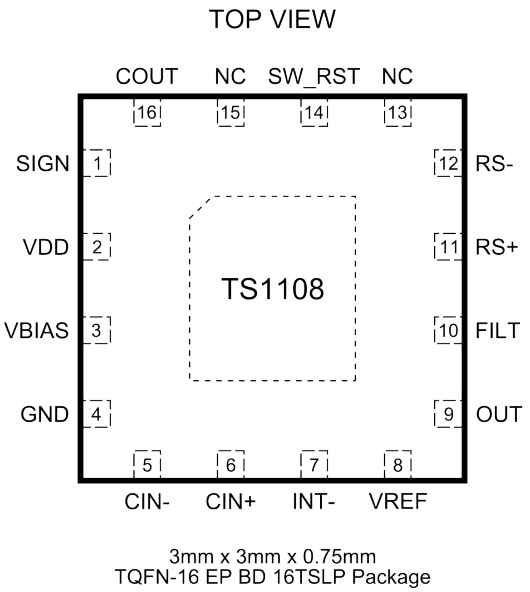


Figure 5.1. TS1108 Pinout

Table 5.1. Pin Descriptions

Pin	Label	Function
1	SIGN	Sign output. SIGN is HIGH for $V_{RS+} > V_{RS-}$ and LOW for $V_{RS-} > V_{RS+}$.
2	VDD	External power supply pin. Connect this to the system's VDD supply.
3	VBIAS	Bias voltage for CSA output. When VREF is activated, leave open.
4	GND	Ground. Connect to analog ground.
5	CIN–	Inverting terminal of Comparator. Supply a reference voltage for integration limit. CIN- voltage must be greater than VBIAS. If VREF is activated, leave open.
6	CIN+	Integrator Output and Non-inverting terminal of Comparator. Connect C_{INT} in series from INT–.
7	INT–	Inverting Terminal of Integrator. Connect R_{INT} in series from OUT. Connect C_{INT} in series to CIN+.
8	VREF	Voltage reference. To activate, a minimum voltage of 0.9 V is required. To disable voltage divider, connect to analog ground, GND.
9	OUT	CSA buffered output. Connect R_{INT} in series to INT–.
10	FILT	Inverting terminal of CSA Buffer. Connect a series RC Filter of 4 kΩ and 0.47 µF, otherwise leave open.
11	RS+	External Sense Resistor Power-Side Connection
12	RS–	External Sense Resistor Load-Side Connection. Connect external PFET's source.
13	NC	No connection. Leave open.
14	SW_RST	Integrator Reset Switch control. To enable coulomb counting, connect SW_RST to GND or COUT. Hold SW_RST HIGH to short CIN+ and INT–.
15	NC	No connection. Leave open.
16	COUT	Coulomb Comparator Counter Output.
Exposed Pad	EPAD	Exposed backside paddle. For best electrical and thermal performance, solder to analog ground.

6. Packaging

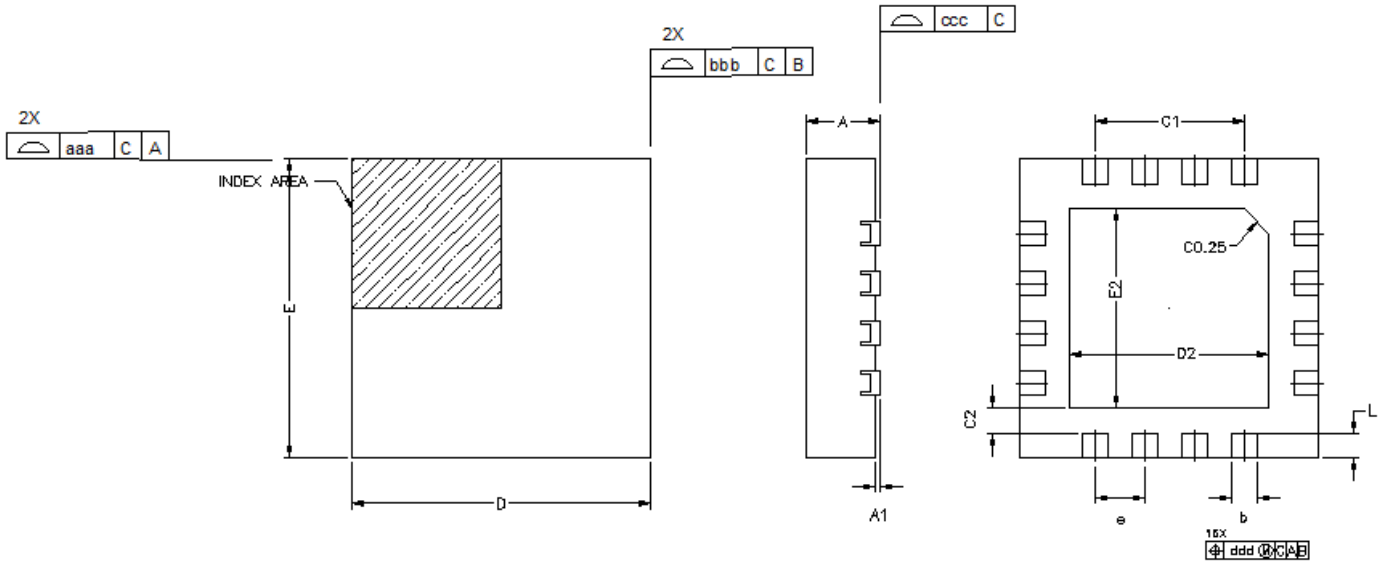


Figure 6.1. TS1108 3x3 mm 16-QFN Package Diagram

Table 6.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
C1		1.50 REF	
C2		0.25 REF	
D		3.00 BSC	
D2	1.90	2.00	2.10
e		0.50 BSC	
E		3.00 BSC	
E2	1.90	2.00	2.10
L	0.20	0.25	0.30
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.05
ddd	—	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

7. Top Marking

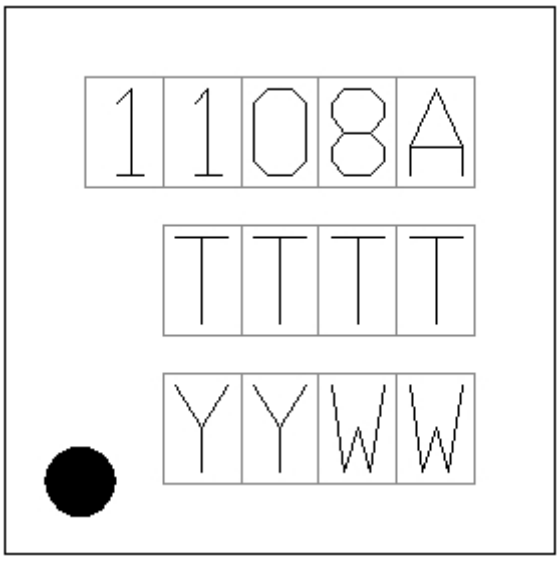


Figure 7.1. Top Marking

Table 7.1. Top Marking Explanation

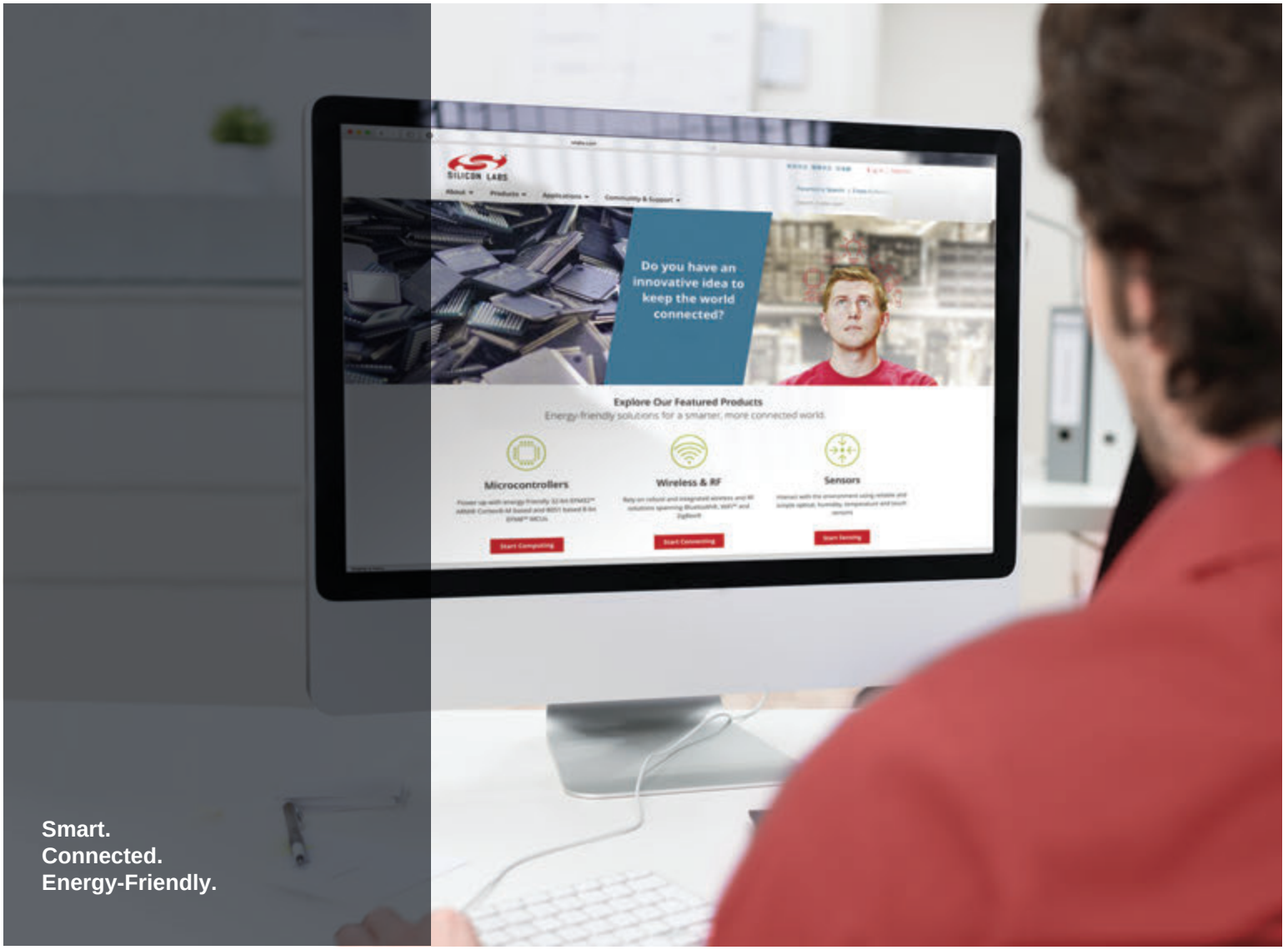
Mark Method	Laser	
Pin 1 Mark:	Circle = 0.50 mm Diameter (lower left corner)	
Font Size:	0.50 mm (20 mils)	
Line 1 Mark Format:	Product ID	Note: A = 20 gain, B = 200 gain
Line 2 Mark Format:	TTTT – Mfg Code	Manufacturing code
Line 3 Mark Format:	YY = Year; WW = Work Week	Year and week of assembly

8. Document Change List

Revision 1.0 to Revision 1.1

- Updated 1. Ordering Information with correct part numbers.

Table of Contents



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