

SNx4AHC594 8-Bit Shift Registers With Output Registers

1 Features

- Operating Range 2-V to 5.5-V V_{CC}
- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Shift and Storage Registers
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Network Switches
- Power Infrastructures
- PCs and Notebooks
- LED Displays
- Servers

3 Description

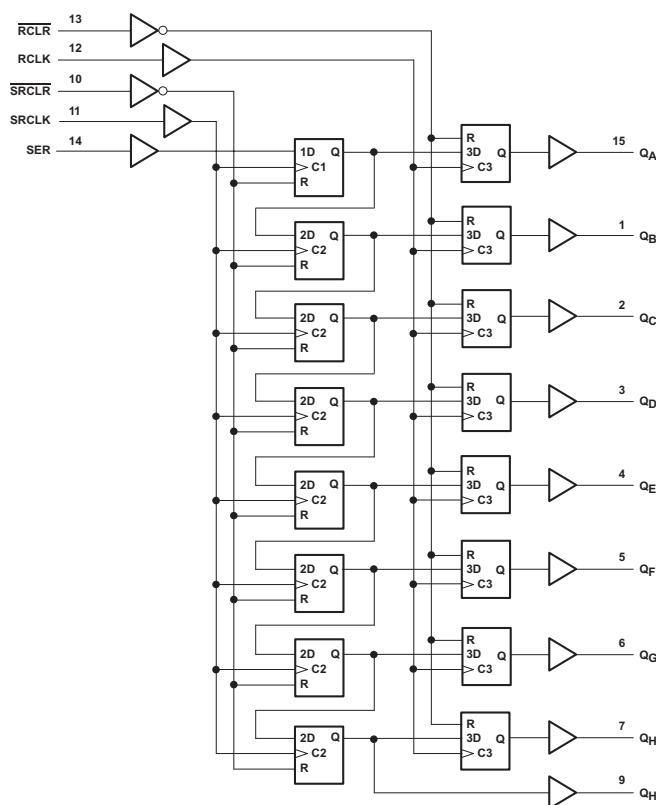
The SNx4AHC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear (SRCLR, RCLR) inputs are provided on the shift and storage registers. A serial (Q_H') output is provided for cascading purposes.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHC594	SOIC (16)	9.90 mm × 3.91 mm
	SSOP (16)	6.20 mm × 5.30 mm
	PDIP (16)	19.30 mm × 6.35 mm
	SOP (16)	12.60 mm × 5.30 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

Table of Contents

1	Features	1	8	Detailed Description	11
2	Applications	1	8.1	Overview	11
3	Description	1	8.2	Functional Block Diagram	11
4	Revision History	2	8.3	Feature Description	12
5	Pin Configuration and Functions	3	8.4	Device Functional Modes	12
6	Specifications	4	9	Application and Implementation	13
6.1	Absolute Maximum Ratings	4	9.1	Application Information	13
6.2	Handling Ratings	4	9.2	Typical Application	13
6.3	Recommended Operating Conditions	4	10	Power Supply Recommendations	14
6.4	Thermal Information	5	11	Layout	14
6.5	Electrical Characteristics	5	11.1	Layout Guidelines	14
6.6	Timing Requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	6	11.2	Layout Example	14
6.7	Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	6	12	Device and Documentation Support	15
6.8	Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	7	12.1	Related Links	15
6.9	Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	8	12.2	Trademarks	15
6.10	Noise Characteristics	8	12.3	Electrostatic Discharge Caution	15
6.11	Operating Characteristics	8	12.4	Glossary	15
6.12	Typical Characteristics	9	13	Mechanical, Packaging, and Orderable	15
7	Parameter Measurement Information	10	Information		

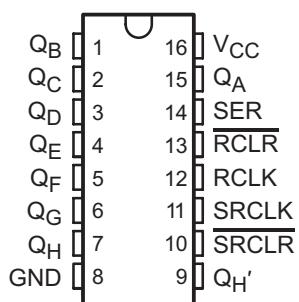
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

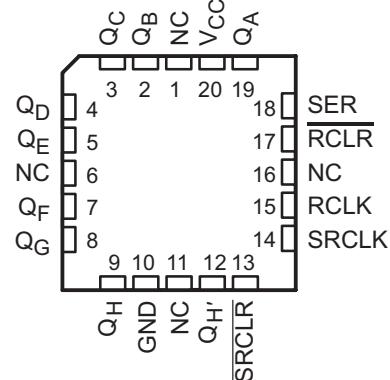
Changes from Revision F (September 2003) to Revision G	Page
• Updated document to new TI data sheet standards.	1
• Deleted Ordering Information table.	1
• Added Applications.	1
• Added Pin Functions table.	3
• Added Handling Ratings table.	4
• Changed MAX operating temperature from 85°C to 125°C in Recommended Operating Conditions table.	4
• Added Thermal Information table.	5
• Added Typical Characteristics section.	9
• Added Detailed Description section.	11
• Added Application and Implementation section.	13
• Added Power Supply Recommendations and Layout sections.	14

5 Pin Configuration and Functions

**SN54AHC594 . . . J OR W PACKAGE
SN74AHC594 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)**



**SN54AHC594 . . . FK PACKAGE
(TOP VIEW)**



NC – No internal connection

Pin Functions

Name	Pin			I/O	Description
	FK	J, W	D, DB, N, NS, PW		
GND	10	8	8	—	Ground Pin
NC	1	—	—	—	No connect
	6				
	11				
	16				
Q _A	19	15	15	O	Q _A Output
Q _B	2	1	1	O	Q _B Output
Q _C	3	2	2	O	Q _C Output
Q _D	4	3	3	O	Q _D Output
Q _E	5	4	4	O	Q _E Output
Q _F	7	5	5	O	Q _F Output
Q _G	8	6	6	O	Q _G Output
Q _H	9	7	7	O	Q _H Output
Q _{H'}	12	9	9	O	Q _{H'} Output
RCLK	15	12	12	I	RCLK Input
RCLR	17	13	13	I	\overline{RCLR} Input
SER	18	14	14	I	SER Input
SRCLK	14	11	11	I	SRCLK Input
SRCLR	13	10	10	I	\overline{SRCLR} Input
V _{CC}	20	16	16	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	7	V
V_I	Input voltage range ⁽²⁾	-0.5	7	V
V_O	Output voltage range ⁽²⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current $V_I < 0$		-20	mA
I_{OK}	Output clamp current $V_O < 0$ or $V_O > V_{CC}$		± 20	mA
I_O	Continuous output current $V_O = 0$ to V_{CC}		± 25	mA
	Continuous current through V_{CC} or GND		± 75	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	-65	150	°C
$V_{(ESD)}$	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN54AHC594 ⁽²⁾		SN74AHC594		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5	1.5		V
		$V_{CC} = 3$ V	2.1	2.1		
		$V_{CC} = 5.5$ V	3.85	3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0.5	0.5		V
		$V_{CC} = 3$ V	0.9	0.9		
		$V_{CC} = 5.5$ V	1.65	1.65		
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V	-50	-50		μA
		$V_{CC} = 3$ V ± 0.3 V	-4	-4		
		$V_{CC} = 5.5$ V ± 0.5 V	-8	-8		
I_{OL}	Low-level output current	$V_{CC} = 2$ V	50	50		μA
		$V_{CC} = 3$ V ± 0.3 V	4	4		
		$V_{CC} = 5.5$ V ± 0.5 V	8	8		
$\Delta t/\Delta V$	Input transition rise and fall time	$V_{CC} = 3$ V ± 0.3 V	100	100		ns/V
		$V_{CC} = 5.5$ V ± 0.5 V	20	20		
T_A	Operating free-air temperature	-55	125	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

(2) Product Preview

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHC594					UNIT
		D	DB	N	NS	PW	
		16 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.2	97.5	47.5	79.1	105.7	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	39.1	47.7	34.9	35.4	40.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	27.7	48.1	27.5	39.9	50.7	
Ψ_{JT}	Junction-to-top characterization parameter	9.9	9.8	19.8	5.4	3.7	
Ψ_{JB}	Junction-to-board characterization parameter	37.4	47.6	27.4	39.5	50.1	
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the TI application report *IC Package Thermal Metrics* ([SPRA953](#)).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54AHC594 ⁽¹⁾		SN74AHC594		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48		2.48		
	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		3.8		
	$Q_A - Q_H \quad I_{OH} = -8 \text{ mA}$		3.94			3.8		3.8		
V_{OL}	$I_{OL} = 50 \mu\text{A}$	2 V	0.1			0.1		0.1		V
		3 V	0.1			0.1		0.1		
		4.5 V	0.1			0.1		0.1		
	$I_{OL} = 4 \text{ mA}$	3 V	0.36			0.5		0.44		
	$I_{OL} = 8 \text{ mA}$	4.5 V	0.36			0.5		0.44		
			0.36			0.5		0.44		
I_I	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V	± 0.1			$\pm 1^{(2)}$		± 1	μA	
I_{CC}	$V_I = V_{CC} \text{ or GND}$	5.5 V	4			40		40	μA	
C_I	$V_I = V_{CC} \text{ or GND}$	5 V	2	10				10	pF	

(1) Product Preview

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0 \text{ V}$.

6.6 Timing Requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 4](#))

		$T_A = 25^\circ\text{C}$		SN54AHC594 ⁽¹⁾		SN74AHC594		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse Duration	RCLK or SRCLK high or low		5.5		5.5		ns
		RCLR or SRCLR low		5		5		
t_{su}	Setup time	SER before SRCLK \uparrow		3.5		3.5		ns
		SRCLK \uparrow before RCLK \uparrow ⁽²⁾		8		8.5		
		SRCLR low before SRCLK \uparrow		8		9		
		SRCLR high (inactive) before SRCLK \uparrow		4.2		4.8		
		RCLR high (inactive) before RCLK \uparrow		4.6		5.3		
t_h	Hold time, data after CLK \uparrow	SER after SRCLK \uparrow		1.5		1.5		ns

(1) Product Preview

(2) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

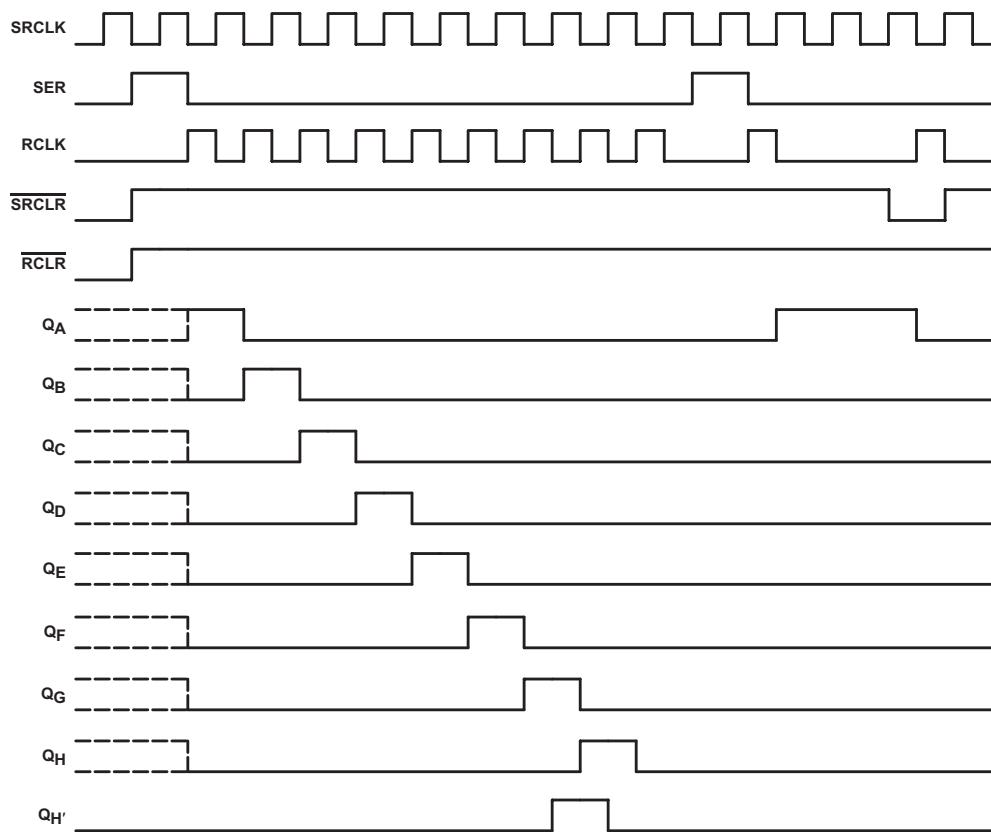
6.7 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 4](#))

		$T_A = 25^\circ\text{C}$		SN54AHC594 ⁽¹⁾		SN74AHC594		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse Duration	RCLK or SRCLK high or low		5		5		ns
		RCLR or SRCLR low		5.2		5.2		
t_{su}	Setup time	SER before SRCLK \uparrow		3		3		ns
		SRCLK \uparrow before RCLK \uparrow ⁽²⁾		5		5		
		SRCLR low before SRCLK \uparrow		5		5		
		SRCLR high (inactive) before SRCLK \uparrow		2.9		3.3		
		RCLR high (inactive) before RCLK \uparrow		3.2		3.7		
t_h	Hold time, data after CLK \uparrow	SER after SRCLK \uparrow		2		2		ns

(1) Product Preview

(2) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.


Figure 1. Timing Diagram

6.8 Switching Characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC594 ⁽¹⁾		SN74AHC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	80 ⁽²⁾	120 ⁽¹⁾		70 ⁽²⁾		70		MHz
			$C_L = 50 \text{ pF}$	55	105		50		50		
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 15 \text{ pF}$	4.6 ⁽³⁾	8 ⁽³⁾	1 ⁽³⁾	8.5 ⁽³⁾	1 ⁽³⁾	8.5		ns
				4.9 ⁽³⁾	8.2 ⁽³⁾	1 ⁽³⁾	8.8 ⁽³⁾	1 ⁽³⁾	8.8		
t_{PLH}	SRCLK	Q_H'	$C_L = 15 \text{ pF}$	5.4 ⁽³⁾	9.1 ⁽³⁾	1 ⁽³⁾	9.7 ⁽³⁾	1 ⁽³⁾	9.7		ns
				5.5 ⁽³⁾	9.2 ⁽³⁾	1 ⁽³⁾	9.9 ⁽³⁾	1 ⁽³⁾	9.9		
t_{PHL}	\overline{RCLR}	$Q_A - Q_H$	$C_L = 15 \text{ pF}$	6 ⁽³⁾	9.8 ⁽³⁾	1 ⁽³⁾	10.6 ⁽³⁾	1 ⁽³⁾	10.6		ns
t_{PHL}	\overline{SRCLR}	Q_H'	$C_L = 15 \text{ pF}$	5.6 ⁽³⁾	9.2 ⁽³⁾	1 ⁽³⁾	10 ⁽³⁾	1 ⁽³⁾	10		ns
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 50 \text{ pF}$	6.9	10.5	1	11.1	1	11.1		ns
				8.1	11.9	1	13.1	1	13.1		
t_{PLH}	SRCLK	Q_H'	$C_L = 50 \text{ pF}$	7.7	11.7	1	12.4	1	12.4		ns
				8.4	12.5	1	13.9	1	13.9		
t_{PHL}	\overline{RCLR}	$Q_A - Q_H$	$C_L = 50 \text{ pF}$	9.1	13.1	1	14.4	1	14.4		ns
t_{PHL}	\overline{SRCLR}	Q_H'	$C_L = 50 \text{ pF}$	8.5	12.4	1	14	1	14		ns

(1) Product Preview

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Switching Characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC594 ⁽¹⁾		SN74AHC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	135 ⁽²⁾	170 ⁽²⁾		115 ⁽²⁾		115		MHz
			$C_L = 50 \text{ pF}$	120	140		95		95		
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 15 \text{ pF}$	3.3 ⁽²⁾	6.2 ⁽²⁾		1 ⁽²⁾	6.5 ⁽²⁾	1	6.5	ns
t_{PHL}				3.7 ⁽²⁾	6.5 ⁽²⁾		1 ⁽²⁾	6.9 ⁽²⁾	1	6.9	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 15 \text{ pF}$	3.7 ⁽²⁾	6.8 ⁽²⁾		1 ⁽¹⁾	7.2 ⁽²⁾	1	7.2	ns
t_{PHL}				4.1 ⁽²⁾	7.2 ⁽²⁾		1 ⁽²⁾	7.6 ⁽²⁾	1	7.6	
t_{PHL}	\overline{RCLR}	$Q_A - Q_H$	$C_L = 15 \text{ pF}$	4.5 ⁽²⁾	7.6 ⁽²⁾		1 ⁽²⁾	8.2 ⁽²⁾	1	8.2	ns
t_{PHL}	\overline{SRCLR}	$Q_{H'}$	$C_L = 15 \text{ pF}$	4.1 ⁽²⁾	7.1 ⁽²⁾		1 ⁽²⁾	7.6 ⁽²⁾	1	7.6	ns
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 50 \text{ pF}$	4.9	7.8		1	8.3	1	8.3	ns
t_{PHL}				5.8	8.9		1	9.7	1	9.7	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 50 \text{ pF}$	5.5	8.6		1	9.1	1	9.1	ns
t_{PHL}				6	9.2		1	10.1	1	10.1	
t_{PHL}	\overline{RCLR}	$Q_A - Q_H$	$C_L = 50 \text{ pF}$	6.6	10		1	10.7	1	10.7	ns
t_{PHL}	\overline{SRCLR}	$Q_{H'}$	$C_L = 50 \text{ pF}$	6	9.2		1	10.1	1	10.1	ns

(1) Product Preview

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.10 Noise Characteristics

$V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER	SN74AHC594			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.6	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.8	V
$V_{IH(D)}$	High-level dynamic input voltage		3.5	V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

(1) Characteristics are for surface-mount packages only.

6.11 Operating Characteristics

$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance No load, $f = 1 \text{ MHz}$	112	pF

6.12 Typical Characteristics

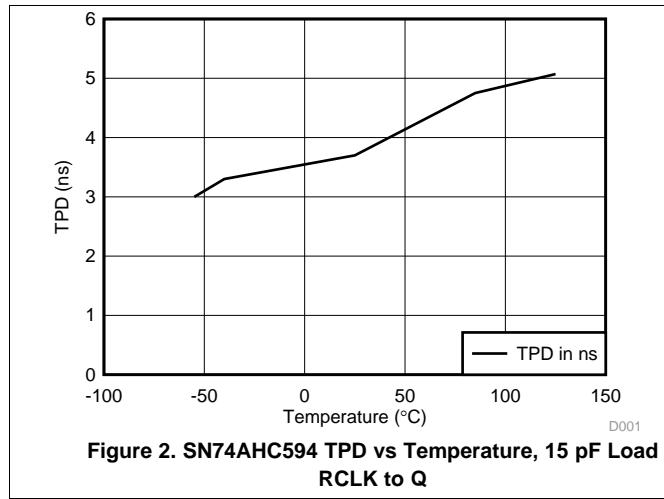


Figure 2. SN74AHC594 TPD vs Temperature, 15 pF Load
RCLK to Q

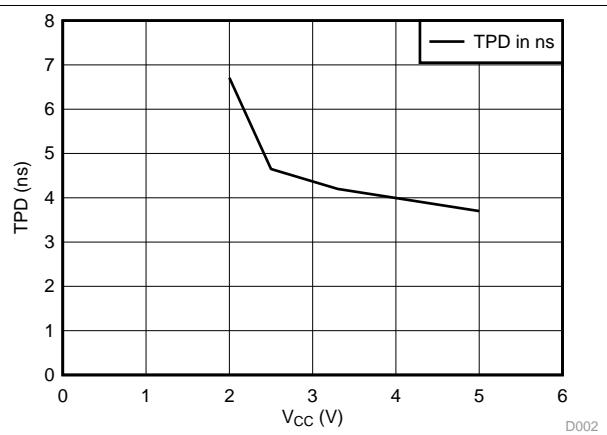
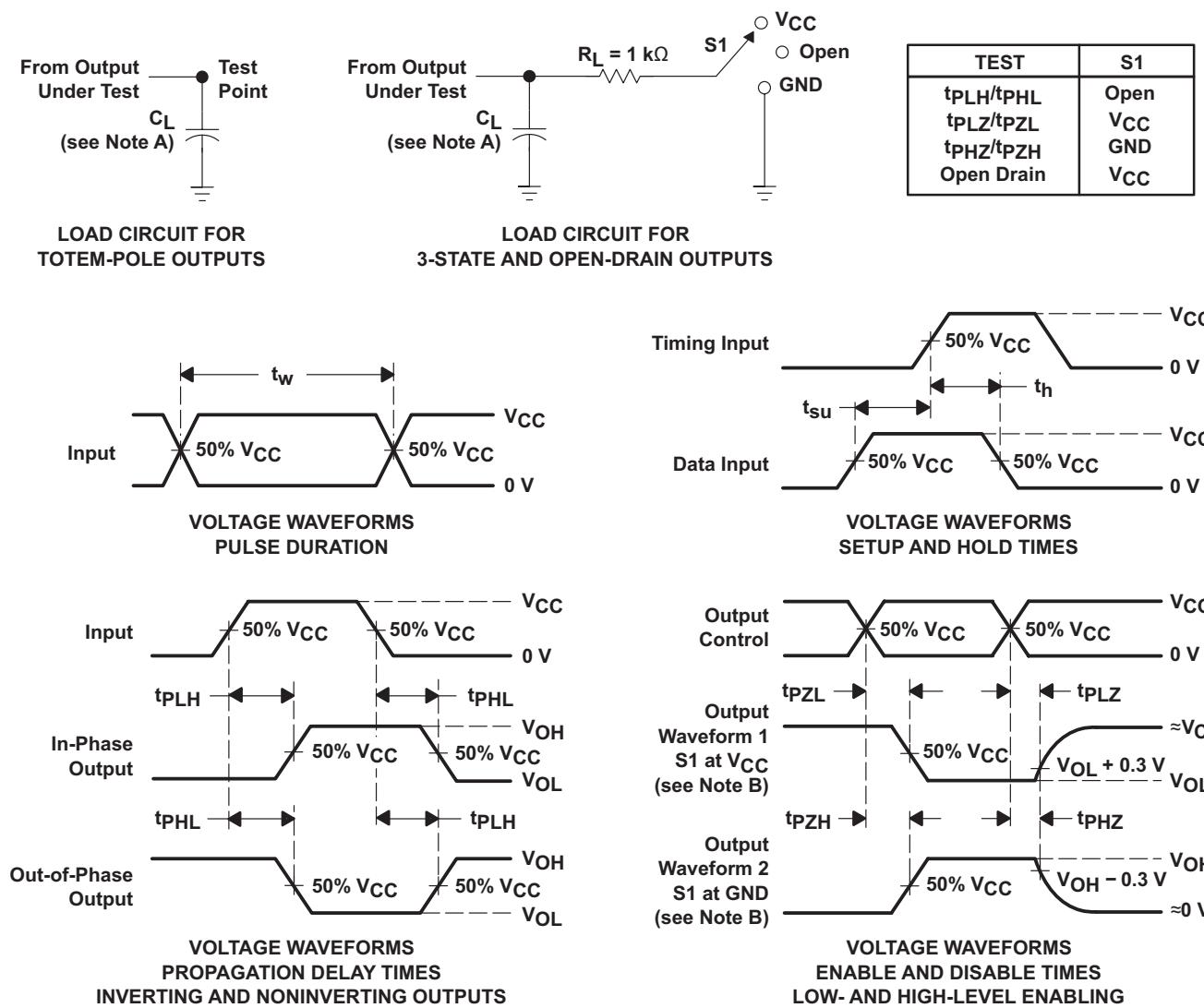


Figure 3. TPD vs V_{CC}

7 Parameter Measurement Information



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
- The outputs are measured one at a time with one input transition per measurement.

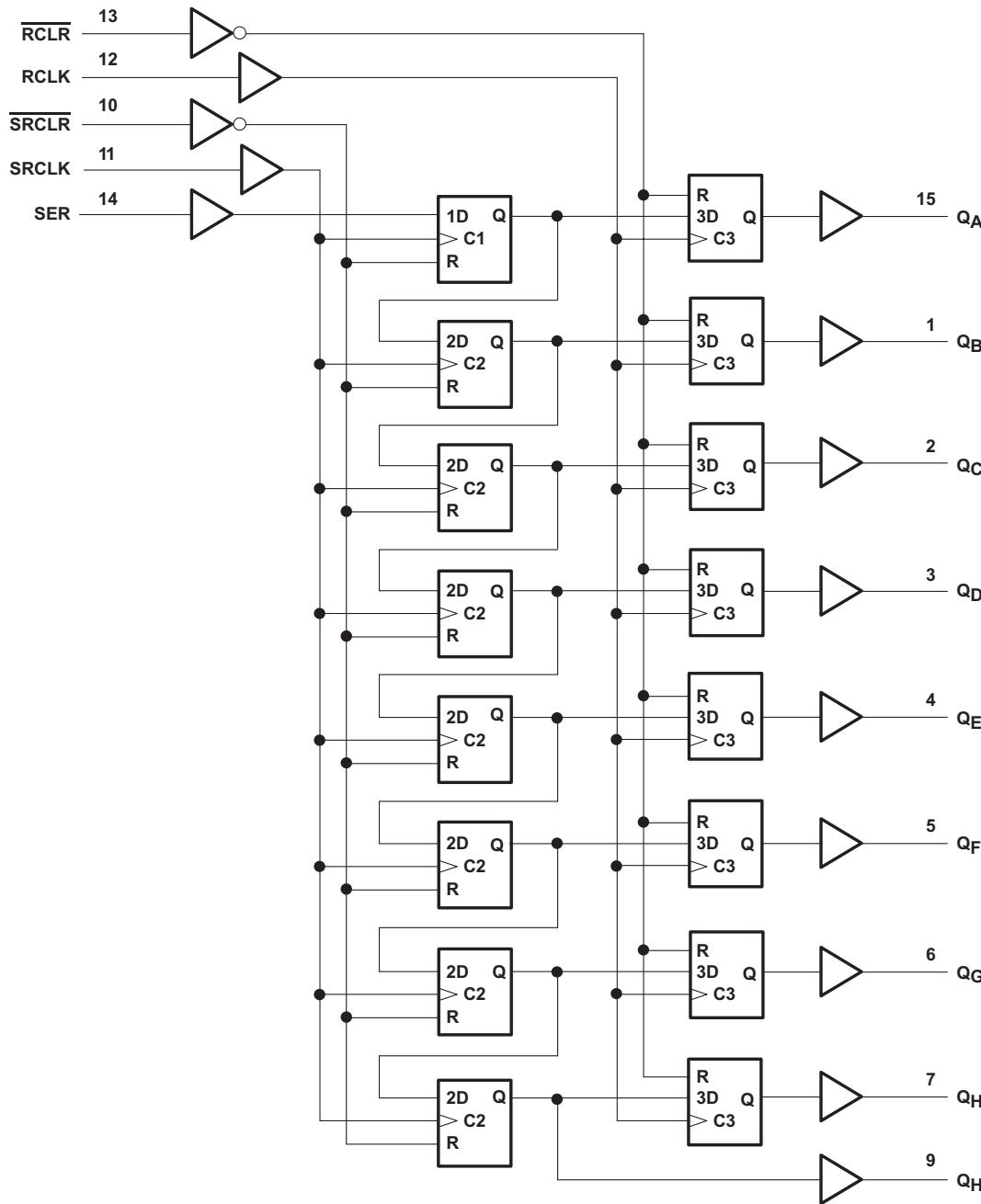
Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4AHC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear (SRCLR, RCLR) inputs are provided on the shift and storage registers. A serial (Q_H') output is provided for cascading purposes. The shift register (SRCLK) and storage register (RCLK) clocks are positive-edge triggered. If the clocks are tied together, the shift register always is one clock pulse ahead of the storage register.

8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

8.3 Feature Description

- Allows for down translation
 - Inputs are tolerant up to 5.5 V
- Slow edges for reduced noise
- Low power

8.4 Device Functional Modes

Table 1. Function Table

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	RCLR	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

9 Application and Implementation

9.1 Application Information

The SN74AHC594 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs accept voltages up to 5.5 V allowing down translation to the V_{CC} level. [Figure 6](#) shows how the slower edges can reduce ringing on the output compared to higher drive parts like AC.

9.2 Typical Application

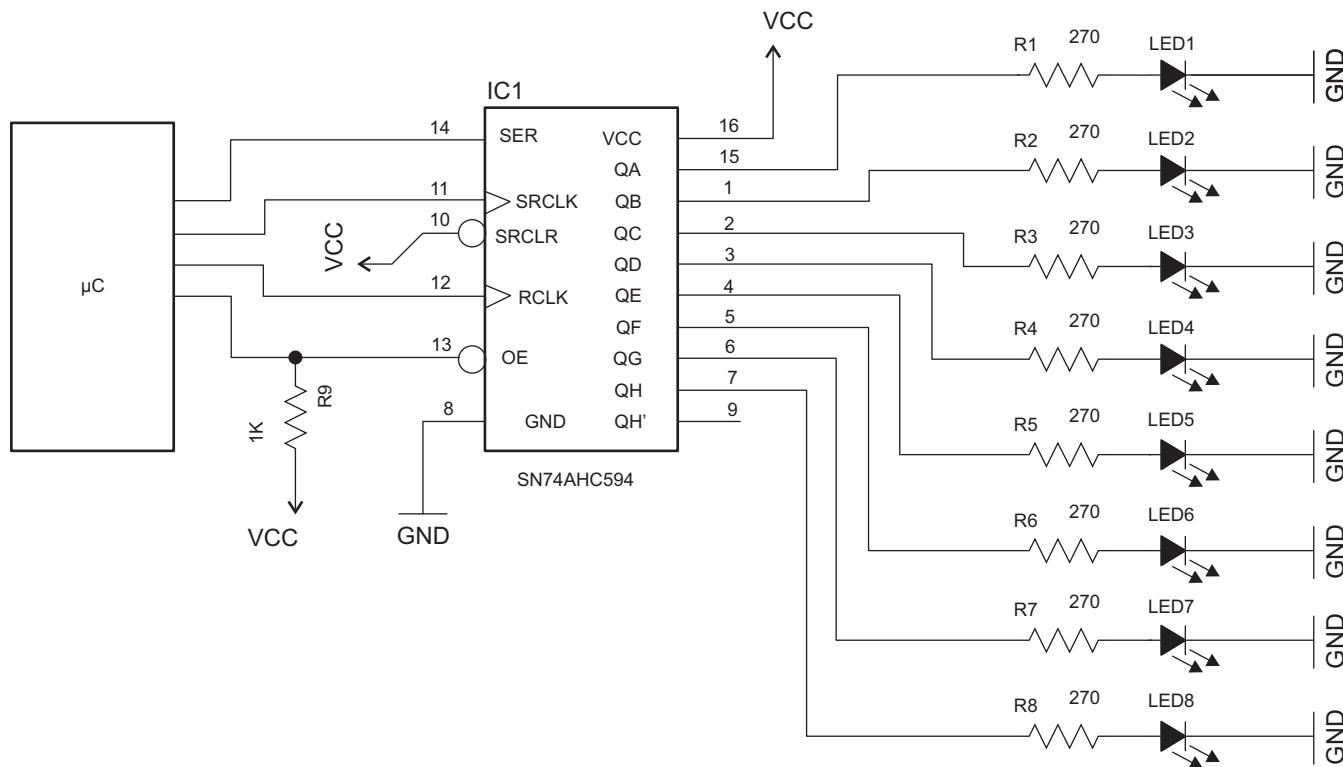


Figure 5. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - Rise time and fall time specs: See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels: See $(V_{IH}$ and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 75 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

9.2.3 Application Curves

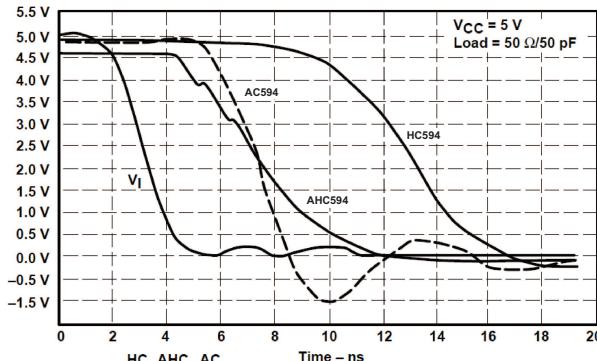


Figure 6. Switching Characteristics Comparison

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended; if there are multiple V_{CC} pins, then 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and a 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 7 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

11.2 Layout Example

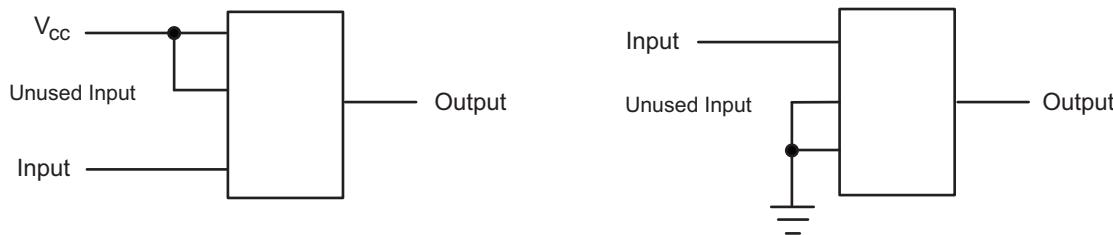


Figure 7. Layout Diagram

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC594	Click here				
SN74AHC594	Click here				

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022 — TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC594D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594	Samples
SN74AHC594DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA594	Samples
SN74AHC594DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594	Samples
SN74AHC594DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594	Samples
SN74AHC594DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594	Samples
SN74AHC594N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC594N	Samples
SN74AHC594NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC594N	Samples
SN74AHC594NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594	Samples
SN74AHC594NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594	Samples
SN74AHC594PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA594	Samples
SN74AHC594PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA594	Samples
SN74AHC594PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA594	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

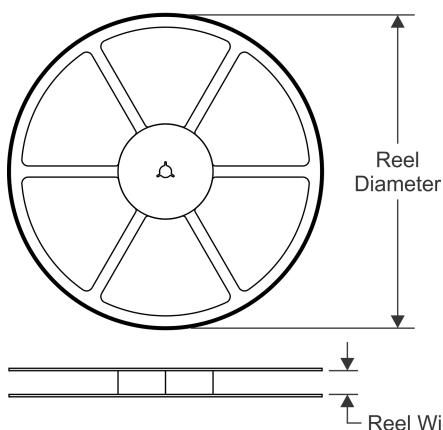
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

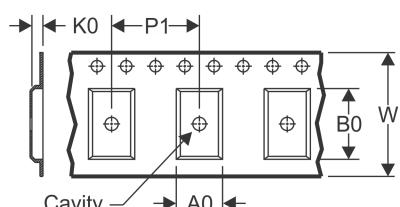
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

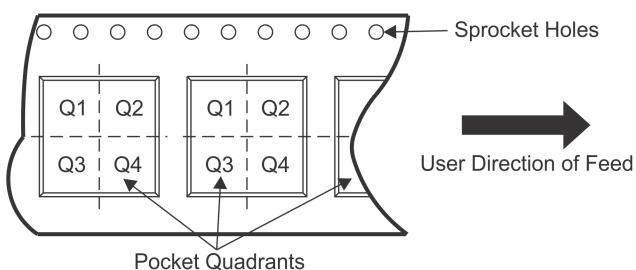


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All dimensions are nominal													
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant	
SN74AHC594DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1	
SN74AHC594DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1	
SN74AHC594NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1	
SN74AHC594PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1	

TAPE AND REEL BOX DIMENSIONS

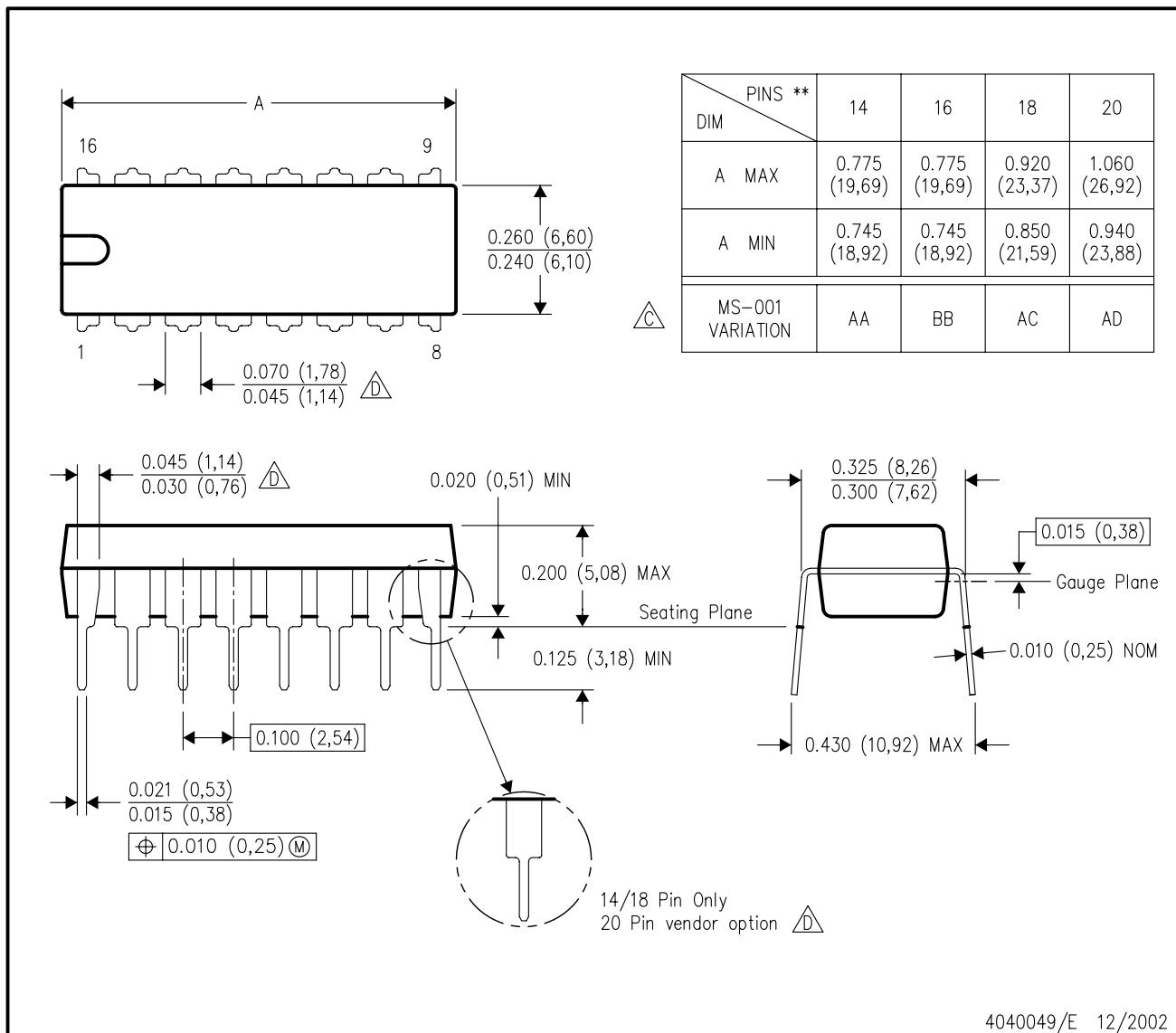

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC594DBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74AHC594DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74AHC594NSR	SO	NS	16	2000	367.0	367.0	38.0
SN74AHC594PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



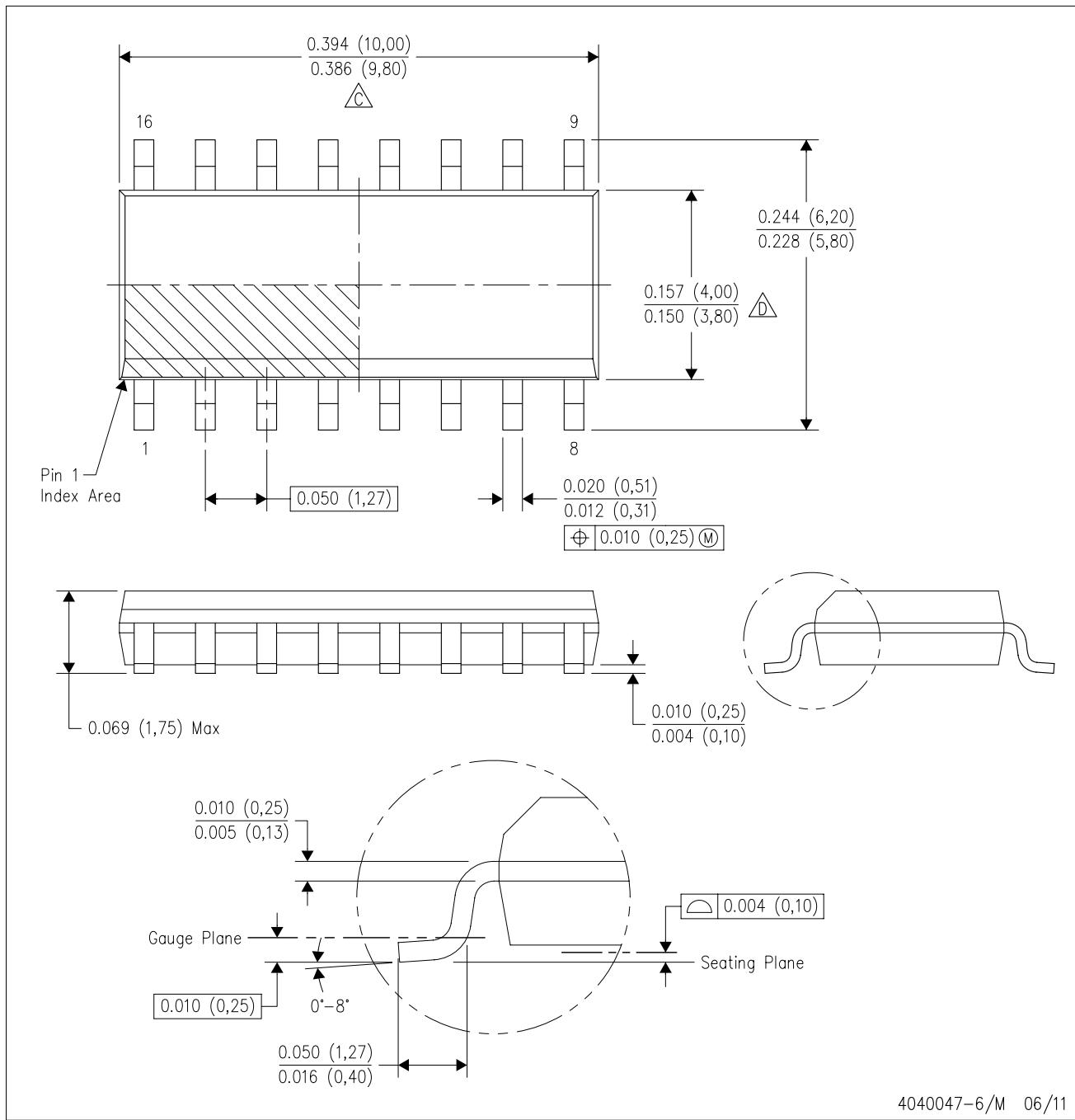
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

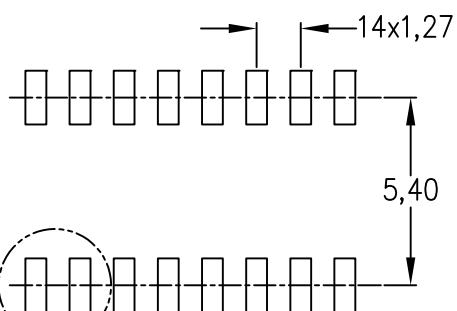
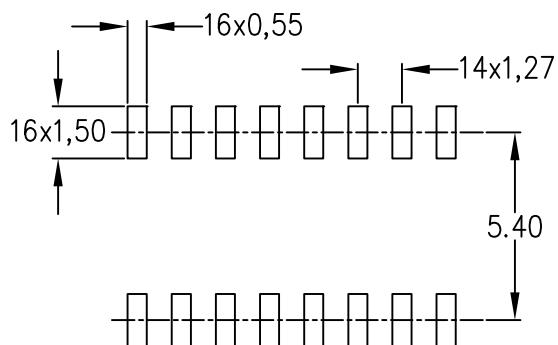
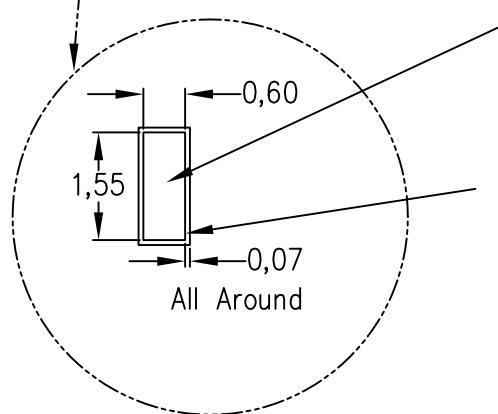
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

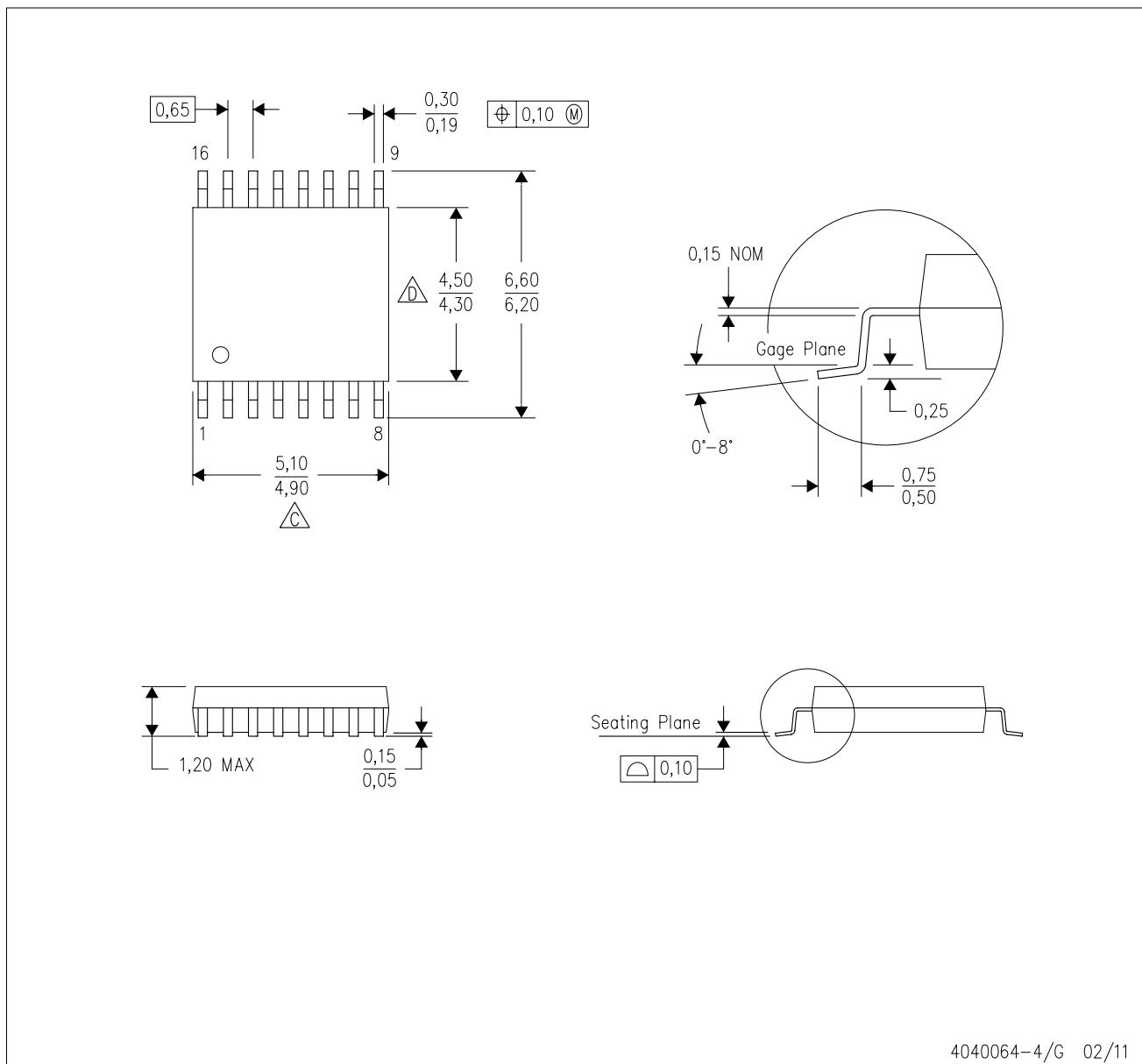
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

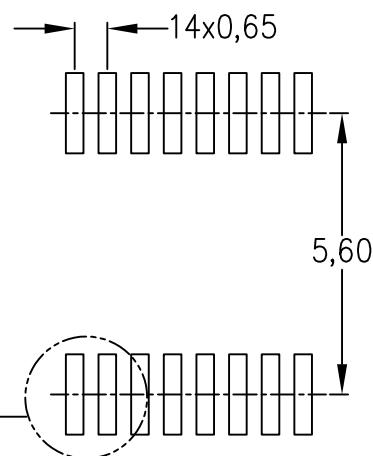
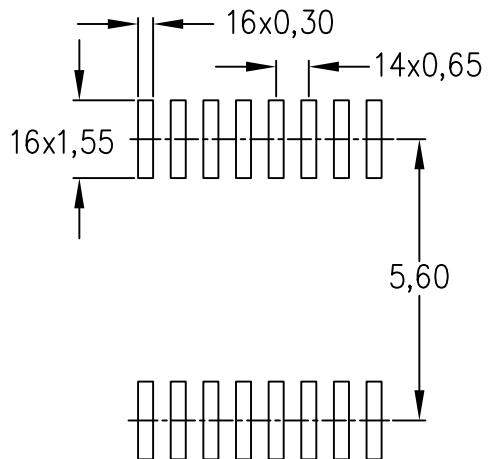
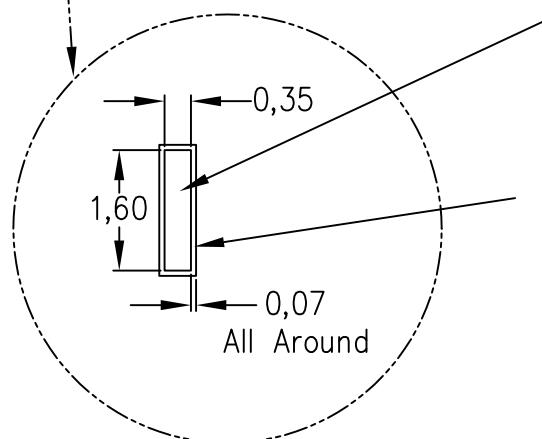
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

4040064-4/G 02/11

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211284-3/F 12/12

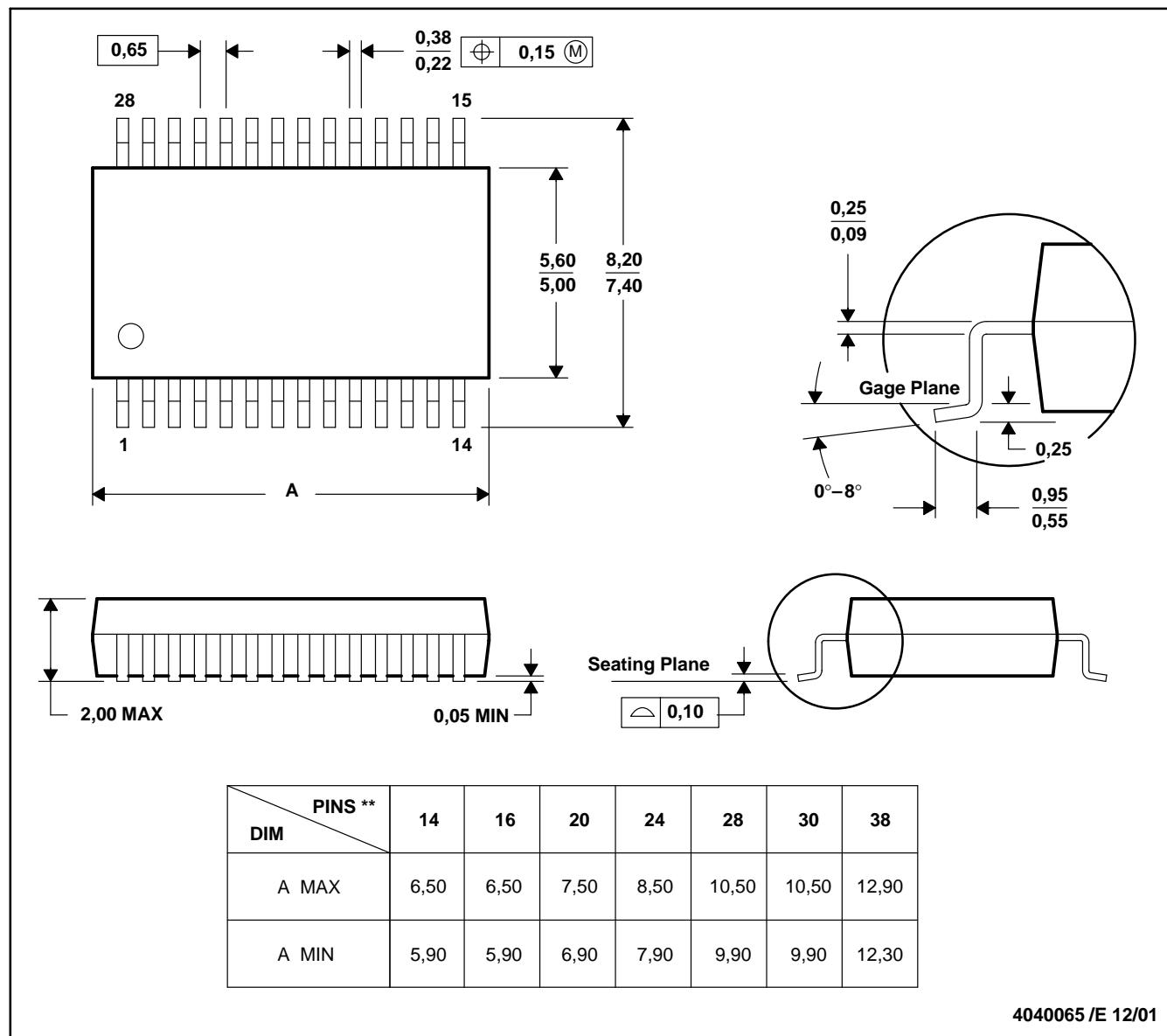
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



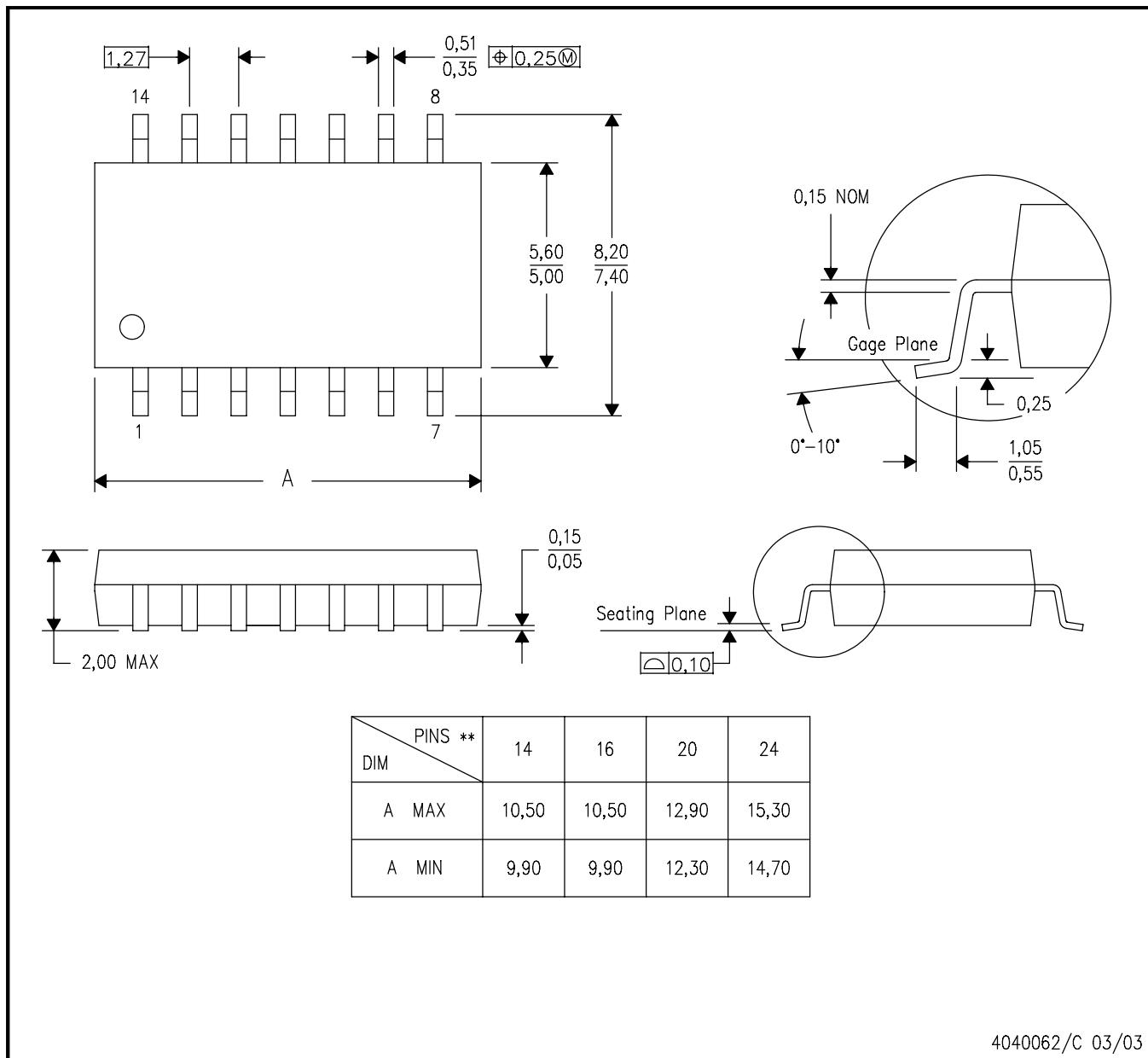
NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications
Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity
	TI E2E Community
	e2e.ti.com