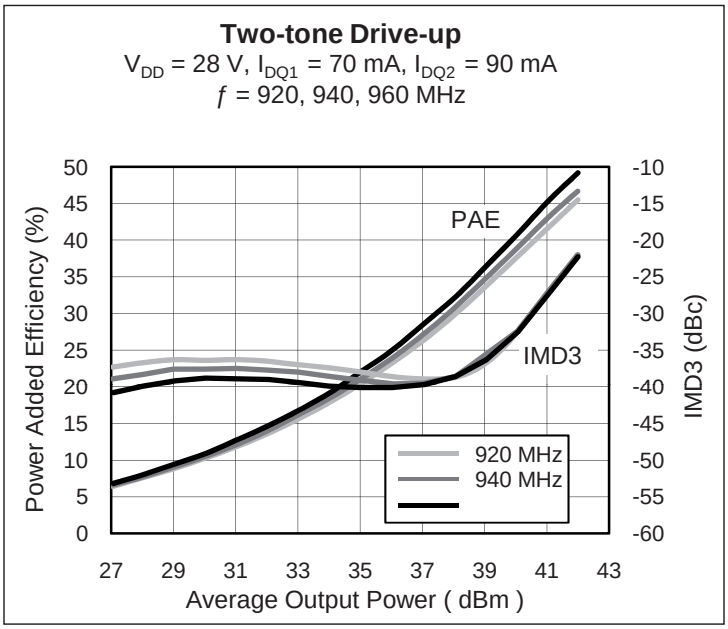
Wideband RF LDMOS Integrated Power Amplifier
15 W, 28 V, 700 – 1000 MHz

Description

The PTMA080152M is a wideband, on chip–matched, 15-watt, 2-stage LDMOS integrated power amplifier intended for wideband driver applications in the 700 to 1000 MHz frequency range. It is offered in a 20-lead thermally-enhanced overmolded package for cool and reliable operation.

PTMA080152M
Package PG-DSO-20-63



Features

- Broadband on-chip matching, 50-ohm input and ~10-ohm output
- Typical GSM/EDGE performance at 28 V, 920 to 960 MHz
  - Gain = 30 dB
  - Efficiency = 34% at 8 W output power
  - EVM @ 8 W = 1.5%
  - ACPR @ 400 kHz = –61 dBc
  - ACPR @ 600 kHz = –75 dBc
- Typical CW performance, 940 MHz, 28 V
  - Output power at P_{1dB} = 20 W
  - Efficiency = 49%
- Integrated ESD protection. Meets HBM Class 1B (minimum), per JESD22-A114F.
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 28 V, 20 W (CW) output power
- RoHS-compliant package

RF Characteristics

GSM/EDGE Characteristics (not subject to production test—verified by design/characterization in Infineon test fixture)

V_{DD} = 28 V, I_{DQ1} = 70 mA, I_{DQ2} = 120 mA, f = 920 to 960 MHz, P_{OUT} = 8 W Avg.

Characteristic	Symbol	Min	Typ	Max	Unit
Input Return Loss	IRL	—	–15	—	dB
Gain	G_{ps}	—	30	—	dB
Power Added Efficiency	PAE	—	34	—	%
Error Vector Magnitude	EVM (RMS)	—	1.5	—	%

table continued next page

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

GSM/EDGE Characteristics (cont.)

V_{DD} = 28 V, I_{DQ1} = 70 mA, I_{DQ2} = 120 mA, f = 920 to 960 MHz, P_{OUT} = 8 W Avg.

Characteristic		Symbol	Min	Typ	Max	Unit
Modulation Spectrum	400 kHz offset	ACPR1	—	–61	—	dBc
	600 kHz offset	ACPR2	—	–75	—	dBc
Spurs Load 3:1		—	—	—	–60	dBc
Gain Flatness		ΔG	—	0.2	—	dB

Two-tone Measurements (tested in Infineon test fixture)

V_{DD} = 28 V, I_{DQ1} = 70 mA, I_{DQ2} = 90 mA, P_{OUT} = 8 W avg., f = 940 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	29	30	—	dB
Drain Efficiency	η_D	32.5	33.5	—	%
Third Order Intermodulation Distortion	IMD3	—	–34	–31	dBc

DC Characteristics

Stage 1 Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA
On-state Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	3.48	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ1} = 70 mA,	V_{GS}	2.0	2.5	3.0	V

Stage 2 Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA
On-state Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.6	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ2} = 90 mA	V_{GS}	2.0	—	3.0	V

Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	65	V
Gate-Source Voltage		V_{GS}	–0.5 to +12	V
Junction Temperature		T_J	200	°C
Input Power		P_{IN}	15	dBm
Total Device Dissipation		P_D	91	W
Above 25°C derate by			0.52	W/°C
Storage Temperature Range		T_{STG}	–40 to +150	°C
Overall Thermal Resistance (T_{CASE} = 70°C)	Stage 1	$R_{\theta JC}$	8.5	°C/W
P_{OUT} = 15 W, I_{DQ1} = 70 mA, I_{DQ2} = 90 mA	Stage 2	$R_{\theta J0C}$	2.5	°C/W

Moisture Sensitivity Level

Level	Test Standard	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	°C

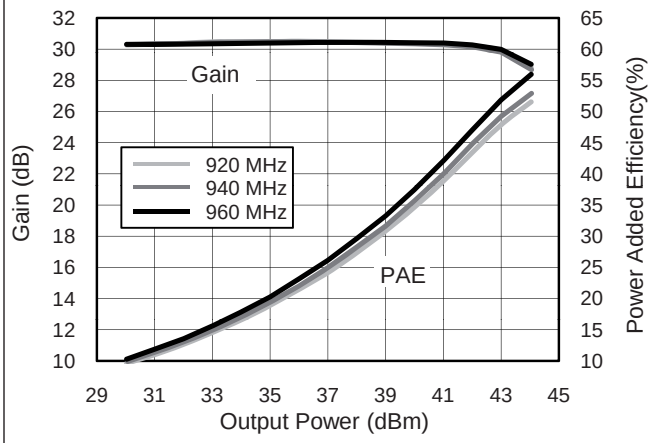
Ordering Information

Type and Version	Order Code	Package and Description	Shipping
PTMA080152M V1	PTMA080152MV1AUMA1	PG-DSO-20-63, molded plastic	Tape & Reel, 250 pcs
PTMA080152M V1 R500	PTMA080152MV1R500AUMA1	PG-DSO-20-63, molded plastic	Tape & Reel, 500 pcs

Typical Performance (data taken in Infineon production test fixture)

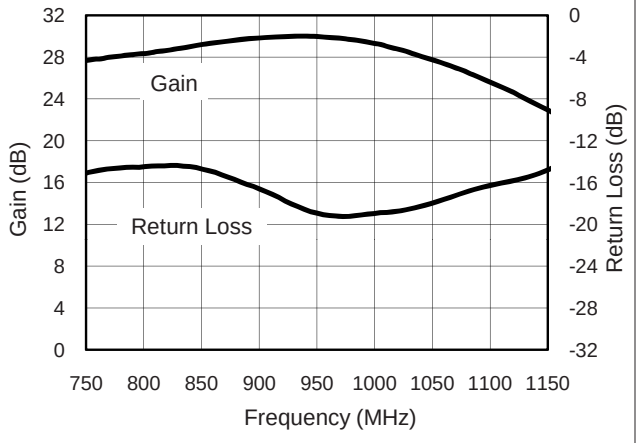
CW Performance

V_{DD} = 28 V, I_{DQ1} = 70 mA, I_{DQ2} = 90 mA
f = 920 , 940, 960 MHz



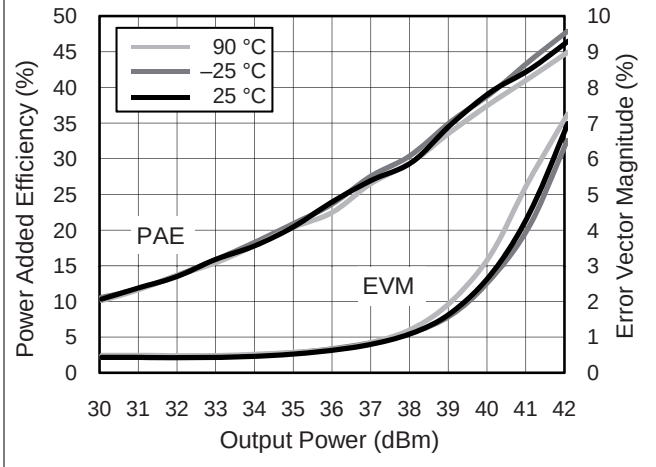
Broadband Performance

V_{DD} = 28 V, I_{DQ1} = 70 mA, I_{DQ2} = 90 mA,
fixture tuned for 920 – 960 MHz



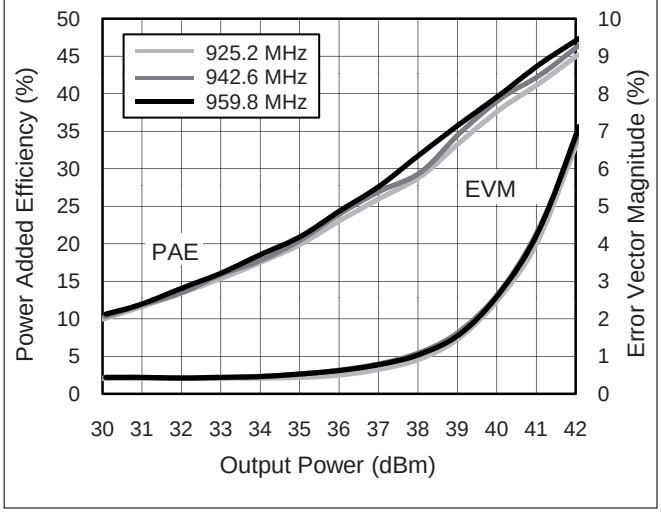
EDGE - EVM

V_{DD} = 28 V, I_{DQ1} = 70 mA, I_{DQ2} = 120 mA,
f = 942.6 MHz



EDGE - EVM

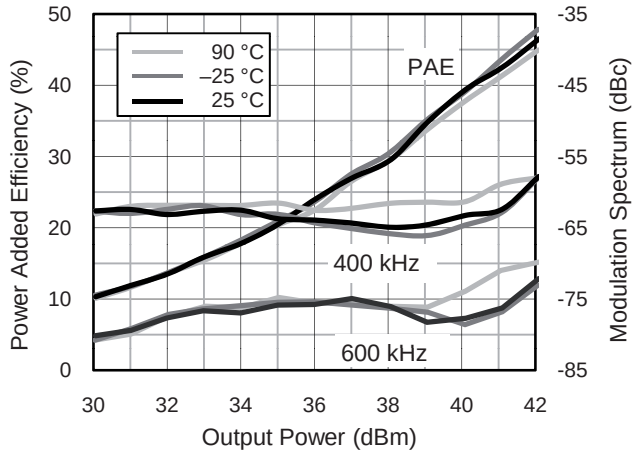
V_{DD} = 28 V, I_{DQ1} = 70 mA, I_{DQ2} = 120 mA,
series are at selected frequencies



Typical Performance (cont.)

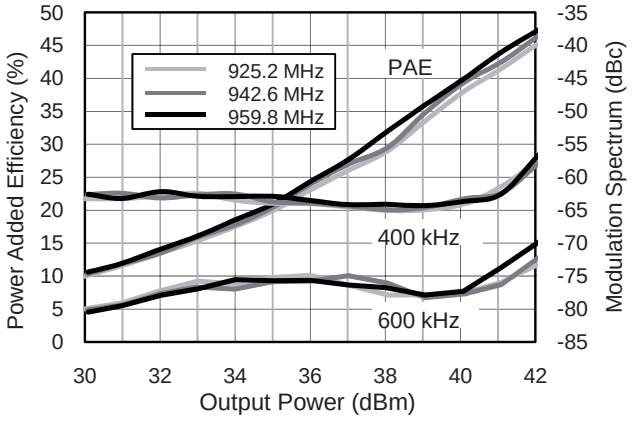
EDGE Modulation Spectrum Performance

V_{DD} = 28 V, I_{DQ1} = 70 mA, I_{DQ2} = 120 mA,
series show f = 942.6 MHz, at selected temperatures



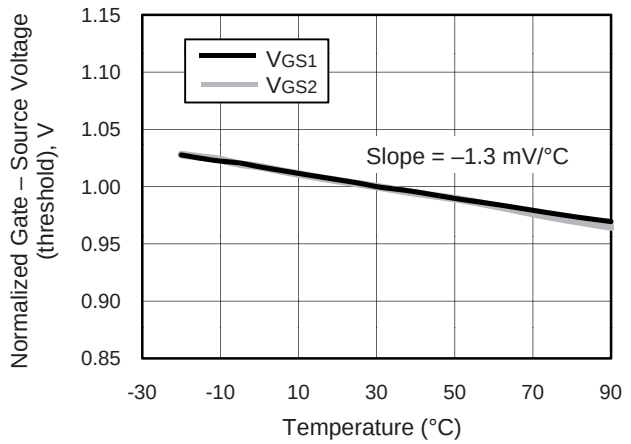
EDGE Modulation Spectrum Performance

V_{DD} = 28 V, I_{DQ1} = 70 mA, I_{DQ2} = 120 mA,
series are at selected frequencies



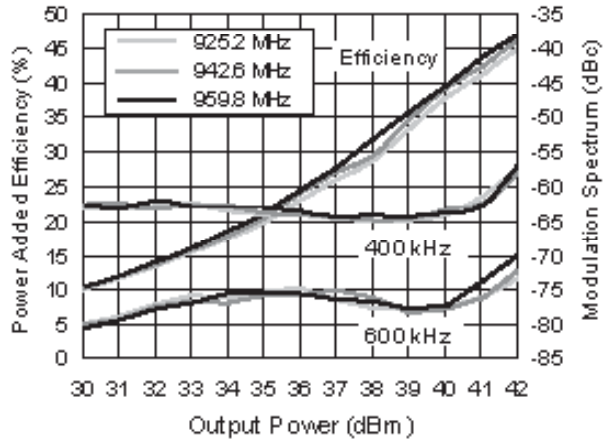
Gate – Source Voltage vs. Temperature

V_{DD} = 28 V, I_{DQ1} = 70 mA, I_{DQ2} = 90 mA



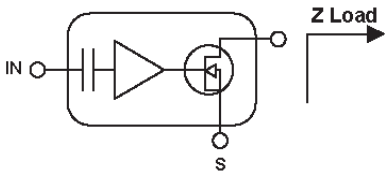
EDGE Modulation Spectrum Performance

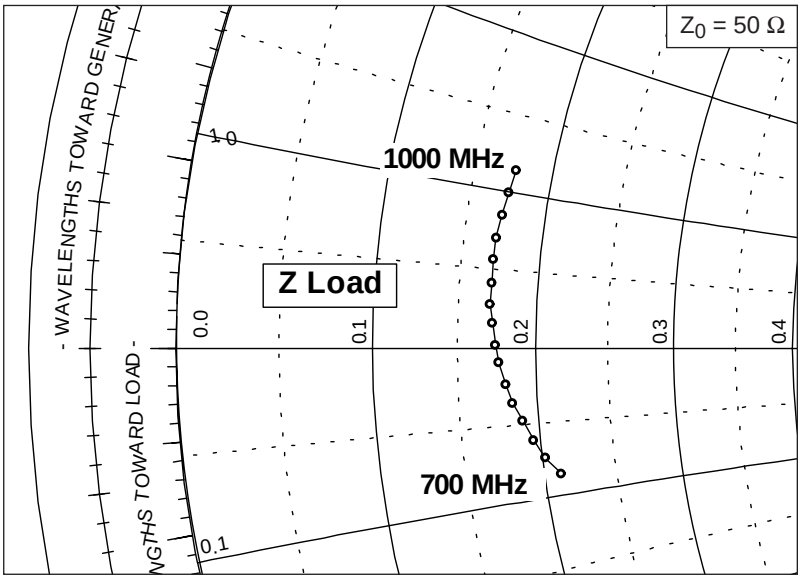
V_{DD} = 28 V, I_{DQ1} = 70 mA, I_{DQ2} = 120 mA,
series are at selected frequencies



Broadband Circuit Impedance

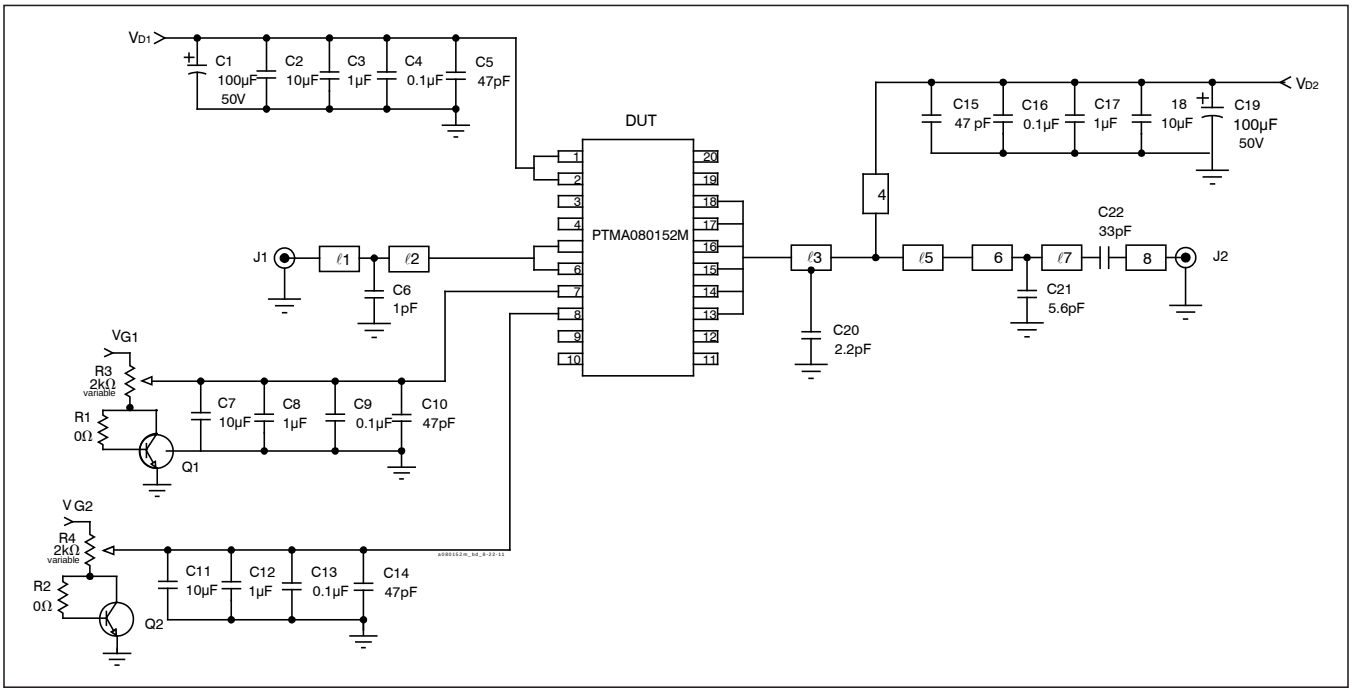
Frequency	Z Load Ω	
MHz	R	jX
700	10.6	–4.3
720	10.1	–3.7
740	9.8	–3.1
760	9.5	–2.4
780	9.2	–1.8
800	9.0	–1.2
820	8.8	–0.5
840	8.7	0.1
860	8.6	0.8
880	8.5	1.4
900	8.5	2.1
920	8.5	2.8
940	8.5	3.5
960	8.6	4.3
980	8.7	5.0
1000	8.8	5.8





See next page for reference circuit information

Reference Circuit

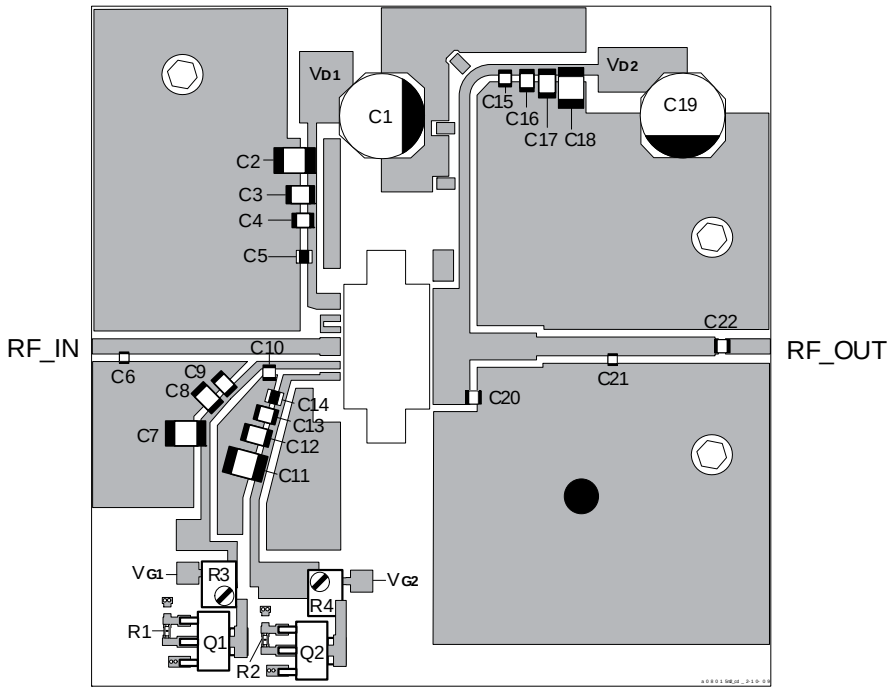


Reference circuit schematic for ƒ = 940 MHz

Circuit Assembly Information	
DUT	PTMA080152M, LDMOS IC
Reference Fixture Part No.	LTN/PTMA080152M
PCB	0.76 mm [.030"] thick, ε_r = 3.48, Rogers RO4350, 1 oz. copper
Find Gerber files for this reference fixture on the Infineon Web site at (**http://www.infineon.com/rfpower**)	

Microstrip	Electrical Characteristics at 940 MHz	L x W (mm)	L x W (in.)
ℓ1	0.017 λ, 50.0 Ω	3.00 x 1.70	0.118 x 0.067
ℓ2	0.143 λ, 50.0 Ω	24.71 x 1.70	0.973 x 0.067
ℓ3	0.024 λ, 10.6 Ω	4.09 x 12.70	0.161 x 0.500
ℓ4	0.144 λ, 59.0 Ω	24.77 x 1.30	0.975 x 0.051
ℓ5	0.044 λ, 34.0 Ω	7.57 x 3.02	0.298 x 0.119
ℓ6	0.044 λ, 44.0 Ω	8.33 x 2.11	0.328 x 0.083
ℓ7	0.0702 λ, 44.0 Ω	12.12 x 2.11	0.477 x 0.083
ℓ8	0.030 λ, 44.0 Ω	5.18 x 2.11	0.204 x 0.083

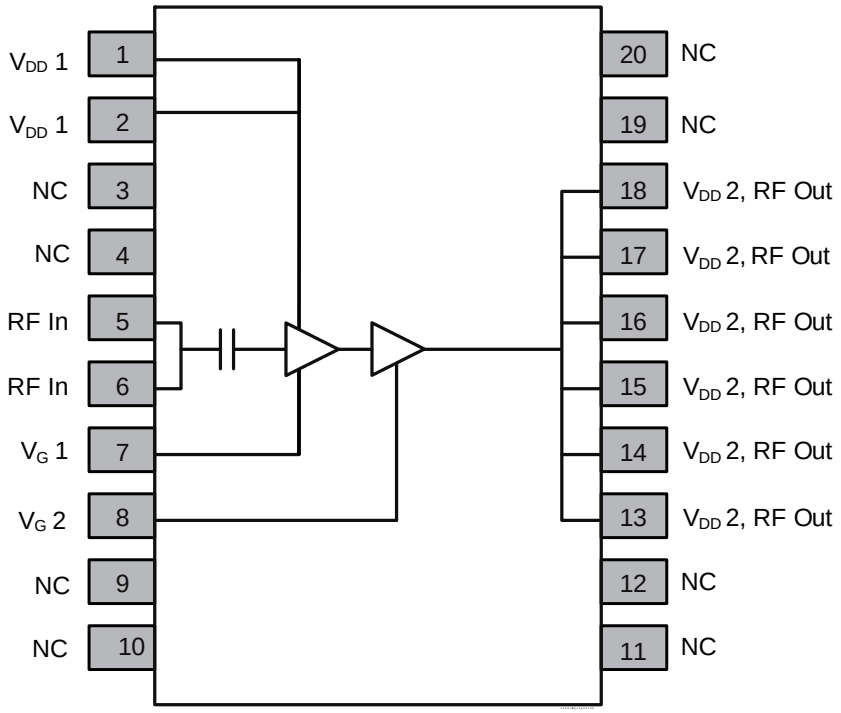
Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)

Component	Description	Suggested Manufacturer	P/N or Comment
C3, C8, C12, C17	Ceramic capacitor, 1 µF	Digi-Key	445-1411-2-ND
C4, C9, C13, C16	Capacitor, 0.1 µF	Digi-Key	PCC104BCT-ND
C2, C7, C11, C18	Tantalum capacitor, 10 µF, 50 V	Digi-Key	P5571-ND
C1, C19	Electrolytic capacitor, 100 µF, 50 V	Digi-Key	PCE3718CT-ND
C6	Ceramic capacitor, 1.0 pF	ATC	600S 1RO CT
C20	Ceramic capacitor, 2.2 pF	ATC	600S 2R2 CT
C21	Ceramic capacitor, 5.6 pF	ATC	600S 5R6 CT
C22	Ceramic capacitor, 33 pF	ATC	600S 330 JT
C5, C10, C14, C15	Ceramic capacitor, 47 pF	ATC	600S 470 JT
Q1, Q2	Transistor	Infineon Technologies	BCP56
R1, R2	Chip resistor, 0 ohms	Digi-Key	PXXECT-ND
R3, R4	Variable resistor, 2K ohms	Digi-Key	3224W-202ETR-ND

Pinout Diagram (top view)



Source/ground: plated copper heatslug on backside of package

Find the latest and most complete information about products and packaging at the Infineon Internet page
http://www.infineon.com/rfpower

Package Outline Specifications

Package PG-DSO-20-63

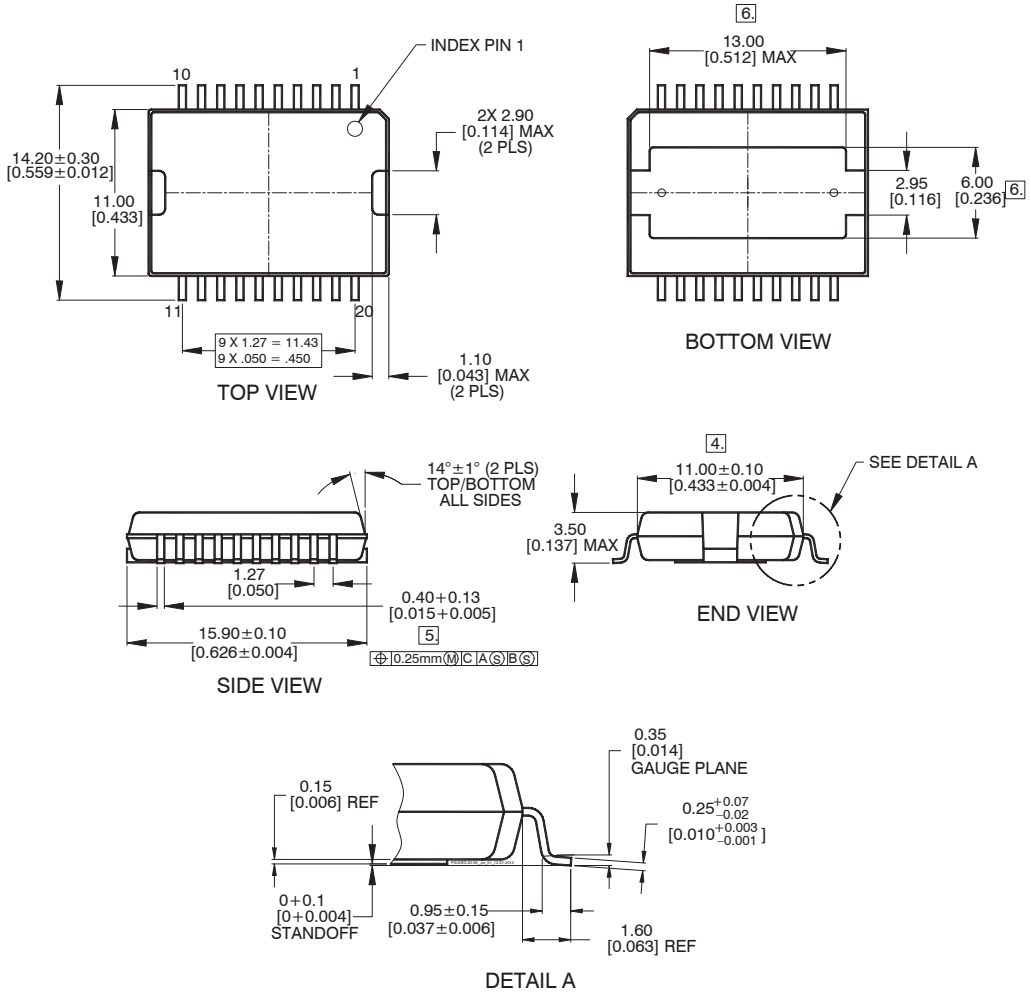


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Package dimensions: 11.0 mm by 15.9 mm by 3.35 mm.
3. JEDEC drawing number: MO-166.
4. Does not include plastic or metal protrusion of 0.15 mm max per side.
5. Does not include dambar protrusion; maximum allowable dambar protrusion shall be 0.08 mm.
6. Bottom metallization.
7. Sn plating (matte): 5 – 15 micron [196.85 – 590.55 microinch].

Refer to Application Note "Recommendations for Printed Circuit Board Assembly of Infineon DSO and SSOP Packages" for additional information.

Revision History

Revision	Date	Data Sheet	Page	Subjects (major changes since last revision)
01	2007-05-05	Preliminary	all	Preliminary specification for new product in development.
02	2009-02-27	Production	all	Revise package information and circuit diagrams, add impedance information.
03	2009-08-31	Production	1	Revise VSWR rating.
04	2010-04-16	Production	3; 10	Add moisture sensitivity information; update package outline notes.
05	2011-05-17	Production	2; 4	Revise DC table; remove graph.
06	2011-08-22	Production	2; all	Revise two-tone table; minor updates to graphics and diagrams for readability.
07	2014-05-07	Production	3	Add shipping option.

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(**highpowerRF@infineon.com**)

To request other information, contact us at:
+1 877 465 3667 (1-877-GO-LDMOS) USA
or +1 408 776 0600 International

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