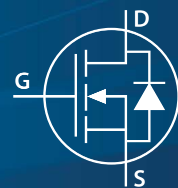
# EPC2007C – Enhancement Mode Power Transistor

$V_{DS}$ , 100 V
$R_{DS(on)}$ , 30 mΩ
$I_D$ , 6 A




EFFICIENT POWER CONVERSION

RoHS | Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low $Q_G$ and zero $Q_{RR}$. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

| Maximum Ratings | | | |
|---|---|---|---|
| PARAMETER | | VALUE | UNIT |
| $V_{DS}$ | Drain-to-Source Voltage (Continuous) | 100 | V |
| $I_D$ | Continuous ($T_A$ = 25˚C, $R_{θJA}$ = 62°C/W) | 6 | A |
| | Pulsed (25°C, $T_{PULSE}$ = 300 µs) | 40 | |
| $V_{GS}$ | Gate-to-Source Voltage | 6 | V |
| | Gate-to-Source Voltage | -4 | |
| $T_J$ | Operating Temperature | -40 to 150 | °C |
| $T_{STG}$ | Storage Temperature | -40 to 150 | |

| Thermal Characteristics | | | |
|---|---|---|---|
| PARAMETER | | TYP | UNIT |
| $R_{θJC}$ | Thermal Resistance, Junction to Case | 3.6 | °C/W |
| $R_{θJB}$ | Thermal Resistance, Junction to Board | 9.3 | |
| $R_{θJA}$ | Thermal Resistance, Junction to Ambient (Note 1) | 80 | |

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

EPC2007C eGaN® FETs are supplied only in passivated die form with solder bumps

**Applications**
- High Speed DC-DC conversion
- Class-D Audio
- Wireless Power Transfer
- LiDAR

**Benefits**
- Ultra High Efficiency
- Zero $Q_{RR}$
- Ultra low $Q_G$
- Ultra small footprint

www.epc-co.com/epc/Products/eGaNFETs/EPC2007C.aspx

| Static Characteristics ($T_J$ = 25˚C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $BV_{DSS}$ | Drain-to-Source Voltage | $V_{GS}$ = 0 V, $I_D$ = 75 µA | 100 | | | V |
| $I_{DSS}$ | Drain-Source Leakage | $V_{GS}$ = 0 V, $V_{DS}$ = 80 V | | 20 | 60 | µA |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | $V_{GS}$ = 5 V | | 0.25 | 2 | mA |
| | Gate-to-Source Reverse Leakage | $V_{GS}$ = -4 V | | 20 | 60 | µA |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 1.2 mA | 0.8 | 1.4 | 2.5 | V |
| $R_{DS(on)}$ | Drain-Source On Resistance | $V_{GS}$ = 5 V, $I_D$ = 6 A | | 24 | 30 | mΩ |
| $V_{SD}$ | Source-Drain Forward Voltage | $I_S$ = 0.5 A, $V_{GS}$ = 0 V | | 2.1 | | V |

All measurements were done with substrate connected to source.

| Dynamic Characteristics ($T_J$ = 25°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $C_{ISS}$ | Input Capacitance | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V | | 170 | 220 | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | 1.9 | 2.7 | |
| $C_{OSS}$ | Output Capacitance | | | 110 | 165 | |
| $R_G$ | Gate Resistance | | | 0.4 | | Ω |
| $Q_G$ | Total Gate Charge | $V_{DS}$ = 50 V, $V_{GS}$ = 5 V, $I_D$ = 6 A | | 1.6 | 2.2 | nC |
| $Q_{GS}$ | Gate-to-Source Charge | $V_{DS}$ = 50 V, $I_D$ = 6 A | | 0.6 | | |
| $Q_{GD}$ | Gate-to-Drain Charge | | | 0.3 | 0.6 | |
| $Q_{G(TH)}$ | Gate Charge at Threshold | | | 0.4 | | |
| $Q_{OSS}$ | Output Charge | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V | | 8.3 | 12.5 | |
| $Q_{RR}$ | Source-Drain Recovery Charge | | | 0 | | |

All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50% $BV_{DSS}$.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50% $BV_{DSS}$.

**Figure 1: Typical Output Characteristics at 25 °C**

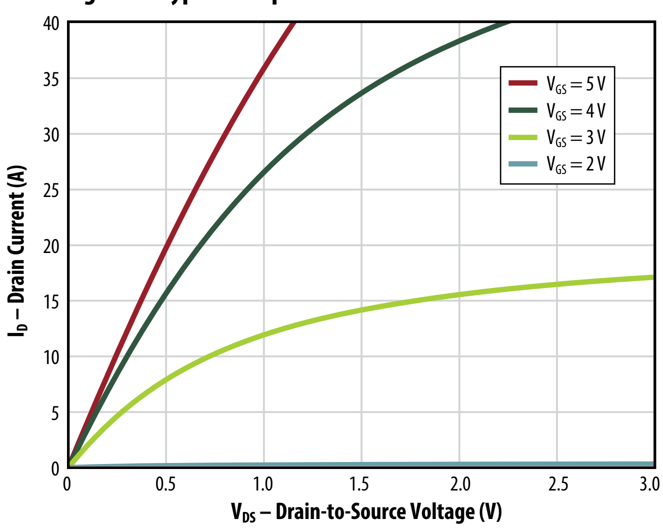



**Figure 2: Transfer Characteristics**

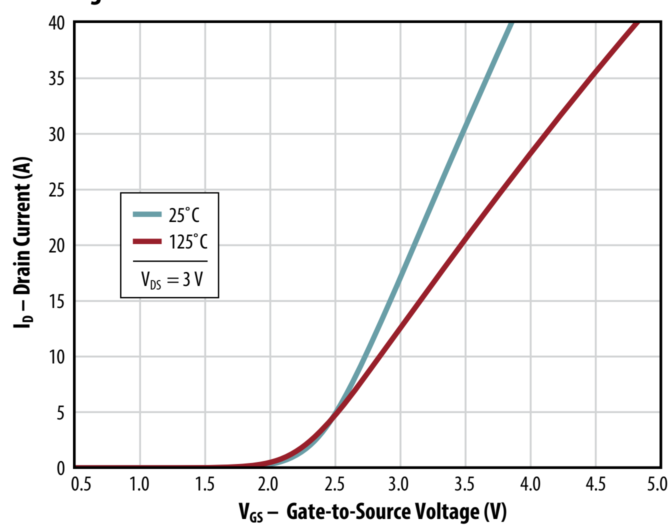



**Figure 3: $R_{DS(on)}$ vs. $V_{GS}$ for Various Drain Currents**

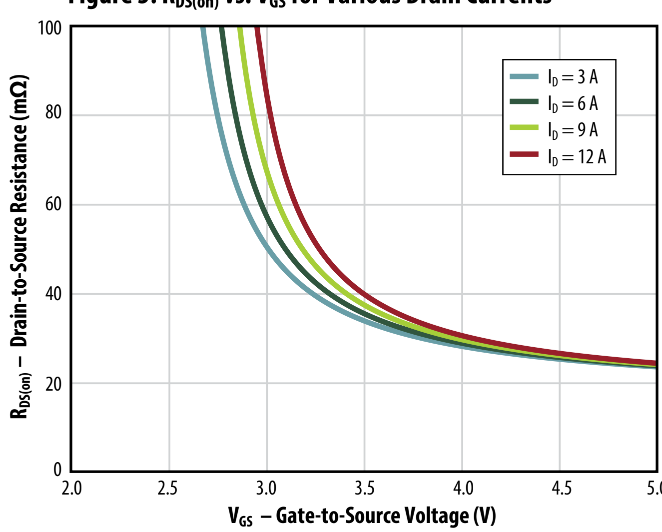



**Figure 4: $R_{DS(on)}$ vs. $V_{GS}$ for Various Temperatures**

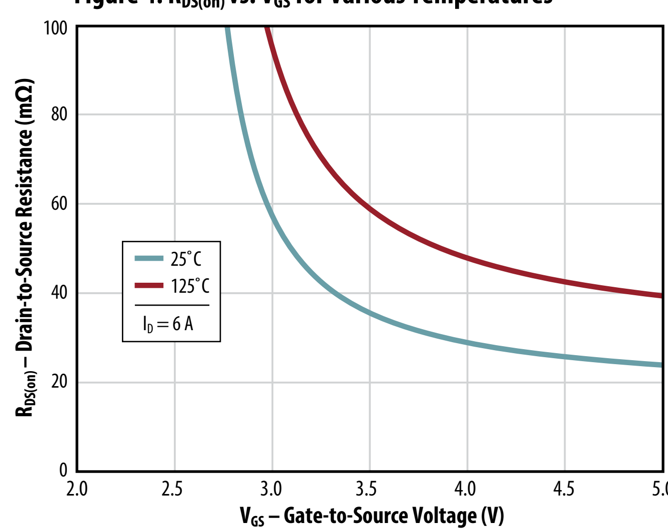


**Figure 5a: Capacitance (Linear Scale)**

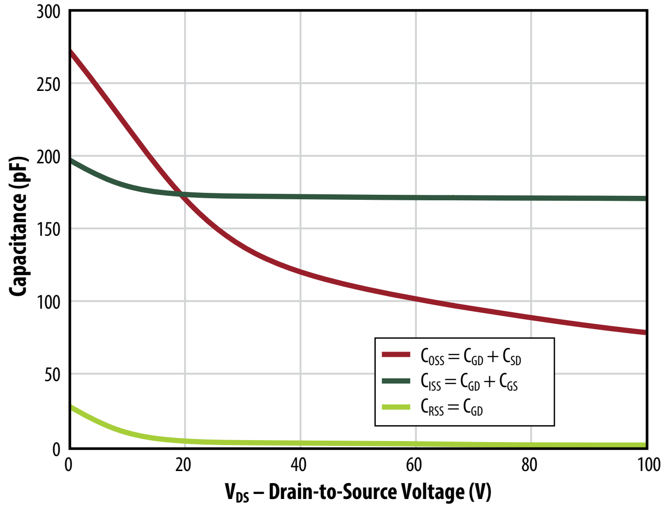



**Figure 5b: Capacitance (Log Scale)**

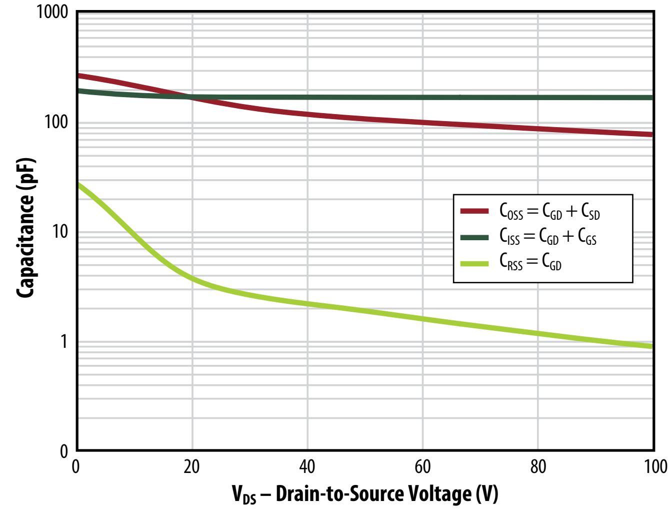



**Figure 6: Gate Charge**

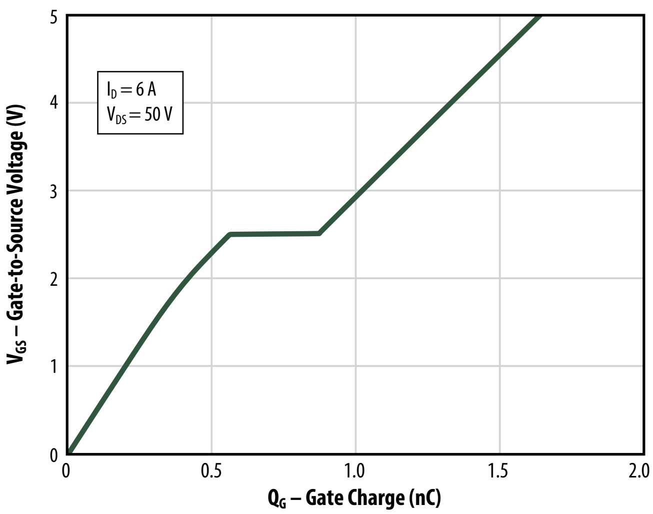



**Figure 7: Reverse Drain-Source Characteristics**

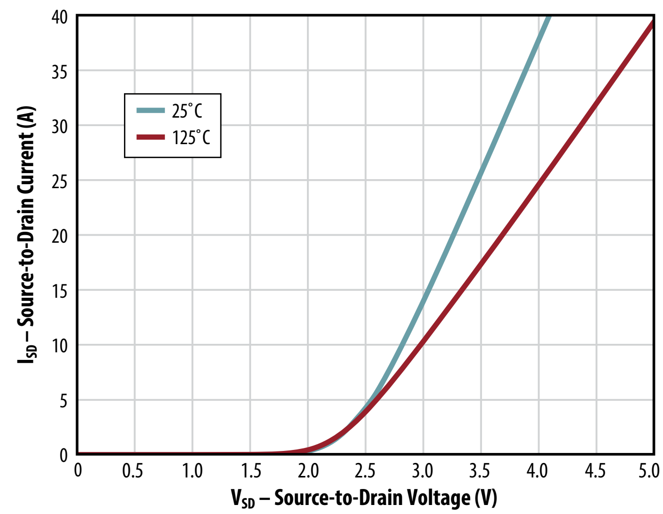



**Figure 8: Normalized On-State Resistance vs. Temperature**

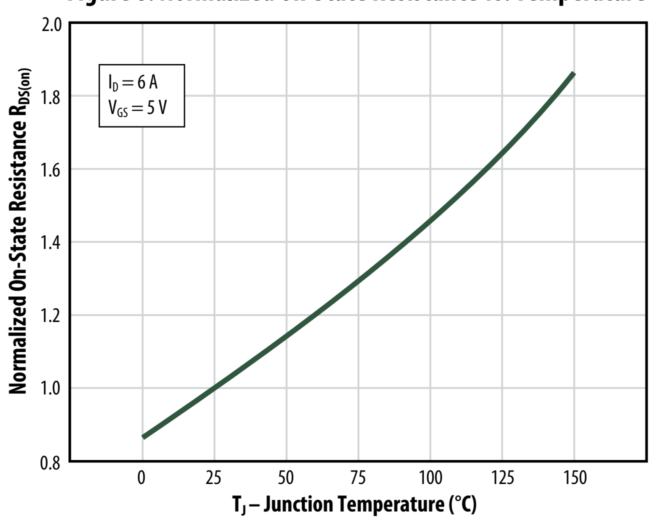
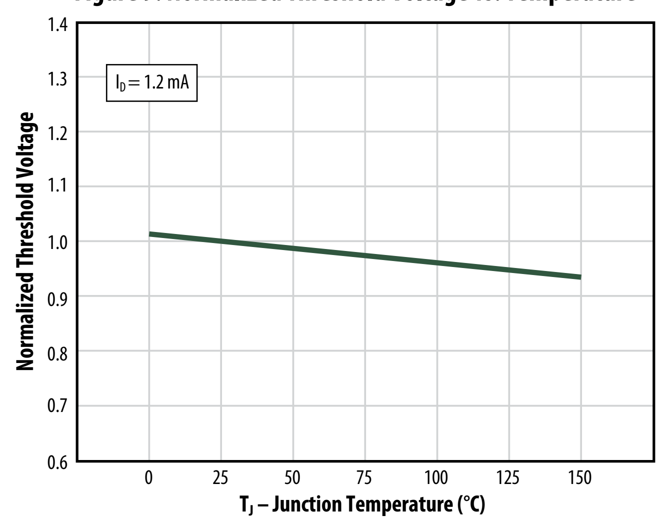



**Figure 9: Normalized Threshold Voltage vs. Temperature**




All measurements were done with substrate shortened to source.

**Figure 10: Gate Leakage Current**

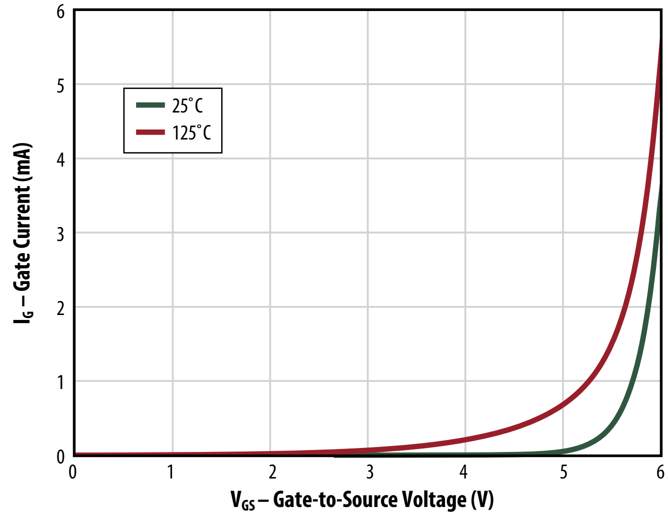
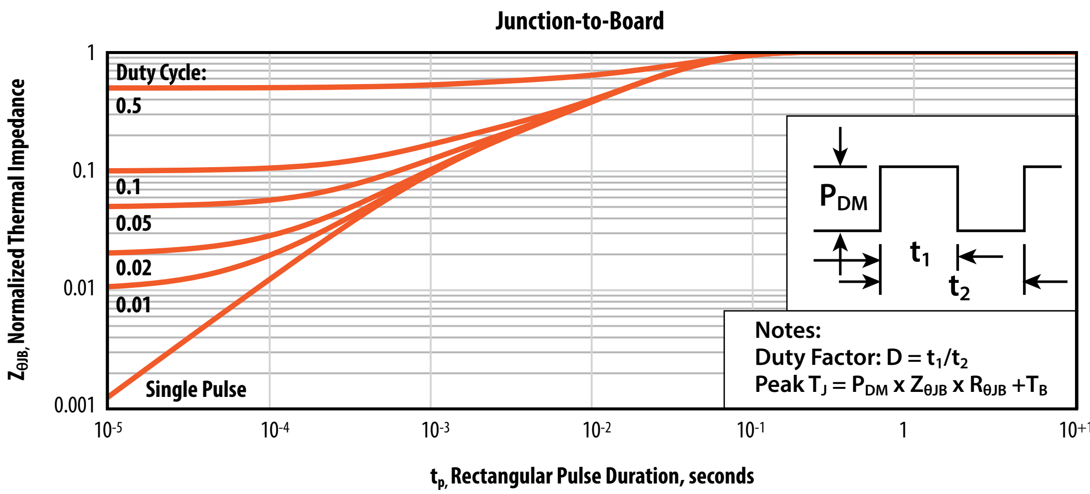



**Figure 11: Transient Thermal Response Curves**



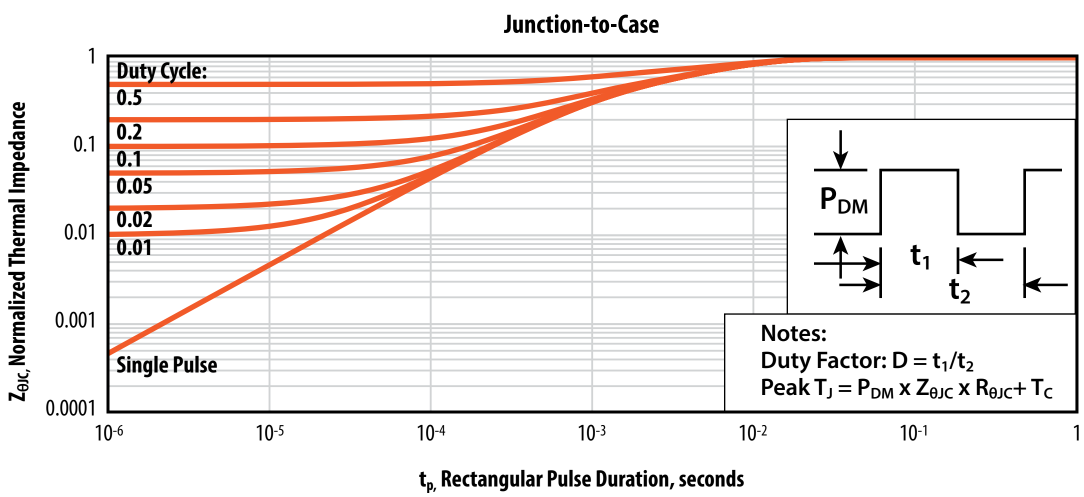
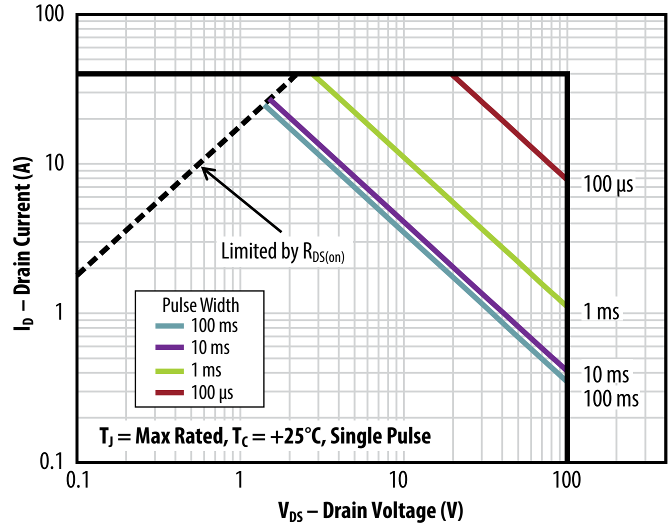
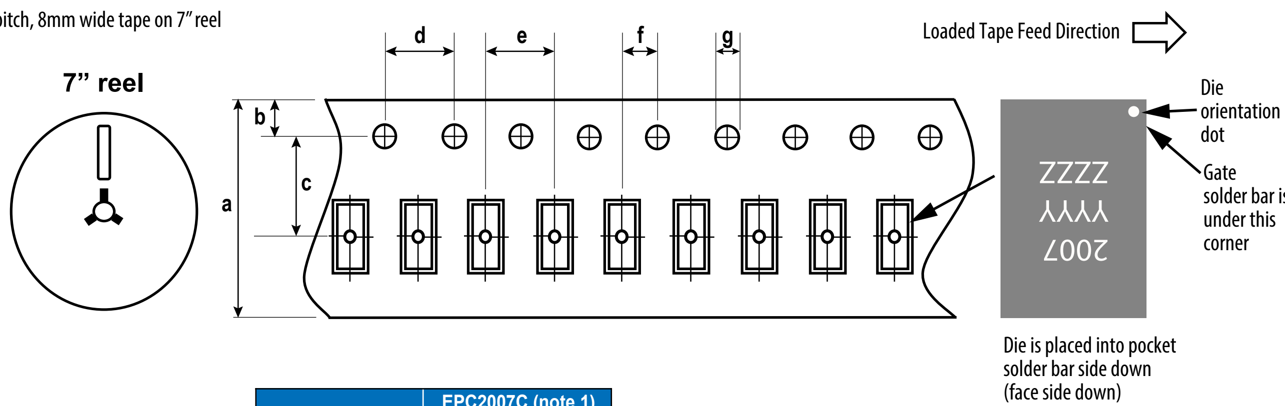



**Figure 12: Safe Operating Area**




## TAPE AND REEL CONFIGURATION

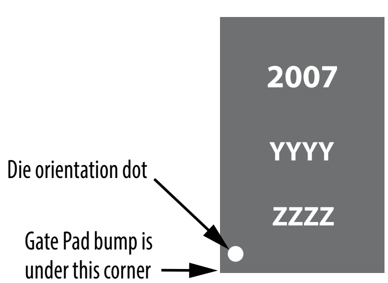
4mm pitch, 8mm wide tape on 7" reel




| | EPC2007C (note 1) | | |
|---|---|---|---|
| Dimension (mm) | target | min | max |
| a | 8.00 | 7.90 | 8.30 |
| b | 1.75 | 1.65 | 1.85 |
| c (note 2) | 3.50 | 3.45 | 3.55 |
| d | 4.00 | 3.90 | 4.10 |
| e | 4.00 | 3.90 | 4.10 |
| f (note 2) | 2.00 | 1.95 | 2.05 |
| g | 1.5 | 1.5 | 1.6 |

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

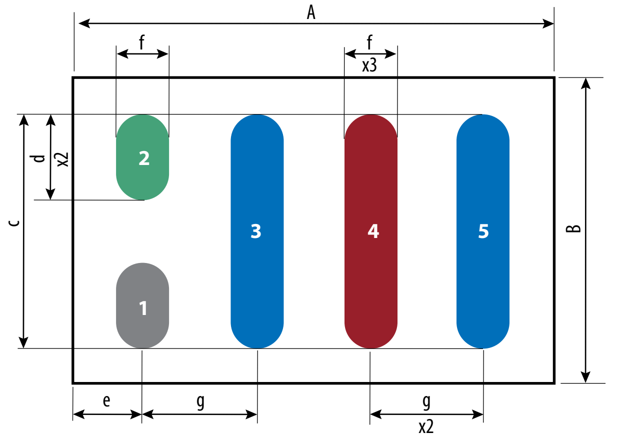
## DIE MARKINGS




| Part Number | Laser Markings | | |
|---|---|---|---|
| | Part # Marking Line 1 | Lot_Date Code Marking line 2 | Lot_Date Code Marking Line 3 |
| EPC2007C | 2007 | YYYY | ZZZZ |

## DIE OUTLINE

Solder Bar View




| DIM | MICROMETERS | | |
|---|---|---|---|
| | MIN | Nominal | MAX |
| A | 1672 | 1702 | 1732 |
| B | 1057 | 1087 | 1117 |
| c | 829 | 834 | 839 |
| d | 311 | 316 | 321 |
| e | 235 | 250 | 265 |
| f | 195 | 200 | 205 |
| g | 400 | 400 | 400 |

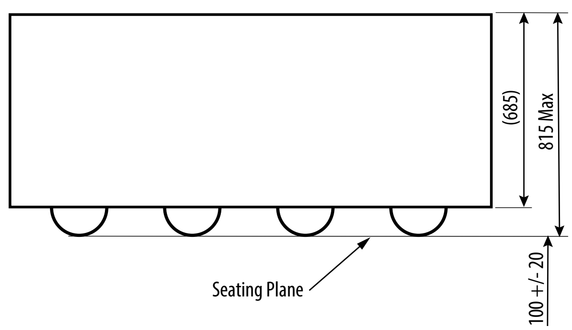
Pad no. 1 is Gate;

Pad no. 2 is Substrate;

Pads no. 3 and 5 are Drain;

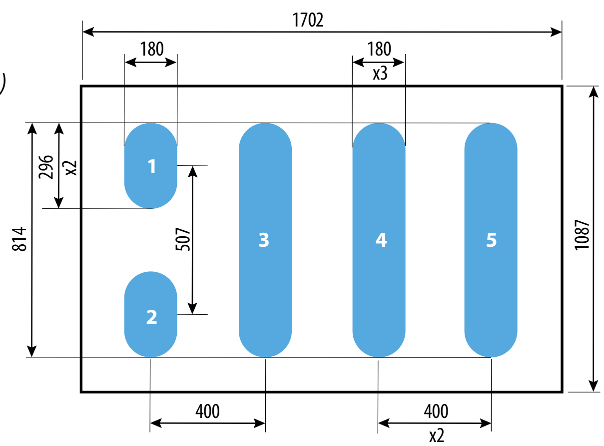
Pad no. 4 is Source

Side View




## RECOMMENDED LAND PATTERN

*(measurements in µm)*




The land pattern is solder mask defined

Solder mask is 10 µm smaller per side than bump

Pad no. 1 is Gate

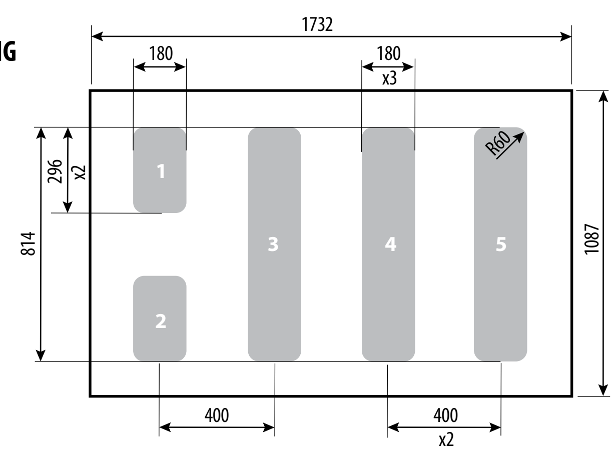
Pad no. 2 is Substrate

Pads no. 3 and 5 are Drain

Pad no. 4 is Source

## RECOMMENDED STENCIL DRAWING

*(units in µm)*




Recommended stencil should be 4 mil (100 µm) thick, must be laser cut , opening per drawing. The corner has a radius of R60.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx



Information subject to change without notice.

Revised October, 2018