

SN54ABT833, SN74ABT833 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS195C – FEBRUARY 1991 – REVISED JANUARY 1997

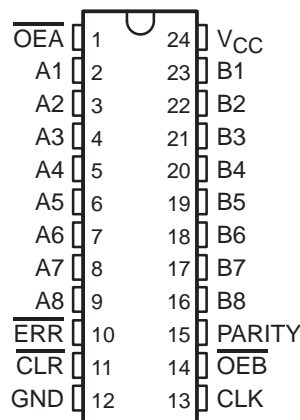
- State-of-the-Art **EPIC-IITM** BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Parity Error Flag With Parity Generator/Checker
- Register for Storage of the Parity Error Flag
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

description

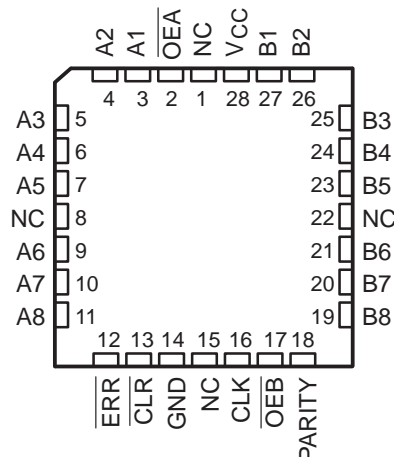
The 'ABT833 8-bit to 9-bit parity transceivers are designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error (\overline{ERR}) output indicates whether or not an error in the B data has occurred. The output-enable (\overline{OEA} and \overline{OEB}) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT833 provide true data at their outputs.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the \overline{ERR} flag. \overline{ERR} is clocked into the register on the rising edge of the clock (CLK) input. The error flag register is cleared with a low pulse on the clear (\overline{CLR}) input. When both \overline{OEA} and \overline{OEB} are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

SN54ABT833 ... JT PACKAGE
SN74ABT833 ... DW OR NT PACKAGE
(TOP VIEW)



SN54ABT833 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection



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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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description (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

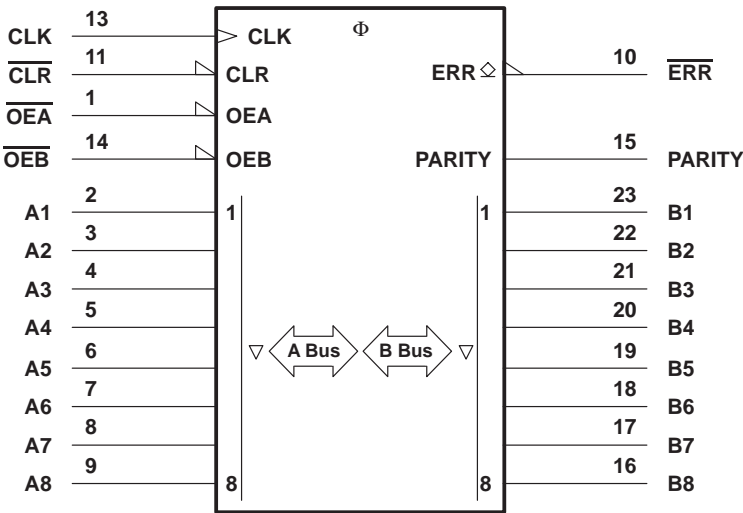
The SN54ABT833 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT833 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
\overline{OEB}	\overline{OEA}	\overline{CLR}	CLK	A_i Σ OF H's	B_i^{\dagger} Σ OF H's	A	B	PARITY	$\overline{ERR}^{\ddagger}$	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	\uparrow	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error-flag register
H	H	H	No \uparrow	X	X	Z	Z	Z	NC	Isolation §
		L	No \uparrow	X					H	
		H	\uparrow	Odd					H	
		H	\uparrow	Even					L	
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

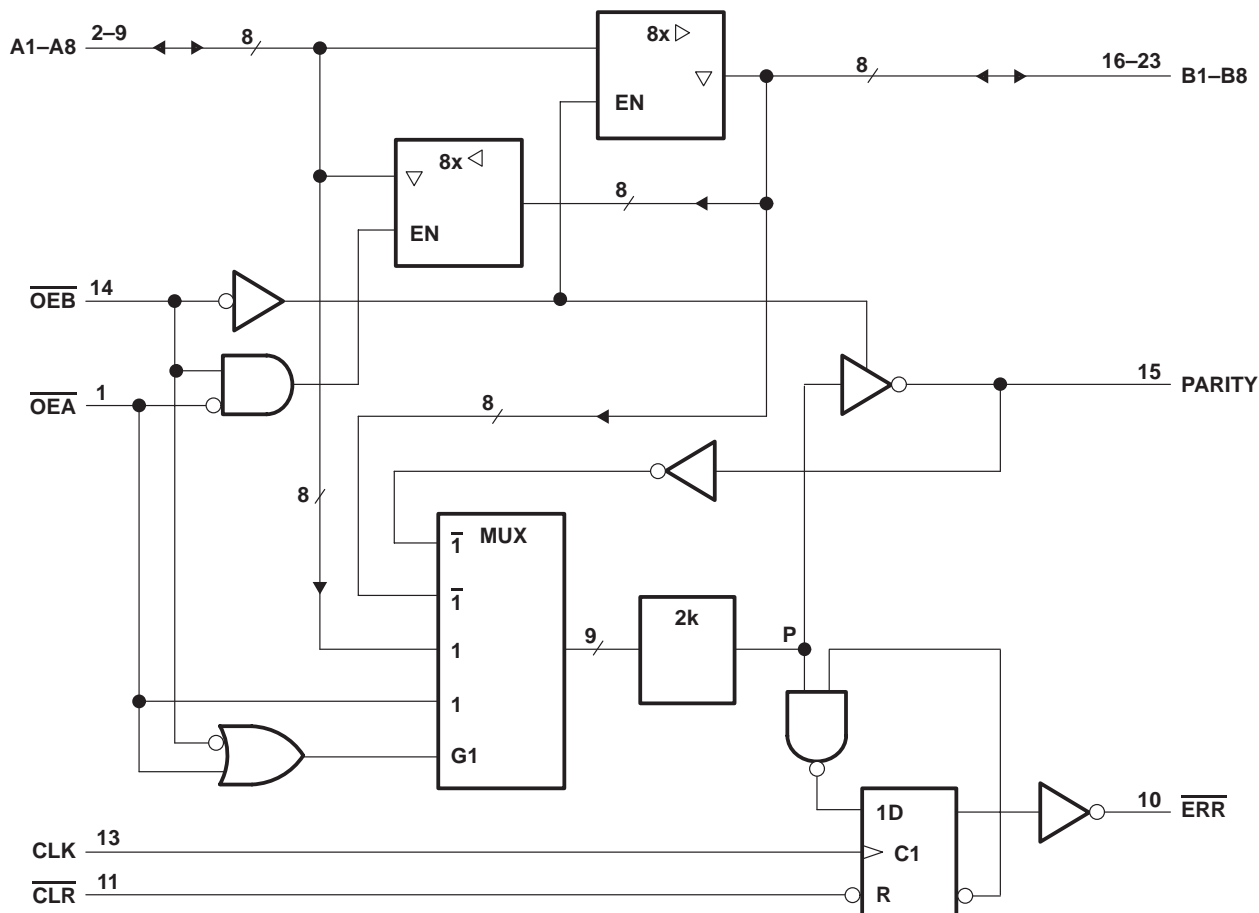
NA = not applicable, NC = no change, X = don't care
 \dagger Summation of high-level inputs includes PARITY along with B_i inputs.
 \ddagger Output states shown assume \overline{ERR} was previously high.
 \S In this mode, \overline{ERR} (when clocked) shows inverted parity of the A bus.

logic symbol ¶



¶ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT $\overline{\text{ERR}}$	FUNCTION
$\overline{\text{CLR}}$	CLK	POINT P	$\overline{\text{ERR}}_{n-1}^\dagger$		
H	\uparrow	H	H	H	Sample
H	\uparrow	X	L	L	
H	\uparrow	L	X	L	
L	X	X	X	H	Clear

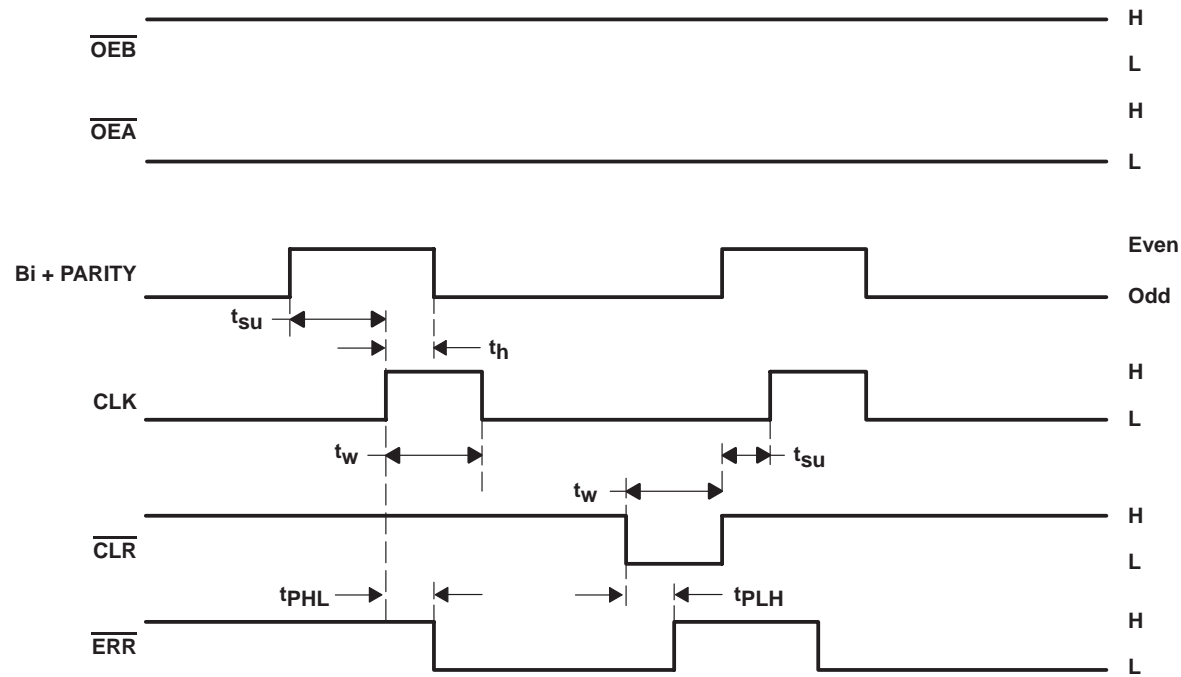
† The state of ERR before any changes at CLR, CLK, or point P

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error-flag waveforms



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT833	96 mA
SN74ABT833	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	81°C/W
NT package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions (see Note 3)

		SN54ABT833		SN74ABT833		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _{OH}	High-level output voltage	$\overline{\text{ERR}}$		5.5		V
I _{OH}	High-level output current	Except $\overline{\text{ERR}}$		–32		mA
I _{OL}	Low-level output current			64		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		ns/V
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A = 25°C			SN54ABT833		SN74ABT833		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA				-1.2		-1.2		-1.2	V
V _{OH}	All outputs except ERR	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = -3 mA		3			3		3		
		V _{CC} = 4.5 V	I _{OH} = -24 mA	2			2				
			I _{OH} = -32 mA	2*					2		
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 24 mA			0.55		0.55			V
			I _{OL} = 64 mA			0.55*				0.55	
V _{hys}					100						mV
I _{OH}	ERR	V _{CC} = 4.5 V, V _{OH} = 5.5 V				20		20		20	μA
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND				±1		±1		±1	μA
	A or B ports					±100		±100		±100	
I _{IL}	A or B ports	V _{CC} = 0, V _I = GND				-50		-50		-50	μA
I _{OZH} ‡		V _{CC} = 5.5 V, V _O = 2.7 V				50		50		50	μA
I _{OZL} ‡		V _{CC} = 5.5 V, V _O = 0.5 V				-50		-50		-50	μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V				±100				±100	μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50		50		50	μA
I _O §		V _{CC} = 5.5 V, V _O = 2.5 V		-50	-100	-200¶	-50	-200¶	-50	-200¶	mA
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		1	250		250		250	μA
			Outputs low		24	38¶		38¶		38¶	mA
			Outputs disabled		0.5	250		250		250	μA
ΔI _{CC} #	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			50		50		50	μA
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND				1.5		1.5		1.5	mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V				4.5					pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V				10.5					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ These limits may vary among suppliers.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		SN54ABT833		SN74ABT833		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLK high or low	3		3		3		ns
		$\overline{\text{CLR}}$ low	3		3		3		
t_{su}	Setup time before CLK \uparrow	B or PARITY high	9.8		9.8		9.8		ns
		B or PARITY low	8.1		8.1		8.1		
		$\overline{\text{CLR}}$	2		2		2		
t_h	Hold time after CLK \uparrow	B or PARITY	0		0		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$			SN54ABT833		SN74ABT833		UNIT
			MIN	TYP \dagger	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.2	2.8	4.8	1.2	5.4	1.2	5.3	ns
t_{PHL}			1	3	4.8 \ddagger	1	5.4	1	5.3 \ddagger	
t_{PLH}	A	PARITY	2.1	5.5	9.5	2.1	11.3	2.1	11.2	ns
t_{PHL}			2.5	5.3	9.7	2.5	11.1	2.5	11	
t_{PZH}	$\overline{\text{OE}}$	PARITY	2.6	6.2	8.5	2.6	10.6	2.6	10.5	ns
t_{PZL}			2.6 \ddagger	5.8	8.6	2.6 \ddagger	10.1	2.6 \ddagger	10	
t_{PLH}	$\overline{\text{CLR}}$	$\overline{\text{ERR}}$	1	3.2	4.8 \ddagger	1	5.3	1	5.2	ns
t_{PHL}	CLK		1.2 \ddagger	2.8	5.7	1.2 \ddagger	6.3	1.2 \ddagger	6.2	
t_{PZH}	$\overline{\text{OE}}$	A, B, or PARITY	1	3.7	5.8 \ddagger	1	6.6	1	6.5 \ddagger	ns
t_{PZL}			1.3 \ddagger	3.8	5.8	1.3 \ddagger	6.6	1.3 \ddagger	6.5 \ddagger	
t_{PHZ}	$\overline{\text{OE}}$	A, B, or PARITY	1.9 \ddagger	4.4	7.3	1.9 \ddagger	8	1.9 \ddagger	7.9	ns
t_{PLZ}			2.2 \ddagger	4.4	7.7	2.2 \ddagger	8.2	2.2 \ddagger	8.1	

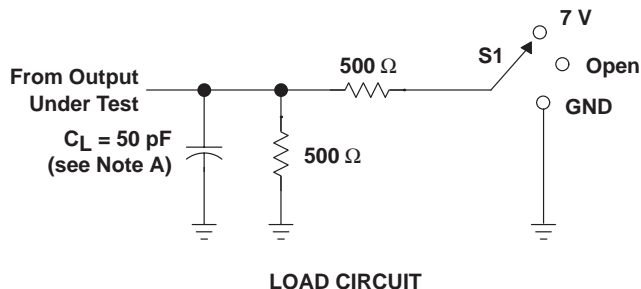
\dagger All typical values are at $V_{CC} = 5\text{ V}$.

\ddagger These limits may vary among suppliers.

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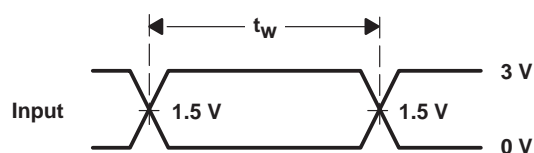
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PARAMETER MEASUREMENT INFORMATION

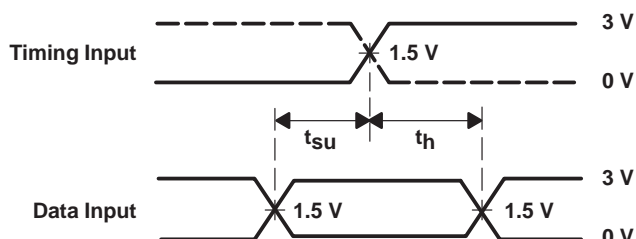


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

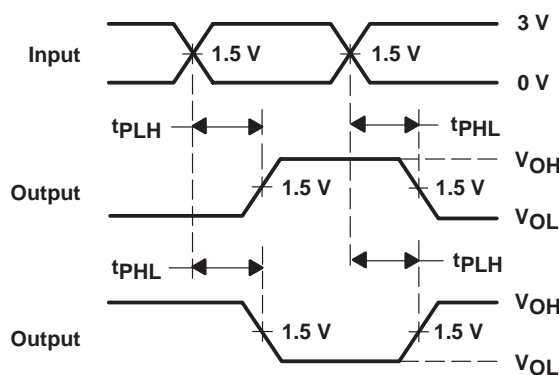
ERR	S1
t_{PHL}	7 V
t_{PLH}	7 V



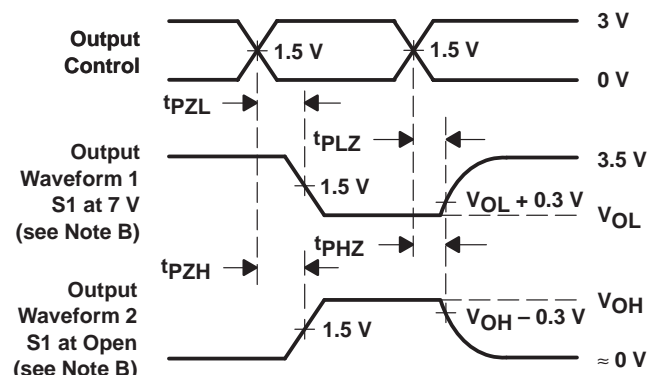
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT833DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT833	Samples
SN74ABT833DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		
SN74ABT833DWRE4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		Samples
SN74ABT833DWRG4	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		
SN74ABT833NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT833NT	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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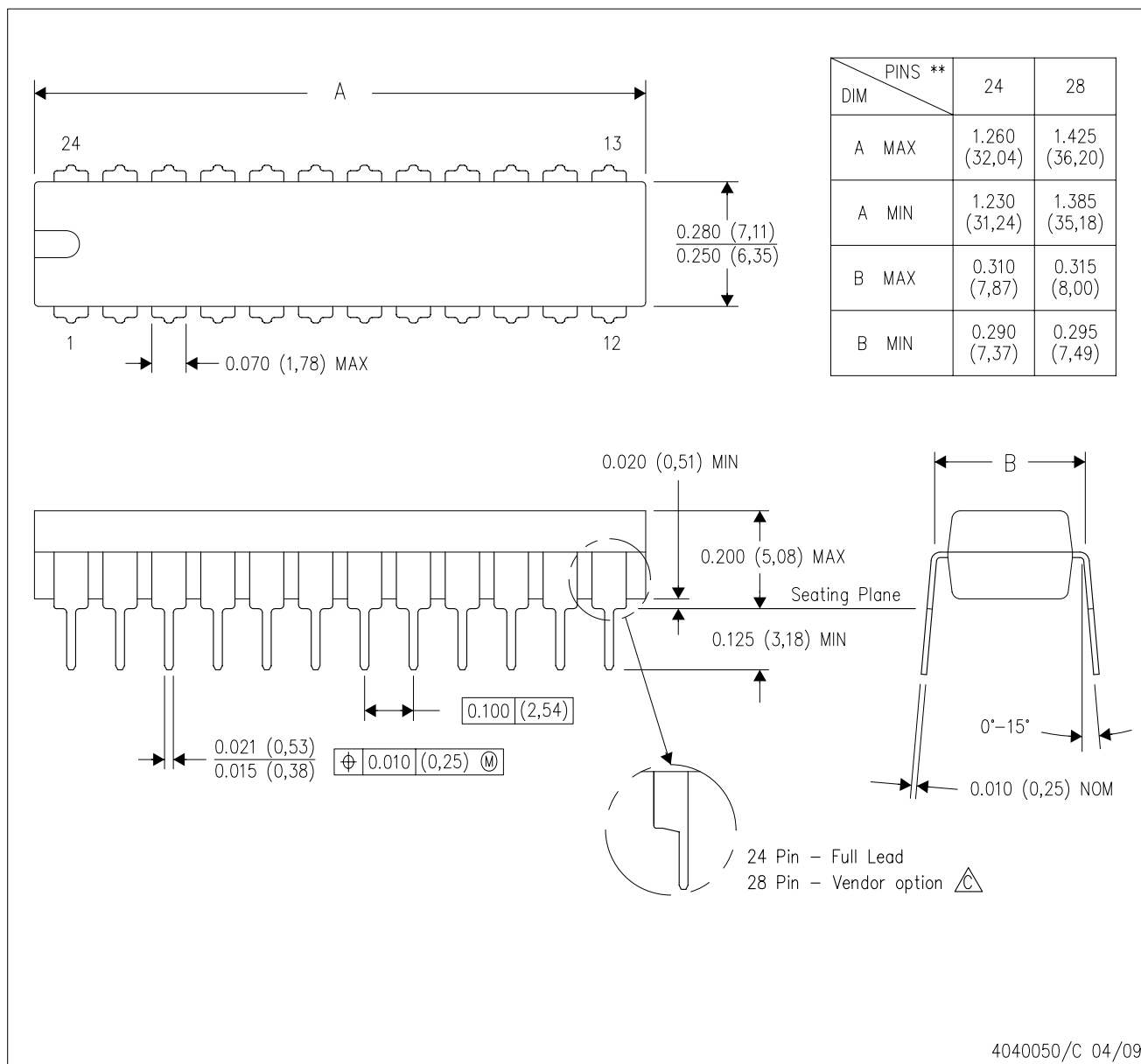
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MECHANICAL DATA

NT (R-PDIP-T**)

24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

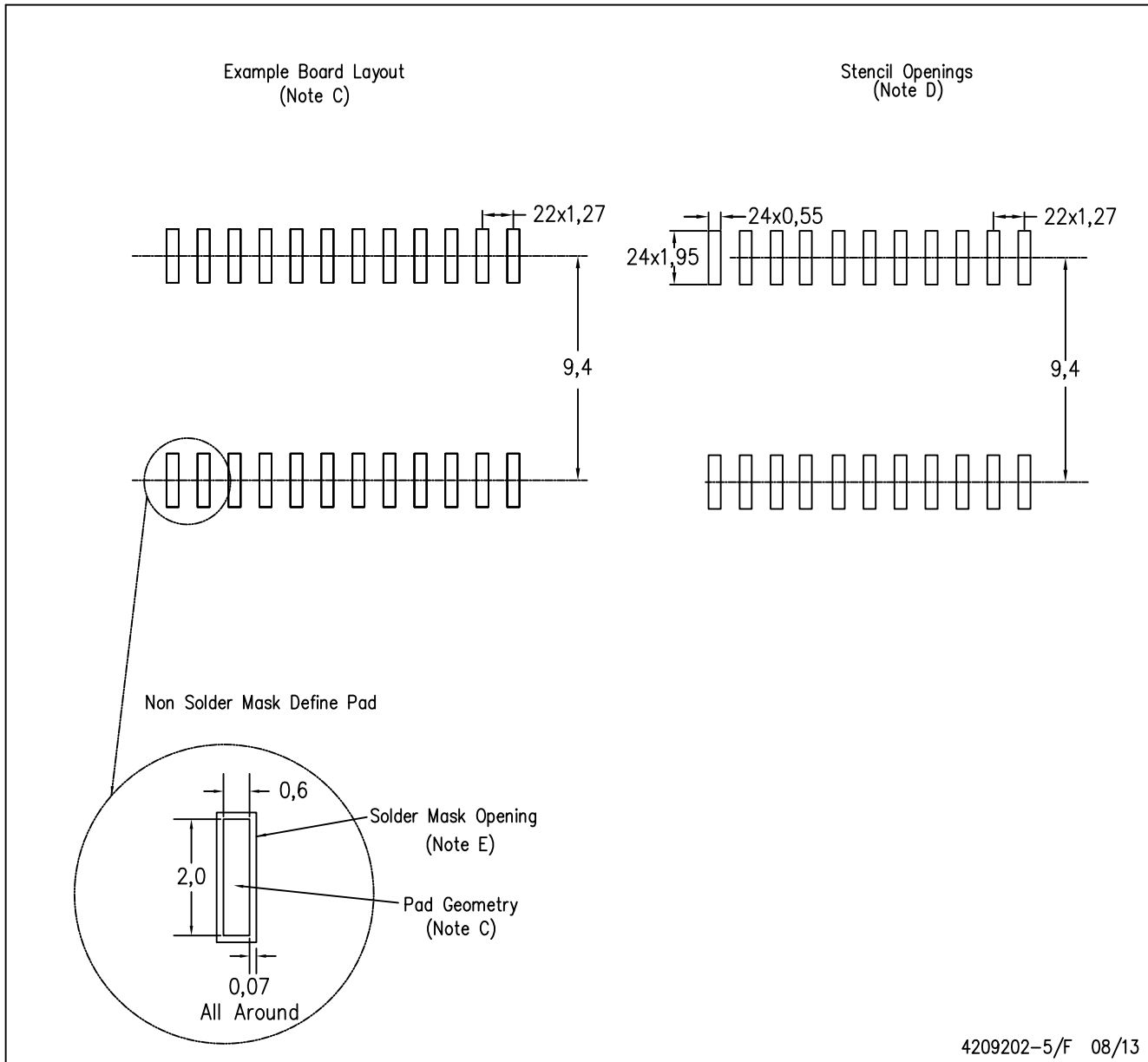
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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