# Dual Channel USB3.0 Redriver/Equalizer

Check for Samples: SN65LVPE502

## FEATURES

- **Single Lane USB 3.0 Equalizer/Redriver**
- **Selectable Equalization, De-emphasis and Output Swing Control**
- **Integrated Termination**
- **Hot-Plug Capable**
- **Receiver Detect**
- **Low Power:**
  - **315mW(TYP), $V_{CC}$ = 3.3V**
- **Auto Low Power Modes:**
  - **5mW (TYP) When no Connection Detected**
  - **70mW (TYP) When in U2/U3 Mode**

- **Excellent Jitter and Loss Compensation Capability: to 24"**
  - **24" of 6 mil Stripline on FR4**
  - **12" on Input and 4m, 26AWG USB 3.0 Cable on Output**
- **Small foot print – 24 Pin (4mm × 4mm) QFN Package**
- **High Protection Against ESD Transient**
  - **HBM: 5,000 V**
  - **CDM: 1,500 V**
  - **MM: 200 V**

## APPLICATIONS

- **Notebooks, Desktops, Docking Stations, Backplane and Cabled Application**

## DESCRIPTION

The SN65LVPE502 is a dual channel, single lane USB 3.0 redriver and signal conditioner supporting data rates of 5.0Gbps. The device complies with USB 3.0 spec revision 1.0, supporting electrical idle condition and low frequency periodic signals (LFPS) for USB 3.0 power management modes.

**Programmable EQ, De-Emphasis and Amplitude Swing**

The SN65LVPE502 is designed to minimize signal degradation effects such as crosstalk and inter-symbol interference (ISI) that limits the interconnect distance between two devices. The input stage of each channel offers selectable equalization settings that can be programmed to match loss in the channel. The differential outputs provide selectable de-emphasis to compensate for the anticipated distortion USB 3.0 signal will experience. Level of de-emphasis will depend on the length of interconnect and its characteristics. The SN65LVPE502 provides a unique way to tailor output de-emphasis on a per channel basis with use of DE and OS pins. All Rx and Tx equalization settings supported by the device are programmed by six 3-state pins as shown in Table 2.

**Low Power Modes**

The device supports three low power modes as described below.

1. Sleep Mode

   Initiated anytime EN_RXD undergoes a high to low transition or when device powers up with EN_RXD set low. In sleep mode both input and output terminations are held at HiZ and device ceases operation to conserve power. Sleep mode max power consumption is 1mW, entry time is 2μs, device exits sleep mode to Rx.Detect mode after EN_RXD is driven to $V_{CC}$, exit time is 100μs max.

2. RX Detect Mode – When no remote device is connected

   Anytime SN65LVPE502 detects a break in link (i.e., when upstream device is disconnected) or after powerup fails to find a remote device, SN65LVPE502 goes to Rx Detect mode and conserves power by shutting down majority of the internal circuitry. In this mode, input termination for both channels are driven to Hi-Z. In Rx Detect mode device power is <10mW(TYP) or less than 5% of its normal operating power This feature is useful in saving system power in mobile applications like notebook PC where battery life is critical.

   Anytime an upstream device gets reconnected the redriver automatically senses the connection and goes to normal operating mode. This operation requires no setting to the device.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

3. U2/U3 Mode

With the help of internal timers the device tracks when link enters USB 3.0 low power modes U2 and U3, in these modes link is in electrical idle state. SN65LVPE502 will selectively turn-off internal circuitry to save on power. Typical power saving is about 75% lower than normal operating mode. The device will automatically revert to active mode when signaling activity (LFPS) is detected.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION CONTINUED

### Receiver Detection
RX.Detect cycle is performed by first setting Rx termination for each channel to Hi-Z, device then starts sensing for receiver termination that may be attached at the other end of each TX.

If receiver is detected on both channel:

- The TX and RX terminations are switched to $Z_{DIFF-TX}$, $Z_{DIFF-RX}$, respectively

If no receiver is detected on one or both channels:

- The transmitter is pulled to Hi-Z
- The channel is put in low power mode
- Device attempts to detect Rx termination in 12 ms (TYP) interval until termination is found or the device is put in sleep mode.

### USB Compliance Mode
The device enters USB compliance mode when both EN_RXD and CM pins are set H. This mode is used to test the transmitter for compliance to voltage and timing specifications per USB 3.0 compliance specs. In this mode each channel will maintain its low-impedance termination $R_{DC-RX}$, while auto Rx detect operation in the device is disabled.

### Electrical Idle Support
The electrical idle support is needed for low frequency periodic signaling (LFPS) used in USB 3.0 side band communication. A link is in an electrical idle state when the TX± voltage is held at a steady constant value like the common mode voltage. SN65LVPE502 detects an electrical idle state when RX± voltage at the device pin falls below $V_{RX\_IDLE\_DIFFpp}$ min. After detection of an idle state in a given channel the device asserts electrical idle state in its corresponding TX. When RX± voltage exceeds $V_{RX\_IDLE\_DIFFpp}$ max normal operation is restored and output start passing input signal. The electrical idle exit and entry time is specified at ≤6 ns.
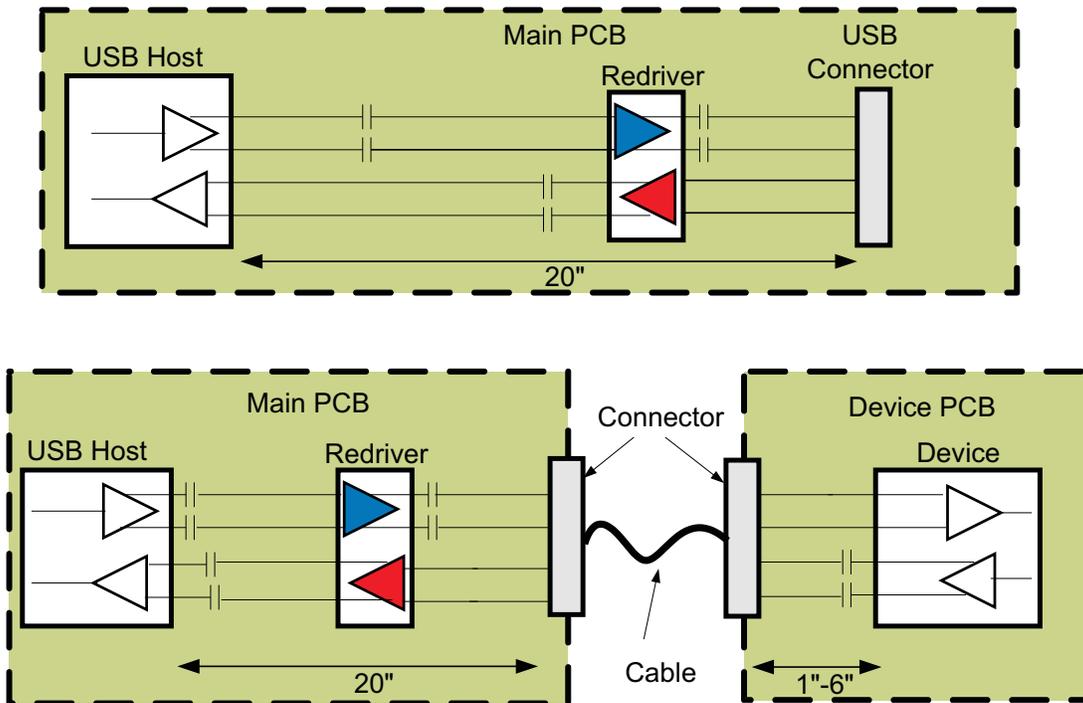
**Figure 1. Typical Application**
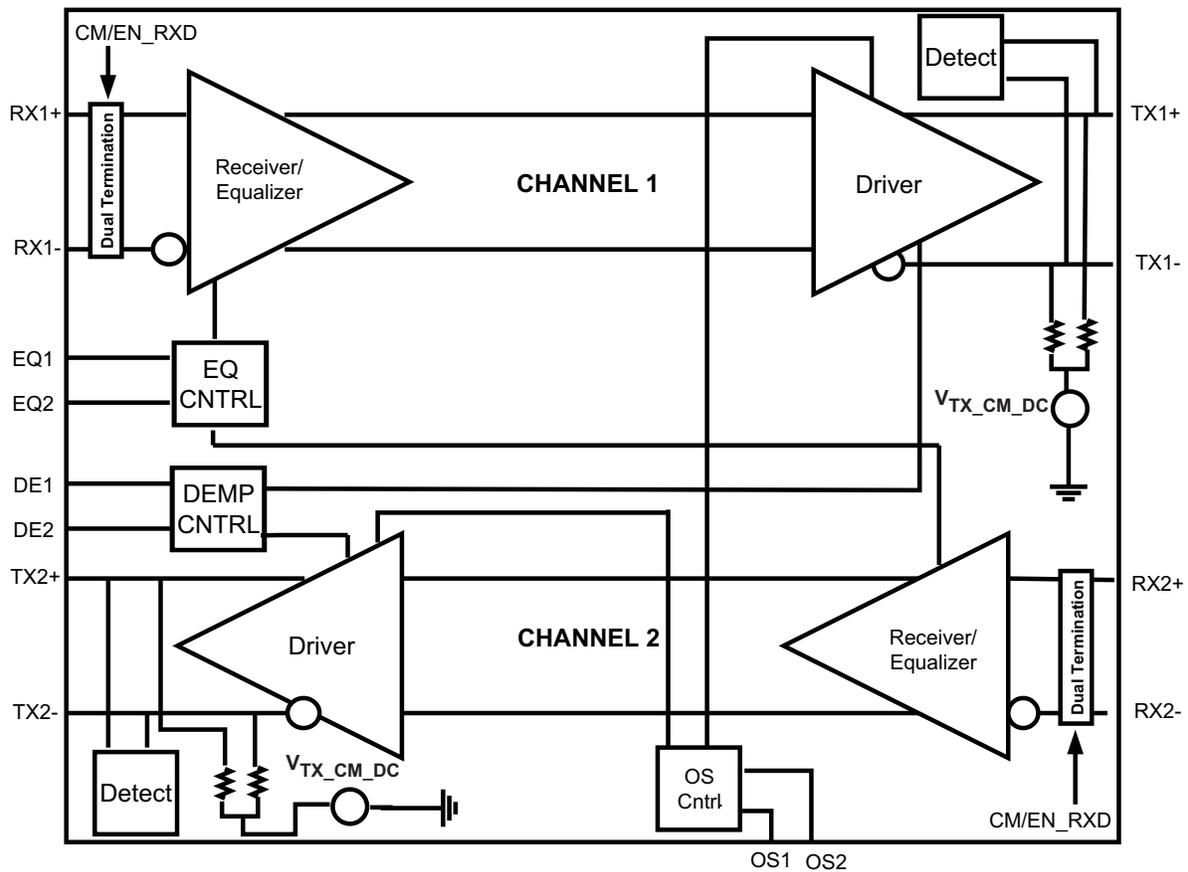


**Figure 2. Data FLow Block Diagram**

**BOTTOM VIEW**



**TOP VIEW**
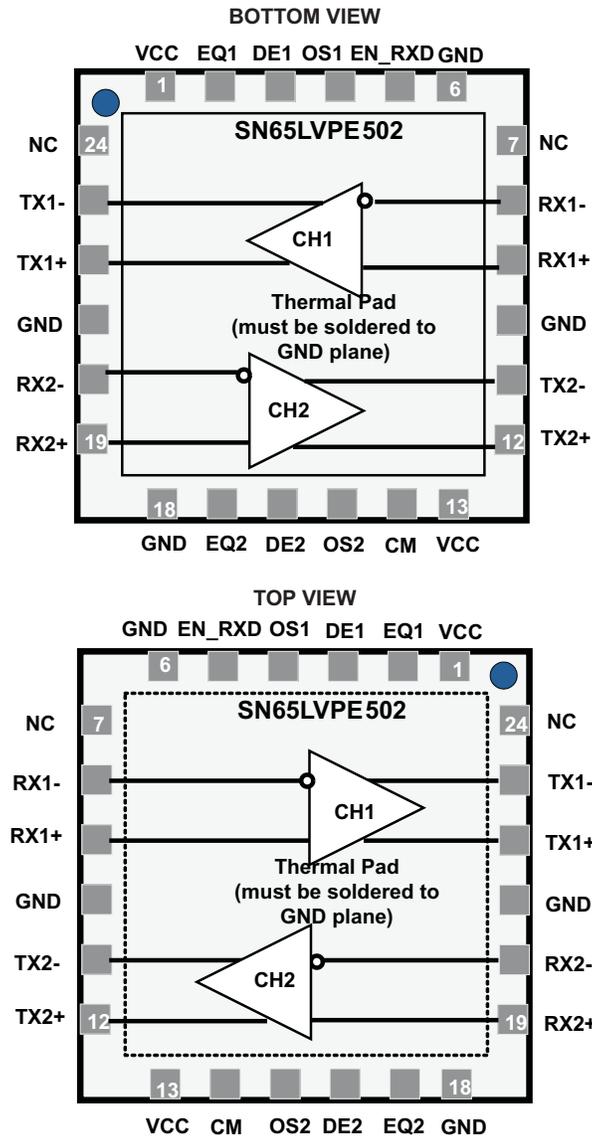


**Figure 3. Flow-Through Pin-Out**

**Table 1. Pin Description**

| PIN | | | |
|---|---|---|---|
| NUMBER | NAME | I/O TYPE | DESCRIPTION |
| **HIGH SPEED DIFFERENTIAL I/O PINS** | | | |
| 8 | RX1– | I, CML | Non-inverting and inverting CML differential input for CH 1 and CH 2. These pins are tied to an internal voltage bias by dual termination resistor circuit |
| 9 | RX1+ | I, CML | |
| 20 | RX2– | I, CML | |
| 19 | RX2+ | I, CML | |
| 23 | TX1– | O, VML | Non-inverting and inverting VML differential output for CH 1 and CH 2. These pins are internally tied to voltage bias by termination resistors |
| 22 | TX1+ | O, VML | |
| 11 | TX2– | O, VML | |
| 12 | TX2+ | O, VML | |

Product Folder Link(s): *SN65LVPE502*

## Table 1. Pin Description (continued)

| PIN | | | |
|---|---|---|---|
| **DEVICE CONTROL PIN** | | | |
| 5 | EN_RXD | I, LVCMOS | Sets device operation modes per Table 2. Internally pulled to VCC |
| 14 | CM | I, LVCMOS | Sets device in compliance mode when pulled to VCC, internally pulled to GND |
| 7,24 | NC | | Pads not internally connected |
| **EQ CONTROL PINS[1]** | | | |
| 3,16 | DE1, DE2 | I, LVCMOS | Selects de-emphasis settings for CH 1 and CH 2 per Table 2. Internally tied to $V_{CC}/2$ |
| 2,17 | EQ1, EQ2 | I, LVCMOS | Selects equalization settings for CH 1 and CH 2 per Table 2. Internally tied to $V_{CC}/2$ |
| 4, 15 | OS1, OS2 | I, LVCMOS | Selects output amplitude for CH 1 and CH 2 per Table 2. Internally tied to $V_{CC}/2$ |
| **POWER PINS** | | | |
| 1,13 | VCC | Power | Positive supply should be 3.3V ± 10% |
| 6,10,18,21 | GND | Power | Supply ground |

(1)   Internally biased to $V_{CC}/2$ with >200kΩ pull-up/pull-down. When pins are left as NC board leakage at this pin pad must be < 1 μA otherwise drive to $V_{CC}/2$ to assert mid-level state.

## Table 2. Signal Control Pin Setting

| OSx[1] | *TRANSITION* BIT AMPLITUDE (TYP mVpp) | | |
|---|---|---|---|
| NC (default) | 1000 | | |
| 0 | 870 | | |
| 1 | 1085 | | |
| **EQx[1]** | **EQUALIZATION dB** | | |
| NC (default) | 0 | | |
| 0 | 7 | | |
| 1 | 15 | | |
| **DEx[1]** | **OSx[1] = NC** | **OSx[1] = 0** | **OSx[1] = 1** |
| NC | −3.5 dB | −2.2 dB | −4.4 dB |
| 0 | −6.0 dB | −5.2 dB | −6.0 dB |
| 1 | −8.5 dB | −8.9 dB | −7.6 dB |
| **EN_RXD** | **DEVICE FUNCTION** | | |
| 1 (default) | Normal operating mode | | |
| 0 | Sleep mode | | |
| **CM** | **DEVICE FUNCTION** | | |
| 0 (default) | Normal Mode | | |
| 1 | Compliance mode | | |

(1)   Applies to Channel 1 and Channel 2 at 2.5 GHz.
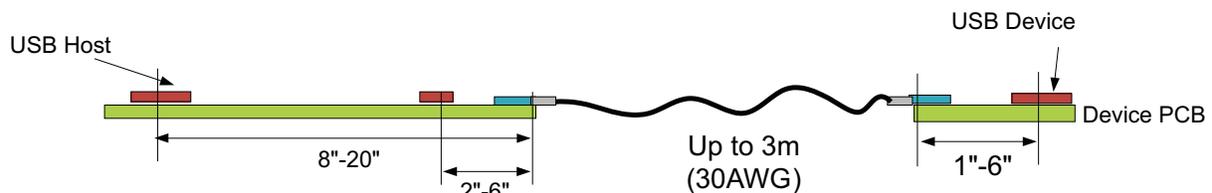


**Figure 4.  Redriver Placement Example**

## ORDERING INFORMATION[1]

| PART NUMBER | PART MARKING | PCAKAGE |
|---|---|---|
| SN65LVPE502RGER | LVPE502 | 24-pin RGE Reel (large) |
| SN65LVPE502RGET | LVPE502 | 24-pin RGE Reel (small) |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

|  |  | UNITS / VALUES |
|---|---|---|
| Supply Voltage Range[2] | $V_{CC}$ | –0.5 V to 4 V |
| Voltage Range | Differential I/O | –0.5 V to 4 V |
|  | Control I/O | –0.5 V to $V_{CC}$ + 0.5V |
| Electrostatic discharge | Human Body Model[3] | ±5000V |
|  | Charged Device Model[4] | ±1500V |
|  | Machine Model[5] | ±200V |
| Continuous power dissipation |  | See Dissipation Rating Table |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A.
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

## PACKAGE CHARACTERIZATION

over operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_D$ | Device power dissipation | CM, EN_RXD, EQ cntrl pins = NC, K28.5 pattern at 5 Gbps, $V_{ID}$ = 1000 mVpp | | 330 | 450 | mW |
| $P_{SD}$ | Device power dissipation under low power mode | EN_RXD= GND | | 0.3 | 1 | mW |

## THERMAL INFORMATION

| | THERMAL METRIC[1] | SN65LVPE502 RGE 24 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 46 | °C/W |
| $\theta_{JC(TOP)}$ | Junction-to-case(top) thermal resistance | 42 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 13 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.5 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 9 | |
| $\theta_{JC(BOTTOM)}$ | Junction-to-case(bottom) thermal resistance | 4 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3 | 3.3 | 3.6 | V |
| $C_{COUPLING}$ | AC Coupling Capacitor | 75 |  | 200 | nF |
|  | Operating free-air temperature | 0 |  | 85 | °C |

## DEVICE POWER

The SN65LVPE502 is designed to operate from a single 3.3 V supply.

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DEVICE PARAMETERS** | | | | | | |
| $I_{CC}$ | | EN_RXD, CM, EQ cntrl = NC, K28.5 pattern at 5 Gbps, $V_{ID}$ = 1000 mV$_{pp}$ | | 100 | 120 | mA |
| $ICC_{Rx.Detect}$ | Supply Current | In Rx.Detect mode | | 2 | 5 | |
| $ICC_{sleep}$ | | EN_RXD = GND | | | 0.1 | |
| $ICC_{U2-U3}$ | | Link in USB low power state | | 21 | | |
| | Maximum Data Rate | | | | 5 | Gbps |
| $t_{ENB}$ | Device Enable Time | Sleep mode exit time EN_RXD L→ H With Rx termination present | | | 100 | µs |
| $t_{DIS}$ | Device Disable Time | Sleep mode entry time EN_RXD H→ L | | | 2 | µs |
| $T_{RX.DETECT}$ | Rx.Detect Start Event | Power-up time | | | 100 | µs |
| **CONTROL LOGIC (under recommended operating conditions)** | | | | | | |
| $V_{IH}$ | High level Input Voltage | | 1.4 | | $V_{CC}$ | V |
| $V_{IL}$ | Low Level Input Voltage | | –0.3 | | 0.5 | V |
| $V_{HYS}$ | Input Hysteresis | | | 150 | | mV |
| $I_{IH}$ | High Level Input Current | OSx, EQx, DEx = $V_{CC}$ | | | 30 | µA |
| | | EN_RXD = $V_{CC}$ | | | 1 | |
| | | CM = $V_{CC}$ | | | 30 | |
| $I_{IL}$ | Low Level Input Current | OSx, EQx, DEx = GND | –30 | | | µA |
| | | EN_RXD = GND | –30 | | | |
| | | CM = GND | –1 | | | |
| **RECEIVER AC/DC** | | | | | | |
| Vin$_{diff\_pp}$ | RX1, RX2 Input Voltage Swing | AC coupled differential RX peak to peak signal | 100 | | 1200 | mVpp |
| $V_{CM\_RX}$ | RX1, RX2 Common Mode Voltage | | | 3.3 | | V |
| Vin$_{COM\_P}$ | RX1, RX2 AC Peak common mode voltage | Measured at Rx pins with termination enabled | | | 150 | mVP |
| $Z_{DC\_RX}$ | DC common mode impedance | | 18 | 26 | 30 | Ω |
| $Z_{diff\_RX}$ | DC differential input impedance | | 72 | 80 | 120 | Ω |
| $Z_{RX\_High\_IMP+}$ | DC Input High Impedance | Device in sleep mode Rx termination not powered. Measured with respect to GND over 500mV max | 50 | 85 | | kΩ |
| $V_{RX-LFPS-DETpp}$ | Low Voltage Periodic Signaling (LFPS) Detect Threshold | Measured at receiver pin, below minimum output is squelched, above max input signal is passed to output | 100 | | 300 | mVpp |
| $RL_{RX-DIFF}$ | Differential Return Loss | 50 MHz – 1.25 GHz | 10 | 11 | | dB |
| | | 1.25 GHz – 2.5 GHz | 6 | 7 | | |
| $RL_{RX-CM}$ | Common Mode Return Loss | 50 MHz – 2.5 GHz | 11 | 13 | | dB |

## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **TRANSMITTER AC/DC** | | | | | | | |
| $V_{TXDIFF\_TB\_PP}$ | Differential peak-to-peak Output Voltage (VID = 800, 1200 mVpp, 5Gbps) | $R_L$ =100Ω +1%, DEx, OSx = NC, **Transition Bit** | | 800 | 1000 | 1200 | mV |
| | | $R_L$ =100Ω +1%, DEx, OSx = GND **Transition Bit** | | | 870 | | |
| | | $R_L$ =100Ω +1%, DEx, OSx = VCC **Transition Bit** | | | 1085 | | |
| $V_{TXDIFF\_NTB\_PP}$ | | $R_L$ =100Ω +1%, DEx=NC, OSx = 0,1,NC **Non-Transition Bit** | | | 665 | | |
| | | $R_L$ =100Ω +1%, DEx=0, OSx = 0,1,NC **Non-Transition Bit** | | | 510 | | |
| | | $R_L$ =100Ω +1%, DEx=1 OSx = 0,1,NC **Non-Transition Bit** | | | 375 | | |
| | De-Emphasis Level | OS1,2 = NC (for OS1,2 = 1 and 0 see Table 2) | | −3.0 | −3.5 | −4.0 | dB |
| | | | | | −6.0 | | |
| | | | | | −8.5 | | |
| $T_{DE}$ | De-Emphasis Width | | | | 0.85 | | UI |
| $Z_{diff\_TX}$ | DC Differential Impedance | | | 72 | 90 | 120 | Ω |
| $Z_{CM\_TX}$ | DC Common Mode Impedance | Measured w.r.t to AC ground over 0-500mV | | 18 | 23 | 30 | Ω |
| $RL_{diff\_TX}$ | Differential Return Loss | f = 50 MHz – 1.25 GHz | | 9 | 10 | | dB |
| | | f = 1.25 GHz – 2.5 GHz | | 6 | 7 | | |
| $RL_{CM\_TX}$ | Common Mode Return Loss | f = 50 MHz – 2.5 GHz | | 11 | 12 | | dB |
| $I_{TX\_SC}$ | TX short circuit current | TX± shorted to GND | | | | 60 | mA |
| $V_{TX\_CM\_DC}$ | Transmitter DC common-mode voltage | | | 2.0 | 2.6 | 3.0 | V |
| $V_{TX\_CM\_AC\_Active}$ | TX AC common mode voltage active | | | | 30 | 100 | mVpp |
| $V_{TX\_idle\_diff-AC-pp}$ | Electrical idle differential peak to peak output voltage | HPF to remove DC | | 0 | | 10 | mV |
| $V_{TX\_CM\_DeltaU1-U0}$ | Absolute delta of DC CM voltage during active and idle states | | | | 35 | 200 | mV |
| $V_{TX\_idle\_diff-DC}$ | DC Electrical idle differential output voltage | Voltage must be low pass filtered to remove any AC component | | 0 | | 10 | mV |
| $V_{detect}$ | Voltage change to allow receiver detect | Positive voltage to sense receiver termination | | | | 600 | mV |
| $t_R, t_F$ | Output Rise/Fall time | 20%-80% of differential voltage measure 1" from the output pin | | 30 | 50 | | ps |
| $t_{RF\_MM}$ | Output Rise/Fall time mismatch | | | | | 20 | ps |
| $T_{diff\_LH}, T_{diff\_HL}$ | Differential Propagation Delay | De-Emphasis = −3.5dB (CH 0 and CH 1). Propagation delay between 50% level at input and output See Figure 5 | | | 290 | 350 | ps |
| $t_{idleEntry} t_{idleExit}$ | Idle entry and exit times | See Figure 6 | | | 4 | 6 | ns |
| $C_{TX}$ | Tx input capacitance to GND | At 2.5 GHz | | | 1.25 | | pF |
| **EQUALIZATION** | | | | | | | |
| $T_{TX-EYE}$ [1] [2] | **Total Jitter (Tj) at point A** | Device setting: OS1 = L, DE1 = H, EQ1 = L | | | 0.14 | 0.5 | UIpp [3] |
| $DJ_{TX}$ [2] | Deterministic Jitter (Dj) | | | | 0.06 | 0.3 | |
| $RJ_{TX}$ [2] [4] | Random Jitter (Rj) | | | | 0.08 | 0.2 | |
| $T_{TX-EYE}$ [1] [2] | **Total Jitter (Tj) at point B** | Device setting: OS2 = H, DE2 = H, EQ2 = L | | | 0.14 | 0.5 | UIpp [3] |
| $DJ_{TX}$ [2] | Deterministic Jitter (Dj) | | | | 0.06 | 0.3 | |
| $RJ_{TX}$ [2] [4] | Random Jitter (Rj) | | | | 0.08 | 0.2 | |

(1) Includes Rj at $10^{-12}$
(2) Measured at the end of reference channel in Figure 8 with K28.5 pattern, $V_{ID}$=1000mVpp, 5Gbps, −3.5dB DE from source.
(3) UI = 200ps
(4) Rj calculated as 14.069 times the RMS random jitter for $10^{-12}$ BER

Product Folder Link(s): *SN65LVPE502*
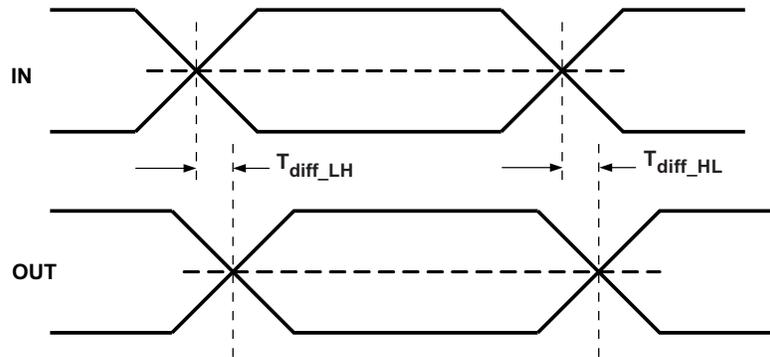
**Figure 5. Propagation Delay**
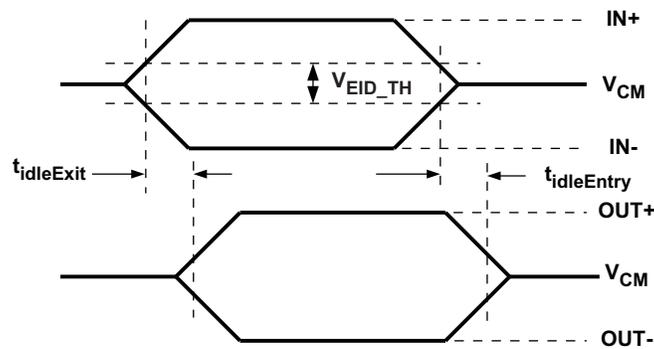
**Figure 6. Electrical Idle Mode Exit and Entry Delay**
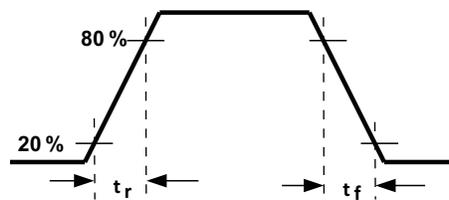
**Figure 7. Output RIse and Fall Times**

| *Source Jitter Measurements | (ps) |
| --- | --- |
| Total Jitter | 21pp |
| Deterministic Jitter | 8pp |
| Random Jitter | 0.95 rms |
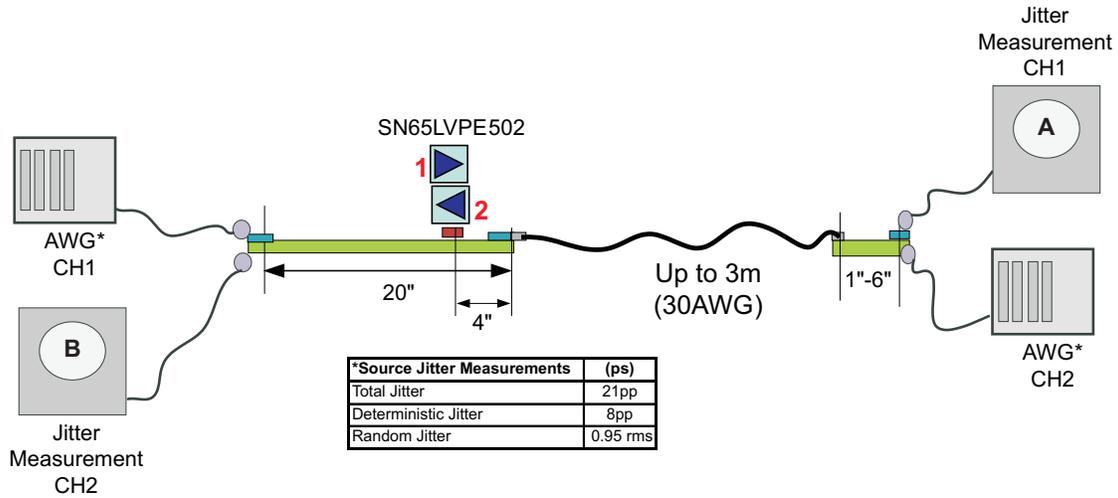
**Figure 8. Jitter Measurement Setup**
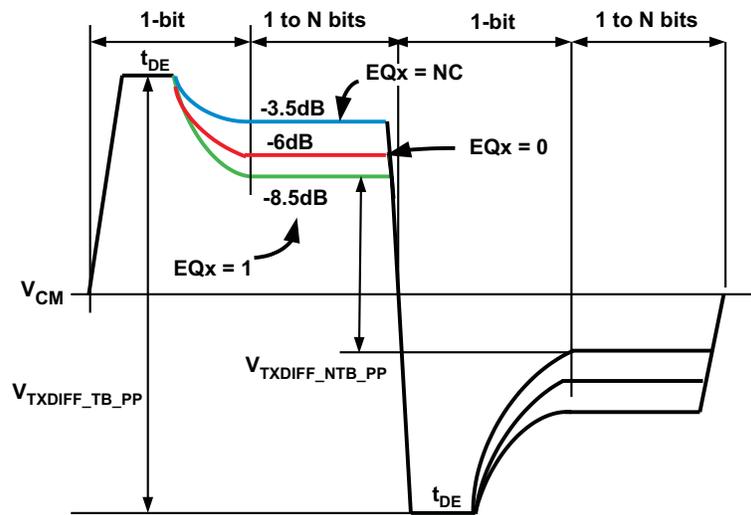


**Figure 9. Output De-Emphasis Levels OSx = NC**

## Typical Eye Diagram and Performance Curves

Input Signal Characteristics: Data Rate = 5 Gbps, $V_{ID}$ = 1000 mVpp, DE = -3.5 dB, Pattern = K28.5 Device Operating Conditions: VCC = 3.3 V, Temp = 25°C

## Input Trace Length Held Constant and Output Cable Length Varied
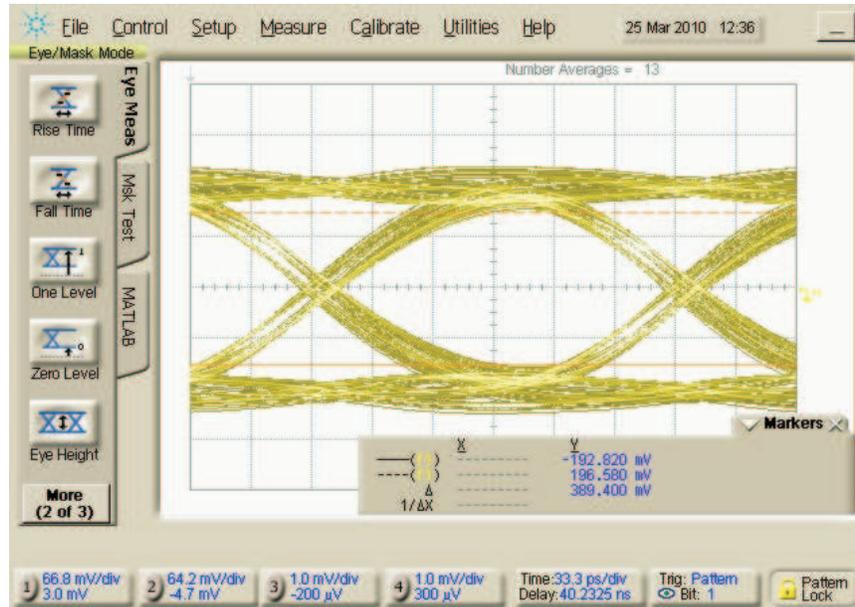


**Figure 10. Input Trace = 12 Inches, 6 mil and Output USB 3 Cable Length = 1 M**
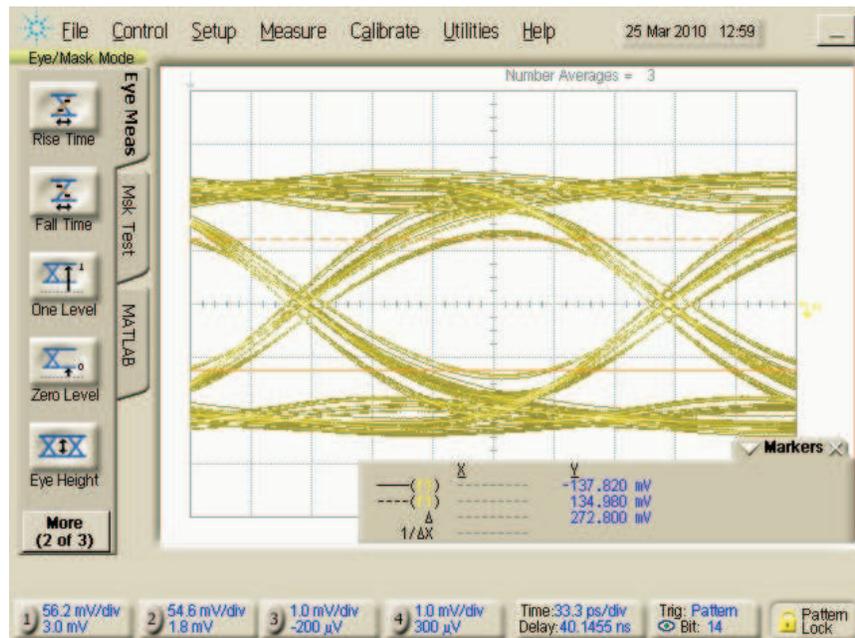


**Figure 11. Input Trace = 12 Inches, 6 mil and Output USB 3 Cable Length = 2 M**

Product Folder Link(s): *SN65LVPE502*
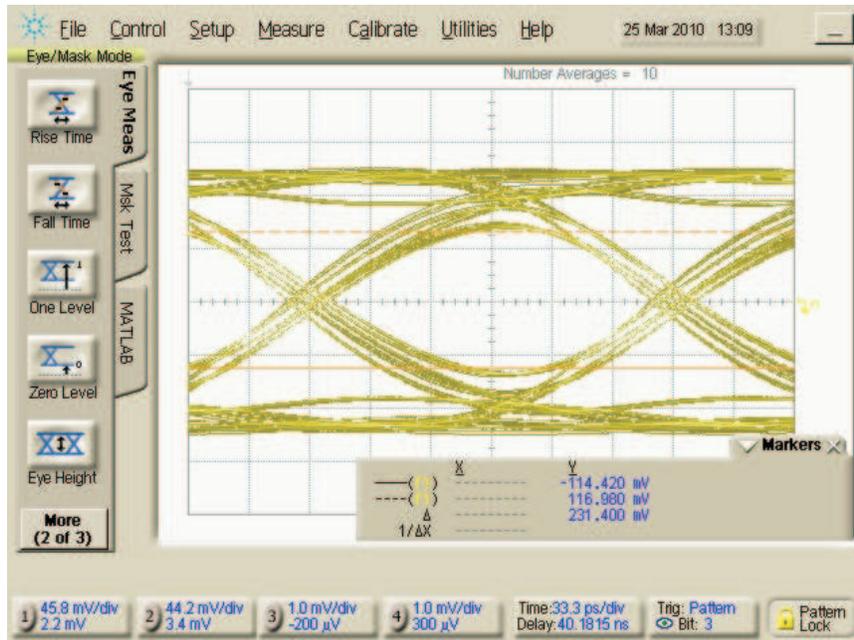
**Figure 12.  Input Trace = 12 Inches, 6 mil and Output USB 3 Cable Length = 3 M**
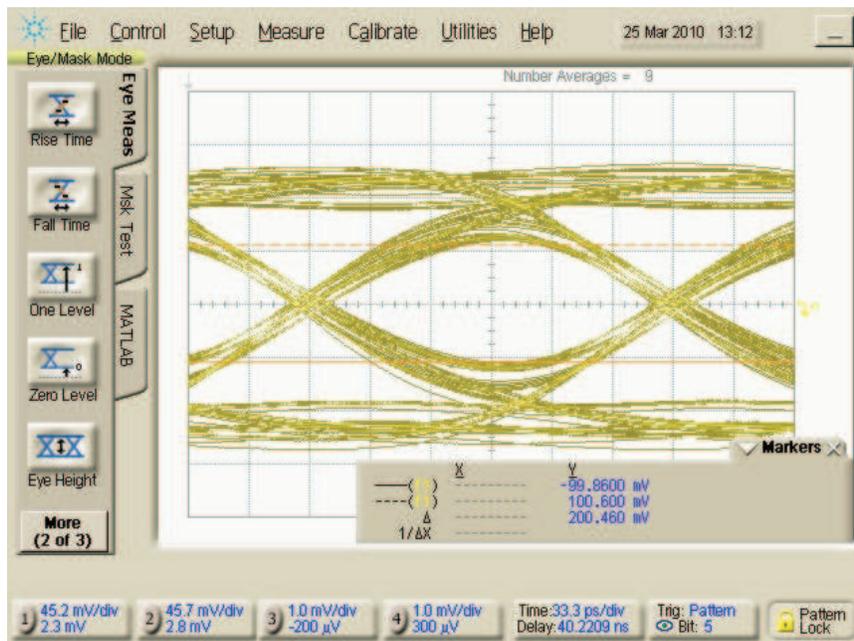


**Figure 13.  Input Trace = 12 Inches, 6 mil and Output USB 3 Cable Length = 4 M**
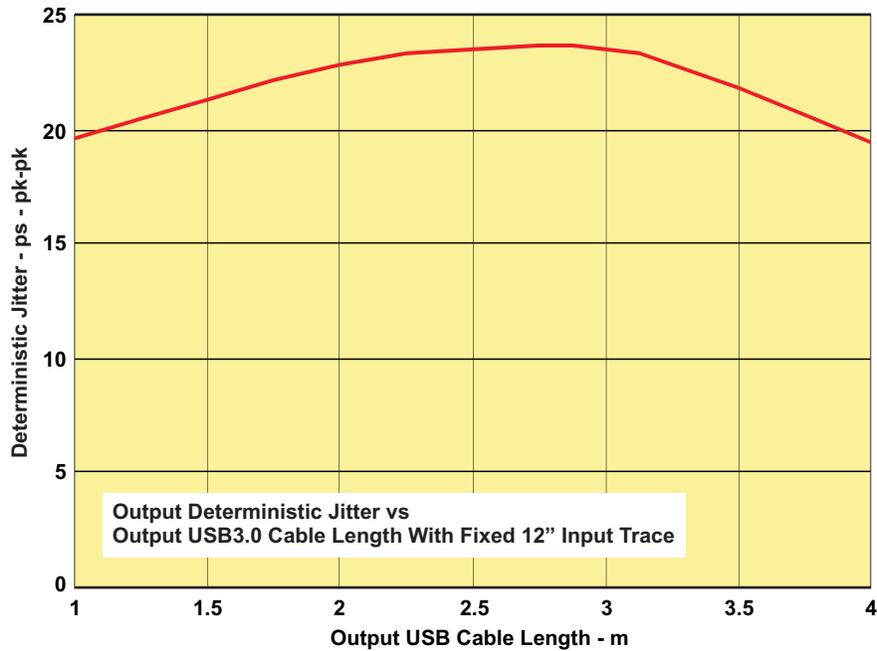
**Figure 14. Jitter Performance Over Different Cable Lengths**

## Input Trace Length Held Constant and Output Trace Varied
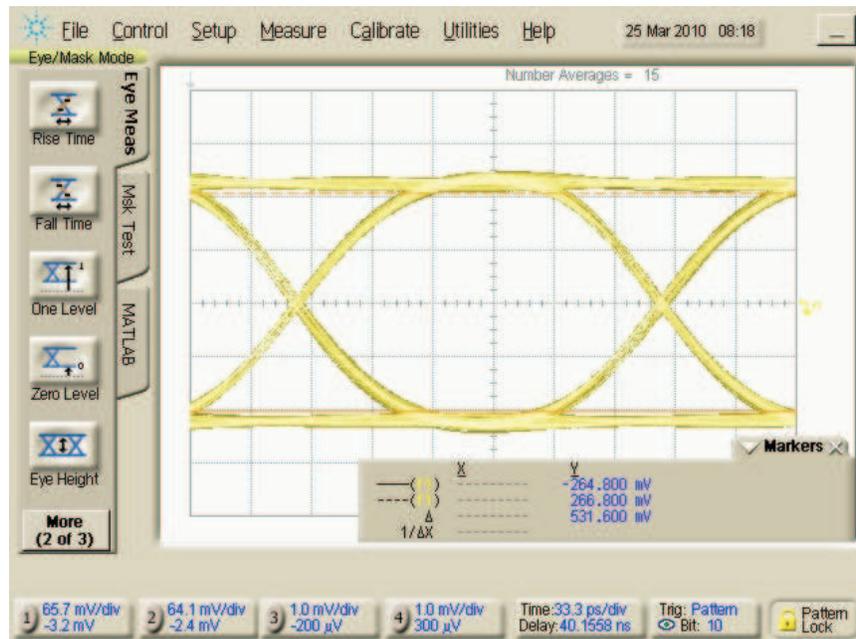


**Figure 15. Input Trace = 4 Inches, 6 mil and Output Trace = 4 Inches, 6 mil**

Product Folder Link(s): SN65LVPE502
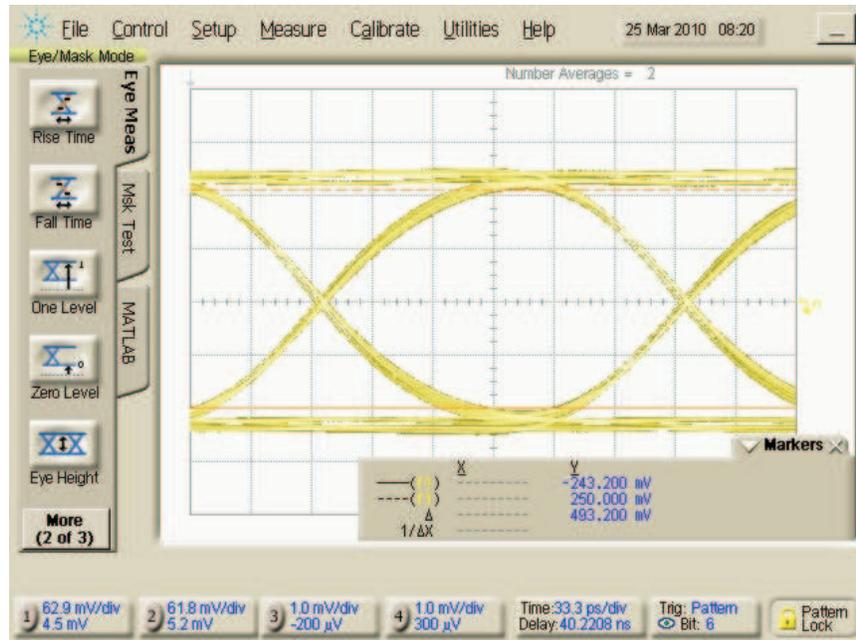
**Figure 16. Input Trace = 4 Inches, 6 mil and Output Trace = 8 Inches, 6 mil**
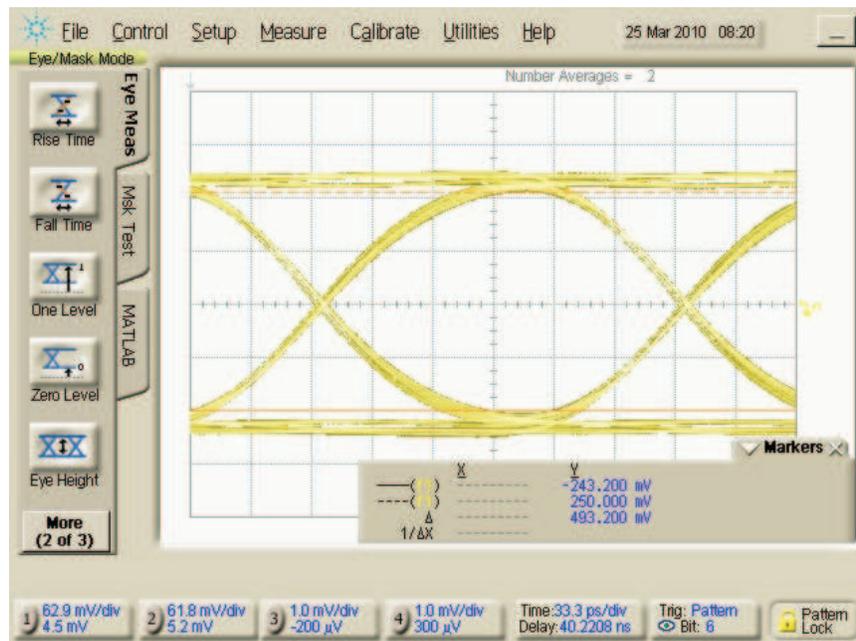


**Figure 17. Input Trace = 4 Inches, 6 mil and Output Trace = 12 Inches, 6 mil**
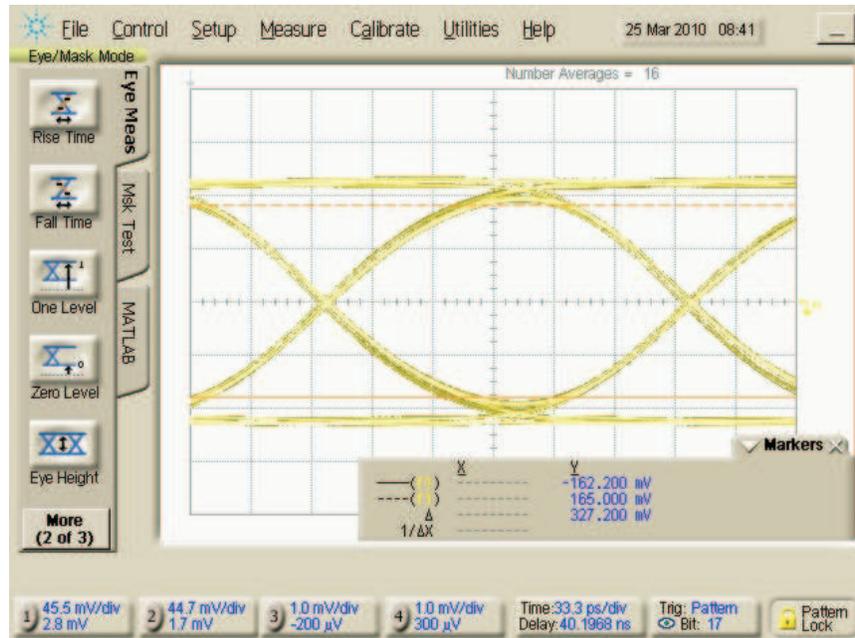
**Figure 18.  Input Trace = 4 Inches, 6 mil and Output Trace = 16 Inches, 6 mil**
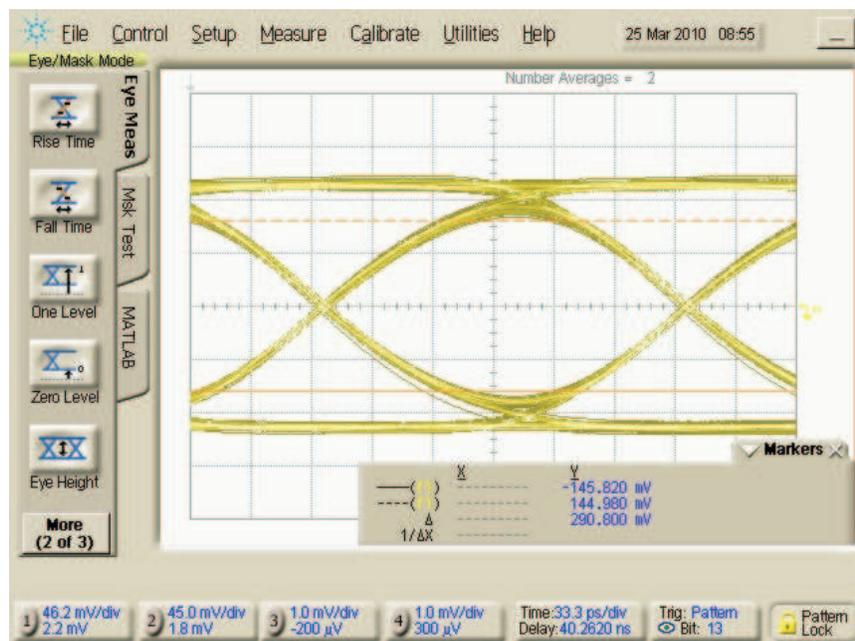


**Figure 19.  Input Trace = 4 Inches, 6 mil and Output Trace = 20 Inches, 6 mil**

**Figure 20. Jitter Performance Over Different Output Trace Lengths**

## Output Trace Length Held Constant and Input Trace Length Varied
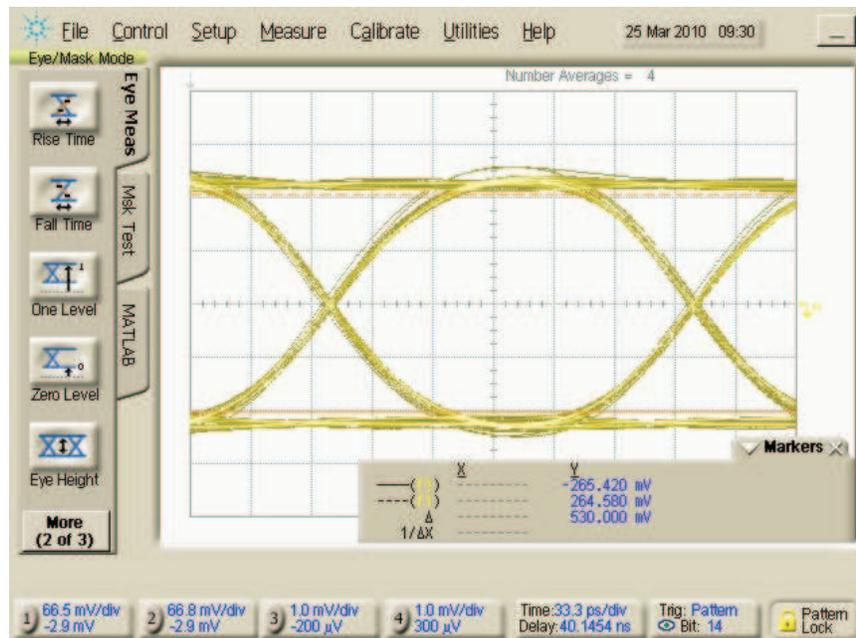


**Figure 21. Input Trace = 4 Inches, 6 mil and Output Trace = 4 Inches, 6 mil**

Product Folder Link(s): *SN65LVPE502*
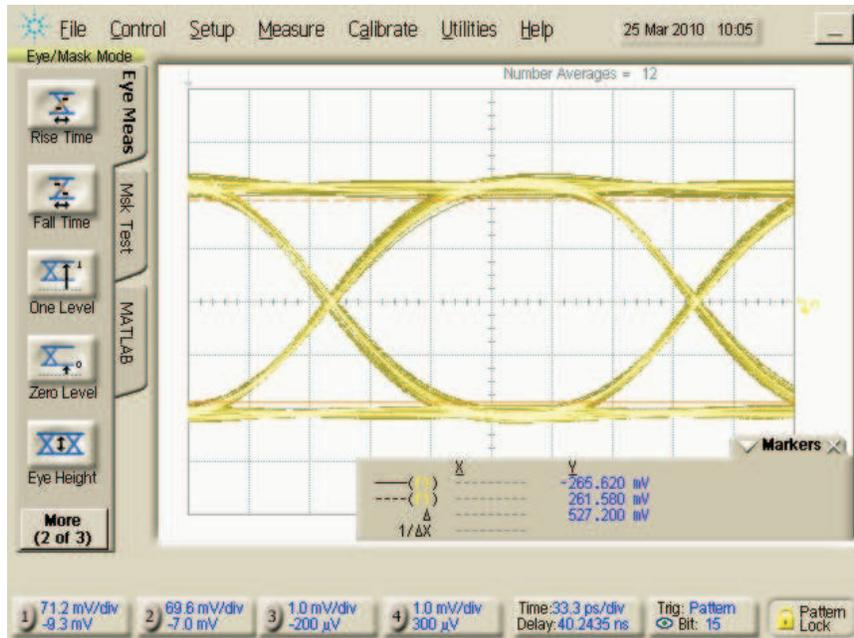
**Figure 22. Input Trace = 8 Inches, 6 mil and Output Trace = 4 Inches, 6 mil**
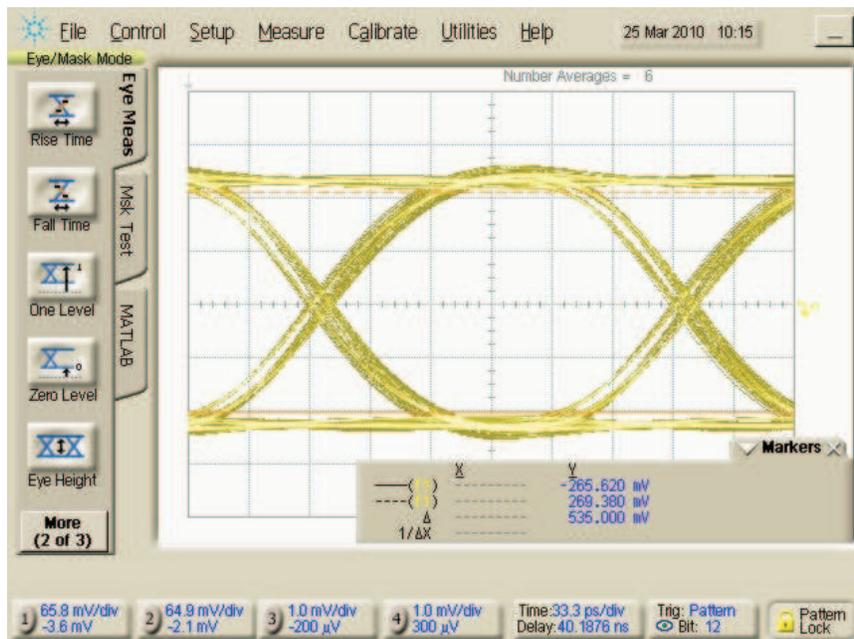


**Figure 23. Input Trace = 12 Inches, 6 mil and Output Trace = 4 Inches, 6 mil**
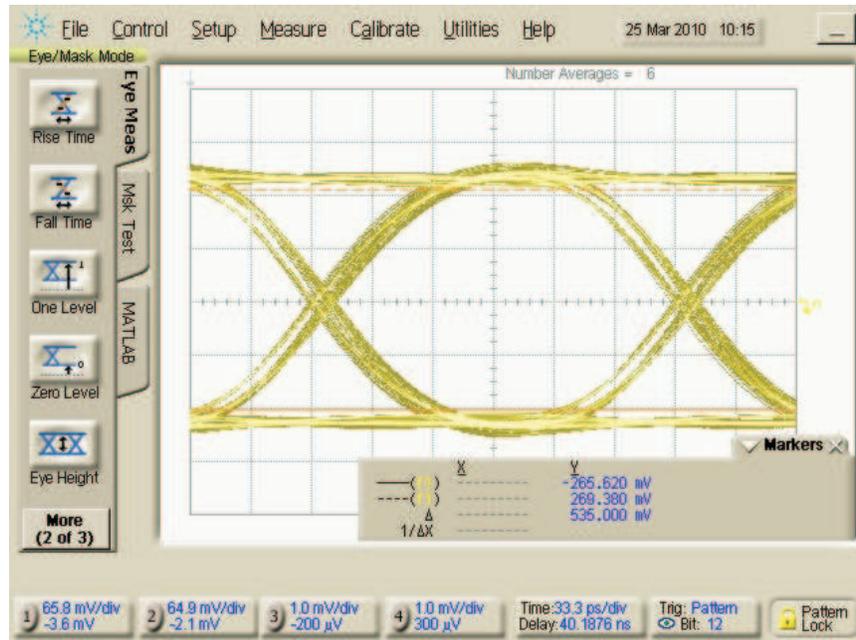
**Figure 24. Input Trace = 16 Inches, 6 mil and Output Trace = 4 Inches, 6 mil**
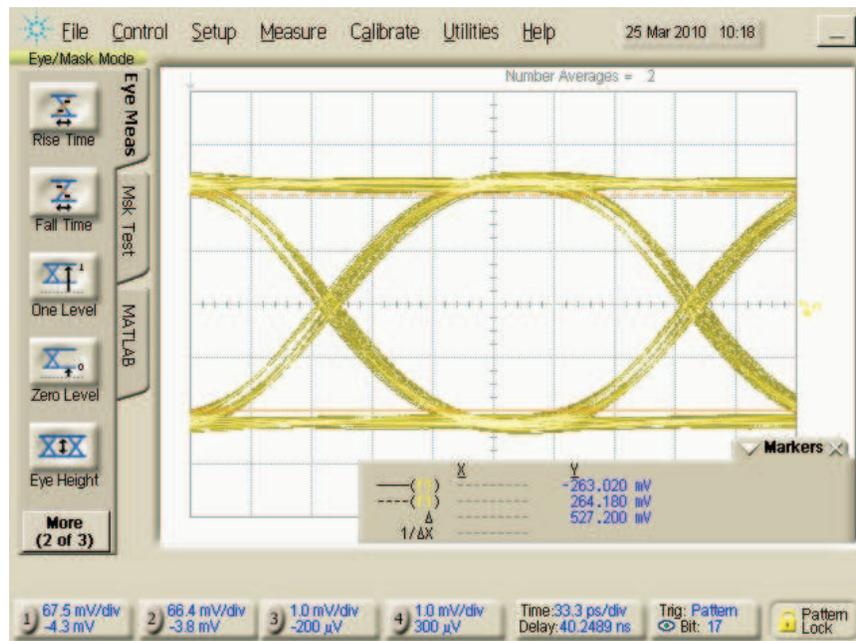


**Figure 25. Input Trace = 20 Inches, 6 mil and Output Trace = 4 Inches, 6 mil**
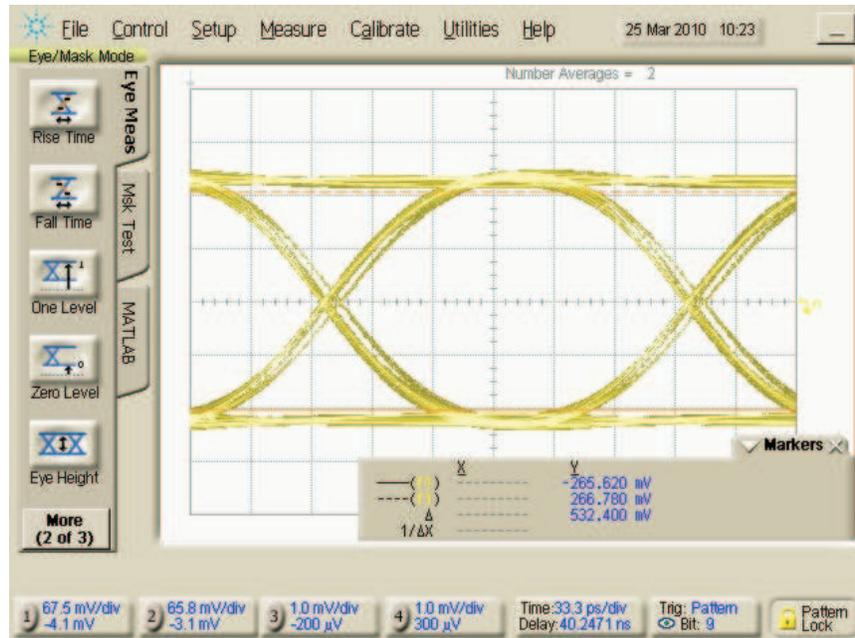
**Figure 26. Input Trace = 28 Inches, 6 mil and Output Trace = 4 Inches, 6 mil**
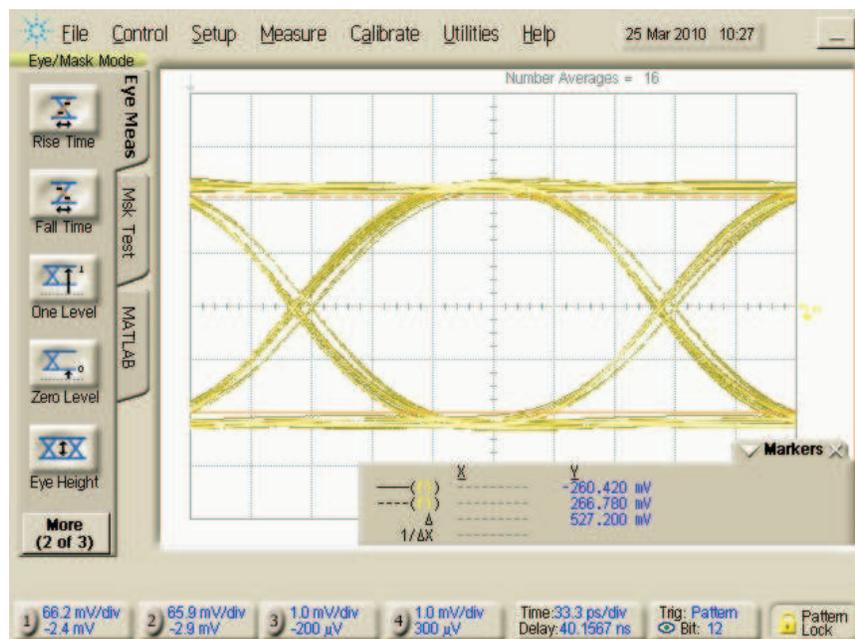


**Figure 27. Input Trace = 32 Inches, 6 mil and Output Trace = 4 Inches, 6 mil**
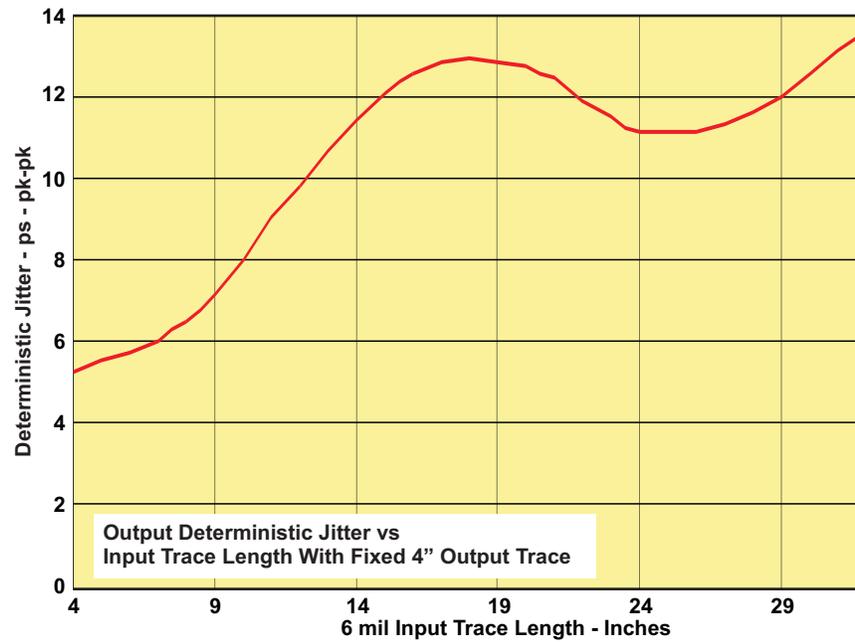
**Figure 28. Jitter Performance Over Different Input Trace Lengths**

Product Folder Link(s): *SN65LVPE502*

# REVISION HISTORY

**Changes from Original (April 2010 ) to Revision A**                                          **Page**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LVPE502RGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 85 | LVPE502 | Samples |
| SN65LVPE502RGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 85 | LVPE502 | Samples |

**(1)** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**
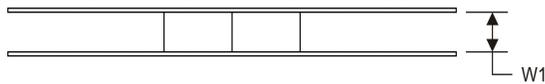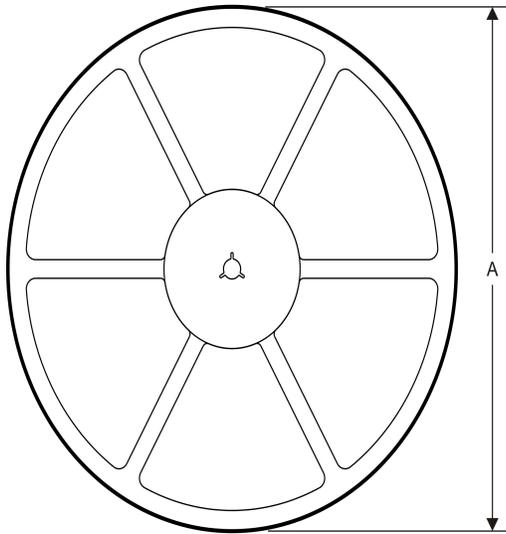
**TAPE DIMENSIONS**
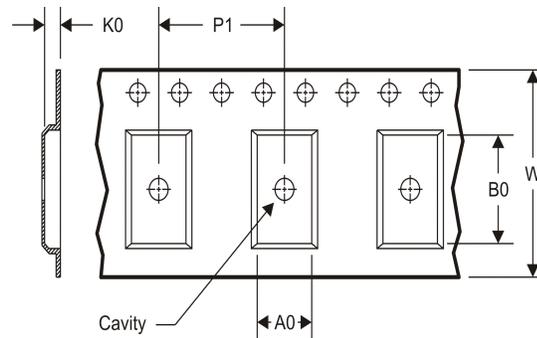


| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LVPE502RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| SN65LVPE502RGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65LVPE502RGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| SN65LVPE502RGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |

RGE (S−PVQFN−N24)                    PLASTIC QUAD FLATPACK NO−LEAD



PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{4,15}{3,85}$

$\frac{4,15}{3,85}$

$\frac{1,00}{0,80}$

0,20 REF.

SEATING PLANE

$\frac{0,05}{0,00}$

0,08

0,50

24X $\frac{0,50}{0,30}$

1        6

24                    7

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

19                    12

18        13    24X $\frac{0,30}{0,18}$

| ⊕ | 0,10 Ⓜ | C | A | B |
|---|---|---|---|---|
|   | 0,05 Ⓜ | C |   |   |
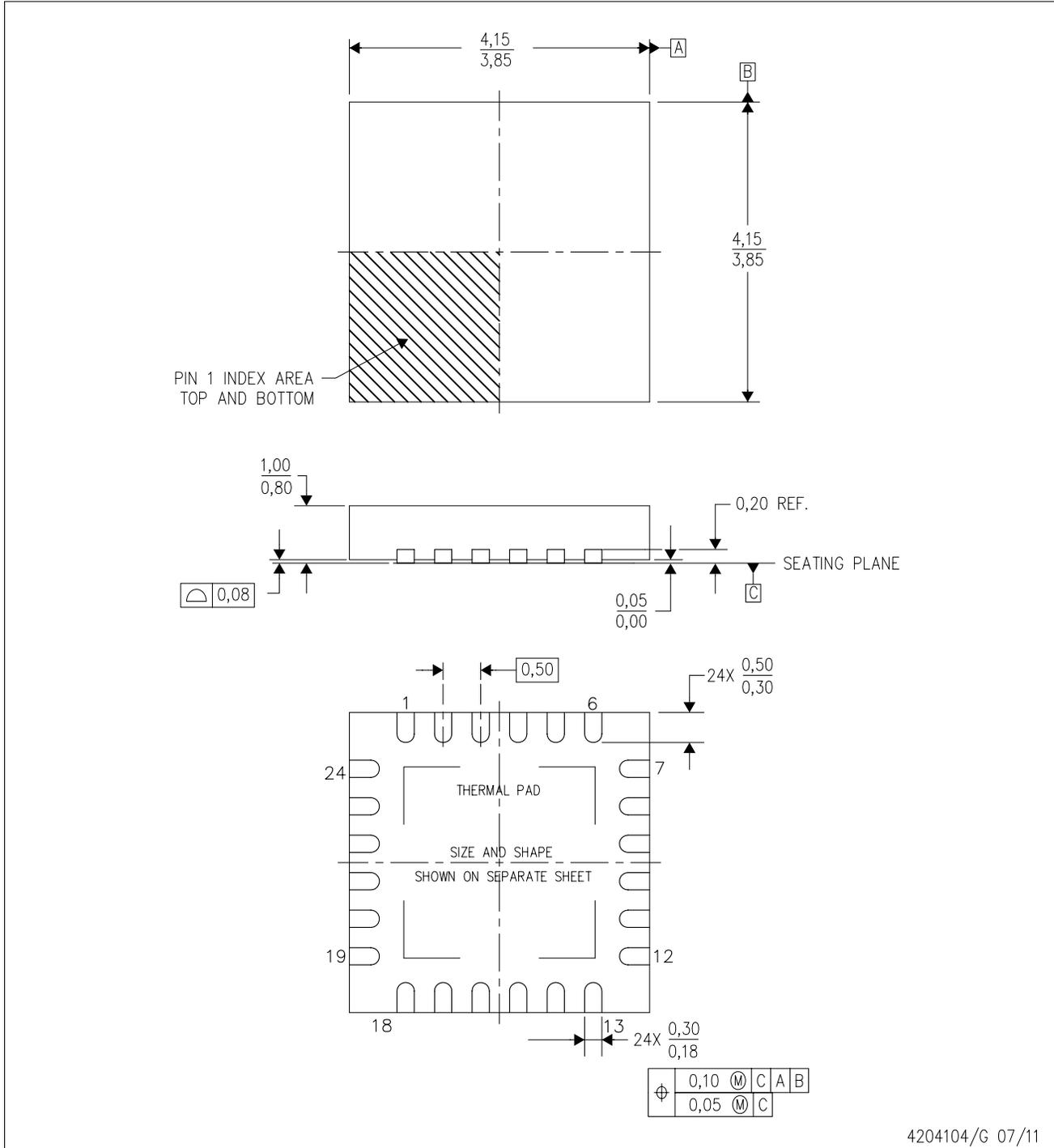
4204104/G 07/11

NOTES:    A.    All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.    This drawing is subject to change without notice.
          C.    Quad Flatpack, No−Leads (QFN) package configuration.
          D.    The package thermal pad must be soldered to the board for thermal and mechanical performance.
          E.    See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
          F.    Falls within JEDEC MO−220.

**TEXAS INSTRUMENTS**
www.ti.com

RGE (S−PVQFN−N24)                    PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR (OPTIONAL)

Exposed Thermal Pad

2,10±0,10

2,10±0,10
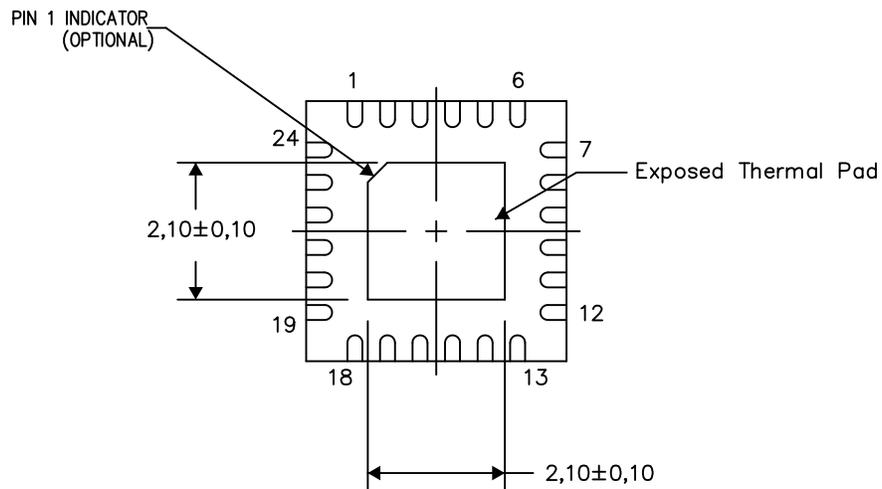
Bottom View

Exposed Thermal Pad Dimensions

4206344−7/AK  08/15

NOTES:    A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24)          PLASTIC QUAD FLATPACK NO–LEAD
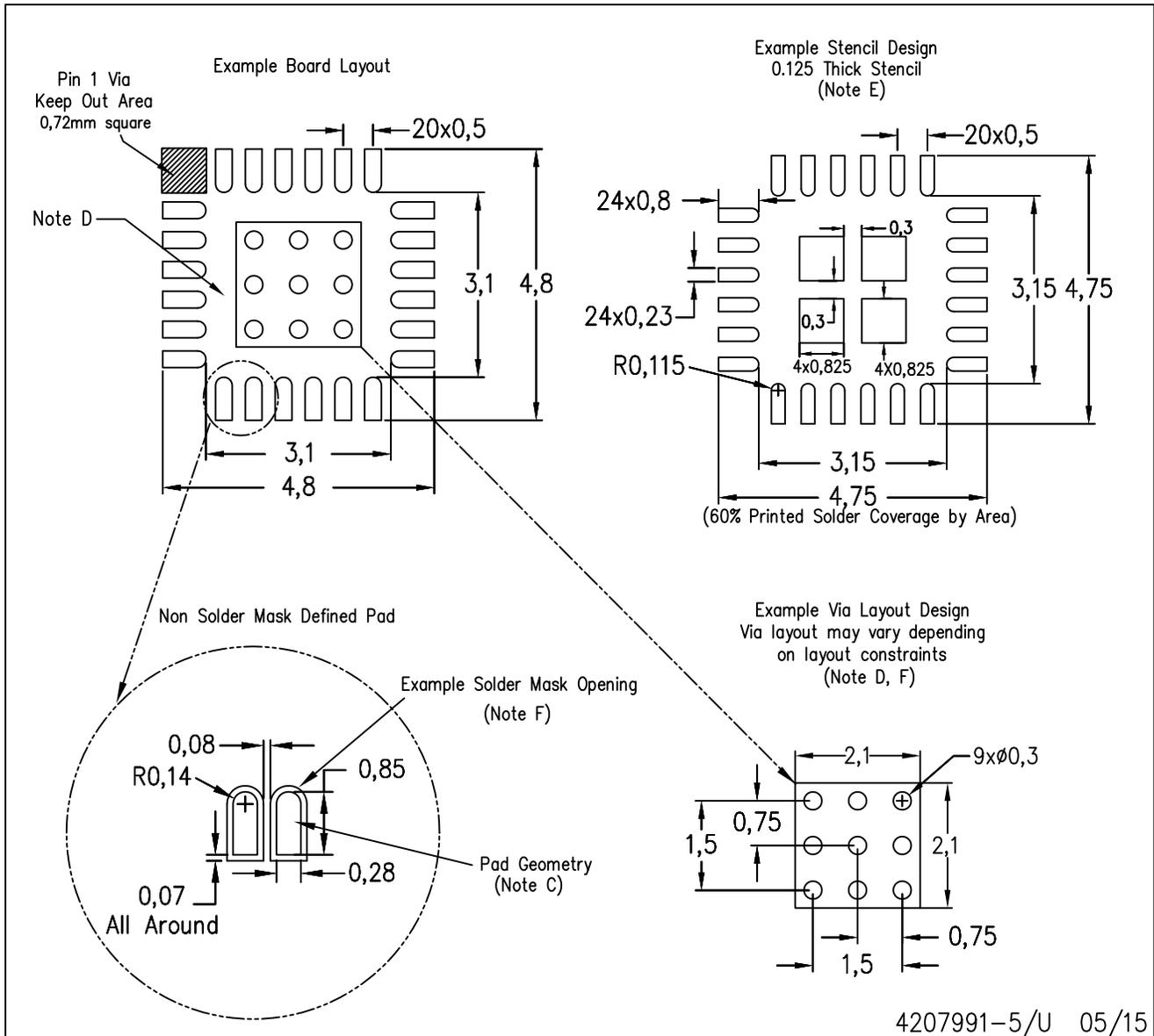
Example Board Layout

Pin 1 Via
Keep Out Area
0,72mm square

Note D

20x0,5

3,1   4,8

3,1
4,8

Example Stencil Design
0.125 Thick Stencil
(Note E)

20x0,5

24x0,8

0,3

24x0,23

0,3

R0,115

4x0,825   4X0,825

3,15   4,75

3,15
4,75
(60% Printed Solder Coverage by Area)

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,07
All Around

0,28

Pad Geometry
(Note C)

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

2,1          9xØ0,3

0,75

1,5          2,1

0,75

1,5

4207991–5/U   05/15

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board.  Refer to Application Note, Quad Flat–Pack
              Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout.  These documents are available at
              www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations.  Refer to IPC 7525 for stencil design
              considerations.
         F.   Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
              recommendations for vias placed in the thermal pad.

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