Low Power Consumption Current Mode Controller

DESCRIPTION

The SiP280X family includes six high-speed, low power consumption, BiCMOS Current Mode Controllers. These integrated circuits contain all of the control and drive functions required for off-line and DC/DC current-mode switching power supplies. Their advanced architecture enables the implementation of full-featured designs with minimal external parts count.

The SiP280X family controllers is available in lead (Pb)-free, SO-8 packages, and are rated for operation over the industrial temperature range of - 40 °C to 85 °C.

FEATURES

- Pin-for-pin compatible with UCC280X controllers
- Enhanced performance UC284X for new designs
- 100 µA typical start-up current
- 500 µA typical operating current
- Internal soft start at power-on and after fault
- 100 ns internal leading edge blanking
- **Compliant to RoHS Directive 2002/95/EC**

Pb-free Available

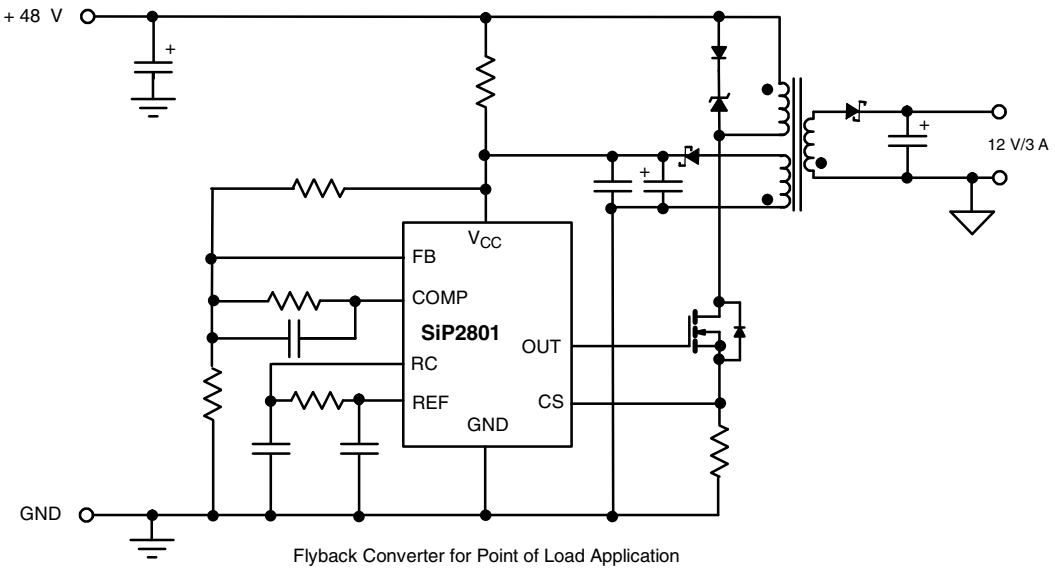
RoHS* COMPLIANT

APPLICATIONS

- Efficiency-enhanced DC/DC converter modules
- Low quiescent current standby power supplies
- Offline (AC/DC) power supplies
- Universal input power supplies
- Buck, boost, and buck-boost converters

Part Number	Maximum Duty Cycle	Reference Voltage	Turn-On Threshold	Turn-Off Threshold
SiP2800	100 %	5 V	7.2 V	6.9 V
SiP2801	50 %	5 V	9.4 V	7.4 V
SiP2802	100 %	5 V	12.5 V	8.3 V
SiP2803	100 %	4 V	4.1 V	3.6 V
SiP2804	50 %	5 V	12.5 V	8.3 V
SiP2805	50 %	4 V	4.1 V	3.6 V

TYPICAL APPLICATION CIRCUIT



Flyback Converter for Point of Load Application

* Pb containing terminations are not RoHS compliant, exemptions may apply.

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ABSOLUTE MAXIMUM RATINGS[a]

Parameter	Limit	Unit
V_{CC}[b]	12	V
FB, Comp, CS	- 0.3 to 6	
Power Dissipation SO-8	1	W
Power Dissipation TSSOP-8	830	mW
Storage Temperature	- 55 to 150	°C

Notes:

a. Currents are positive into, negative out of the specificed terminal.

b. In normal operation V_{CC} is powered through a current limiting resistor. An absolute maximum of 12 V applies when V_{CC} is driven from a low impedance source such that I_{CC} does not exceed 30 mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
Operating Temperature Range	- 40 to 85	°C

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified V_{CC} = 10 V, R_T = 100 kΩ, C_T = 330 pF C_{REF} = 0.1 µF, - 40 °C < T_A < 85 °C		Limits Min.[a]	Typ.[b]	Max.[a]	Unit
Reference							
Reference Voltage	V_{REF}	I_{LOAD} = 0.2 mA, T_A = 25 °C	SiP2800 / SiP2801 / SiP2802 / SiP2804	4.925	5.000	5.075	V
			SiP2803 / SiP2805	3.940	4.000	4.06	
		SiP2800 / SiP2801 / SiP2802 / SiP2804		4.88	5.00	5.10	
		SiP2803 / SiP2805		3.90	4.00	4.08	
Load Regulation	ΔV_{LOAD}	0.2 mA < I_{LOAD} < 5 mA			10	30	mV
Line Regulation	ΔV_{LINE}	V_{CC} = 10 V to Clamp, T_A = 25 °C				1.9	mV/V
		V_{CC} = 10 V to Clamp				2.5	
Noise	V_{NOISE}	10 Hz < f < 10 kHz, T_A = 25 °C			130		µV
Short Circuit Current	I_{SC}			- 5		- 35	mA
Oscillator							
Frequency	f_{OSC}		SiP2800 / SiP2801 / SiP2802 / SiP2804	40	46	52	kHz
			SiP2803 / SiP2805	26	31	36	
Temperature Stability					2.5		%
Amplitude	V_{P-P}			2.25	2.40	2.55	V
Peak Voltage	V_P				2.45		

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SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified V_{CC} = 10 V, R_T = 100 kΩ, C_T = 330 pF C_{REF} = 0.1 µF, - 40 °C < T_A < 85 °C		Limits Min.[a]	Typ.[b]	Max.[a]	Unit
Error Amplifier							
Input Voltage	V_{IN}	COMP = 2.5 V	SiP2800 / SiP2801 / SiP2802 / SiP2804	2.44	2.50	2.56	V
		COMP = 2.0 V	SiP2803 / SiP2805	1.95	2.00	2.05	
Input Bias Current	I_{BIAS1}			- 1		1	µA
Open Loop Gain	A_V			60	80		dB
COMP Sink Current	I_{SINK}	FB = 2.7 V, COMP = 1.1 V		0.3		3.5	mA
COMP Source Current	I_{SOURCE}	FB = 1.8 V, COMP = V_{REF} - 1.2 V		- 0.2	- 0.5	- 0.8	
Gain Bandwidth	B_W				2		MHz

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified V_{CC} = 10 V, R_T = 100 kΩ, C_T = 330 pF C_{REF} = 0.1 µF, - 40 °C < T_A < 85 °C		Limits Min.[a]	Typ.[b]	Max.[a]	Unit
PWM and Overcurrent Comparator							
Maximum Duty Cycle	D_{MAX}		SiP2800 / SiP2802 / SiP2803	97	99	100	%
			SiP2801 / SiP2804 / SiP2805	48	49	50	
Minimum Duty Cycle	D_{MIN}	COMP = 0 V				0	
Gain[c]	A_V	0 < V_{CS} < 0.8 V		1.2	1.65	1.9	V/V
Max. Input Signal	V_{IMAX}	COMP = 5 V		0.9	1.0	1.1	V
Input Bias Current 2	I_{BIAS2}			- 200		200	nA
COMP to CS Offset		CS = 0 V		0.45	0.90	1.35	V
CS Pin Blanking Time				50	100	150	ns
Overcurrent Comparator Fault Threshold				1.47		1.73	
Output							
Output Voltage	V_{OL}	I = 20 mA	All Parts		0.1	0.40	V
		I = 200 mA			0.35	0.90	
		I = 50 mA, V_{CC} = 5 V	SiP2803 / SiP2805		0.15	0.40	
		I = 20 mA, V_{CC} = 0 V	All Parts		0.70	1.20	
	V_{CC} - V_{OH}	I = - 20 mA	All Parts		0.15	0.40	
		I = - 200 mA			1.00	1.90	
		I = - 50 mA, V_{CC} = 5 V	SiP2803 / SiP2805		0.40	0.90	
Rise Time	t_r	CL = 1 nF			41	70	ns
Fall Time	t_f				44	75	

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SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified V_{CC} = 10 V, R_T = 100 kΩ, C_T = 330 pF C_{REF} = 0.1 µF, - 40 °C < T_A < 85 °C		Limits Min.[a]	Limits Typ.[b]	Limits Max.[a]	Unit
Undervoltage Lockout							
Start Threshold[d]	V_{START}		SiP2800	6.6	7.2	7.8	V
			SiP2801	8.6	9.4	10.2	
			SiP2802 / SiP2804	11.5	12.5	13.5	
			SiP2803 / SiP2805	3.7	4.1	4.5	
Stop Threshold[d]	V_{STOP}		SiP2800	6.3	6.9	7.5	
			SiP2801	6.8	7.4	8.0	
			SiP2802 / SiP2804	7.6	8.3	9.0	
			SiP2803 / SiP2805	3.2	3.6	4.0	
Start to Stop Hysteresis	V_{HYS}		SiP2800	0.05	0.30	0.48	
			SiP2801	1.5	2.0	2.4	
			SiP2802 / SiP2804	3.0	4.2	5.1	
			SiP2803 / SiP2805	0.2	0.5	0.8	
Soft-Start							
COMP Rise Time	τ_{SS}	FB = 1.8 V, Rise from 0.5 V to V_{REF} - 1 V			4	10	ms
Overall							
Start-up Current	I_{START}	V_{CC} < Start Threshold			0.1	0.2	mA
Operating Supply Current	I_{CC}	FB = 0 V, CS = 0 V			0.5	1.0	
V_{CC} Internal Zener Voltage[d]	V_Z	I_{CC} = 10 mA		12.0	13.5	15.0	V
V_{CC} Internal Zener Voltage Minus Start Threshold Voltage[d]	V_Z - V_{START}		SiP2802 / SiP28004	0.5	1.0		

Notes:

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (- 40 °C to 85 °C).

b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing and are measured at V_{CC} = 12 V unless otherwise noted.

c. Gain is defined by A = DVCOMP/DVCS, 0 V ≤ VCS ≤ 0.8 V.

d. Start, Stop, and Zener voltages track each other.

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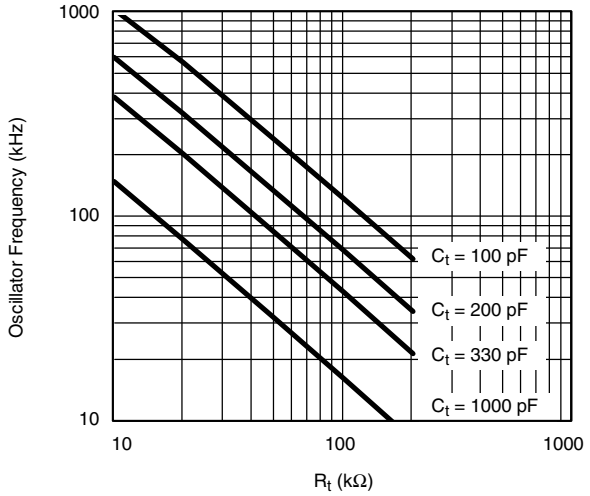
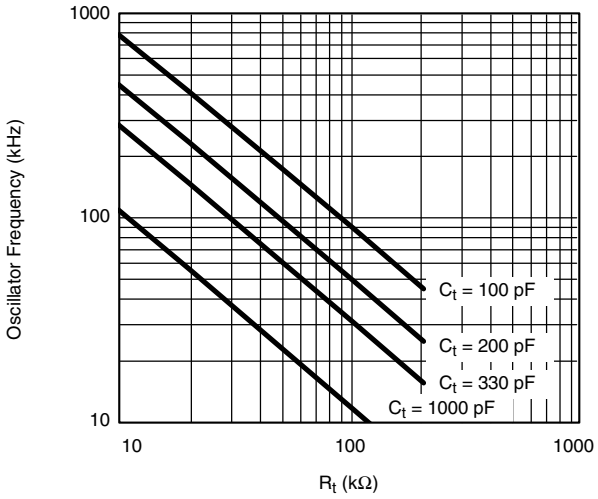
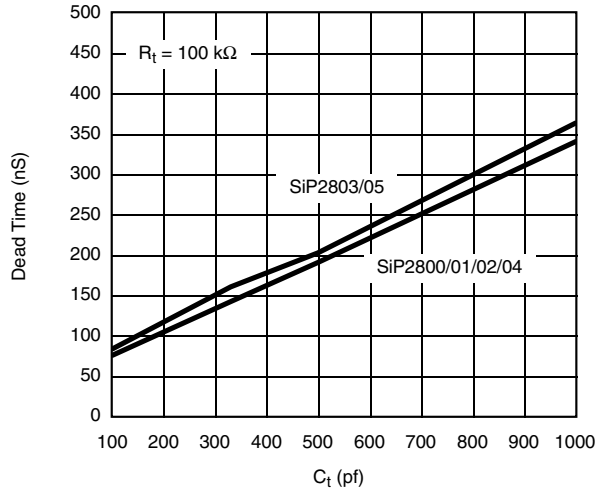
TYPICAL CHARACTERISTICS



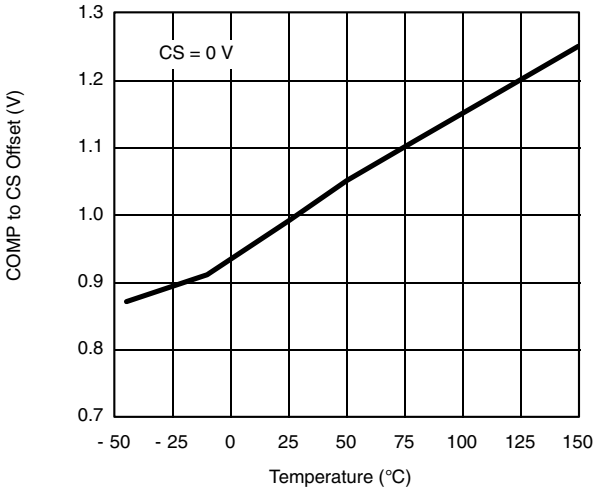
SiP2800 / SiP2801 / SiP2802 / SiP2804
Oscillator Frequency vs. R_t and C_t



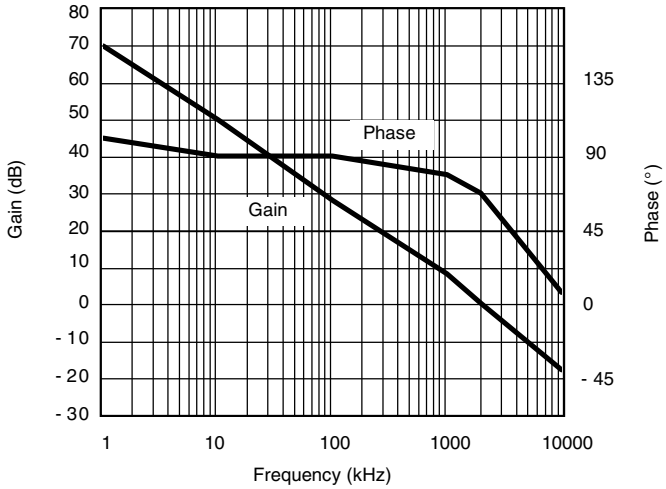
SiP2803 / SiP2805
Oscillator Frequency vs. R_t and C_t



Oscillator Dead Time vs. C_t



COMP to CS Offset Voltage vs. Temperature



Error Amplifier Gain and Phase vs. Frequency

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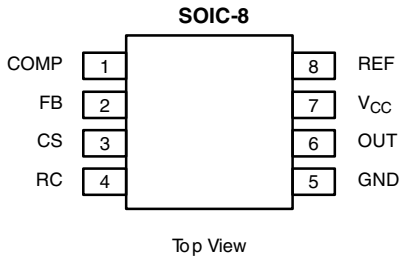
PIN CONFIGURATION



Top View

Additional voltage options are available.

ORDERING INFORMATION

SOIC-8			
Part Number	Lead (Pb)-free Part Number	Marking	Temperature
SiP2800DY-T1	SiP2800DY-T1-E3	2800	- 40 °C to 85 °C
SiP2801DY-T1	SiP2801DY-T1-E3	2801	
SiP2802DY-T1	SiP2802DY-T1-E3	2802	
SiP2803DY-T1	SiP2803DY-T1-E3	2803	
SiP2804DY-T1	SiP2804DY-T1-E3	2804	
SiP2805DY-T1	SiP2805DY-T1-E3	2805	

PIN DESCRIPTION

Pin Number	Name	Function
1	COMP	Output of the Voltage Error Amplifier, and the inverting input to the PWM's Current Sense Comparator
2	FB	Inverting input of the Voltage Error Amplifier
3	CS	Non-inverting input of the PWM Current Sense Comparator, and inverting input of the Overcurrent Fault Comparator (both comparators are fed from the output of the internal 100 ns Leading Edge Blanking circuit)
4	RC	Connection for the PWM Oscillator's timing resistor and timing capacitor
5	GND	Ground Pin
6	OUT	PWM Output Signal (capable of driving ± 750 mA into the gate of an external MOSFET power switch)
7	V_{CC}	Positive supply voltage for the IC
8	REF	IC Reference Voltage

DETAILED PIN DESCRIPTION

COMP

COMP is the output of the Voltage Error Amplifier (VEA). The VEA is a low output impedance operational amplifier, providing the input to the PWM cycle-by-cycle current limit comparator. As the SiP280X series of parts use a true operational amplifier for the VEA, the COMP terminal can both source and sink current. To add flexibility to these parts, the VEA is internally current limited, which allows OUT to be forced to zero duty cycle by taking the COMP pin to GND.

The voltage on COMP is passed through an internal diode to develop an offset voltage of approximately 0.6 V, and then through a resistive divider with a gain of 0.606 V/V, before being presented to the control input of the cycle-by-cycle current limit comparator. Clamping the COMP pin to less than the diode's forward voltage (i.e., < 0.5 V) will command the current loop to deliver 0 A, by holding the control input of the cycle-by-cycle current comparator at 0 V. Similarly, the current loop will command the maximum inductor current on each cycle when COMP is at 2.25 V or greater, which drives the control input of the cycle-by-cycle current comparator to 1 V (since [2.25 V - 0.6 V] x 0.606 V/V = 1 V).

The SiP280X series additionally features a built-in soft-start function, which functions by clamping the output level of the VEA to an internally generated voltage. This clamp will hold COMP at a low voltage ($V_{COMP} \approx 0$ V) until V_{CC} and V_{REF} are at their proper levels. When these levels are appropriate for circuit operation, the internal voltage will begin rising, at the rate of 1 V/ms. This rising clamp level allows the voltage on the COMP pin to rise, which in turn allows the voltage at the control input of the cycle-by-cycle current comparator to increase. The maximum soft-start interval occurs under conditions requiring full duty cycle (50 % or 100 %, depending upon the part type), and is given by the time required for the voltage on the cycle-by-cycle current comparator's control input to reach 1 V. Since 1 V at the control input to the comparator requires that the COMP pin be at 2.25 V, the maximum soft-start interval is approximately 2.25 ms.

CS

Input to both the cycle-by-cycle and overcurrent fault current sense comparators. The cycle-by-cycle current limit comparator is the mechanism by which the VEA's output voltage commands the level of inductor or transformer current during a given "on" interval, thereby regulating the overall circuit's output.This comparator forms the inner loop of the two loops used in current-mode regulation.

The overcurrent comparator has a trip threshold that is 50 % higher than that of the cycle-by-cycle comparator. Under normal operating conditions, this comparator will not trip: its purpose is to provide enhanced protection of the power path components during severe faults (e.g., a short circuit). If the overcurrent comparator is tripped by a fault condition, it will command the SiP280X to do a "full-cycle restart". During this restart, the power supply will be quickly driven to the "off" state, and will be required to wait for five milliseconds (typical) before restarting. When the supply does restart, it will do so using the built-in soft-start function of the SiP280X.

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The SiP280X family incorporates internal leading-edge blanking on the CS pin, to keep any spurious voltages on the CS pin from reaching the comparator inputs during the 100 ns interval immediately following the rising edge on OUT (for example, voltages due to capacitive charging currents). Because of this internal leading-edge blanking, many applications require no external RC filter on the CS input. Compared to circuits requiring the use of an external RC filter circuit, leading-edge blanking provides a shorter effective CS to OUT propagation delay.

FB

FB is the inverting input of the VEA. Internally compared against $V_{REF}/2$ appearing on the VEA's non-inverting input. To avoid stability problems, keep lead lengths to FB as short as possible, and use good layout practices to minimize the stray capacitances of components connected to this pin.

GND

The GND pin is both the reference ground and the power ground for this part.

OUT

OUT is the output of a high-current driver capable of peak currents in excess of ± 750 mA. OUT is therefore well suited to driving the gates of power MOSFETs. This pin is specifically held low when V_{CC} is below the SiP280X's UVLO threshold, to ensure a predictable system turn-on. Since the OUT pin is internally connected to a low impedance CMOS buffer, it is capable of rapid rail-to-rail transitions. This output topology also mitigates the effects of undershoot and overshoot. For this reason, external Schottky clamp diodes are generally not required on this pin.

RC

RC is the oscillator frequency programming pin. F_{OSC} is set by the combination of R_T and C_T. The charging current for C_T is provided through R_T, which is normally connected between REF and the SiP280X RC pin. C_T then connects from RC to GND. Due to the high impedances encountered in low power control circuits, this connection must be a short and quiet return to GND (preferably by means of a dedicated signal trace, separated from all other circuit functions).

The oscillator frequency for the SiP280X family of parts is approximated by the following formulas:

For the SiP2800, SiP2801, SiP2802, and SiP2804:

- $F_{OSC} \approx (1.5)/R_TC_T$

For the SiP2803 and SiP2805:

- $F_{OSC} \approx (1.0)/R_TC_T$

Here R_T is in ohms and C_T is in farads.

More accurate formulas for F_{OSC} are:

For the SiP2800, SiP2801, SiP2802 and SiP2804:

- $F_{OSC} = 1/\{[(C_T + C_{STRAY}) \times R_T \times 0.652] + [(C_T + C_{STRAY}) \times R_{DISCH} \times 2.53] + T_{DELAY}\}$

For the SiP2803 and SiP2805:

- $F_{OSC} = 1/\{[(C_T + C_{STRAY}) \times R_T \times 0.93] + [(C_T + C_{STRAY}) \times R_{DISCH} \times 2.53] + T_{DELAY}\}$

Here R_T is in ohms and C_T is in farads, R_{DISCH} is the value of the resistor through which C_T is discharged (normally an on-chip 130 Ω resistor, unless the circuit is configured with additional external discharge-path resistance), and t_{DELAY} is an inherent internal comparator delay time of 100 ns. The capacitance associated with the RC pin is approximately 7.5 pF, and should be included as a part of C_{STRAY}.

Note that the SiP2801, SiP2804, and SiP2805 have an internal toggle flip-flop at the output of the oscillator, to ensure that the output duty cycle never exceeds 50 %. This divides the frequency appearing at the OUT pin to one-half of the oscillator frequency for these three parts.

Values of R_T below 10 kΩ are not recommended. Low values of R_T cause high circuit operating currents, and very low values will prevent the oscillator from properly discharging C_T.

REF

The reference generator block of the Si280X provides an accurate and stable 4.0 V or 5.0 V (depending upon part number), which is available at this pin of the IC. This voltage is also used internally for other functions on the IC. One of these uses is as the logic power supply for high speed switching logic on the IC; this, and stability concerns, make it important to bypass V_{REF} to GND with a good quality 0.1 µF ceramic capacitor, as close to the part as possible. An electrolytic or tantalum capacitor may be used in addition to the ceramic capacitor. When 1 V < V_{CC} < the UVLO threshold, REF is pulled to ground through a 5 kΩ resistor. Hence, REF can also be used as an output to indicate the part's V_{CC} status.

V_{CC}

V_{CC} is the positive power connection for the SiP280X controller IC, and should be the most positive terminal on the part. In normal operation, V_{CC} is powered through a current limiting resistor. The required start-up supply current will generally be on the order of 100 µA with V_{CC} below the UVLO voltage of the SiP280X, and can remain at or below 500 µA total supply current once the part starts switching.

To prevent the IC from being damaged by overvoltage conditions, each of the SiP2800 family of parts has an internal clamp (effectively a 13.5 V Zener diode) between V_{CC} and GND. If the part's V_{CC} pin is current-fed through an appropriate dropping resistor, the V_{CC} pin will never exceed its rated voltage, nor will the device as a whole exceed its rated power dissipation. This does require knowing what the operating current of the IC will be, so that the value of the dropping resistor can be calculated. A good estimate of the actual operating current (I_{CC}) may be made by summing three components:

(a) Any external current loading on the V_{CC} or REF pins
(b) The operating current required by the IC itself, and
(c) The drive current (I_{DRIVE}) required by the external power switch.

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Item (a) in the above list is a static dc value, and can generally be calculated with good accuracy. Item (b) will increase with operating frequency, but will be fixed for a given value of F_{OSC}. Item (c) is usually the dominant term in the calculation of I_{CC}, as the power required to drive the external power switch will typically increase as F_{OUT} is increased. The most common example of this is seen in driving the gate of a power MOSFET. In such applications, the gate capacitances must be charged once each switching cycle. This calculation is simplified by using the gate charge term given by most MOSFET manufacturers, allowing the use of the formula:

$I_{DRIVE} = F_{OUT} \times Q_g$ of the chosen MOSFET.

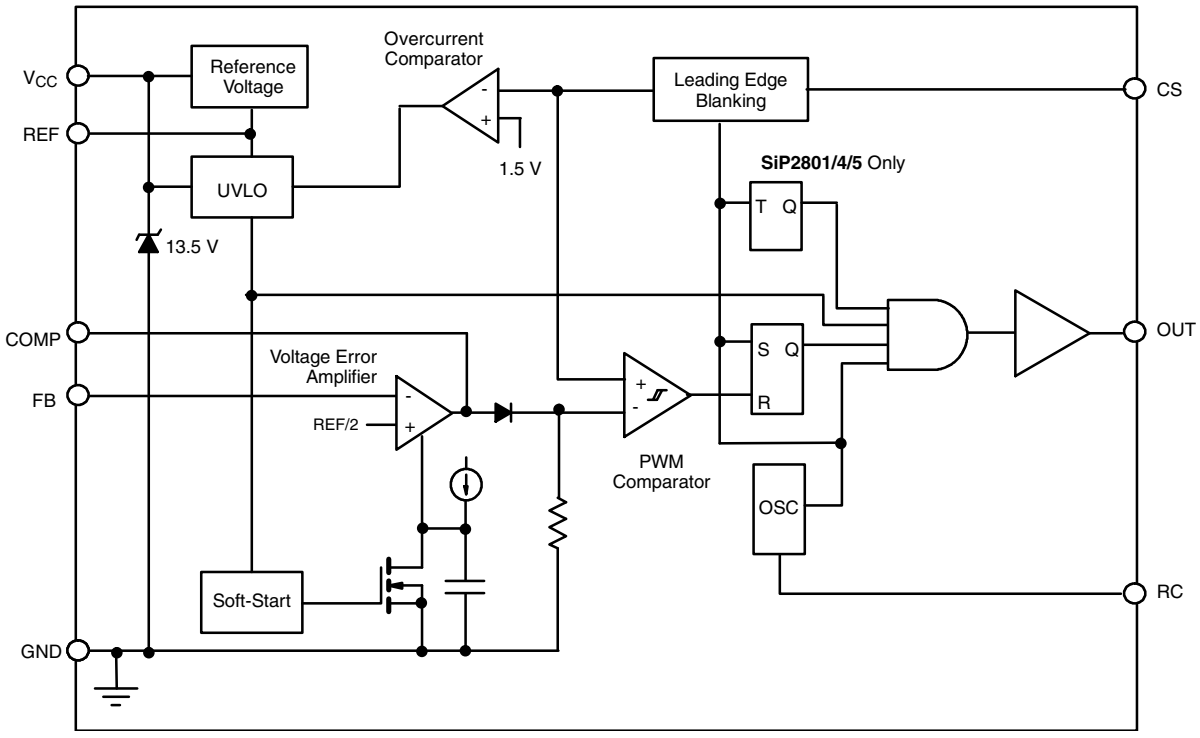
A first approximation of the necessary dropping resistor value is then given by:

$R = [(\text{Nominal } V_{SUPPLY}) - 12\ V]/(\text{Nominal } I_{CC})$

Here R is in ohms and I_{CC} is in amperes.

The resistor limiting the current into the V_{CC} pin should be selected such that $I_{CC(min)}$ equals the worst-case maximum sum of the above currents, while holding $I_{CC(max)}$ to as low a value above that number as practicable (for best overall efficiency), and nevermore than 25 mA above that number (to avoid exceeding the IC's internal clamp diode ratings). V_{CC} must be bypassed to GND with a good quality 0.1 µF ceramic capacitor, as close to the part as possible. This will help avoid problems created by high-frequency noise on the power supply of the part. An electrolytic or tantalum capacitor may be placed in parallel with the ceramic capacitor if more capacitance is needed or desired.

FUNCTIONAL BLOCK DIAGRAM



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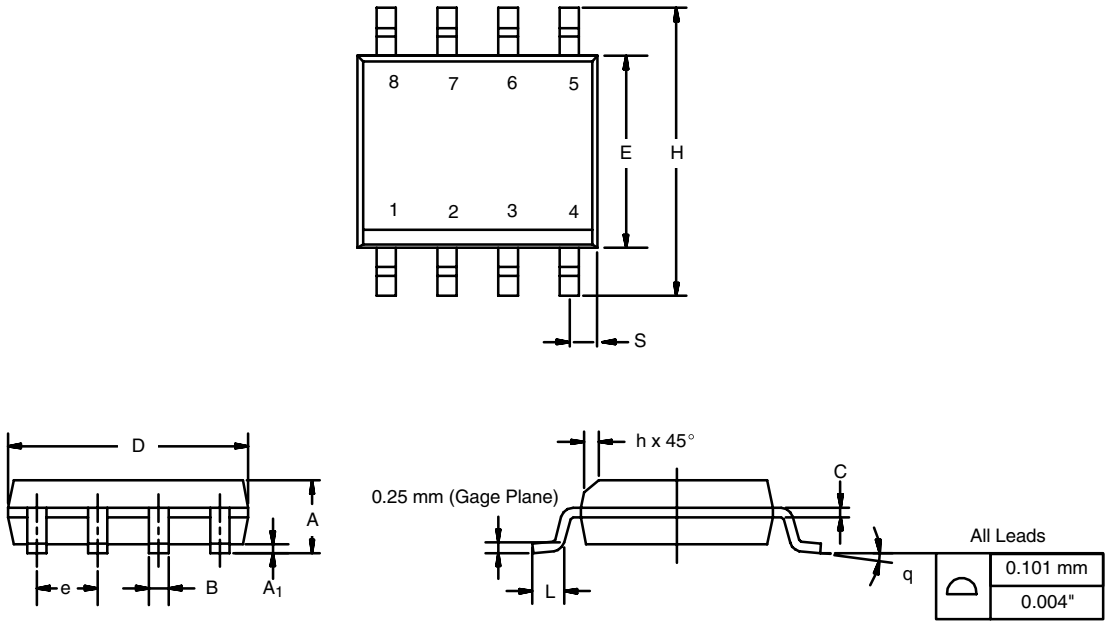
SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

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