

## 1 ps MAX JITTER CRYSTAL OSCILLATOR (XO) (10 MHz TO 810 MHz)

### Features

- Available with any-frequency output frequencies from 10 to 810 MHz
- 3rd generation DSPLL® with superior jitter performance: 1 ps max jitter
- Better frequency stability than SAW-based oscillators
- Internal fundamental mode crystal ensures high reliability
- Available CMOS, LVPECL, LVDS, and CML outputs
- 3.3, 2.5, and 1.8 V supply options
- Industry Standard 5x7 and 3.2x5 mm packages
- Pb-free/RoHS-compliant
- -40 to +85 °C operating temperature range

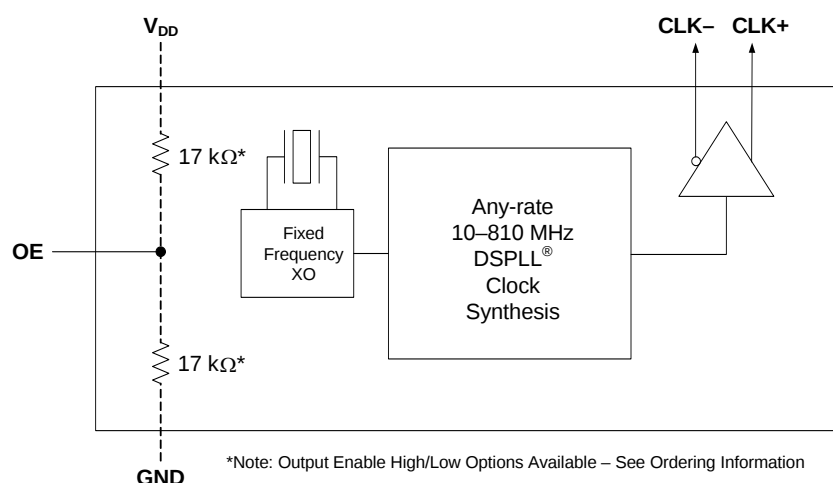
### Applications

- SONET/SDH (OC-3/12/48)
- Networking
- SD/HD SDI/3G SDI video
- Test and measurement
- Storage
- FPGA/ASIC clock generation

### Description

The Si590/591 XO utilizes Silicon Laboratories' advanced DSPLL® circuitry to provide a low jitter clock at high frequencies. The Si590/591 supports any frequency from 10 to 810 MHz. Unlike a traditional XO, where a unique crystal is required for each output frequency, the Si590/591 uses one fixed crystal to provide a wide range of output frequencies. This IC based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments typically found in communication systems. The Si590/591 IC based XO is factory configurable for a wide variety of user specifications including frequency, supply voltage, output format, and stability. Specific configurations are factory programmed at time of shipment, thereby eliminating long lead times associated with custom oscillators.

### Functional Block Diagram



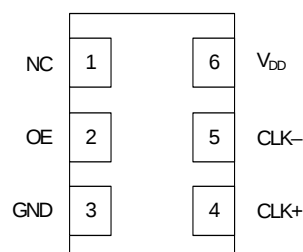
### Ordering Information:

See page 8.

### Pin Assignments:

See page 7.

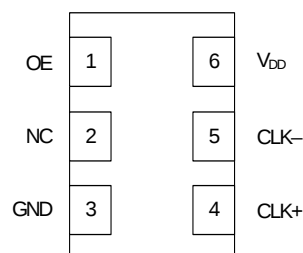
#### (Top View)



**Si590 (LVDS/LVPECL/CML)**



**Si590 (CMOS)**



**Si591 (LVDS/LVPECL/CML)**

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## 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                        | Symbol          | Test Condition           | Min                    | Typ | Max  | Units |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|--------------------------|------------------------|-----|------|-------|
| Supply Voltage <sup>1</sup>                                                                                                                                                                                                                                                                                                                                                                                      | V <sub>DD</sub> | 3.3 V option             | 2.97                   | 3.3 | 3.63 | V     |
|                                                                                                                                                                                                                                                                                                                                                                                                                  |                 | 2.5 V option             | 2.25                   | 2.5 | 2.75 |       |
|                                                                                                                                                                                                                                                                                                                                                                                                                  |                 | 1.8 V option             | 1.71                   | 1.8 | 1.89 |       |
| Supply Current                                                                                                                                                                                                                                                                                                                                                                                                   | I <sub>DD</sub> | Output enabled<br>LVPECL | —                      | 110 | 125  | mA    |
|                                                                                                                                                                                                                                                                                                                                                                                                                  |                 | CML                      | —                      | 100 | 110  |       |
|                                                                                                                                                                                                                                                                                                                                                                                                                  |                 | LVDS                     | —                      | 90  | 100  |       |
|                                                                                                                                                                                                                                                                                                                                                                                                                  |                 | CMOS                     | —                      | 80  | 90   |       |
|                                                                                                                                                                                                                                                                                                                                                                                                                  |                 | Tristate mode            | —                      | 60  | 75   |       |
| Output Enable (OE) <sup>2</sup>                                                                                                                                                                                                                                                                                                                                                                                  |                 | V <sub>IH</sub>          | 0.75 x V <sub>DD</sub> | —   | —    | V     |
|                                                                                                                                                                                                                                                                                                                                                                                                                  |                 | V <sub>IL</sub>          | —                      | —   | 0.5  |       |
| Operating Temperature Range                                                                                                                                                                                                                                                                                                                                                                                      | T <sub>A</sub>  |                          | –40                    | —   | 85   | °C    |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. Selectable parameter specified by part number. See Section 3. "Ordering Information" on page 8 for further details.</li> <li>2. OE pin includes an internal 17 kΩ pullup resistor to V<sub>DD</sub> for output enable active high or a 17 kΩ pull-down resistor to GND for output enable active low. See 3. "Ordering Information" on page 8.</li> </ol> |                 |                          |                        |     |      |       |

**Table 2. CLK± Output Frequency Characteristics**

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Symbol           | Test Condition                         | Min | Typ  | Max  | Units |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|----------------------------------------|-----|------|------|-------|
| Nominal Frequency <sup>1,2</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | f <sub>O</sub>   | LVPECL/LVDS/CML                        | 10  | —    | 810  | MHz   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                  | CMOS                                   | 10  | —    | 160  |       |
| Initial Accuracy                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | f <sub>i</sub>   | Measured at +25 °C at time of shipping | —   | ±1.5 | —    | ppm   |
| Total Stability                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                  | Note 3, second option code "D"         | —   | —    | ±20  | ppm   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                  | Note 3, second option code "C"         | —   | —    | ±30  | ppm   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                  | Note 4, second option code "B"         | —   | —    | ±50  | ppm   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                  | Note 4, second option code "A"         | —   | —    | ±100 | ppm   |
| Temperature Stability                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                  | second option code "D"                 | —   | —    | ±7   | ppm   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                  | second option code "C"                 | —   | —    | ±20  | ppm   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                  | second option code "B"                 | —   | —    | ±25  | ppm   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                  | second option code "A"                 | —   | —    | ±50  | ppm   |
| Powerup Time <sup>5</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | t <sub>OSC</sub> |                                        | —   | —    | 10   | ms    |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. See Section 3. "Ordering Information" on page 8 for further details.</li> <li>2. Specified at time of order by part number.</li> <li>3. Includes initial accuracy, temperature, shock, vibration, power supply and load drift, and 10 years aging at 40 °C. See 3. "Ordering Information" on page 8.</li> <li>4. Includes initial accuracy, temperature, shock, vibration, power supply and load drift, and 15 years aging at 70 °C. See 3. "Ordering Information" on page 8.</li> <li>5. Time from powerup or tristate mode to f<sub>O</sub>.</li> </ol> |                  |                                        |     |      |      |       |

**Table 3. CLK± Output Levels and Symmetry**

| Parameter                                                                                                                                                                                                                                                     | Symbol                          | Test Condition                                                                            | Min                    | Typ                    | Max                    | Units           |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|-------------------------------------------------------------------------------------------|------------------------|------------------------|------------------------|-----------------|
| LVPECL Output Option <sup>1</sup>                                                                                                                                                                                                                             | V <sub>O</sub>                  | mid-level                                                                                 | V <sub>DD</sub> – 1.42 | —                      | V <sub>DD</sub> – 1.25 | V               |
|                                                                                                                                                                                                                                                               | V <sub>OD</sub>                 | swing (diff)                                                                              | 1.1                    | —                      | 1.9                    | V <sub>PP</sub> |
|                                                                                                                                                                                                                                                               | V <sub>SE</sub>                 | swing (single-ended)                                                                      | 0.55                   | —                      | 0.95                   | V <sub>PP</sub> |
| LVDS Output Option <sup>2</sup>                                                                                                                                                                                                                               | V <sub>O</sub>                  | mid-level                                                                                 | 1.125                  | 1.20                   | 1.275                  | V               |
|                                                                                                                                                                                                                                                               | V <sub>OD</sub>                 | swing (diff)                                                                              | 0.5                    | 0.7                    | 0.9                    | V <sub>PP</sub> |
| CML Output Option <sup>2</sup>                                                                                                                                                                                                                                | V <sub>O</sub>                  | 2.5/3.3 V option mid-level                                                                | —                      | V <sub>DD</sub> – 1.30 | —                      | V               |
|                                                                                                                                                                                                                                                               |                                 | 1.8 V option mid-level                                                                    | —                      | V <sub>DD</sub> – 0.36 | —                      |                 |
|                                                                                                                                                                                                                                                               | V <sub>OD</sub>                 | 2.5/3.3 V option swing (diff)                                                             | 1.10                   | 1.50                   | 1.90                   | V <sub>PP</sub> |
|                                                                                                                                                                                                                                                               |                                 | 1.8 V option swing (diff)                                                                 | 0.35                   | 0.425                  | 0.50                   |                 |
| CMOS Output Option <sup>3</sup>                                                                                                                                                                                                                               | V <sub>OH</sub>                 |                                                                                           | 0.8 x V <sub>DD</sub>  | —                      | V <sub>DD</sub>        | V               |
|                                                                                                                                                                                                                                                               | V <sub>OL</sub>                 |                                                                                           | —                      | —                      | 0.4                    |                 |
| Rise/Fall time (20/80%)                                                                                                                                                                                                                                       | t <sub>R</sub> , t <sub>F</sub> | LVPECL/LVDS/CML                                                                           | —                      | —                      | 350                    | ps              |
|                                                                                                                                                                                                                                                               |                                 | CMOS with C <sub>L</sub> = 15 pF                                                          | —                      | 2                      | —                      | ns              |
| Symmetry (duty cycle)                                                                                                                                                                                                                                         | SYM                             | LVPECL: V <sub>DD</sub> – 1.3 V (diff)<br>LVDS: 1.25 V (diff)<br>CMOS: V <sub>DD</sub> /2 | 45                     | —                      | 55                     | %               |
| <b>Notes:</b><br>1. 50 Ω to V <sub>DD</sub> – 2.0 V.<br>2. R <sub>term</sub> = 100 Ω (differential).<br>3. C <sub>L</sub> = 15 pF. Sinking or sourcing 12 mA for V <sub>DD</sub> = 3.3 V, 6 mA for V <sub>DD</sub> = 2.5 V, 3 mA for V <sub>DD</sub> = 1.8 V. |                                 |                                                                                           |                        |                        |                        |                 |

**Table 4. CLK± Output Phase Jitter**

| Parameter                                                                                                                                                                                                                 | Symbol         | Test Condition                                   | Min | Typ | Max | Units |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|--------------------------------------------------|-----|-----|-----|-------|
| Phase Jitter (RMS) <sup>1</sup><br>for 50 MHz ≤ F <sub>OUT</sub> ≤ 810 MHz<br>(LVPECL/LVDS/CML)                                                                                                                           | φ <sub>J</sub> | 12 kHz to 20 MHz                                 | —   | 0.5 | 1.0 | ps    |
| Phase Jitter (RMS) <sup>1</sup><br>(LVPECL/LVDS/CML)                                                                                                                                                                      | φ <sub>J</sub> | 12 kHz to 20 MHz,<br>155.52 MHz output frequency | —   | 0.4 | 0.7 | ps    |
| Phase Jitter (RMS) <sup>2</sup><br>for 50 MHz ≤ F <sub>OUT</sub> ≤ 160 MHz<br>(CMOS)                                                                                                                                      | φ <sub>J</sub> | 12 kHz to 20 MHz                                 | —   | 0.6 | 1.0 | ps    |
| <b>Notes:</b><br>1. Refer to AN256 for further information.<br>2. Single-ended CMOS output phase jitter measured using 33 Ω series termination into 50 Ω phase noise test equipment.<br>3.3 V supply voltage option only. |                |                                                  |     |     |     |       |

**Table 5. CLK± Output Period Jitter**

| Parameter                                                                                                                  | Symbol           | Test Condition | Min | Typ | Max | Units |
|----------------------------------------------------------------------------------------------------------------------------|------------------|----------------|-----|-----|-----|-------|
| Period Jitter*                                                                                                             | J <sub>PER</sub> | RMS            | —   | —   | 3   | ps    |
|                                                                                                                            |                  | Peak-to-Peak   | —   | —   | 35  |       |
| <b>*Note:</b> Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information. |                  |                |     |     |     |       |

**Table 6. Environmental Compliance and Package Information**

| Parameter                 | Conditions/Test Method   |
|---------------------------|--------------------------|
| Mechanical Shock          | MIL-STD-883, Method 2002 |
| Mechanical Vibration      | MIL-STD-883, Method 2007 |
| Solderability             | MIL-STD-883, Method 2003 |
| Gross and Fine Leak       | MIL-STD-883, Method 1014 |
| Resistance to Solder Heat | MIL-STD-883, Method 2036 |
| Contact Pads              | Gold over Nickel         |

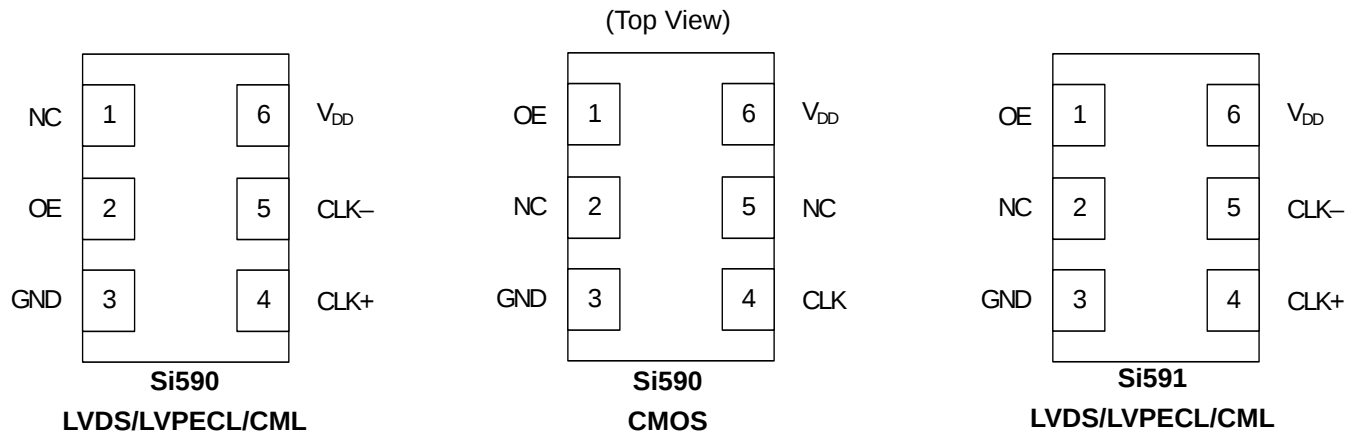
**Table 7. Thermal Characteristics**(Typical values  $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ )

| Parameter                                       | Symbol        | Test Condition | Min | Typ  | Max | Unit                 |
|-------------------------------------------------|---------------|----------------|-----|------|-----|----------------------|
| 5x7mm, Thermal Resistance Junction to Ambient   | $\theta_{JA}$ | Still Air      | —   | 84.6 | —   | $^{\circ}\text{C/W}$ |
| 5x7mm, Thermal Resistance Junction to Case      | $\theta_{JC}$ | Still Air      | —   | 38.8 | —   | $^{\circ}\text{C/W}$ |
| 3.2x5mm, Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still Air      | —   | 31.1 | —   | $^{\circ}\text{C/W}$ |
| 3.2x5mm, Thermal Resistance Junction to Case    | $\theta_{JC}$ | Still Air      | —   | 13.3 | —   | $^{\circ}\text{C/W}$ |
| Ambient Temperature                             | $T_A$         |                | -40 | —    | 85  | $^{\circ}\text{C}$   |
| Junction Temperature                            | $T_J$         |                | —   | —    | 125 | $^{\circ}\text{C}$   |

**Table 8. Absolute Maximum Ratings<sup>1</sup>**

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Symbol     | Rating                 | Units   |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------------------------|---------|
| Maximum Operating Temperature                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | $T_{AMAX}$ | 85                     | °C      |
| Supply Voltage, 1.8 V Option                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | $V_{DD}$   | –0.5 to +1.9           | V       |
| Supply Voltage, 2.5/3.3 V Option                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | $V_{DD}$   | –0.5 to +3.8           | V       |
| Input Voltage (any input pin)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | $V_I$      | –0.5 to $V_{DD} + 0.3$ | V       |
| Storage Temperature                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | $T_S$      | –55 to +125            | °C      |
| ESD Sensitivity (HBM, per JESD22-A114)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | ESD        | 2500                   | V       |
| Soldering Temperature (Pb-free profile) <sup>2</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | $T_{PEAK}$ | 260                    | °C      |
| Soldering Temperature Time @ $T_{PEAK}$ (Pb-free profile) <sup>2</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | $t_P$      | 20–40                  | seconds |
| <b>Notes:</b> <ol style="list-style-type: none"><li>1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.</li><li>2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download at <a href="http://www.silabs.com/VCXO">www.silabs.com/VCXO</a> for further information, including soldering profiles.</li></ol> |            |                        |         |

## 2. Pin Descriptions



**Table 9. Pinout for Si590 Series**

| Pin | Symbol          | LVDS/LVPECL/CML Function                                 | CMOS Function                                            |
|-----|-----------------|----------------------------------------------------------|----------------------------------------------------------|
| 1   | OE*             | No connection<br>Make no external connection to this pin | Output enable                                            |
| 2   | OE*             | Output enable                                            | No connection<br>Make no external connection to this pin |
| 3   | GND             | Electrical and Case Ground                               | Electrical and Case Ground                               |
| 4   | CLK+            | Oscillator Output                                        | Oscillator Output                                        |
| 5   | CLK–            | Complementary Output                                     | No connection<br>Make no external connection to this pin |
| 6   | V <sub>DD</sub> | Power Supply Voltage                                     | Power Supply Voltage                                     |

**\*Note:** OE pin includes an internal 17 kΩ pullup resistor to V<sub>DD</sub> for output enable active high or a 17 kΩ pulldown resistor to GND for output enable active low. See 3. "Ordering Information" on page 8.

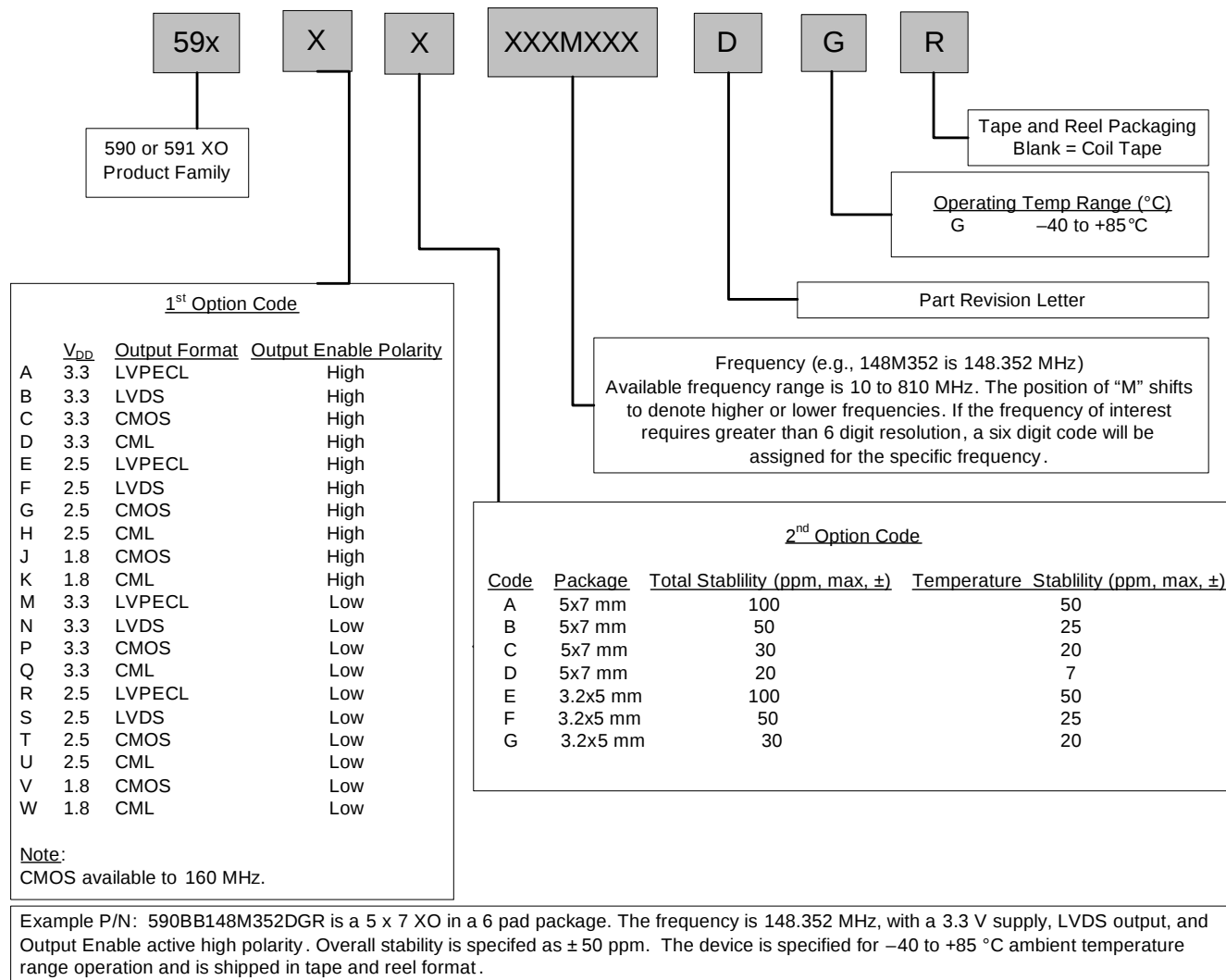
**Table 10. Pinout for Si591 Series**

| Pin | Symbol                                                   | LVDS/LVPECL/CML Function                                 |
|-----|----------------------------------------------------------|----------------------------------------------------------|
| 1   | OE*                                                      | Output enable                                            |
| 2   | No connection<br>Make no external connection to this pin | No connection<br>Make no external connection to this pin |
| 3   | GND                                                      | Electrical and Case Ground                               |
| 4   | CLK+                                                     | Oscillator Output                                        |
| 5   | CLK–                                                     | Complementary output                                     |
| 6   | V <sub>DD</sub>                                          | Power Supply Voltage                                     |

**\*Note:** OE pin includes an internal 17 kΩ pullup resistor to V<sub>DD</sub> for output enable active high or a 17 kΩ pulldown resistor to GND for output enable active low. See 3. "Ordering Information" on page 8.

## 3. Ordering Information

The Si590/591 XO supports a variety of options including frequency, temperature stability, output format, and  $V_{DD}$ . Specific device configurations are programmed into the Si590/591 at time of shipment. Configurations can be specified using the Part Number Configuration chart below. Silicon Laboratories provides a web browser-based part number configuration utility to simplify this process. To access this tool refer to [www.silabs.com/oscillators](http://www.silabs.com/oscillators) and click "Customize" in the product table. The Si590 and Si591 XO series are supplied in an industry-standard, RoHS compliant, 6-pad, 5 x 7 mm and 3.2 x 5 mm packages. The Si591 Series supports an alternate OE pinout (pin #1) for LVPECL, LVDS, and CML output formats. See Tables 9 and 10 for the pinout differences between the Si590 and Si591 series.



**Figure 1. Part Number Convention**

#### 4. Package Outline Drawing: 5 x 7 mm, 6-pin

Figure 2 illustrates the package details for the 5 x 7 mm Si590/591. Table 11 lists the values for the dimensions shown in the illustration.

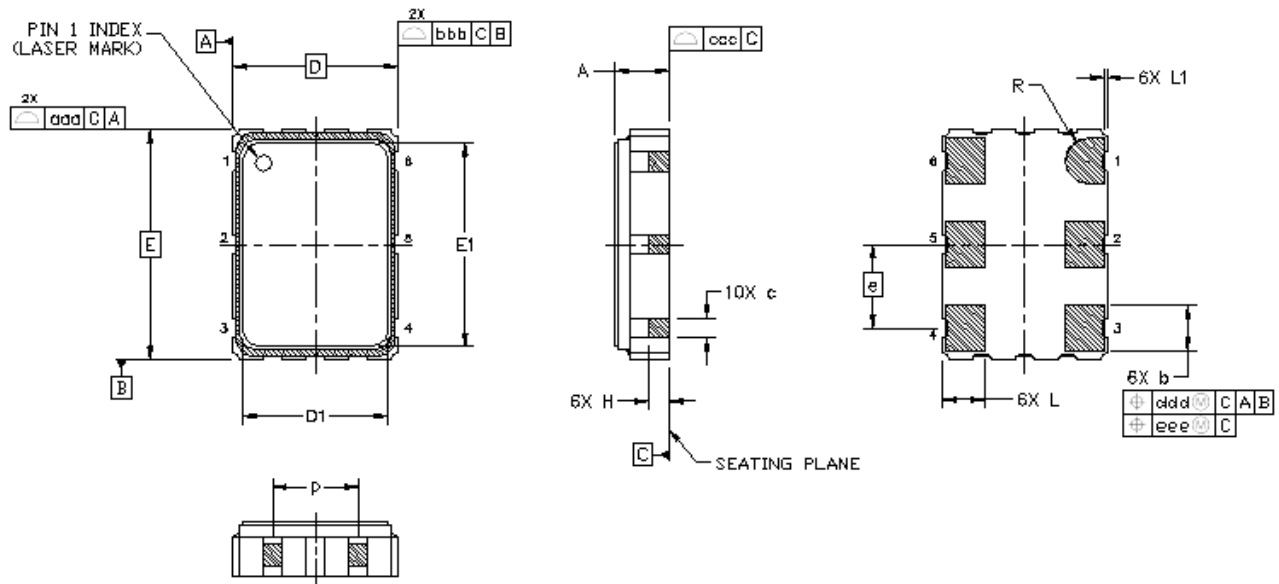


Figure 2. Si590/591 Outline Diagram

Table 11. Package Diagram Dimensions (mm)

| Dimension | Min      | Nom  | Max  |
|-----------|----------|------|------|
| A         | 1.50     | 1.65 | 1.80 |
| b         | 1.30     | 1.40 | 1.50 |
| c         | 0.50     | 0.60 | 0.70 |
| D         | 5.00 BSC |      |      |
| D1        | 4.30     | 4.40 | 4.50 |
| e         | 2.54 BSC |      |      |
| E         | 7.00 BSC |      |      |
| E1        | 6.10     | 6.20 | 6.30 |
| H         | 0.55     | 0.65 | 0.75 |
| L         | 1.17     | 1.27 | 1.37 |
| L1        | 0.05     | 0.10 | 0.15 |
| p         | 1.80     | —    | 2.60 |
| R         | 0.70 REF |      |      |
| aaa       | 0.15     |      |      |
| bbb       | 0.15     |      |      |
| ccc       | 0.10     |      |      |
| ddd       | 0.10     |      |      |
| eee       | 0.05     |      |      |

## 5. PCB Land Pattern: 5 x 7 mm, 6-pin

Figure 3 illustrates the 6-pin PCB land pattern for the 5 x 7 mm Si590/591. Table 12 lists the values for the dimensions shown in the illustration.

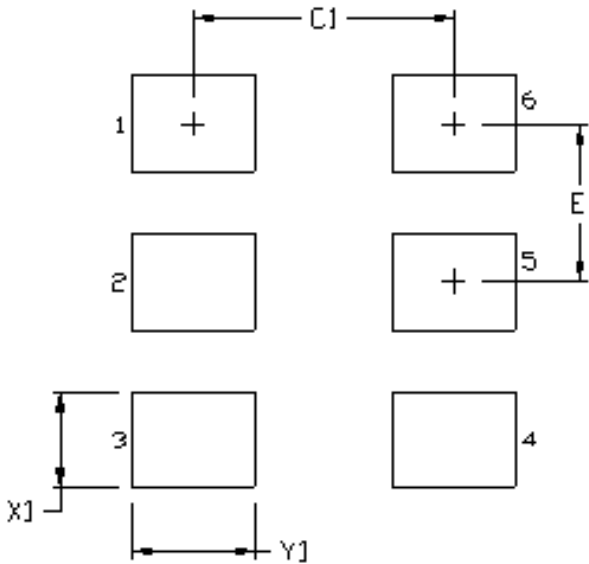


Figure 3. Si590/591 PCB Land Pattern

Table 12. PCB Land Pattern Dimensions (mm)

| Dimension | (mm) |
|-----------|------|
| C1        | 4.20 |
| E         | 2.54 |
| X1        | 1.55 |
| Y1        | 1.95 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 6. Package Outline Drawing: 3.2 x 5 mm, 6-pin

Figure illustrates the package details for the 3.2 x 5 mm Si590/591. Table 13 lists the values for the dimensions shown in the illustration.

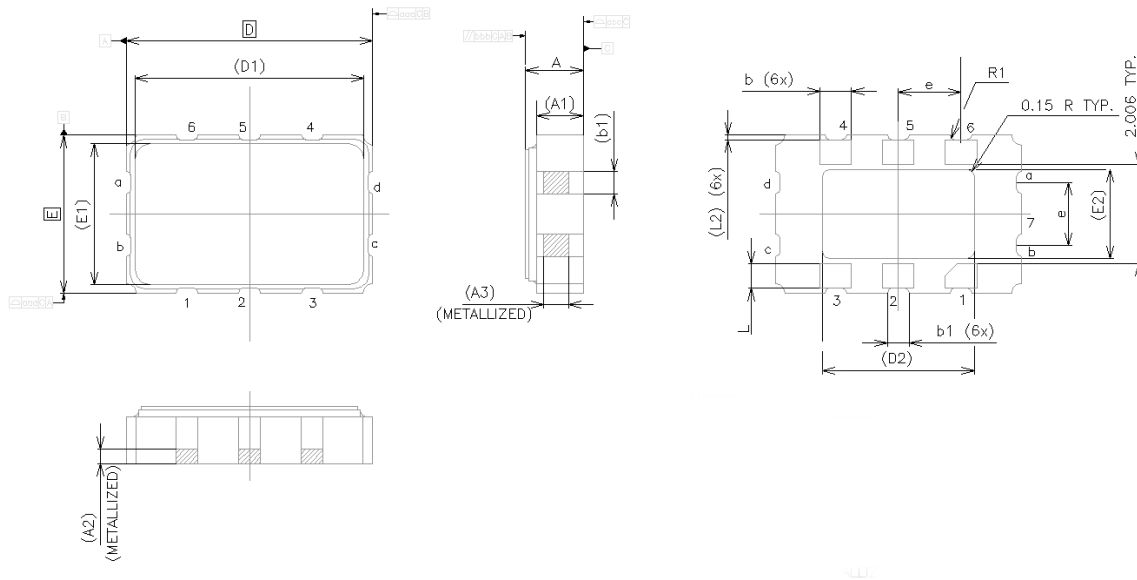


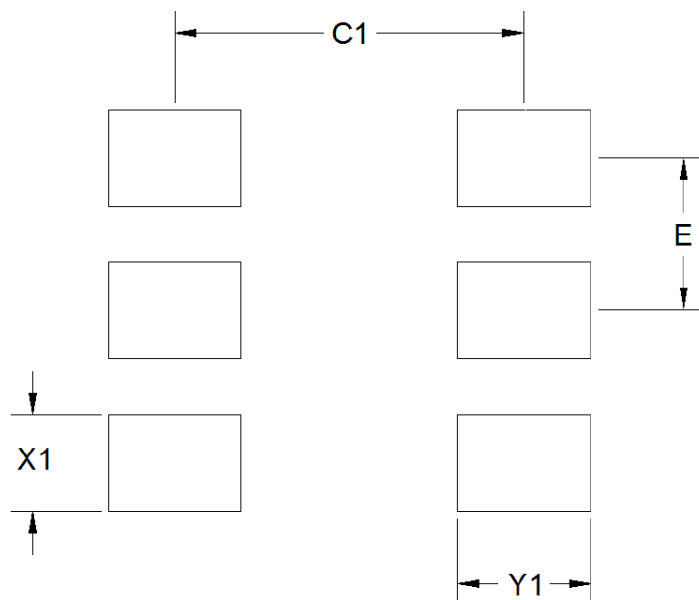
Figure 4. Si590/591 Outline Diagram

Table 13. Package Diagram Dimensions (mm)

| Dimension                                                               | Min      | Nom  | Max  |  | Dimension | Min      | Nom  | Max  |
|-------------------------------------------------------------------------|----------|------|------|--|-----------|----------|------|------|
| A                                                                       | 1.02     | 1.17 | 1.32 |  | E1        | 2.85 BSC |      |      |
| A1                                                                      | 0.99     | 1.10 | 1.21 |  | E2        | 1.91 BSC |      |      |
| A2                                                                      | 0.5 BSC  |      |      |  | L         | 0.35     | 0.45 | 0.55 |
| A3                                                                      | 0.30 BSC |      |      |  | L2        | 0.05     | 0.10 | 0.15 |
| b                                                                       | 0.54     | 0.64 | 0.74 |  | R1        | 0.10 REF |      |      |
| B1                                                                      | 0.35     | 0.45 | 0.55 |  | aaa       | 0.15     |      |      |
| D                                                                       | 5.00 BSC |      |      |  | bbb       | 0.15     |      |      |
| D1                                                                      | 4.65 BSC |      |      |  | ccc       | 0.08     |      |      |
| D2                                                                      | 3.38 BSC |      |      |  | ddd       | 0.10     |      |      |
| e                                                                       | 1.27 BSC |      |      |  | eee       | 0.05     |      |      |
| E                                                                       | 3.20 BSC |      |      |  |           |          |      |      |
| Notes:                                                                  |          |      |      |  |           |          |      |      |
| 1. All dimensions shown are in millimeters (mm) unless otherwise noted. |          |      |      |  |           |          |      |      |
| 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.                   |          |      |      |  |           |          |      |      |

## 7. PCB Land Pattern: 3.2 x 5 mm, 6-pin

Figure 5 illustrates the 6-pin PCB land pattern for the 3.2 x 5 mm Si590/591. Table 14 lists the values for the dimensions shown in the illustration.



**Figure 5. Si590/591 PCB Land Pattern**

**Table 14. PCB Land Pattern Dimensions (mm)**

| Dimension | (mm) |
|-----------|------|
| C1        | 2.91 |
| E         | 1.27 |
| X1        | 0.80 |
| Y1        | 1.10 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

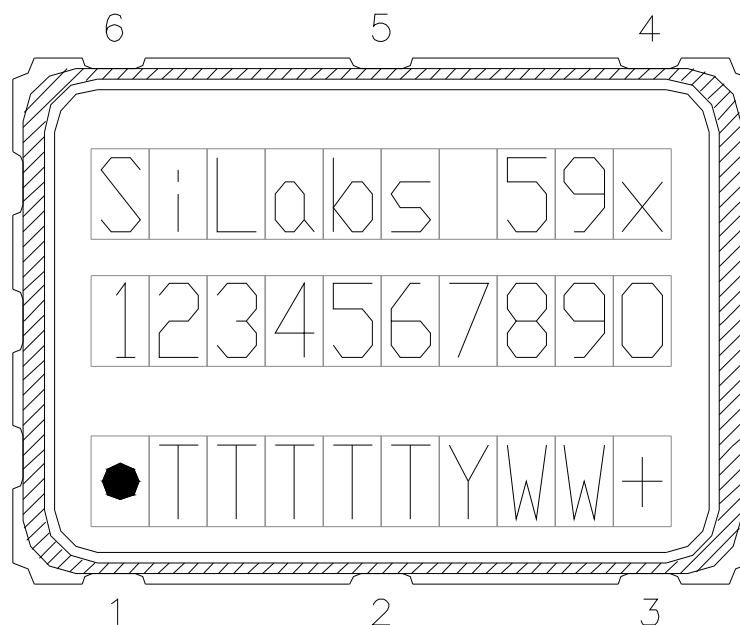
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 8. Si590/Si591 Top Marking: 5 x 7 mm

Figure 6 illustrates the mark specification for the 5 x 7 mm Si590/Si591. Table 15 lists the line information.



**Figure 6. Top Mark Specification**

**Table 15. Si59x Top Mark Description**

| Line | Position          | Description                                                                                                                               |
|------|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 1    | 1–10              | “SiLabs”+ Part Family Number, 59x (First 3 characters in part number where x = 0 indicates a 590 device and x = 1 indicates a 591 device) |
| 2    | 1–10              | Si590, Si591: Option1 + Option2 + Freq(7) + Temp<br>Si590/Si591 w/ 8-digit resolution: Option1 + Option2 + ConfigNum(6) + Temp            |
| 3    | <b>Trace Code</b> |                                                                                                                                           |
|      | Position 1        | Pin 1 orientation mark (dot)                                                                                                              |
|      | Position 2        | Product Revision (D)                                                                                                                      |
|      | Position 3–6      | Tiny Trace Code (4 alphanumeric characters per assembly release instructions)                                                             |
|      | Position 7        | Year (least significant year digit), to be assigned by assembly site (ex: 2009 = 9)                                                       |
|      | Position 8–9      | Calendar Work Week number (1–53), to be assigned by assembly site                                                                         |
|      | Position 10       | “+” to indicate Pb-Free and RoHS-compliant                                                                                                |

## 9. Si590/Si591 Top Marking: 3.2 x 5 mm

Figure 7 illustrates the mark specification for the 3.2 x 5 mm Si590/Si591. Table 16 lists the line information.

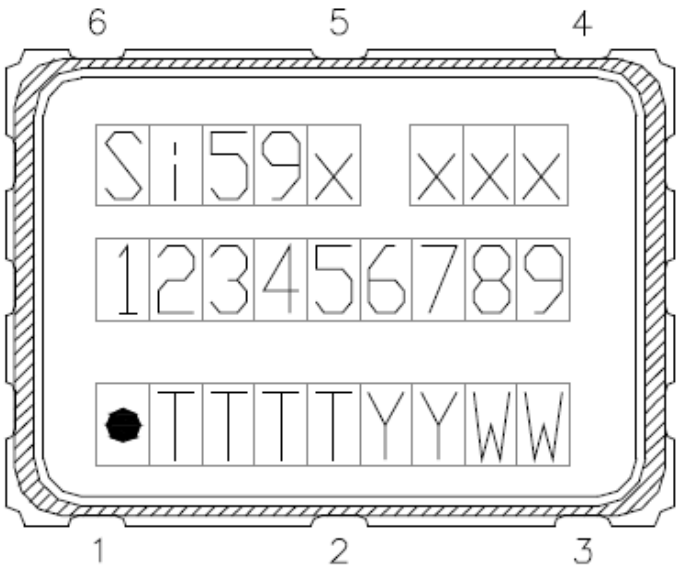


Figure 7. Top Mark Specification

Table 16. Si59x Top Mark Description

| Line | Position          | Description                                                                                                                           |
|------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 1    | 1–5               | “Si”+ Part Family Number, 59x (First 3 characters in part number where x = 0 indicates a 590 device and x = 1 indicates a 591 device) |
|      | 6–8               | Crystal trace code (3 alphanumeric characters assigned by assembly site)                                                              |
| 2    | 1–9               | Si590, Si591: Option1 + Option2 + Freq(7)<br>Si590/Si591 w/ 8-digit resolution: Option1 + Option2 + ConfigNum(6)                      |
| 3    | <b>Trace Code</b> |                                                                                                                                       |
|      | Position 1        | Pin 1 orientation mark (dot)                                                                                                          |
|      | Position 2        | Product Revision (D)                                                                                                                  |
|      | Position 3–5      | Tiny Trace Code (3 alphanumeric characters per assembly release instructions)                                                         |
|      | Position 6–7      | Year (last two digits of year), to be assigned by assembly site (ex: 20017 = 17)                                                      |
|      | Position 8–9      | Calendar Work Week number (1–53), to be assigned by assembly site                                                                     |

## REVISION HISTORY

### Revision 1.2

June, 2018

- Changed “Trays” to “Coil Tape” in 3. “Ordering Information” on page 8.

### Revision 1.1

December, 2017

- Added 3.2 x 5 mm package.

### Revision 1.0

- Updated 2.5 V/3.3 V and 1.8 V CML output level specifications in Table 3 on page 4.
- Updated Si590/591 devices to support frequencies up to 810 MHz for LVPECL, LVDS, and CML outputs.
- Separated 1.8 V, 2.5 V/3.3 V supply voltage. specifications for CML output in Table 3 on page 4.
- Updated Note 1 of Table 4 on page 4 to refer to AN256.
- Updated Table 4 on page 4.
  - Updated phase jitter specification.
- Updated Table 6 on page 5 to include the “Moisture Sensitivity Level” and “Contact Pads” rows.
- Updated Figure 3 and Table 15 on page 13 to reflect specific marking information.
- Added Table 7, “Thermal Characteristics,” on page 5.
- Rearranged sections to conform to new quality standard.

### Revision 0.4

- Added  $\pm 7$  ppm temperature stability ordering option in Table 4 on page 4 and Figure 1 on page 8.

### Revision 0.3

- Updated Table 4 on page 4 by adding the 155.51 MHz “Phase Jitter (RMS) (LVPECL/LVDS/CML)” row.
- Updated and clarified Table 6 on page 5 to correct typos and include the “Moisture Sensitivity Level” and “Contact Pads” rows.
- Corrected BSC value in rows D and E in Table 11 on page 9.

### Revision 0.25

- Total Stability Maximum changed to  $\pm 30$  in Table 2 on page 3.
- Total Stability Maximum changed to  $\pm 30$  in Figure 1 on page 8.

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