

Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes.
- Latch Up Protected
- High Peak Output Current: 8A Peak
- Operates from 4.5V to 25V
- Ability to Disable Output under Faults
- High Capacitive Load
Drive Capability: 2500pF in <15ns
- Matched Rise And Fall Times
- Low Propagation Delay Time
- Low Output Impedance
- Low Supply Current

Applications

- Driving MOSFETs and IGBTs
- Limiting di/dt under Short Circuit
- Motor Controls
- Line Drivers
- Pulse Generators
- Local Power ON/OFF Switch
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Pulse Transformer Driver
- Class D Switching Amplifiers

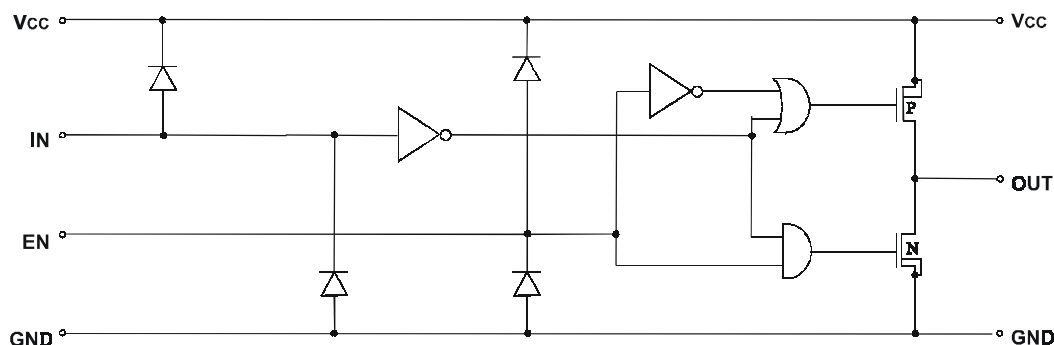
General Description

The IXDD408 is a high speed high current gate driver specifically designed to drive the largest MOSFETs and IGBTs to their minimum switching time and maximum practical frequency limits. The IXDD408 can source and sink 8A of peak current while producing voltage rise and fall times of less than 30ns. The input of the driver is compatible with TTL or CMOS and is fully immune to latch up over the entire operating range. Designed with small internal delays, cross conduction/current shoot-through is virtually eliminated in the IXDD408. Its features and wide safety margin in operating voltage and power make the IXDD408 unmatched in performance and value.

The IXDD408 incorporates a unique ability to disable the output under fault conditions. When a logical low is forced into the Enable input, both final output stage MOSFETs (NMOS and PMOS) are turned off. As a result, the output of the IXDD408 enters a tristate mode and achieves a Soft Turn-Off of the MOSFET/IGBT when a short circuit is detected. This helps prevent damage that could occur to the MOSFET/IGBT if it were to be switched off abruptly due to a dv/dt over-voltage transient.

The IXDD408 is available in the standard 8-pin P-DIP (PI), SOP-8 (SI), 5-pin TO-220 (CI) and in the TO-263 (YI) surface-mount package.

Figure 1 - Functional Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Value
Supply Voltage	25 V
All Other Pins	-0.3 V to $V_{CC} + 0.3$ V
Power Dissipation, $T_{AMBIENT} \leq 25^{\circ}\text{C}$	
8 Pin PDIP (PI)	975mW
8 Pin SOIC (SI)	1055mW
TO220 (CI), TO263 (YI)	17W
Derating Factors (to Ambient)	
8 Pin PDIP (PI)	7.6mW/ $^{\circ}\text{C}$
8 Pin SOIC (SI)	8.2mW/ $^{\circ}\text{C}$
TO220 (CI), TO263 (YI)	0.14W/ $^{\circ}\text{C}$
Storage Temperature	-65 $^{\circ}\text{C}$ to 150 $^{\circ}\text{C}$
Lead Temperature (10 sec)	300 $^{\circ}\text{C}$

Operating Ratings

Parameter	Value
Maximum Junction Temperature	150 $^{\circ}\text{C}$
Operating Temperature Range	-40 $^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$
Thermal Impedance (Junction To Case)	
TO220 (CI), TO263 (YI) (θ_{JC})	0.95 $^{\circ}\text{C/W}$

Electrical Characteristics

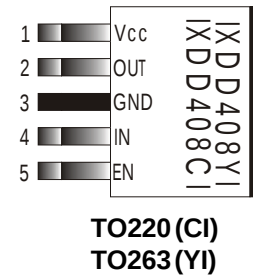
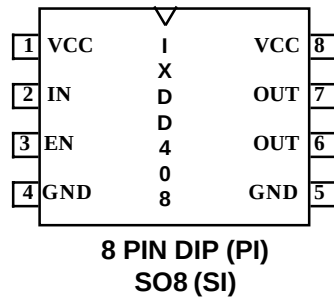
Unless otherwise noted, $T_A = 25^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 25\text{V}$.

All voltage measurements with respect to GND. IXDD408 configured as described in *Test Conditions*.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage		3.5			V
V_{IL}	Low input voltage				0.8	V
V_{IN}	Input voltage range		-5		$V_{CC} + 0.3$	V
I_{IN}	Input current	$0\text{V} \leq V_{IN} \leq V_{CC}$	-10		10	μA
V_{OH}	High output voltage		$V_{CC} - 0.025$			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output high	$I_{OUT} = 10\text{mA}$, $V_{CC} = 18\text{V}$		0.8	1.5	Ω
R_{OL}	Output resistance @ Output Low	$I_{OUT} = 10\text{mA}$, $V_{CC} = 18\text{V}$		0.8	1.5	Ω
I_{PEAK}	Peak output current	V_{CC} is 18V		8		A
I_{DC}	Continuous output current	Limited by package power dissipation			2	A
V_{EN}	Enable voltage range		- .3		$V_{CC} + 0.3$	V
V_{ENH}	High En Input Voltage		2/3 V_{CC}			V
V_{ENL}	Low En Input Voltage				1/3 V_{CC}	V
t_R	Rise time	$C_L = 2500\text{pF}$ $V_{CC} = 18\text{V}$	12	14	18	ns
t_F	Fall time	$C_L = 2500\text{pF}$ $V_{CC} = 18\text{V}$	13	15	19	ns
t_{ONDLy}	On-time propagation delay	$C_L = 2500\text{pF}$ $V_{CC} = 18\text{V}$	37	38	42	ns
t_{OFFDLy}	Off-time propagation delay	$C_L = 2500\text{pF}$ $V_{CC} = 18\text{V}$	32	34	38	ns
t_{ENOH}	Enable to output high delay time	$V_{CC} = 18\text{V}$			52	ns
t_{DOLD}	Disable to output low Disable delay time	$V_{CC} = 18\text{V}$			30	ns
V_{CC}	Power supply voltage		4.5	18	25	V
I_{CC}	Power supply current	$V_{IN} = 3.5\text{V}$		1	3	mA
		$V_{IN} = 0\text{V}$		0	10	μA
		$V_{IN} = + V_{CC}$			10	μA

Specifications Subject To Change Without Notice

Pin Configurations



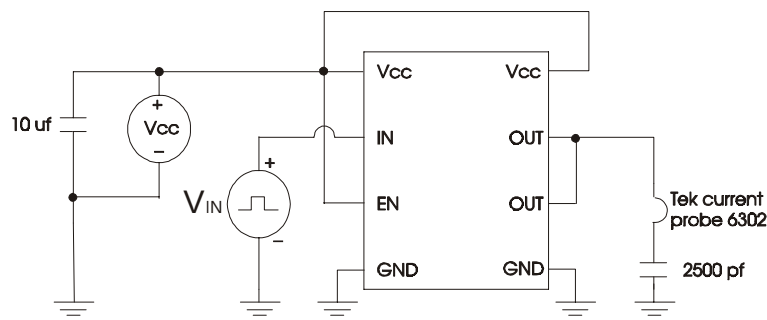
Pin Description

SYMBOL	FUNCTION	DESCRIPTION
VCC	Supply Voltage	Positive power-supply voltage input. This pin provides power to the entire chip. The range for this voltage is from 4.5V to 25V.
IN	Input	Input signal-TTL or CMOS compatible.
EN	Enable	The system enable pin. This pin, when driven low, disables the chip, forcing high impedance state to the output.
OUT	Output	Driver Output. For application purposes, this pin is connected, through a resistor, to Gate of a MOSFET/IGBT.
GND	Ground	The system ground pin. Internally connected to all circuitry, this pin provides ground reference for the entire chip. This pin should be connected to a low noise analog ground plane for optimum performance.

Note 1: Operating the device beyond parameters with listed “absolute maximum ratings” may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD procedures when handling and assembling this component.

Figure 2 - Characteristics Test Diagram



Typical Performance Characteristics

Fig. 3 Rise Time vs. Supply Voltage

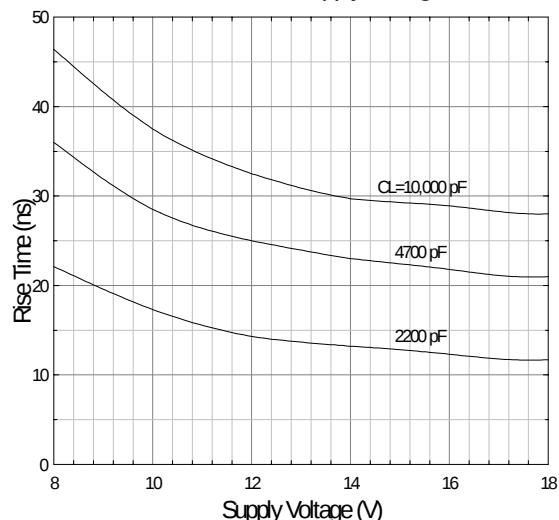


Fig. 4 Fall Time vs. Supply Voltage

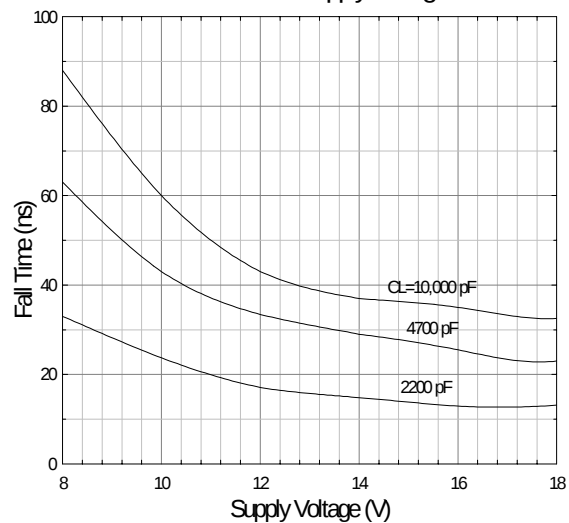
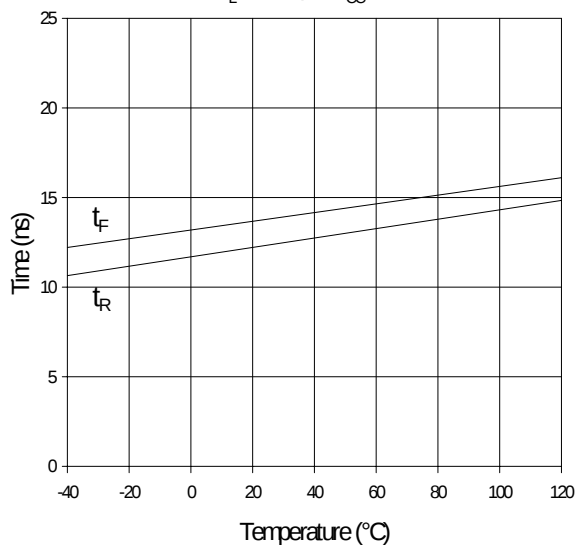
Fig. 5 Rise And Fall Times vs. Junction Temperature
 $C_L = 2500 \text{ pF}$, $V_{CC} = 18 \text{ V}$ 

Fig. 6 Rise Time vs. Load Capacitance

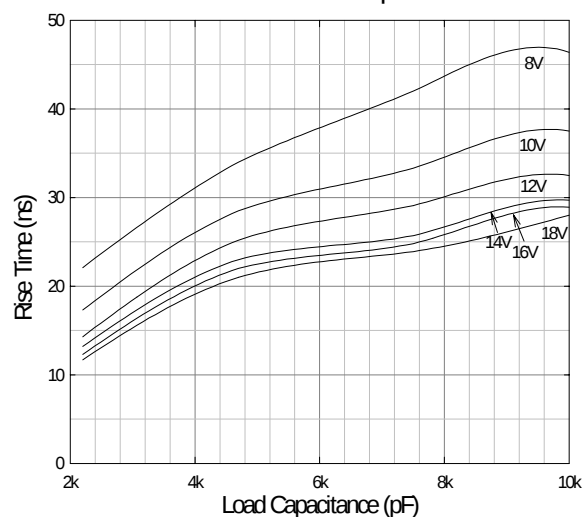


Fig. 7 Fall Time vs. Load Capacitance

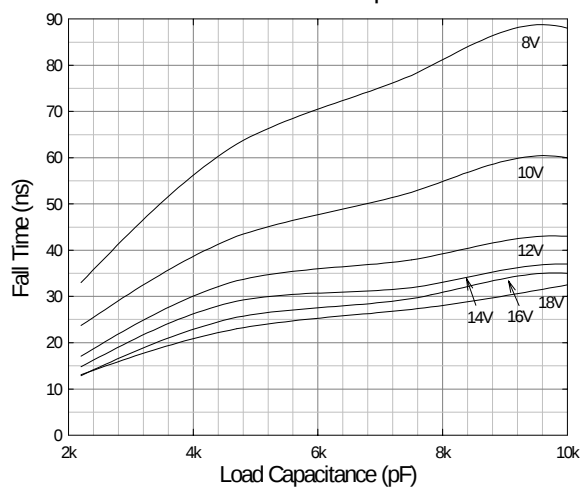
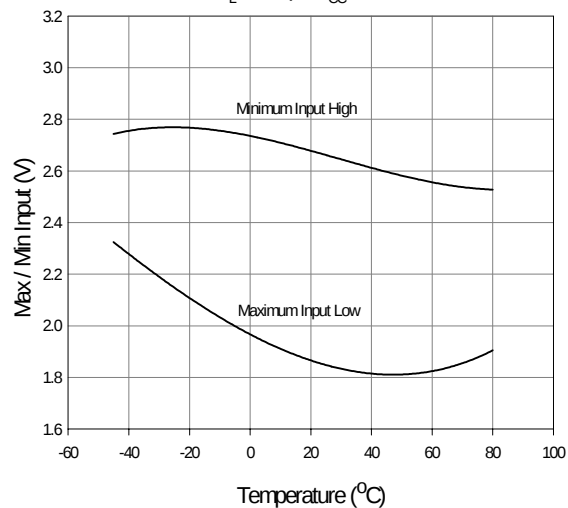
Fig. 8 Max / Min Input vs. Junction Temperature
 $C_L = 2500 \text{ pF}$, $V_{CC} = 18 \text{ V}$ 

Fig. 9 Supply Current vs. Load Capacitance
 $V_{CC}=18V$

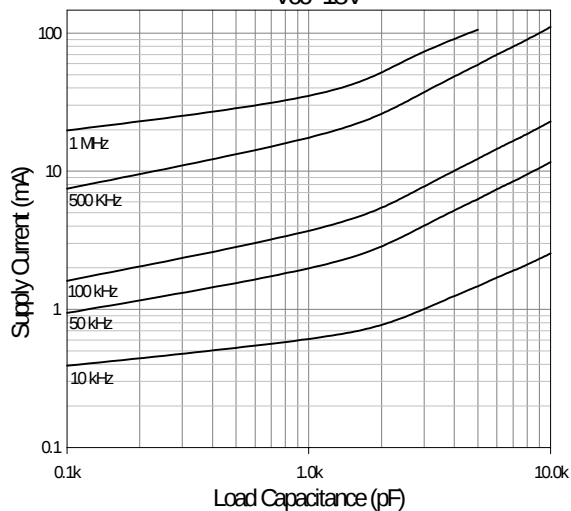


Fig. 10 Supply Current vs. Frequency
 $V_{CC}=18V$

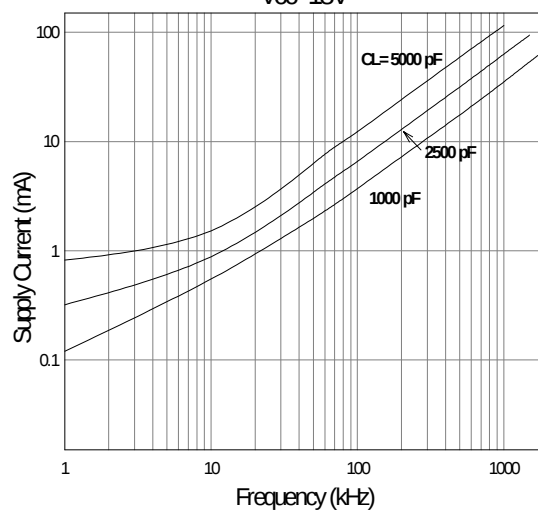


Fig. 11 Supply Current vs. Load Capacitance
 $V_{CC}=12V$

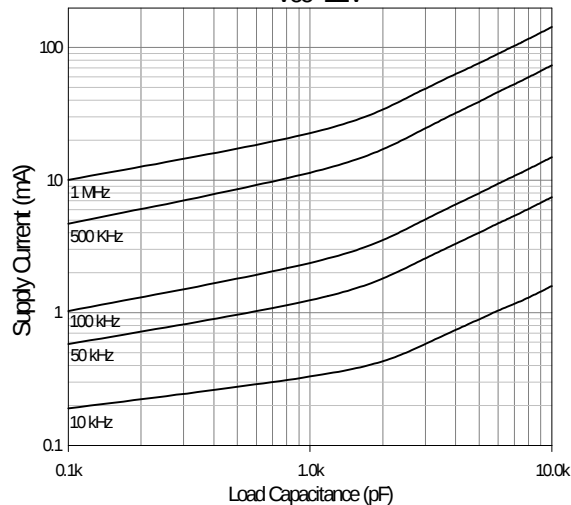


Fig. 12 Supply Current vs. Frequency
 $V_{CC}=12V$

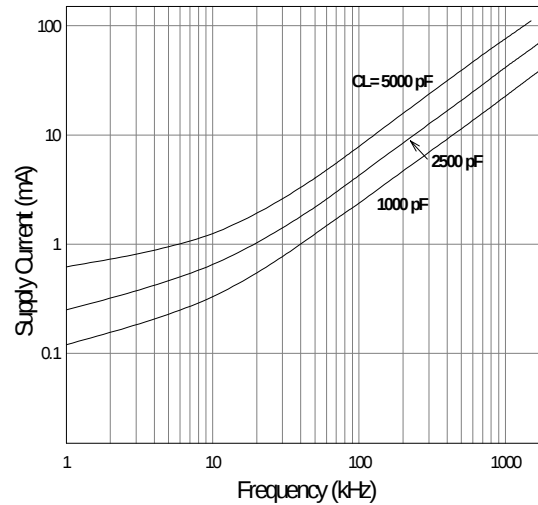


Fig. 13 Supply Current vs. Load Capacitance
 $V_{CC}=8V$

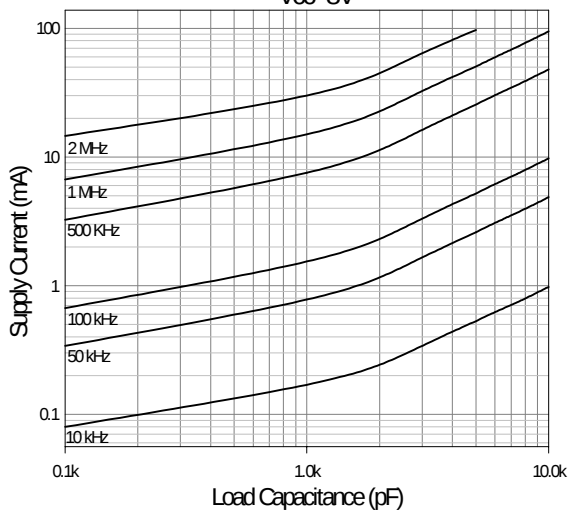


Fig. 14 Supply Current vs. Frequency
 $V_{CC}=8V$

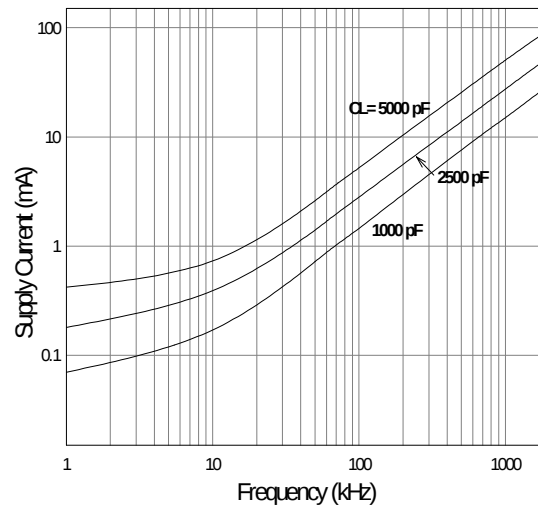


Fig. 15 Propagation Delay vs. Supply Voltage
 $C_L=2500\text{pF}$ $V_{IN}=5\text{V}@1\text{kHz}$

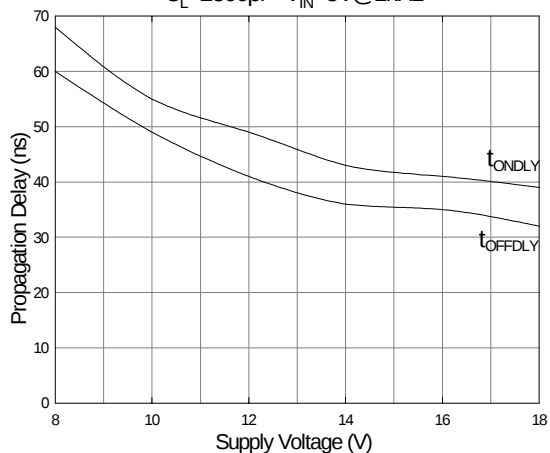


Fig. 16 Propagation Delay vs. Input Voltage
 $C_L=2500\text{pF}$ $V_{CC}=15\text{V}$

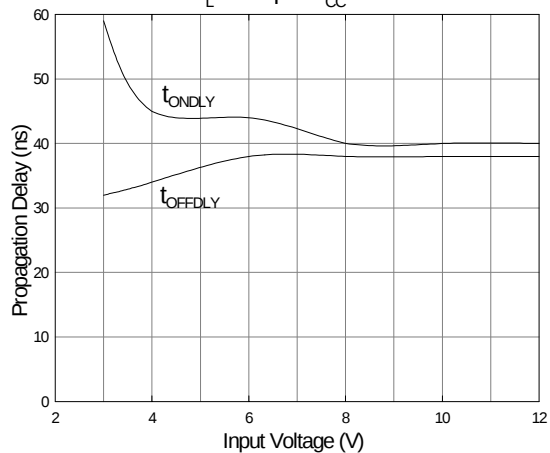


Fig. 17 Propagation Delay Times vs. Junction Temperature
 $C_L = 2500\text{pF}$ $V_{CC} = 18\text{V}$

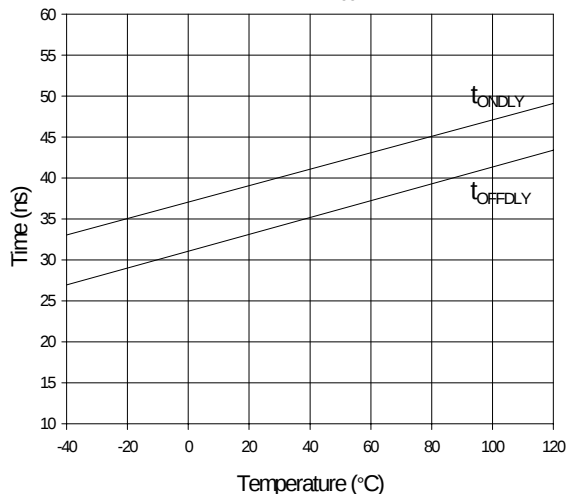


Fig. 18 Quiescent Supply Current vs. Junction Temperature
 $V_{CC}=18\text{V}$ $V_{IN}=5\text{V}@1\text{kHz}$

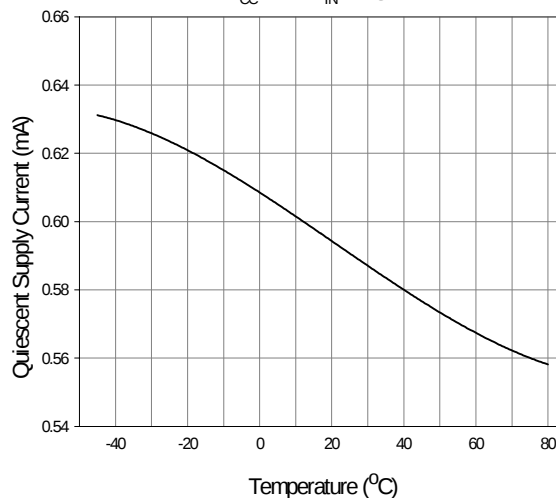


Fig. 19 P Channel Peak Output Current vs. Case Temperature
 CI and YI Packages, $C_L=1\mu\text{F}$ $V_{CC}=18\text{V}$

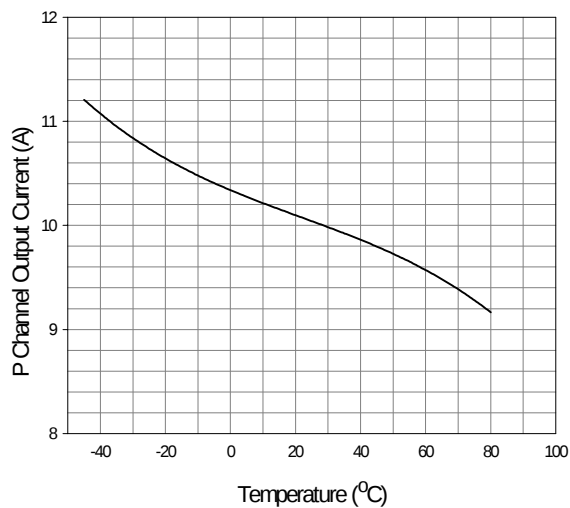
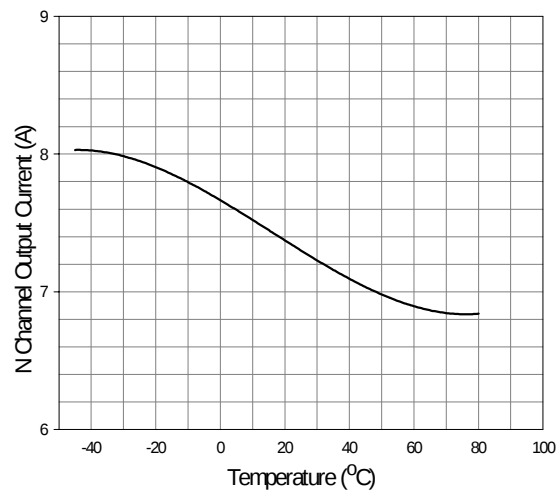
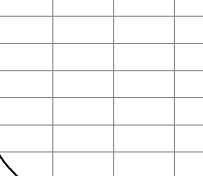


Fig. 20 N Channel Peak Output Current vs. Case Temperature
 CI and YI Packages, $C_L=1\mu\text{F}$ $V_{CC}=18\text{V}$



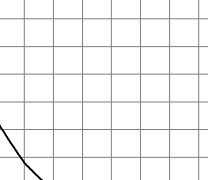
The graph illustrates a linear relationship between the supply voltage and the enable threshold. The x-axis, labeled 'Supply Voltage (V)', ranges from 4 to 26 with major grid lines every 2 units. The y-axis, labeled 'Enable Threshold (V)', ranges from 0 to 14 with major grid lines every 2 units. A single black line represents the data, starting at approximately (5, 2.5) and ending at (25, 12.5). The line has a constant positive slope of 0.5 V/V.

Supply Voltage (V)	Enable Threshold (V)
5	2.5
10	4.5
15	6.5
20	8.5
25	12.5



A line graph showing the relationship between High State Output Resistance (Ohm) and Supply Voltage (V). The y-axis ranges from 0 to 3 Ohms, and the x-axis ranges from 5 to 25 Volts. The resistance decreases as supply voltage increases, starting at approximately 1.7 Ohms at 5V and approaching 0.7 Ohms at 25V.

Supply Voltage (V)	High State Output Resistance (Ohm)
5	1.7
10	1.1
15	0.9
20	0.8
25	0.7



A line graph showing the relationship between Low-State Output Resistance (Ohms) on the y-axis and Supply Voltage (V) on the x-axis. The y-axis ranges from 0.0 to 3.0 with major grid lines every 1.0 unit. The x-axis ranges from 8 to 25 with major grid lines every 5 units. A single black curve starts at approximately (8, 1.8) and decreases monotonically, passing through points like (10, 1.4), (15, 1.0), and (20, 0.8), ending at approximately (25, 0.7).

Supply Voltage (V)	Low-State Output Resistance (Ohms)
8	1.8
10	1.4
15	1.0
20	0.8
25	0.7

A line graph showing the relationship between P-Channel Output Current (A) and Vcc. The x-axis represents Vcc, ranging from 5 to 30. The y-axis represents P-Channel Output Current (A), ranging from 0 to -16. The current decreases linearly as Vcc increases.

Vcc	P-Channel Output Current (A)
5	-1.5
10	-4.0
15	-7.5
20	-11.0
25	-16.0

A graph showing the relationship between the N Channel Output Current (A) on the y-axis and the supply voltage V_{CC} on the x-axis. The y-axis ranges from 0 to 10 with major grid lines every 2 units. The x-axis ranges from 5 to 30 with major grid lines every 5 units. The curve starts at $(5, 0)$ and increases non-linearly, passing through approximately $(10, 1.8)$, $(15, 4.8)$, and $(20, 8.5)$, reaching 10A at $V_{CC} \approx 22.5$ V.

Short Circuit di/dt Limit

When designing a circuit to drive a high speed MOSFET utilizing the IXDD408, it is very important to keep certain design criteria in mind, in order to optimize performance of the driver. Particular attention needs to be paid to **Supply Bypassing**, **Grounding**, and minimizing the **Output Lead Inductance**.

Say, for example, we are using the IXDD408 to charge a 5000pF capacitive load from 0 to 25 volts in 25ns...

Using the formula: $I = \Delta V C / \Delta t$, where $\Delta V = 25V$, $C = 5000pF$ & $\Delta t = 25ns$ we can determine that to charge 5000pF to 25 volts in 25ns will take a constant current of 5A. (In reality, the charging current won't be constant, and will peak somewhere around 8A).

SUPPLY BYPASSING

In order for our design to turn the load on properly, the IXDD408 must be able to draw this 5A of current from the power supply in the 25ns. This means that there must be very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value that is a magnitude larger than the load capacitance. Usually, this would be achieved by placing two different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected, low inductance, low resistance, high-pulse current-service capacitors). Lead lengths may radiate at high frequency due to inductance, so care should be taken to keep the lengths of the leads between these bypass capacitors and the IXDD408 to an absolute minimum.

GROUNDING

In order for the design to turn the load off properly, the IXDD408 must be able to drain this 5A of current into an adequate grounding system. There are three paths for returning current that need to be considered: Path #1 is between the IXDD408 and it's load. Path #2 is between the IXDD408 and it's power supply. Path #3 is between the IXDD408 and whatever logic is driving it. All three of these paths should be as low in resistance and inductance as possible, and thus as short as practical. In addition, every effort should be made to keep these three ground paths distinctly separate. Otherwise, (for instance), the returning ground current from the load may develop a voltage that would have a detrimental effect on the logic line driving the IXDD408.

OUTPUT LEAD INDUCTANCE

Of equal importance to Supply Bypassing and Grounding are issues related to the Output Lead Inductance. Every effort should be made to keep the leads between the driver and it's load as short and wide as possible. If the driver must be placed farther than 2" from the load, then the output leads should be treated as transmission lines. In this case, a twisted-pair should be considered, and the return line of each twisted pair should be placed as close as possible to the ground pin of the driver, and connect directly to the ground terminal of the load.

TTL to High Voltage CMOS Level Translation

The enable (EN) input to the IXDD408 is a high voltage CMOS logic level input where the EN input threshold is $\frac{1}{2} V_{CC}$, and may not be compatible with 5V CMOS or TTL input levels. The IXDD408 EN input was intentionally designed for enhanced noise immunity with the high voltage CMOS logic levels. In a typical gate driver application, $V_{CC} = 15V$ and the EN input threshold at 7.5V, a 5V CMOS logical high input applied to this typical IXDD408 application's EN input will be misinterpreted as a logical low, and may cause undesirable or unexpected results. The note below is for optional adaptation of TTL or 5V CMOS levels.

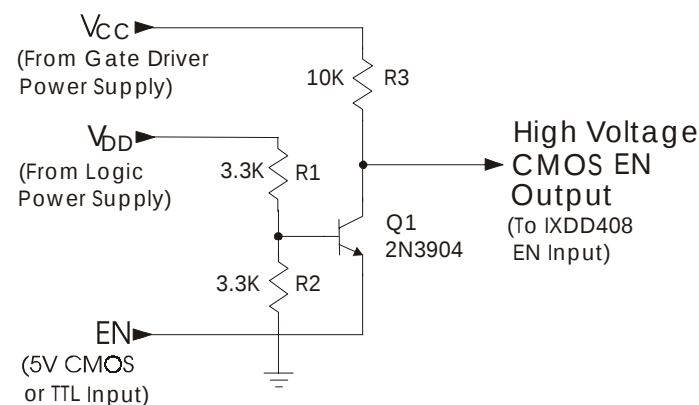
The circuit in Figure 28 alleviates this potential logic level misinterpretation by translating a TTL or 5V CMOS logic input to high voltage CMOS logic levels needed by the IXDD408 EN input. From the figure, V_{CC} is the gate driver power supply, typically set between 8V to 20V, and V_{DD} is the logic power supply, typically between 3.3V to 5.5V. Resistors R1 and R2 form a voltage divider network so that the Q1 base is positioned at the midpoint of the expected TTL logic transition levels.

A TTL or 5V CMOS logic low, $V_{TTLLOW} \approx < 0.8V$, input applied to the Q1 emitter will drive it on. This causes the level translator output, the Q1 collector output to settle to $V_{CESATQ1} + V_{TTLLOW} \approx < 2V$, which is sufficiently low to be correctly interpreted as a high voltage CMOS logic low ($< 1/3 V_{CC} = 5V$ for $V_{CC} = 15V$ given in the IXDD408 data sheet.)

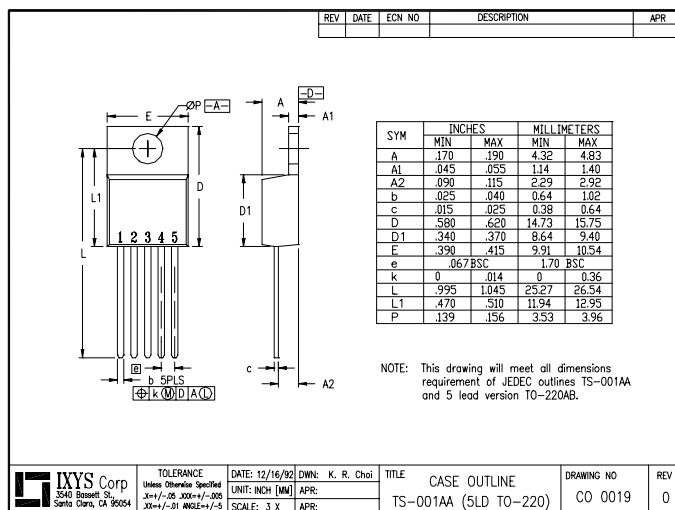
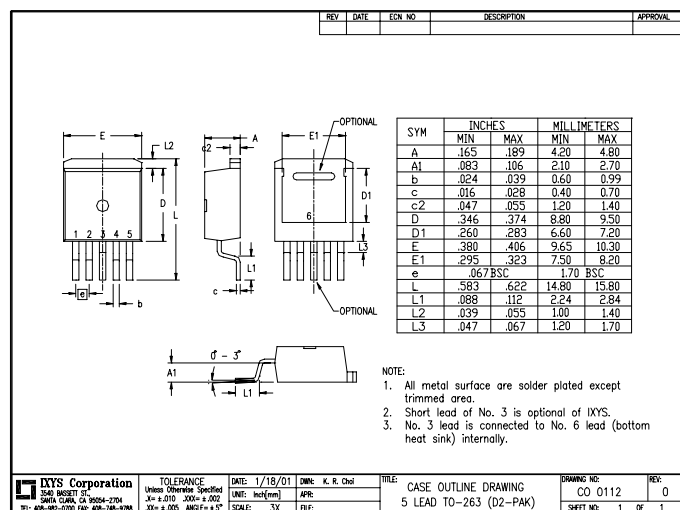
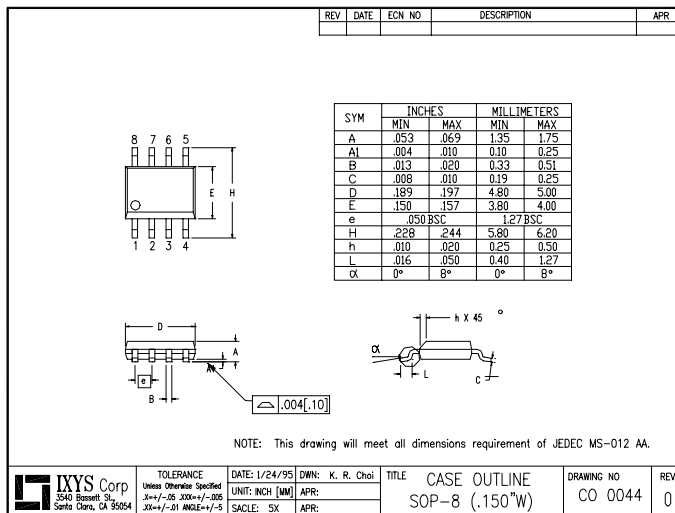
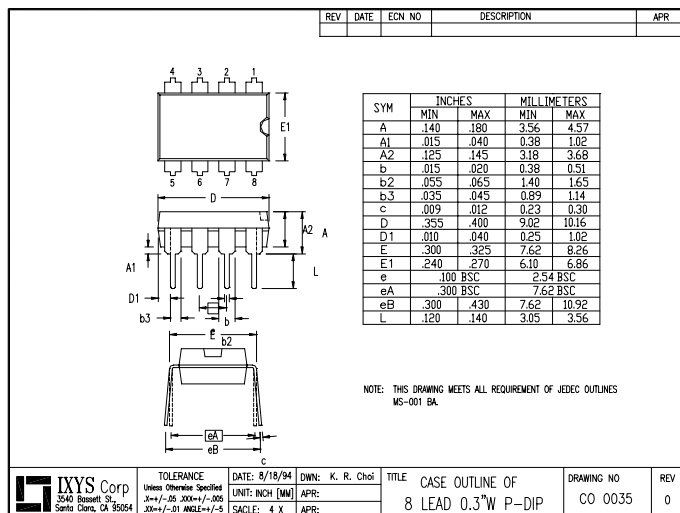
A TTL high, $V_{TTLHIGH} \approx \sim 2.4V$, or a 5V CMOS high, $V_{5VCMOSHIGH} \approx \sim 3.5V$, applied to the EN input of the circuit in Figure 28 will cause Q1 to be biased off. This results in Q1 collector being pulled up by R3 to $V_{CC} = 15V$, and provides a high voltage CMOS logic high output. The high voltage CMOS logical EN output applied to the IXDD408 EN input will enable it, allowing the gate driver to fully function as an 8 Amp output driver.

The total component cost of the circuit in Figure 28 is less than \$0.10 if purchased in quantities >1K pieces. It is recommended that the physical placement of the level translator circuit be placed close to the source of the TTL or CMOS logic circuits to maximize noise rejection.

Figure 28 - TTL to High Voltage CMOS Level Translator



Package Information



NOTE: Mounting or solder tabs on all packages are connected to ground

Ordering Information

Part Number	Package Type	Temp. Range
IXDD408PI	8-Pin PDIP	-40°C to +85°C
IXDD408SI	8-Pin SOIC	-40°C to +85°C
IXDD408YI	5-Pin TO-263	-40°C to +85°C
IXDD408CI	5-Pin TO-220	-40°C to +85°C

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