

74LVC1G175-Q100

Single D-type flip-flop with reset; positive-edge trigger

Rev. 3 — 3 October 2019

Product data sheet

1. General description

The 74LVC1G175-Q100 is a low-power, low-voltage single positive edge triggered D-type flip-flop with individual data (D) input, clock (CP) input, master reset (MR) input, and Q output. The master reset (MR) is an asynchronous active LOW input and operates independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation. The inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment. This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down. Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V).
- ±24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V ($C = 200$ pF, $R = 0$ Ω)

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | | Version |
|-------------------|-------------------|-------|---|--|---------|
| | Temperature range | Name | Description | | |
| 74LVC1G175GW-Q100 | -40 °C to +125 °C | SC-88 | plastic surface-mounted package; 6 leads | | SOT363 |
| 74LVC1G175GV-Q100 | -40 °C to +125 °C | SC-74 | plastic surface-mounted package (SC-74; TSOP6); 6 leads | | SOT457 |

4. Marking

Table 2. Marking

| Type number | Marking code [1] |
|-------------------|------------------|
| 74LVC1G175GW-Q100 | YT |
| 74LVC1G175GV-Q100 | V75 |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

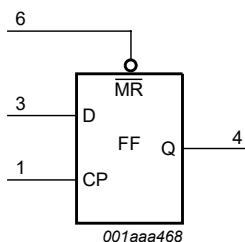


Fig. 1. Logic symbol

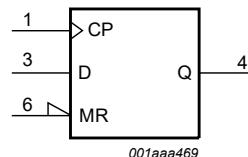


Fig. 2. IEC logic symbol

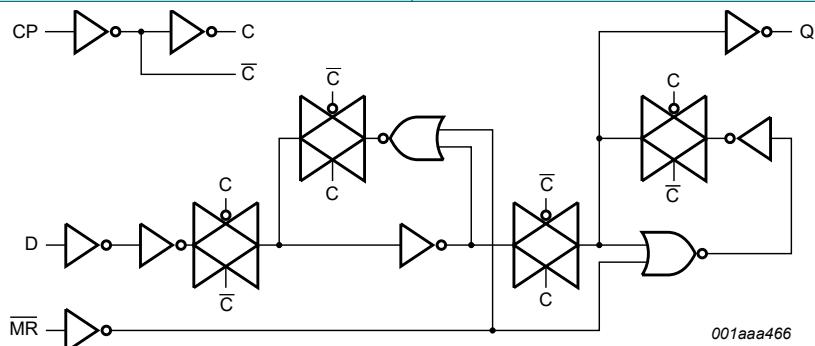


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning

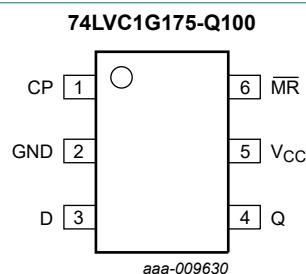


Fig. 4. Pin configuration SOT363 (SC-88) and SOT457 (SC-74)

6.2. Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|-----------------|-----|---|
| CP | 1 | clock input (LOW-to-HIGH, edge-triggered) |
| GND | 2 | ground (0 V) |
| D | 3 | data input |
| Q | 4 | output Q |
| V _{CC} | 5 | supply voltage |
| MR | 6 | master reset input (active LOW) |

7. Functional description

Table 4. Function table

H = HIGH voltage level; *h* = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;

L = LOW voltage level; *l* = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;

↑ = LOW-to-HIGH CP transition; X = don't care.

| Operating mode | Input | | | Output |
|----------------|-------|----|---|--------|
| | MR | CP | D | |
| Reset (clear) | L | X | X | L |
| Load '1' | H | ↑ | h | H |
| Load '0' | H | ↑ | l | L |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|--|------|------|-----------------------|
| V _{CC} | supply voltage | | -0.5 | +6.5 | V |
| I _{IK} | input clamping current | V _I < 0 V | -50 | - | mA |
| V _I | input voltage | | [1] | -0.5 | +6.5 |
| I _{OK} | output clamping current | V _O > V _{CC} or V _O < 0 V | - | ±50 | mA |
| V _O | output voltage | Active mode | [1] | -0.5 | V _{CC} + 0.5 |
| | | Power-down mode; V _{CC} = 0 V | [1] | -0.5 | +6.5 |
| I _O | output current | V _O = 0 V to V _{CC} | - | ±50 | mA |
| I _{CC} | supply current | | - | 100 | mA |
| I _{GND} | ground current | | -100 | - | mA |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C | [2] | - | 250 |
| T _{stg} | storage temperature | | -65 | +150 | °C |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT363 (TSSOP6) packages: P_{tot} derates linearly with 3.7 mW/K above 83 °C.

For SOT457 (TSOP6) packages: P_{tot} derates linearly with 4.1 mW/K above 89 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---------------------------------|------|-----|----------|------|
| V_{CC} | supply voltage | | 1.65 | - | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | Active mode | 0 | - | V_{CC} | V |
| | | Power-down mode; $V_{CC} = 0$ V | 0 | - | 5.5 | V |
| T_{amb} | ambient temperature | | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.65$ V to 2.7 V | - | - | 20 | ns/V |
| | | $V_{CC} = 2.7$ V to 5.5 V | - | - | 10 | ns/V |

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|---------------------------|---|----------------------|------|----------------------|------|
| $T_{amb} = -40$ °C to +85 °C | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 1.65$ V to 1.95 V | $0.65 \times V_{CC}$ | - | - | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | 1.7 | - | - | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 2.0 | - | - | V |
| | | $V_{CC} = 4.5$ V to 5.5 V | $0.7 \times V_{CC}$ | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 1.65$ V to 1.95 V | - | - | $0.35 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | - | - | 0.7 | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | - | - | 0.8 | V |
| | | $V_{CC} = 4.5$ V to 5.5 V | - | - | $0.3 \times V_{CC}$ | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | |
| | | $I_O = -100$ µA; $V_{CC} = 1.65$ V to 5.5 V | $V_{CC} - 0.1$ | - | - | V |
| | | $I_O = -4$ mA; $V_{CC} = 1.65$ V | 1.2 | 1.54 | - | V |
| | | $I_O = -8$ mA; $V_{CC} = 2.3$ V | 1.9 | 2.15 | - | V |
| | | $I_O = -12$ mA; $V_{CC} = 2.7$ V | 2.2 | 2.50 | - | V |
| | | $I_O = -24$ mA; $V_{CC} = 3.0$ V | 2.3 | 2.62 | - | V |
| | | $I_O = -32$ mA; $V_{CC} = 4.5$ V | 3.8 | 4.11 | - | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | |
| | | $I_O = 100$ µA; $V_{CC} = 1.65$ V to 5.5 V | - | - | 0.10 | V |
| | | $I_O = 4$ mA; $V_{CC} = 1.65$ V | - | 0.07 | 0.45 | V |
| | | $I_O = 8$ mA; $V_{CC} = 2.3$ V | - | 0.12 | 0.30 | V |
| | | $I_O = 12$ mA; $V_{CC} = 2.7$ V | - | 0.17 | 0.40 | V |
| | | $I_O = 24$ mA; $V_{CC} = 3.0$ V | - | 0.33 | 0.55 | V |
| | | $I_O = 32$ mA; $V_{CC} = 4.5$ V | - | 0.39 | 0.55 | V |

Single D-type flip-flop with reset; positive-edge trigger

| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit |
|-----------------|---------------------------|---|-----|-----------|---------|---------------|
| I_I | input leakage current | $V_{CC} = 0 \text{ V to } 5.5 \text{ V}; V_I = 5.5 \text{ V or GND}$ [2] | - | ± 0.1 | ± 1 | μA |
| I_{OFF} | power-off leakage current | $V_{CC} = 0 \text{ V}; V_I \text{ or } V_O = 5.5 \text{ V}$ | - | ± 0.1 | ± 2 | μA |
| I_{CC} | supply current | $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}; I_O = 0 \text{ A}; V_I = 5.5 \text{ V or GND}$ | - | 0.1 | 4 | μA |
| ΔI_{CC} | additional supply current | $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V}; V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}$ [2] | - | 5 | 500 | μA |
| C_I | input capacitance | $V_{CC} = 3.3 \text{ V}; V_I = \text{GND to } V_{CC}$ | - | 2.5 | - | pF |

 $T_{amb} = -40 \text{ }^{\circ}\text{C to } +125 \text{ }^{\circ}\text{C}$

| | | | | | | |
|-----------------|---------------------------|---|----------------------|---|----------------------|---------------|
| V_{IH} | HIGH-level input voltage | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.65 \times V_{CC}$ | - | - | V |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.7 | - | - | V |
| | | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 2.0 | - | - | V |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | $0.7 \times V_{CC}$ | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | - | - | $0.35 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | - | - | 0.7 | V |
| | | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | - | - | 0.8 | V |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | - | - | $0.3 \times V_{CC}$ | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH} \text{ or } V_{IL}$ | | | | |
| | | $I_O = -100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$ | $V_{CC} - 0.1$ | - | - | V |
| | | $I_O = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$ | 0.95 | - | - | V |
| | | $I_O = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$ | 1.7 | - | - | V |
| | | $I_O = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$ | 1.9 | - | - | V |
| | | $I_O = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$ | 2.0 | - | - | V |
| | | $I_O = -32 \text{ mA}; V_{CC} = 4.5 \text{ V}$ | 3.4 | - | - | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH} \text{ or } V_{IL}$ | | | | |
| | | $I_O = 100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$ | - | - | 0.10 | V |
| | | $I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$ | - | - | 0.70 | V |
| | | $I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$ | - | - | 0.45 | V |
| | | $I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$ | - | - | 0.60 | V |
| | | $I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$ | - | - | 0.80 | V |
| | | $I_O = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$ | - | - | 0.80 | V |
| I_I | input leakage current | $V_{CC} = 0 \text{ V to } 5.5 \text{ V}; V_I = 5.5 \text{ V or GND}$ | - | - | ± 1 | μA |
| I_{OFF} | power-off leakage current | $V_{CC} = 0 \text{ V}; V_I \text{ or } V_O = 5.5 \text{ V}$ | - | - | ± 2 | μA |
| I_{CC} | supply current | $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}; I_O = 0 \text{ A}; V_I = 5.5 \text{ V or GND}$ | - | - | 4 | μA |
| ΔI_{CC} | additional supply current | $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V}; V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}$ | - | - | 500 | μA |

[1] All typical values are measured at $T_{amb} = 25 \text{ }^{\circ}\text{C}$.[2] These typical values are measured at $V_{CC} = 3.3 \text{ V}$.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Fig. 7](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-----------|-------------------|---|------------------|-------------------------|------|-------------------|-----|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| t_{pd} | propagation delay | CP to Q; see Fig. 5 [2] | | | | | | |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | 1.5 | 4.9 | 13.4 | 1.5 | 17 | ns |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.0 | 3.1 | 7.1 | 1.0 | 9.0 | ns |
| | | $V_{CC} = 2.7 \text{ V}$ | 1.0 | 3.2 | 7.1 | 1.0 | 9.0 | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.0 | 3.1 | 5.7 | 0.5 | 7.5 | ns |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | 1.0 | 2.2 | 4.0 | 0.5 | 5.5 | ns |
| | | MR to Q; see Fig. 6 | | | | | | |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | 1.5 | 4.3 | 12.9 | 1.5 | 17 | ns |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.0 | 2.8 | 7.0 | 1.0 | 9.0 | ns |
| | | $V_{CC} = 2.7 \text{ V}$ | 1.0 | 3.0 | 7.0 | 1.0 | 9.0 | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.0 | 2.5 | 5.8 | 0.5 | 7.5 | ns |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | 1.0 | 2.0 | 4.1 | 0.5 | 5.5 | ns |
| t_w | pulse width | CP HIGH or LOW; see Fig. 5 | | | | | | |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | 6.2 | - | - | 6.2 | - | ns |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 2.7 | - | - | 2.7 | - | ns |
| | | $V_{CC} = 2.7 \text{ V}$ | 2.7 | - | - | 2.7 | - | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 2.7 | 1.3 | - | 2.7 | - | ns |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | 2.0 | - | - | 2.0 | - | ns |
| | | MR LOW; see Fig. 6 | | | | | | |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | 6.2 | - | - | 6.2 | - | ns |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 2.7 | - | - | 2.7 | - | ns |
| | | $V_{CC} = 2.7 \text{ V}$ | 2.7 | - | - | 2.7 | - | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 2.7 | 1.6 | - | 2.7 | - | ns |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | 2.0 | - | - | 2.0 | - | ns |
| t_{rec} | recovery time | MR; see Fig. 6 | | | | | | |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | 1.9 | - | - | 1.9 | - | ns |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.4 | - | - | 1.4 | - | ns |
| | | $V_{CC} = 2.7 \text{ V}$ | 1.3 | - | - | 1.3 | - | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.2 | 0.4 | - | 1.2 | - | ns |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | 1.0 | - | - | 1.0 | - | ns |
| t_{su} | set-up time | D to CP; see Fig. 5 | | | | | | |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | 2.9 | - | - | 2.9 | - | ns |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.7 | - | - | 1.7 | - | ns |
| | | $V_{CC} = 2.7 \text{ V}$ | 1.7 | - | - | 1.7 | - | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.3 | 0.5 | - | 1.3 | - | ns |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | 1.1 | - | - | 1.1 | - | ns |

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|---|------------------|---------|-----|-------------------|-----|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| t _h | hold time | D to CP; see Fig. 5 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 0.0 | - | - | 0.0 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0.3 | - | - | 0.3 | - | ns |
| | | V _{CC} = 2.7 V | 0.5 | - | - | 0.5 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.2 | 0.2 | - | 1.2 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 0.5 | - | - | 0.5 | - | ns |
| f _{max} | maximum frequency | CP; see Fig. 5 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 80 | 125 | - | 80 | - | MHz |
| | | V _{CC} = 2.3 V to 2.7 V | 175 | - | - | 175 | - | MHz |
| | | V _{CC} = 2.7 V | 175 | - | - | 175 | - | MHz |
| | | V _{CC} = 3.0 V to 3.6 V | 175 | 300 | - | 175 | - | MHz |
| | | V _{CC} = 4.5 V to 5.5 V | 200 | - | - | 200 | - | MHz |
| C _{PD} | power dissipation capacitance | V _I = GND to V _{CC} ; V _{CC} = 3.3 V [3] | - | 14 | - | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

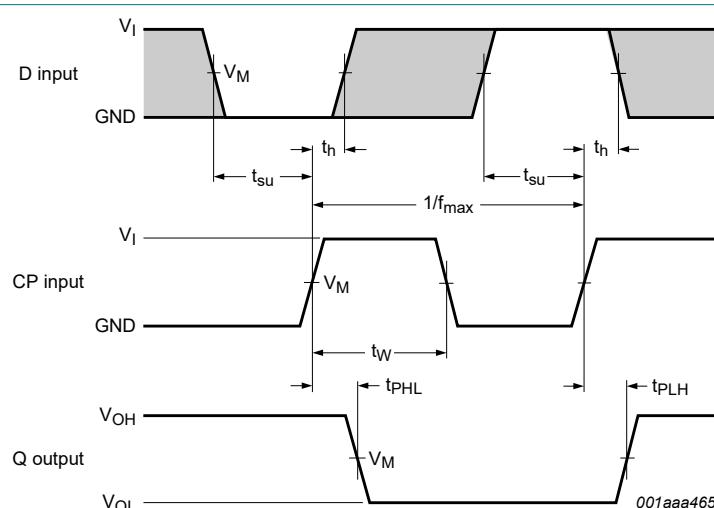
C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$$\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of the outputs.}$$

11.1. Waveforms



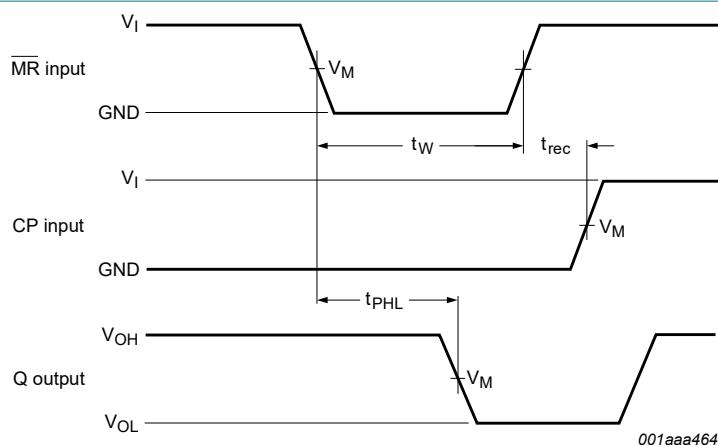
Measurement points are given in Table 9.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The clock input (CP) to output (Q) propagation delays, the clock pulse width, the D to CP set-up, the CP to D hold times, and the maximum clock pulse frequency

Single D-type flip-flop with reset; positive-edge trigger



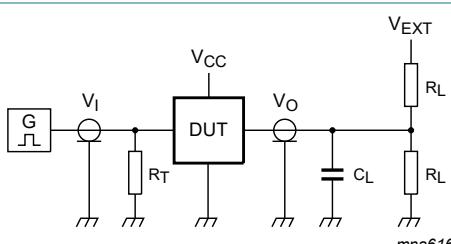
Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. The master reset (MR) input to output (Q) propagation delays, the master reset pulse width, and the MR to CP recovery time

Table 9. Measurement points

| Supply voltage | Input | Output |
|------------------|---------------------|---------------------|
| V_{CC} | V_M | V_M |
| 1.65 V to 1.95 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 2.3 V to 2.7 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 2.7 V | 1.5 V | 1.5 V |
| 3.0 V to 3.6 V | 1.5 V | 1.5 V |
| 4.5 V to 5.5 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Input | Load | V_{EXT} |
|------------------|----------|---------------|-----------|
| V_{CC} | V_I | $t_r = t_f$ | C_L |
| 1.65 V to 1.95 V | V_{CC} | ≤ 2.0 ns | 30 pF |
| 2.3 V to 2.7 V | V_{CC} | ≤ 2.0 ns | 30 pF |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF |
| 4.5 V to 5.5 V | V_{CC} | ≤ 2.5 ns | 50 pF |

12. Package outline

Plastic surface-mounted package; 6 leads

SOT363

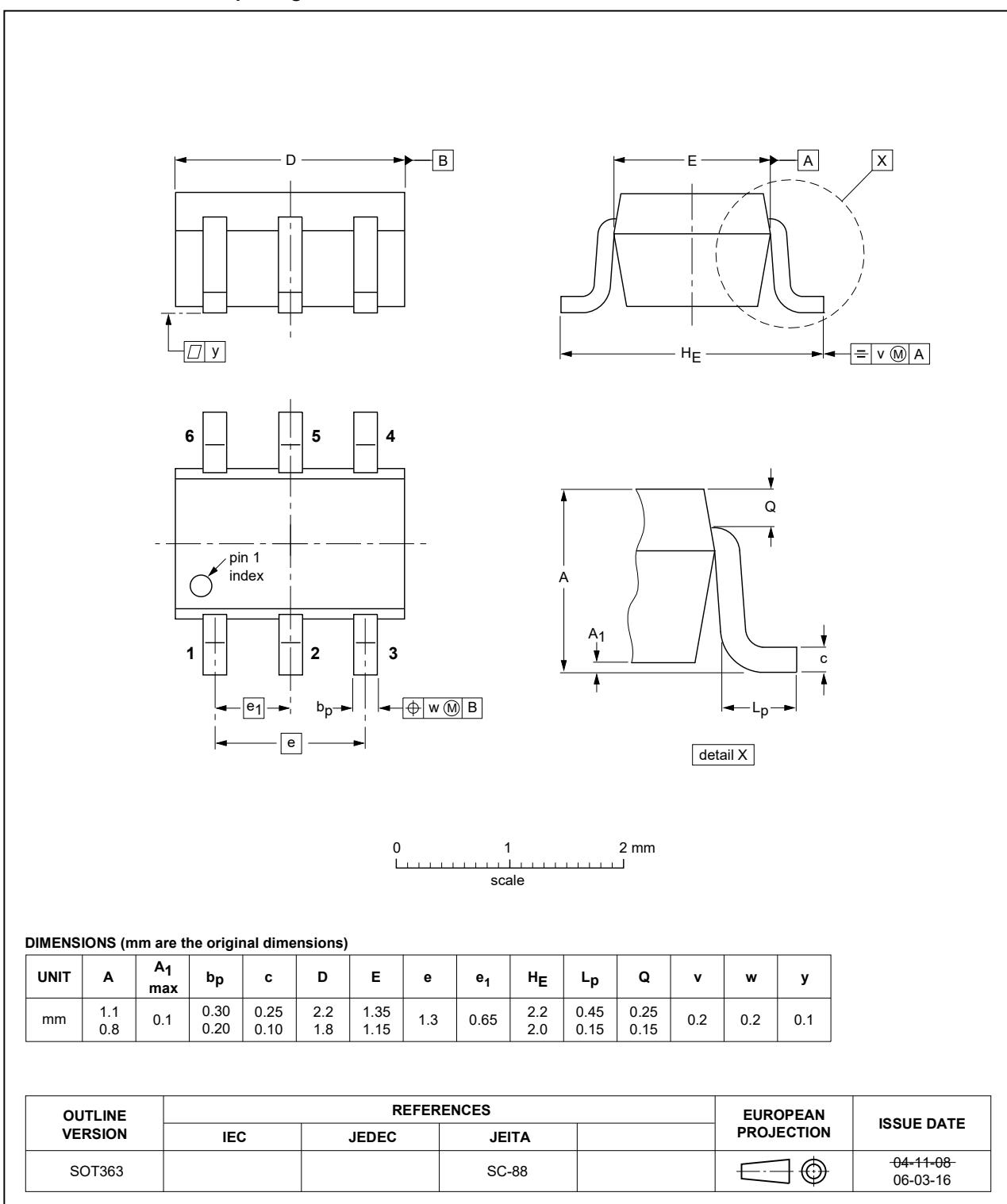


Fig. 8. Package outline SOT363 (SC-88)

Plastic, surface-mounted package (SC-74; TSOP6); 6 leads

SOT457

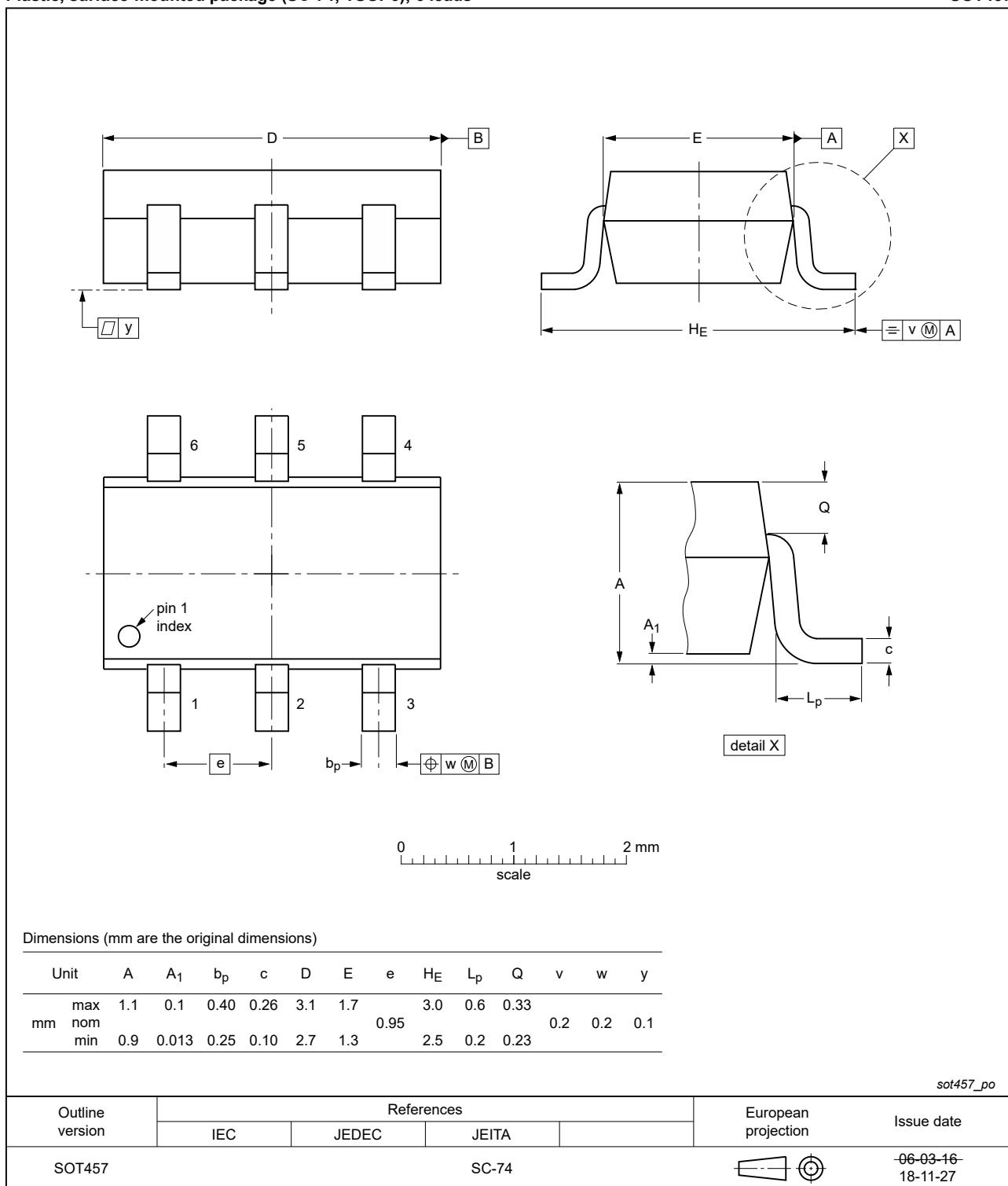


Fig. 9. Package outline SOT457 (SC-74)

13. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MIL | Military |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------------|--|--------------------|---------------|---------------------|
| 74LVC1G175_Q100 v.3 | 20191003 | Product data sheet | - | 74LVC1G175_Q100 v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Table 5: Derating values for P_{tot} total power dissipation updated. Package outline drawing SOT457 (SC-74) updated. | | | |
| 74LVC1G175_Q100 v.2 | 20161209 | Product data sheet | - | 74LVC1G175_Q100 v.1 |
| Modifications: | <ul style="list-style-type: none"> Table 7: The maximum limits for leakage current and supply current have changed. | | | |
| 74LVC1G175_Q100 v.1 | 20131115 | Product data sheet | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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