Dual 20V N-Channel Power MOSFET

GWS9293

The GWS9293 is a dual 20V, 16mΩ, N-channel power MOSFET used for Li ion battery protection. It is offered in a 2mmx2mm MLPD with a very low thickness profile, 1mm maximum thickness. The device has extremely high power density, reducing the board size of Li-ion battery power system. Designed for handheld devices with a high level of ESD protection.

PRODUCT SUMMARY			
$V_{(BR)DSS}$	I_D = 250µA	20V	Minimum
$r_{DS(ON)}$	V_{GS} = 4.5V	16mΩ	Typical

Features

- Low $r_{DS(ON)}$ in a small footprint
- Ultra low gate charge and figure of merit
- MLPD 2mmx2mm package
- Low thermal resistance

Applications

- Li-ion battery protection
- Portable devices, cell phones, PDA
- Rated for short-circuit and overcurrent protection
- Integrated gate diodes provide ESD protection of 2.5kV HBM

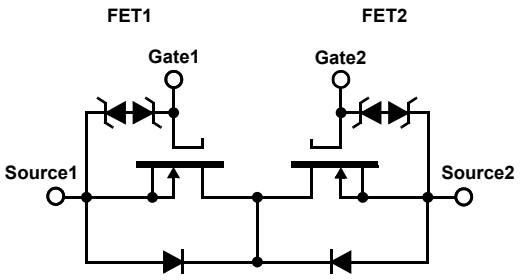

FIGURE 1. EQUIVALENT CIRCUIT

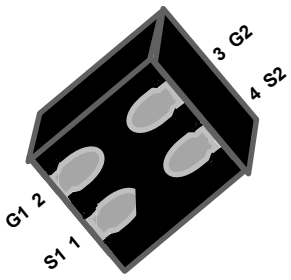

FIGURE 2. MLPD BOTTOM SIDE

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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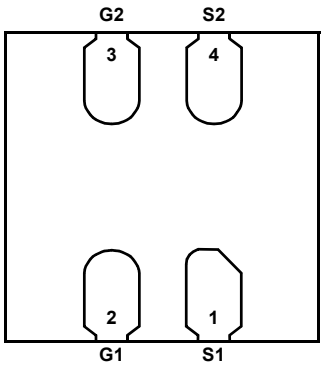
Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)
GWS9293	93	-55 to +150	4 Ld QFN

Pin Configuration

GWS9293
(4 LD QFN)
BOTTOM VIEW



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1	S1	Source of FET1
2	G1	Gate of FET1
3	G2	Gate of FET2
4	S2	Source of FET2

Absolute Maximum Ratings (Note 1)

Drain-to-Source Voltage (V_{DS}) 20V
Gate-to-Source Voltage (V_{GS}) . . . . . ±12V
Drain Current (I_D) (Note 2)
T_A = +25°C . . . . . 9.4A (10s), 6.0A (Steady State)
T_A = +70°C . . . . . 7.5A (10s), 4.8A (Steady State)
Drain Current ($Rthj_{Foot}$)
T_F = +25°C . . . . . 14.1A (Steady State)
Pulsed Drain Current (I_{DM}) 60A
ESD Rating
Human Body Model 2.5kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JF} (°C/W)
t ≤10s.	35	
Steady State	85	16

Maximum Power Dissipation (P_D) (Note 2)
T_A = +25°C . . . . . 3.6W (10s) 1.47W (Steady State)
T_A = +70°C . . . . . 2.29W (10s) 0.94W (Steady State)
Junction and Storage Temperature Range (T_J, T_{stg}) . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. T_J = +25°C unless otherwise noted.
2. Surface mounted on FR4 board.

Electrical Characteristics T_J = +25°C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 3)	TYP (Note 4)	MAX (Note 3)	UNIT
STATIC						
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250µA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0V, V_{DS} = 20V			1	µA
I_{GSS}	Gate Body Leakage	V_{DS} = 0V V_{GS} = ±8V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1mA	0.5	0.8	1.5	V
$r_{DS(ON)}$	Drain-to-Source On-State Resistance (Note 5) (per MOSFET)	V_{GS} = 4.5V, I_D = 3A	11	16	17	mΩ
		V_{GS} = 4.0V, I_D = 3A	11	17	19	mΩ
		V_{GS} = 3.1V, I_D = 3A	12	19	22	mΩ
		V_{GS} = 2.5V, I_D = 3A	15	22	28	mΩ
$r_{SS(ON)}$	Source-to-Source On-State Resistance (Note 5) (both MOSFETs in series)	V_{GS} = 4.5V, I_{SS} = 3A	22	31	35	mΩ
		V_{GS} = 4.0V, I_{SS} = 3A	23	33	37	mΩ
		V_{GS} = 3.1V, I_{SS} = 3A	24	38	44	mΩ
		V_{GS} = 2.5V, I_{SS} = 3A	30	44	55	mΩ
V_{SD}	Source-to-Drain Diode Voltage	V_{GS} = 0, I_S = 6A	0.5	0.8	1	V
DYNAMIC						
Q_g	Total Gate Charge	V_{DS} = 16V, I_D = 6.0A, V_{GS} = 4.0V		3.5		nC
C_{iss}	Input Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1MHz		400		pF
C_{oss}	Output Capacitance			120		pF
C_{rss}	Reverse Transfer Capacitance			100		pF

NOTES:

3. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design..
4. Typical values are for T_A = +25°C.
5. Good Kelvin measurement required.

Test Circuit Examples for Measuring FET1 Key Parameters

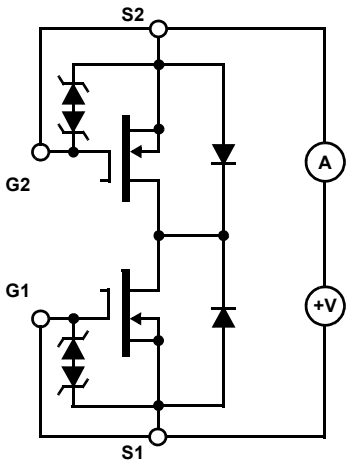


FIGURE 3. I_{SSS} TEST CIRCUIT

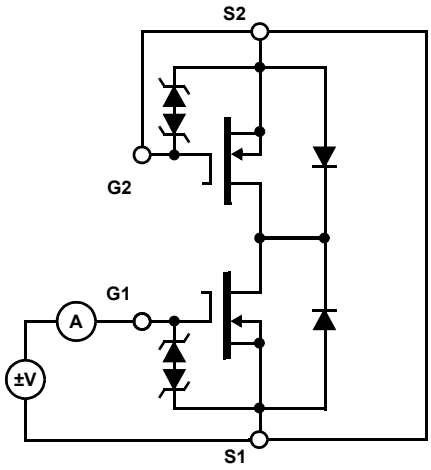


FIGURE 4. I_{GSS} TEST CIRCUIT

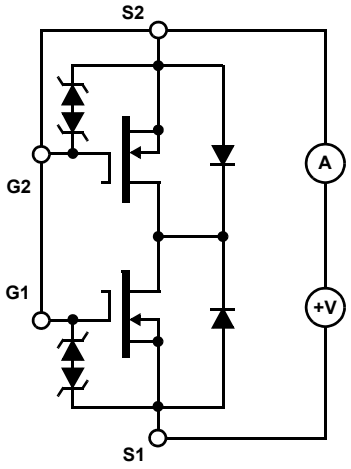


FIGURE 5. $V_{GS(th)}$ TEST CIRCUIT

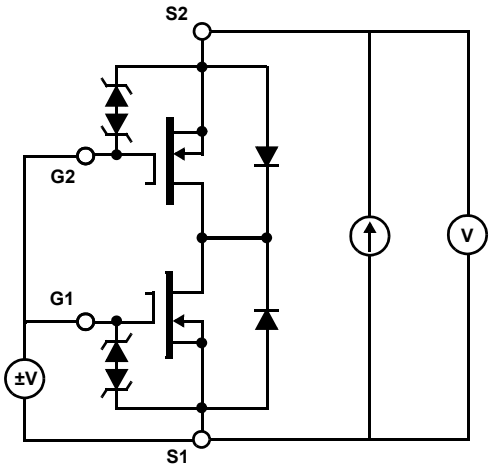


FIGURE 6. $r_{SS(ON)}$ TEST CIRCUIT

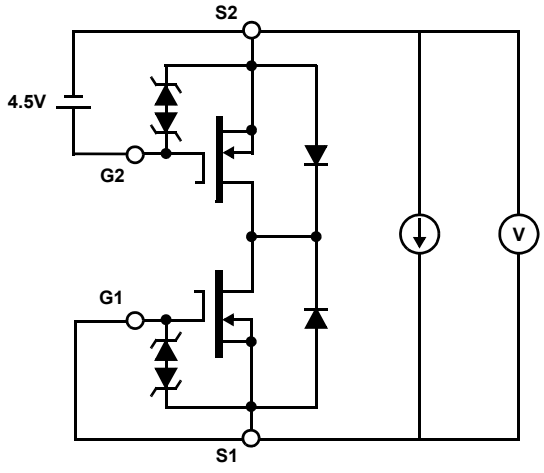


FIGURE 7. V_{FS-S} TEST CIRCUIT

Typical Performance Curves

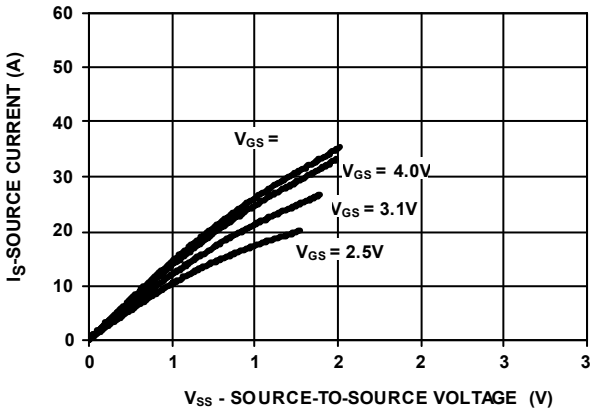


FIGURE 8. OUTPUT CHARACTERISTICS

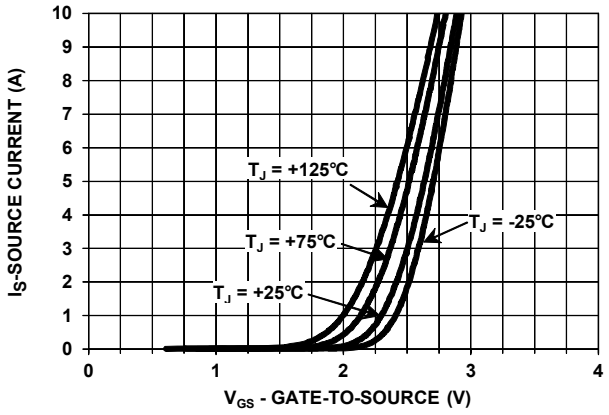


FIGURE 9. TRANSFER CHARACTERISTICS

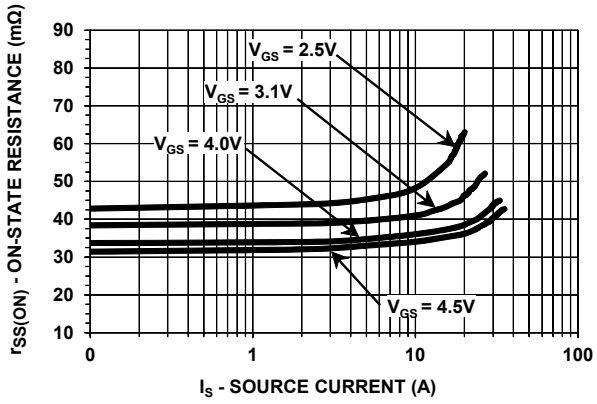


FIGURE 10. SOURCE-TO-SOURCE ON-STATE RESISTANCE vs SOURCE CURRENT

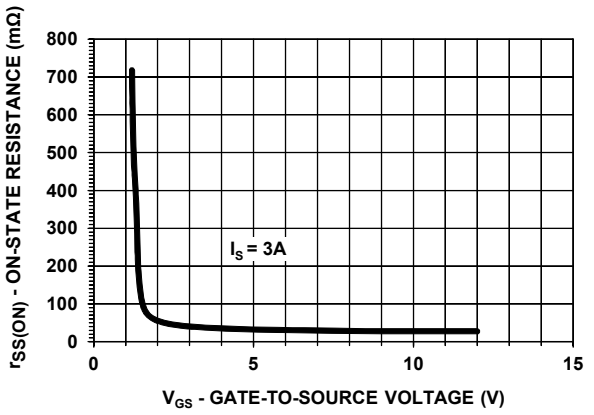


FIGURE 11. SOURCE-TO-SOURCE ON-STATE RESISTANCE vs GATE-TO-SOURCE VOLTAGE

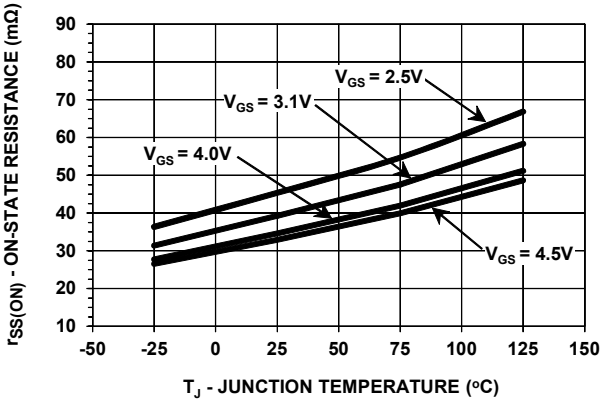


FIGURE 12. SOURCE-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

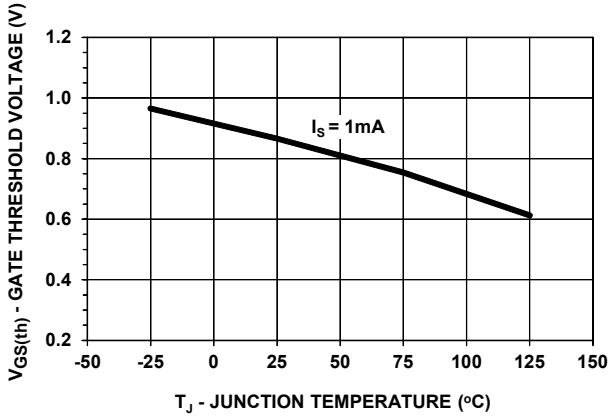


FIGURE 13. GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

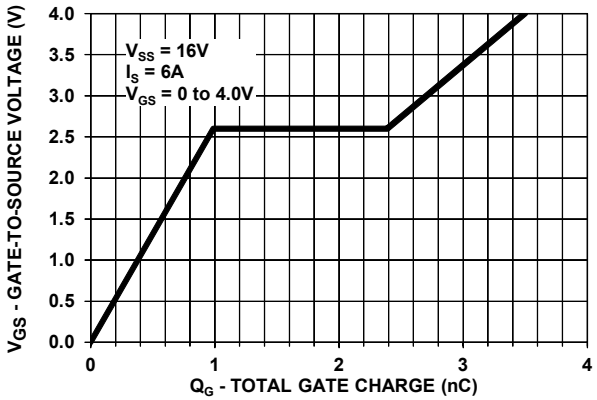


FIGURE 14. GATE CHARGE

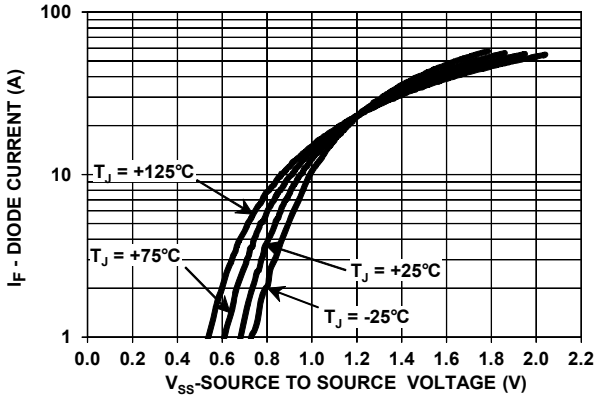


FIGURE 15. SOURCE-TO-SOURCE DIODE FORWARD VOLTAGE

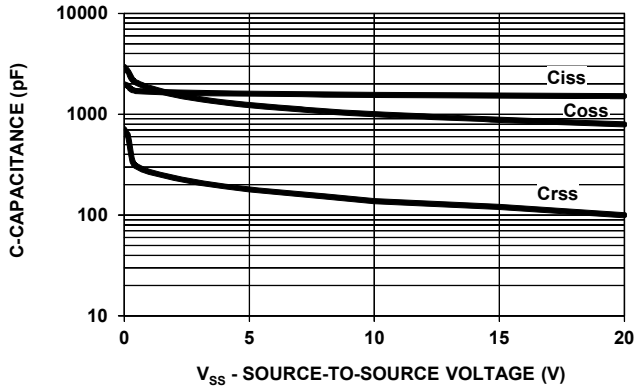


FIGURE 16. CAPACITANCE

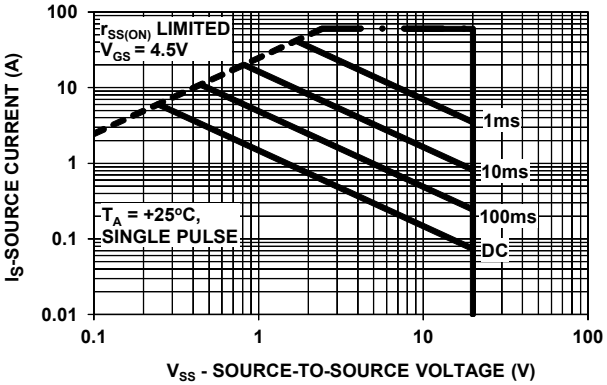


FIGURE 17. MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

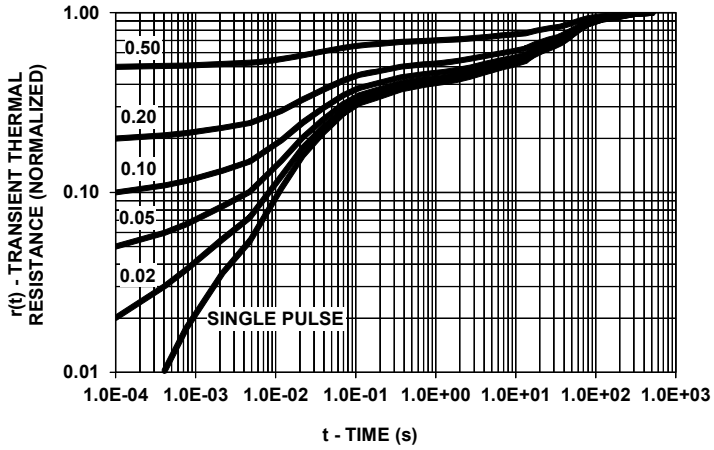


FIGURE 18. TRANSIENT THERMAL RESPONSE, JUNCTION-TO-AMBIENT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 21, 2015	FN8785.1	Added “Note 1. T_J = +25°C unless otherwise noted.” to Abs Max on page 3.
October 30, 2015	FN8785.0	Initial release.

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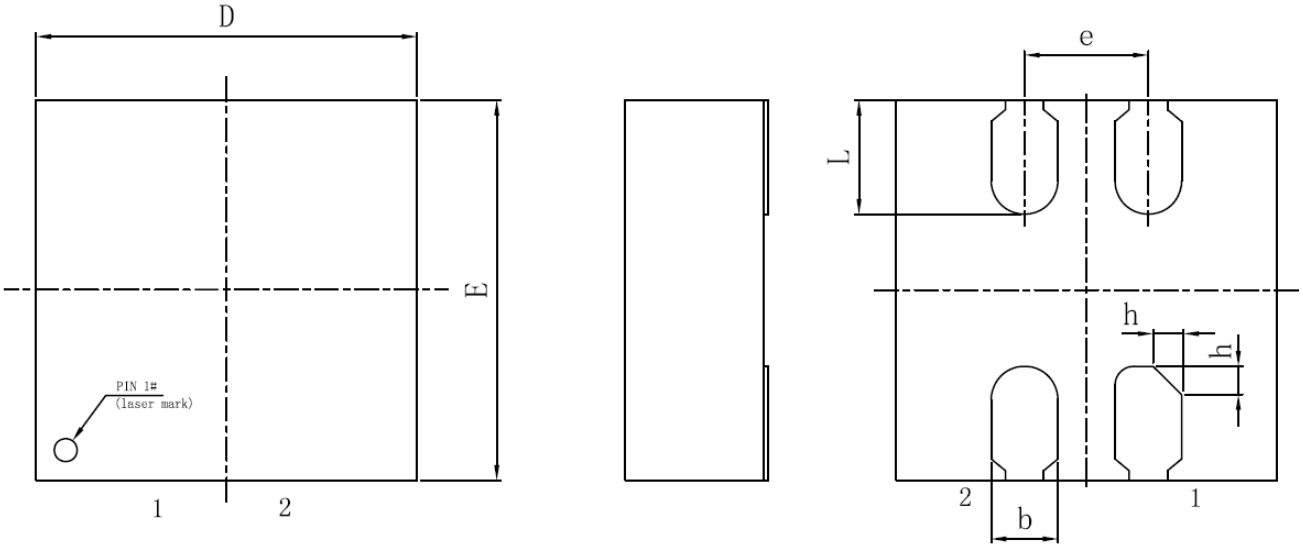
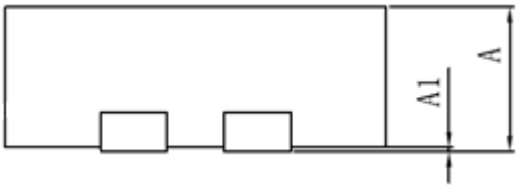
Package Outline and Dimensions



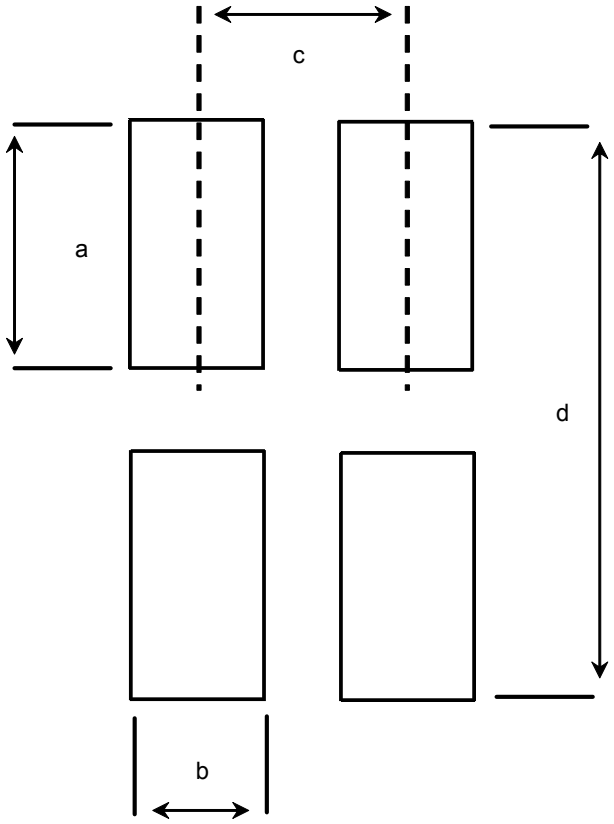


Pin	Node
1	Source 1
2	Gate 1
3	Gate 2
4	Source 2

Symbol	Min	Nom	Max
A	0.70		1.00
A1		0.02	0.05
b	0.275		0.400
D	2.00 BSC		
E	2.00 BSC		
e	0.65 BSC		
L	0.55	0.60	0.65
h	0.10	0.15	0.20

All dimensions in mm

Mounting Pad Layout and Dimensions



Symbol	Min	Nom	Max
a	0.788	0.838	0.888
b	0.358	0.381	0.404
c		0.65 BSC	
d	2.22	2.365	2.50

All dimensions in mm