

- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$
- 3-State Outputs Drive Bus Lines or Buffer-Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- High-Impedance State During Power Up and Power Down
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (N)

### description

This octal buffer and line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the SN64BCT240 and SN64BCT241, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ( $\overline{OE}$ ) inputs, and complementary OE and  $\overline{OE}$  inputs.

The SN64BCT244 is organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

The SN64BCT244 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DW OR N PACKAGE  
(TOP VIEW)

1	20	$V_{CC}$
1A1	2	$\overline{OE}$
2Y4	3	1Y1
1A2	4	2A4
2Y3	5	1Y2
1A3	6	2A3
2Y2	7	1Y3
1A4	8	2A2
2Y1	9	1Y4
GND	10	2A1

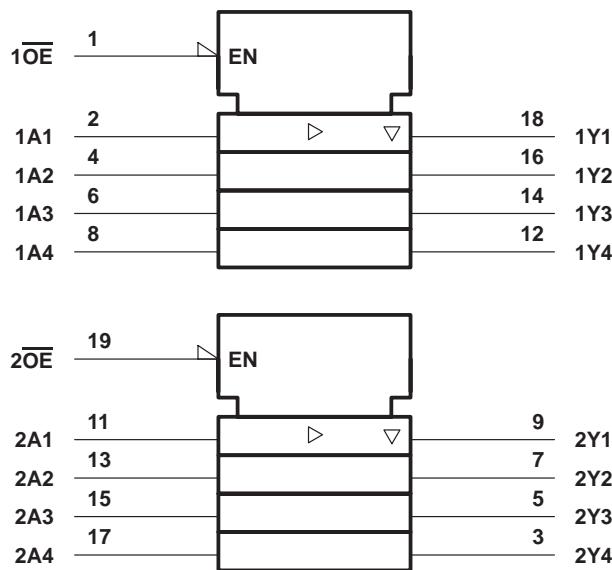
FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

**SN64BCT244**  
**OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

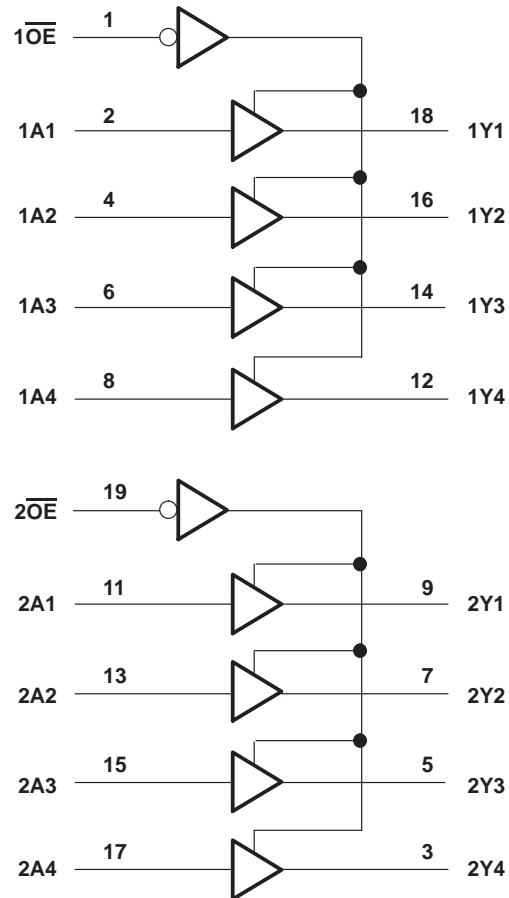
SCBS027A - FEBRUARY 1989 - REVISED JANUARY 1994

**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$ .....	-0.5 V to $V_{CC}$
Current into any output in the low state, $I_O$ .....	128 mA
Operating free-air temperature range .....	-40°C to 85°C
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage		2		V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-15	mA
$I_{OL}$	Low-level output current			64	mA
$T_A$	Operating free-air temperature	-40	85		°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
	$V_{CC} = 4.5$ V,	$I_I = -18$ mA					
$V_{OH}$	$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA		2.4	3.3		V
		$I_{OH} = -15$ mA		2	3.1		
$V_{OL}$	$V_{CC} = 4.5$ V,	$I_{OL} = 64$ mA		0.42	0.55		V
$I_I$	$V_{CC} = 5.5$ V,	$V_I = 7$ V				0.1	mA
$I_{IH}$	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V				20	µA
$I_{IL}$	$V_{CC} = 5.5$ V,	$V_I = 0.5$ V				-1	mA
$I_{OZ}$	$V_{CC} = 0$ to $2.3$ V (power up)	$V_O = 2.7$ V or $0.5$ V, $\overline{OE}$ at $0.8$ V		$\pm 50$		$\pm 50$	µA
	$V_{CC} = 1.8$ V to $0$ (power down)						
$I_{OZH}$	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V				50	µA
$I_{OZL}$	$V_{CC} = 5.5$ V,	$V_O = 0.5$ V				-50	µA
$I_{OS}^†$	$V_{CC} = 5.5$ V,	$V_O = 0$		-100		-225	mA
$I_{CCH}$	$V_{CC} = 5.5$ V,	Output open		23	40		mA
$I_{CCL}$	$V_{CC} = 5.5$ V,	Output open		53	80		mA
$I_{CCZ}$	$V_{CC} = 5.5$ V,	Output open		4	10		mA

† All typical values are at  $V_{CC} = 5$  V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

**switching characteristics (see Note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $C_L = 50$ pF, $R1 = 500$ Ω, $R2 = 500$ Ω, $T_A = 25^\circ C$			UNIT	
			MIN	TYP	MAX		
$t_{PLH}$	A	Y	1.2	2.5	4.4	0.9	ns
			1.7	3.2	5	1.4	
$t_{PHL}$	$\overline{OE}$	Y	2	5.7	7.8	2	ns
			2	5.9	8.1	2	
$t_{PZH}$	$\overline{OE}$	Y	2	5.4	6.7	2	ns
			2	6.1	7.6	2	
$t_{PZL}$	$\overline{OE}$	Y	2	5.9	8.1	2	ns
			2	6.1	7.6	2	
$t_{PHZ}$	$\overline{OE}$	Y	2	5.4	6.7	2	ns
			2	6.1	7.6	2	
$t_{PLZ}$	$\overline{OE}$	Y	2	5.9	8.1	2	ns
			2	6.1	7.6	2	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN64BCT244DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN64BCT244DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN64BCT244DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN64BCT244NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN64BCT244NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN64BCT244NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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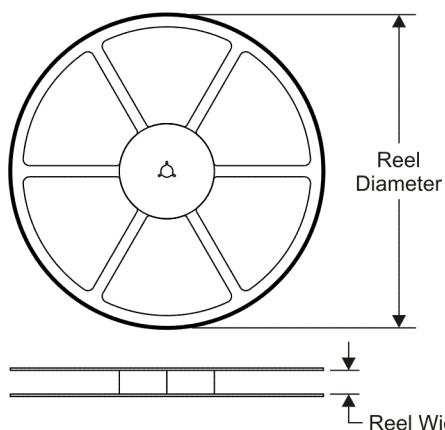
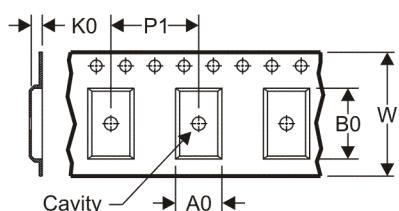
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## PACKAGE OPTION ADDENDUM

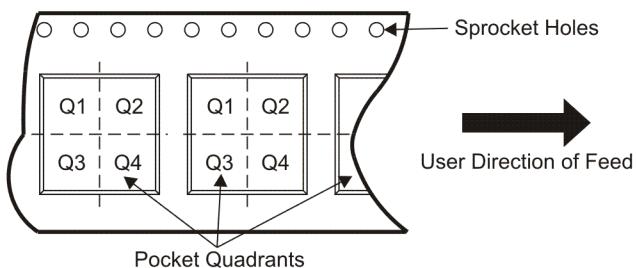
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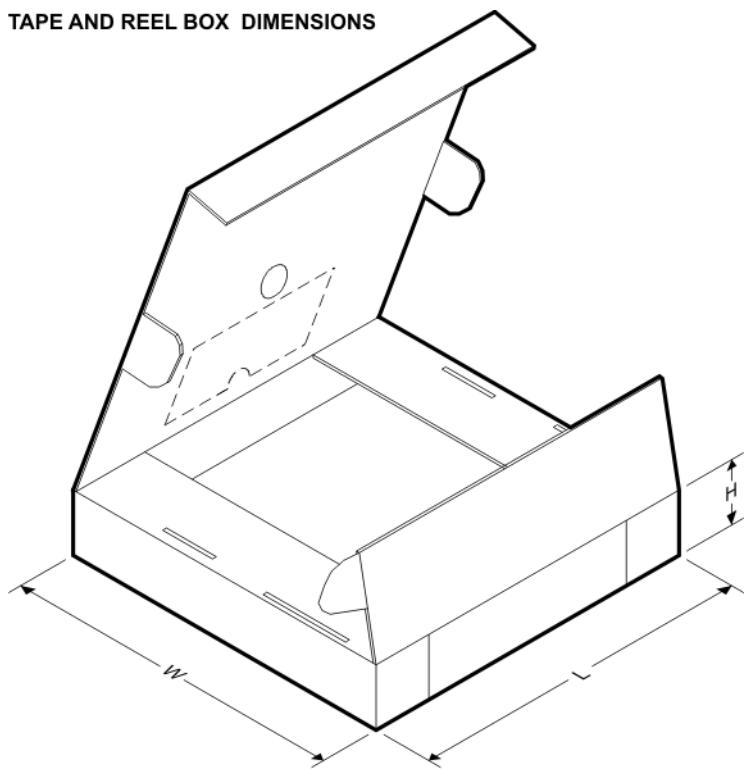
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN64BCT244NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1

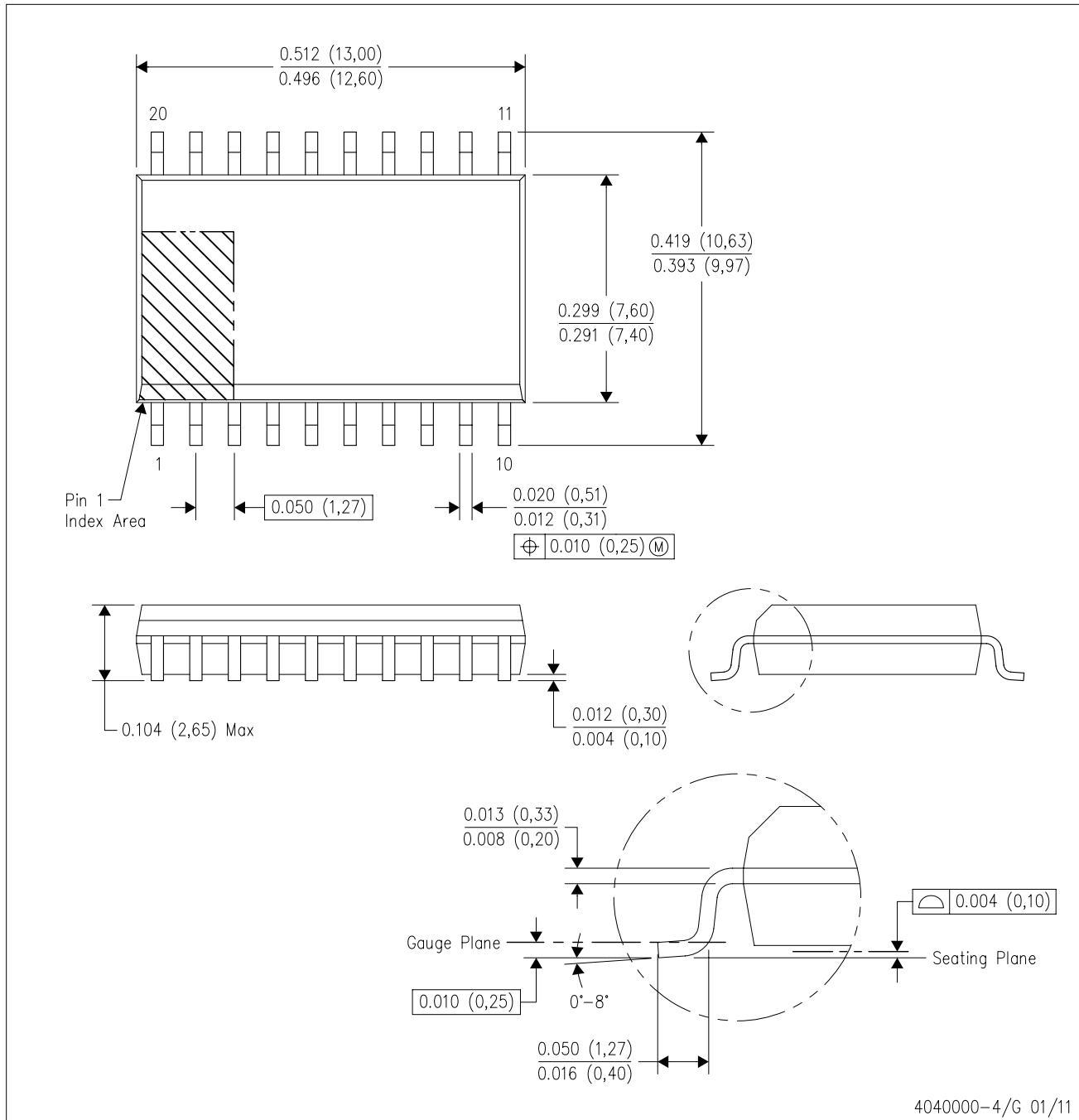
**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN64BCT244NSR	SO	NS	20	2000	346.0	346.0	41.0

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

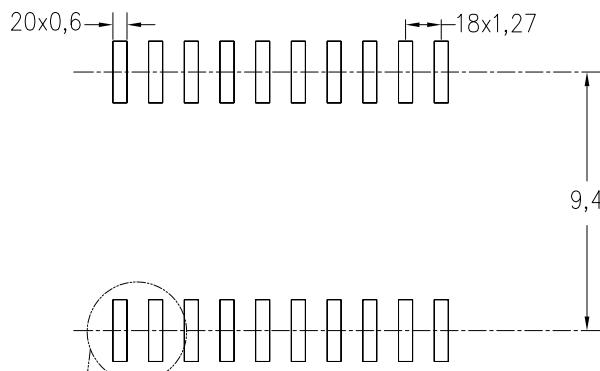
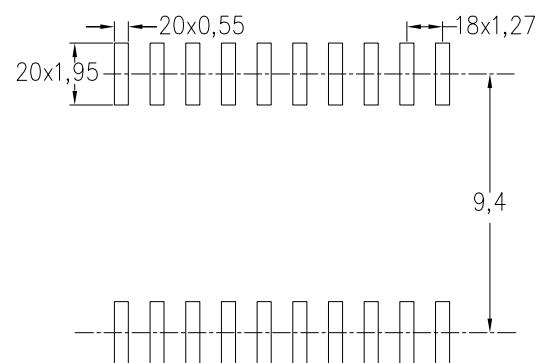


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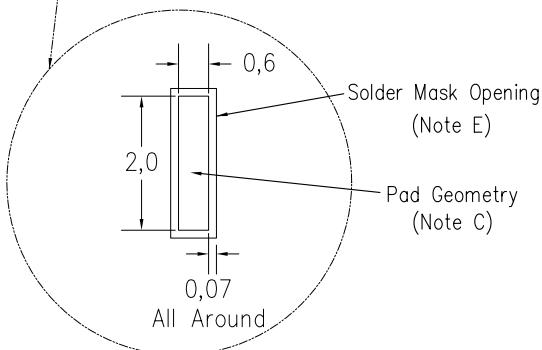
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)

Non Solder Mask Define Pad



4209202-4/E 07/11

NOTES:

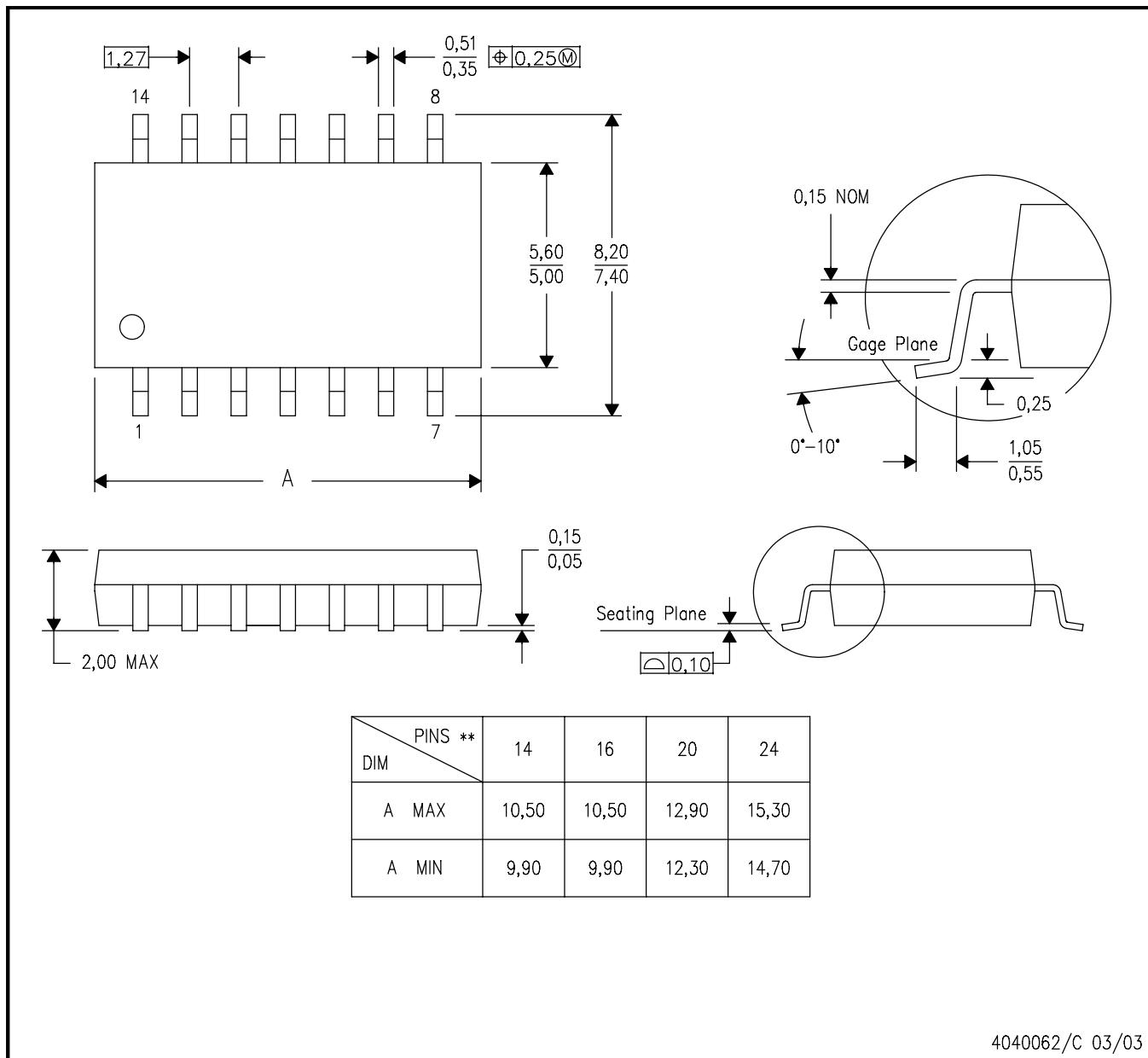
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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