

# NVTFS4824N

## MOSFET – Power, Single N-Channel 30 V, 4.7 mΩ, 46 A



### Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVTFS4824NWF – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	30	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	$I_D$	46	A
		33	
Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)	$P_D$	21	W
		11	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, & 4)	$I_D$	18.2	A
		12.8	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	$P_D$	3.2	W
		1.6	
Pulsed Drain Current	$I_{DM}$	402	A
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to 175	°C
Source Current (Body Diode)	$I_S$	21	A
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}$ , $V_{DD} = 50\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_{L(pk)} = 38\text{ A}$ , $L = 0.1\text{ mH}$ , $R_G = 25\text{ }\Omega$ )	$E_{AS}$	72	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) – Steady State (Notes 2 and 3)	$R_{\Psi J-mb}$	7.2	°C/W
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	47	

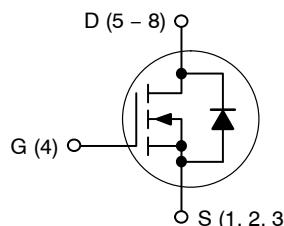
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2.  $\Psi$  is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

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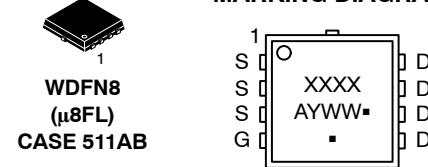
[www.onsemi.com](http://www.onsemi.com)

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
30 V	4.7 mΩ @ 10 V 7.5 mΩ @ 4.5 V	46 A

### N-Channel



### MARKING DIAGRAM



XXXX = Specific Device Code

A = Assembly Location

Y = Year

WW = Work Week

▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVTFS4824N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 30 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 125°C		10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.5		2.5	V
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 23 A		3.5	4.7	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 23 A		5.7	7.5	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 1.5 V, I <sub>D</sub> = 20 A		56		S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 12 V		1740		pF
Output Capacitance	C <sub>oss</sub>			360		
Reverse Transfer Capacitance	C <sub>rss</sub>			200		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 23 A		14		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			1.6		
Gate-to-Source Charge	Q <sub>GS</sub>			5.3		
Gate-to-Drain Charge	Q <sub>GD</sub>			5.5		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 23 A		29		nC

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A, R <sub>G</sub> = 3.0 Ω		12		ns
Rise Time	t <sub>r</sub>			27		
Turn-Off Delay Time	t <sub>d(off)</sub>			20		
Fall Time	t <sub>f</sub>			6		

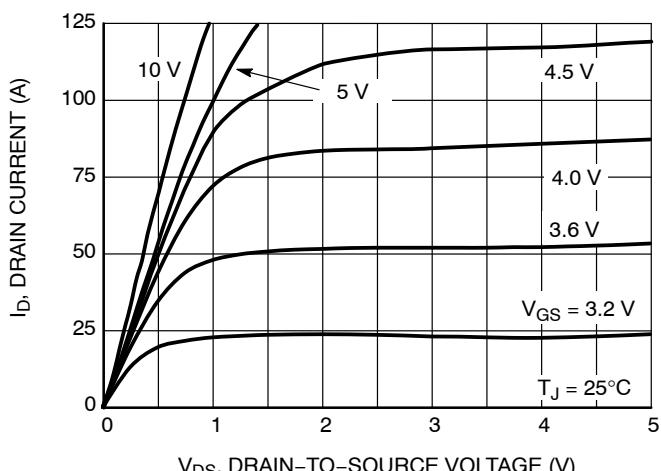
### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 23 A	T <sub>J</sub> = 25°C		0.81	1.1	V
			T <sub>J</sub> = 125°C		0.69		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 23 A			19		ns
Charge Time	t <sub>a</sub>				9.1		
Discharge Time	t <sub>b</sub>				9.6		
Reverse Recovery Charge	Q <sub>RR</sub>				8.8		nC

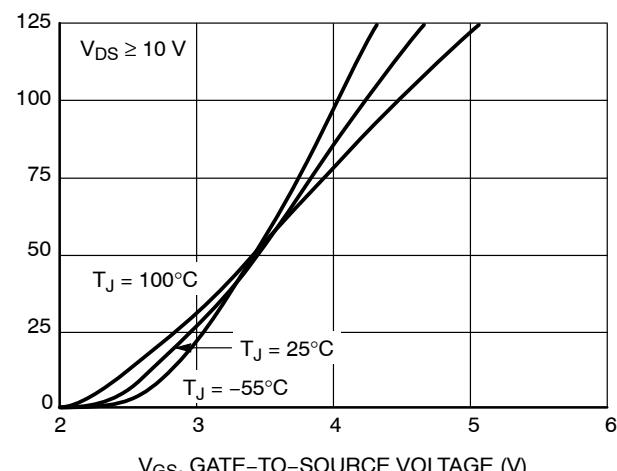
5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

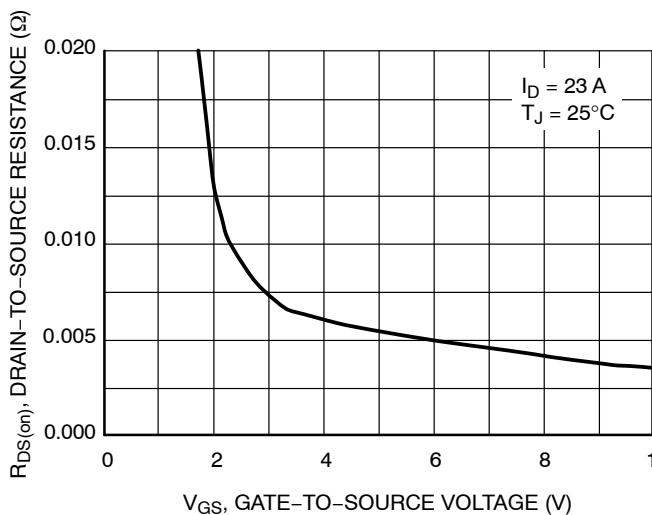
**TYPICAL CHARACTERISTICS**



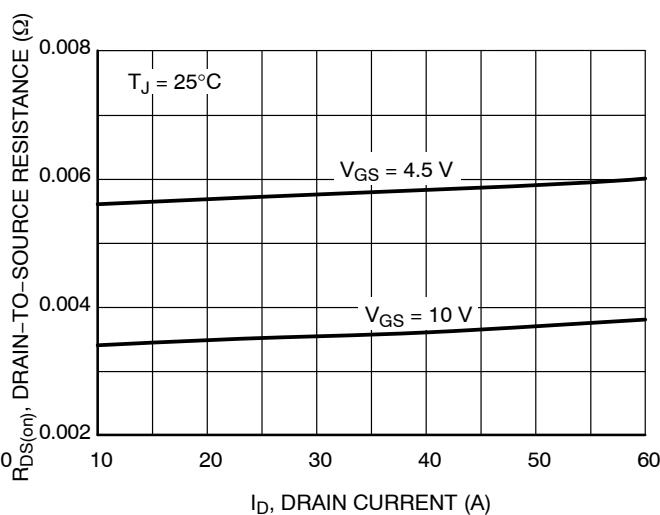
**Figure 1. On-Region Characteristics**



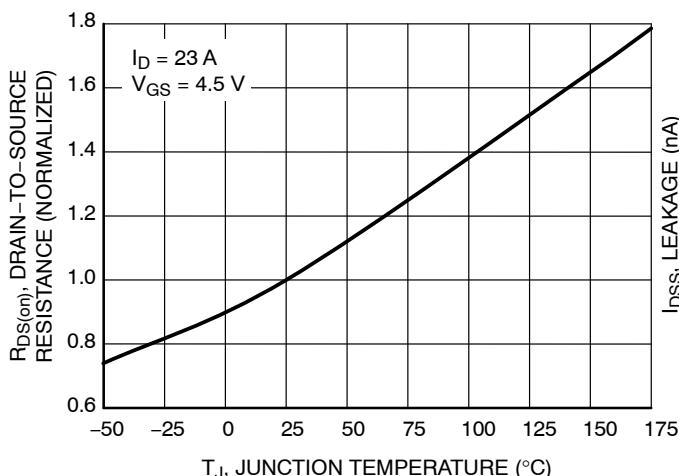
**Figure 2. Transfer Characteristics**



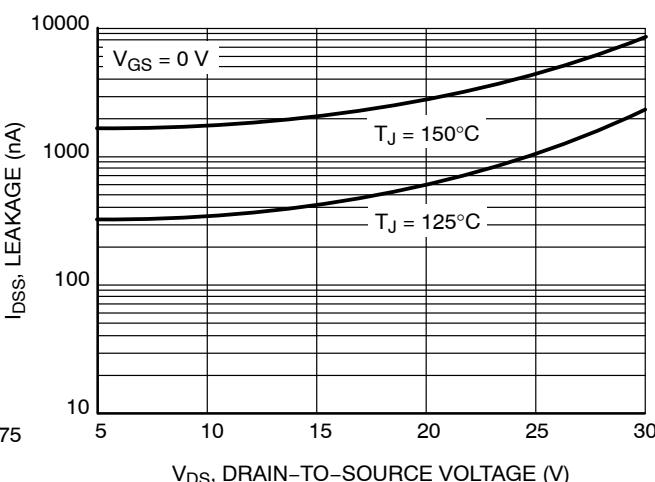
**Figure 3. On-Resistance vs. Gate-to-Source Voltage**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**

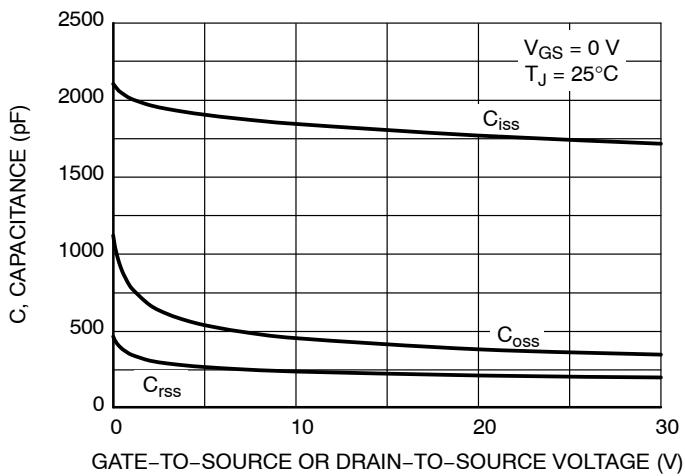


**Figure 5. On-Resistance Variation with Temperature**

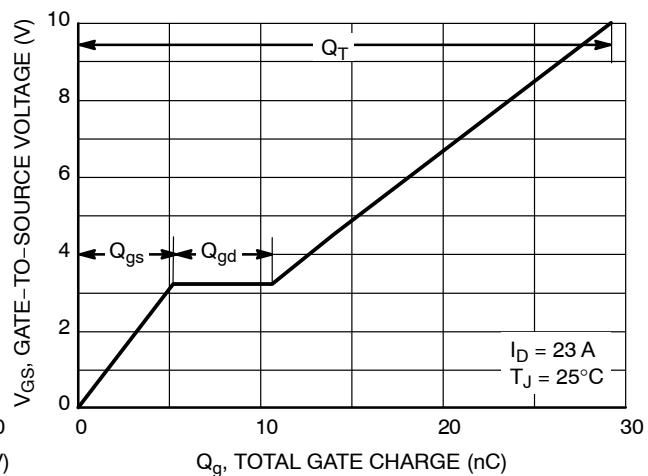


**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

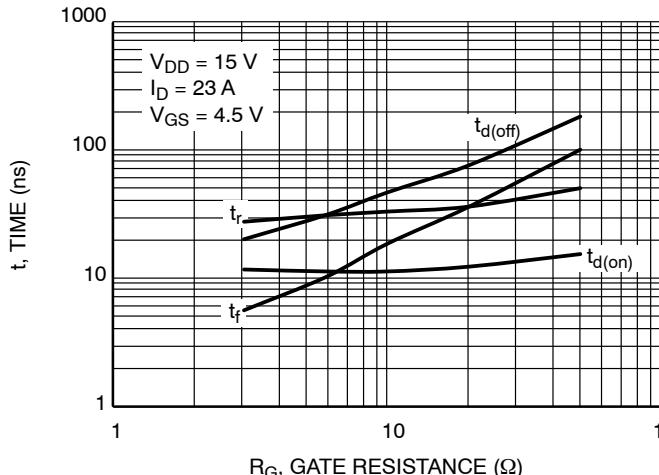
**TYPICAL CHARACTERISTICS**



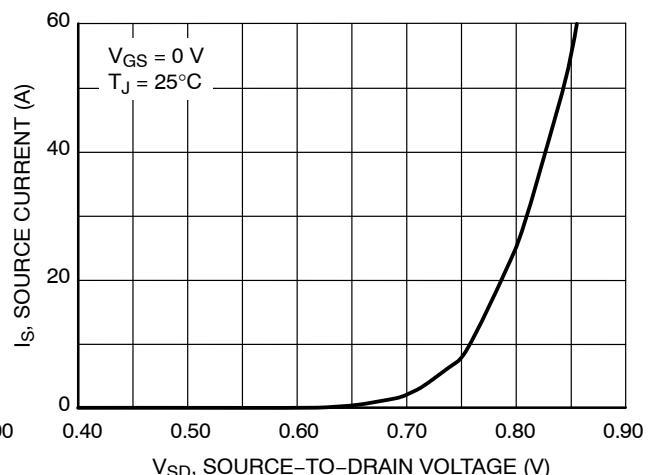
**Figure 7. Capacitance Variation**



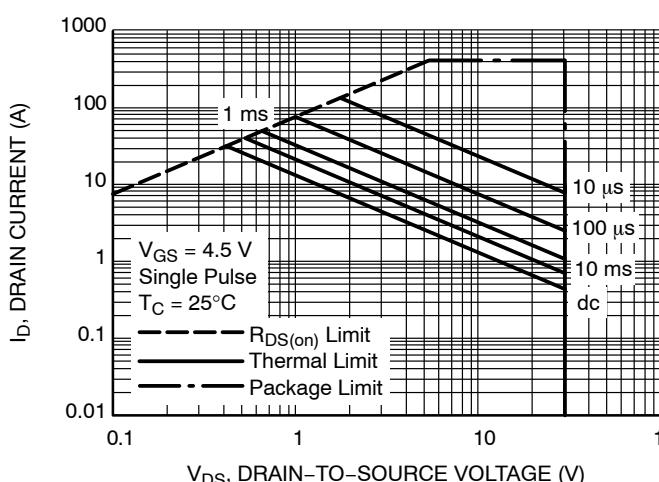
**Figure 8. Gate-to-Source Voltage vs. Total Charge**



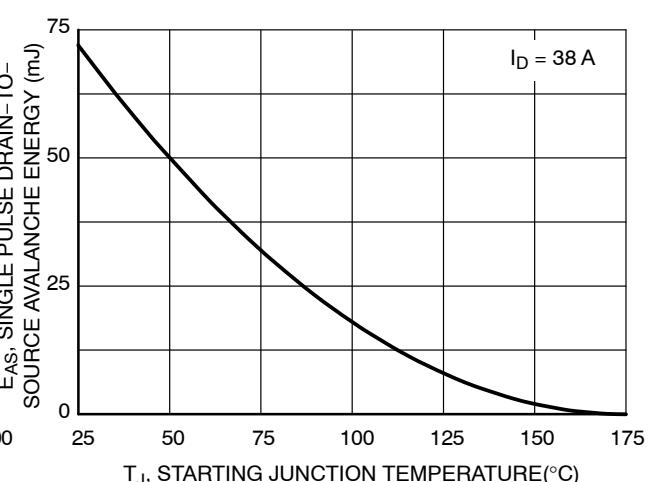
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

## TYPICAL CHARACTERISTICS

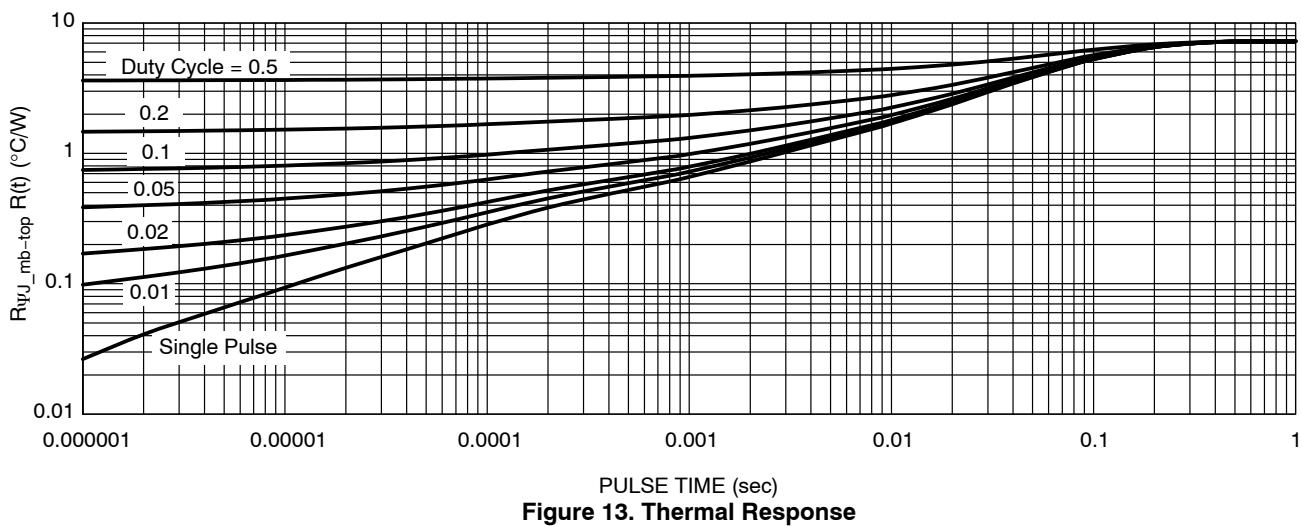


Figure 13. Thermal Response

## DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NVTFS4824NTAG	4824	WDFN8 (Pb-Free)	1500 / Tape & Reel
NVTFS4824NWFTAG	24WF	WDFN8 (Pb-Free)	1500 / Tape & Reel
NVTFS4824NTWG	4824	WDFN8 (Pb-Free)	5000 / Tape & Reel
NVTFS4824NWFTWG	24WF	WDFN8 (Pb-Free)	5000 / Tape & Reel

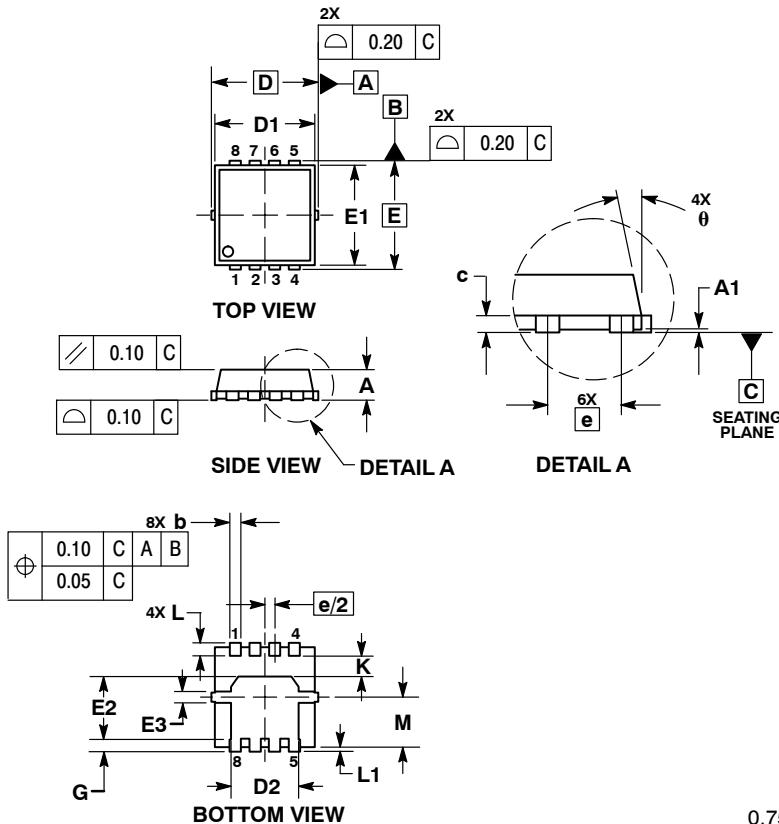
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NVTFS4824N

## PACKAGE DIMENSIONS

### WDFN8 3.3x3.3, 0.65P

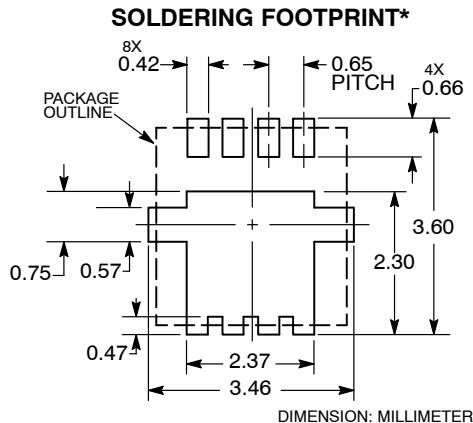
CASE 511AB  
ISSUE D



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30	BSC		0.130	BSC	
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30	BSC		0.130	BSC	
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65	BSC		0.026	BSC	
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
$\theta$	0 °	---	12 °	0 °	---	12 °



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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