EFC2J017NUZ

Power MOSFET
for 1-Cell Lithium-ion Battery Protection
12 V, 3.2 mΩ, 27 A, Dual N-Channel

ON Semiconductor®

www.onsemi.com

This Power MOSFET features a low on-state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1-cell lithium-ion battery applications.

V_{SSS}	R_{SS}(on) Max	I_S Max
12 V	3.2 mΩ @ 4.5 V	27 A
	3.4 mΩ @ 3.8 V	
	4.4 mΩ @ 3.1 V	
	6.3 mΩ @ 2.5 V	

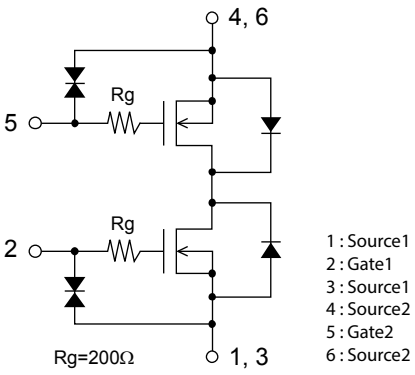
Features

- 2.5 V drive
- 2 kV ESD HBM
- Common-Drain Type
- ESD Diode-Protected Gate
- Pb-Free, Halogen Free and RoHS compliance

Applications

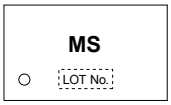
- 1-Cell Lithium-ion Battery Charging and Discharging Switch

ELECTRICAL CONNECTION
N-Channel



MARKING

WLCSP6, 1.77x3.05



MS : Device Code

ORDERING INFORMATION
See detailed ordering and shipping information on page 6 of this data sheet.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS at Ta = 25°C (Note 1)

Parameter	Symbol	Value	Unit
Source to Source Voltage	V_{SSS}	12	V
Gate to Source Voltage	V_{GSS}	±8	V
Maximum Operating Gate to Source Voltage (Note2)	$V_{GSS(OP)}$	±6.4	V
Source Current (DC)	I_S	27	A
Source Current (Pulse) PW ≤ 100 μs, duty cycle ≤ 1%	I_{SP}	100	A
Total Dissipation (Note 3)	P_T	2.5	W
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	−55 to +150	°C

Note 1 : Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note 2 : Functional operation above the stresses listed in the recommended operating ranges is not implied. Extended exposure to stresses beyond the recommended operating ranges limits may affect device reliability.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction to Ambient (Note 3)	$R_{\theta JA}$	50	°C/W

Note 3 : Surface mounted on ceramic substrate (5000 $mm^2 \times 0.8$ mm).

ELECTRICAL CHARACTERISTICS at Ta = 25°C (Notes 4, 5)

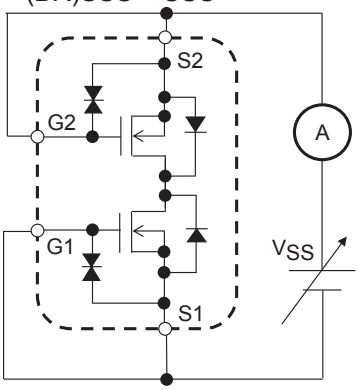
Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Source to Source Breakdown Voltage	$V_{(BR)SSS}$	I_S = 1 mA, V_{GS} = 0 V Test Circuit 1	12			V
Zero-Gate Voltage Source Current	I_{SSS}	V_{SS} = 10 V, V_{GS} = 0 V Test Circuit 1			1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±8 V, V_{SS} = 0 V Test Circuit 2			±1	μA
Gate Threshold Voltage	$V_{GS}(th)$	V_{SS} = 6 V, I_S = 1 mA Test Circuit 3	0.5		1.3	V
Static Source to Source On-State Resistance	$R_{SS}(on)$	I_S = 5 A, V_{GS} = 4.5 V Test Circuit 4	1.8	2.3	3.2	mΩ
		I_S = 5 A, V_{GS} = 3.8 V Test Circuit 4	2.0	2.6	3.4	mΩ
		I_S = 5 A, V_{GS} = 3.1 V Test Circuit 4	2.1	3.3	4.4	mΩ
		I_S = 5 A, V_{GS} = 2.5 V Test Circuit 4	2.7	4.0	6.3	mΩ
Turn-ON Delay Time	$t_d(on)$	V_{SS} = 6 V, V_{GS} = 4.5 V, I_S = 3 A Test Circuit 5		450		ns
Rise Time	t_r			590		ns
Turn-OFF Delay Time	$t_d(off)$			7,600		ns
Fall Time	t_f			2,100		ns
Total Gate Charge	Qg	V_{SS} = 6 V, V_{GS} = 4.5 V, I_S = 27 A Test Circuit 6		95		nC
Forward Source to Source Voltage	$V_{F(S-S)}$	I_S = 3 A, V_{GS} = 0 V Test Circuit 7		0.68	1.2	V

Note 4 : Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

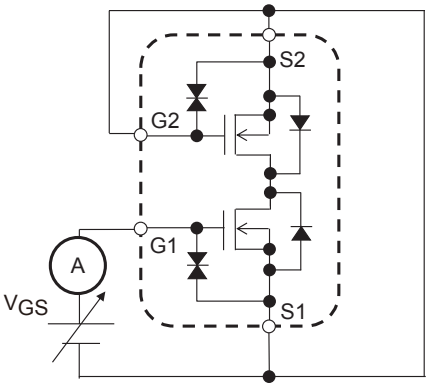
Note 5 : Refer to the JIS 7030 measuring methods for transistors for measuring.

Test circuits are example of measuring FET1 side

Test Circuit 1
$V_{(BR)SSS}$ / I_{SSS}

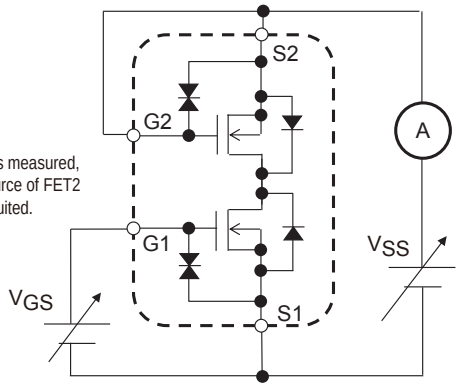


Test Circuit 2
I_{GSS}



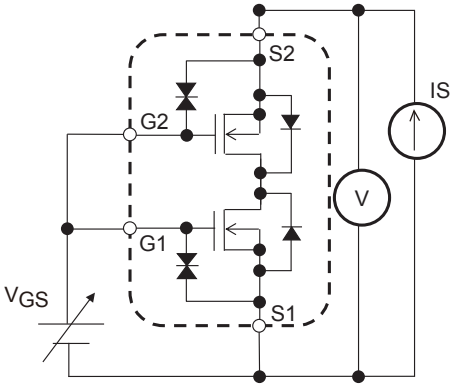
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
$V_{GS(th)}$

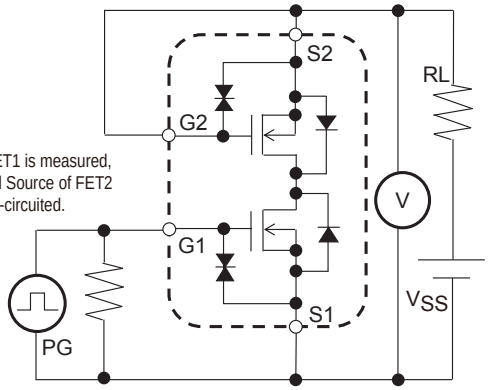


When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 4
$R_{SS(on)}$

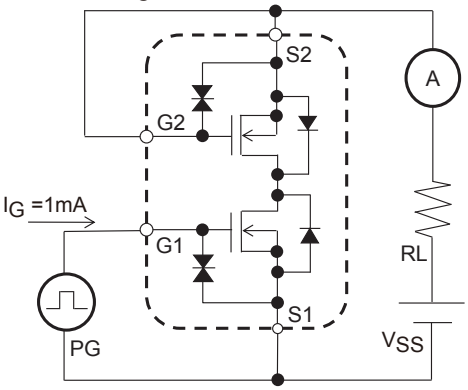


Test Circuit 5
$t_{d(on)}$, t_r, $t_{d(off)}$, t_f



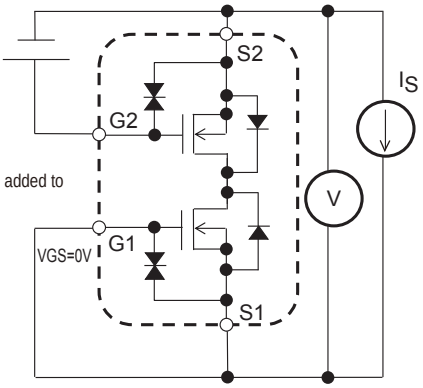
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 6
Qg



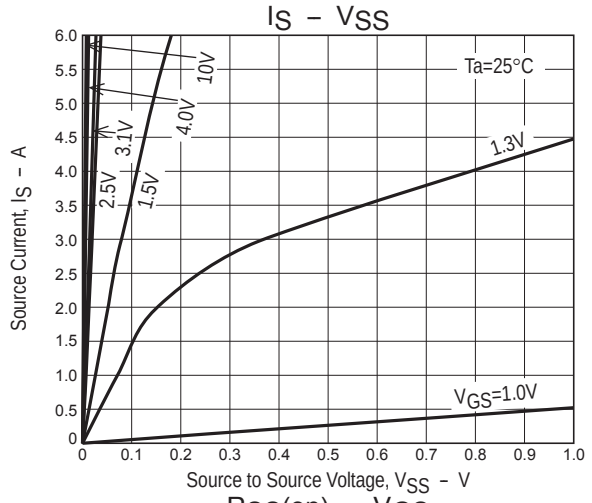
When FET1 is measured, Gate and Source of FET2 are short-circuited.

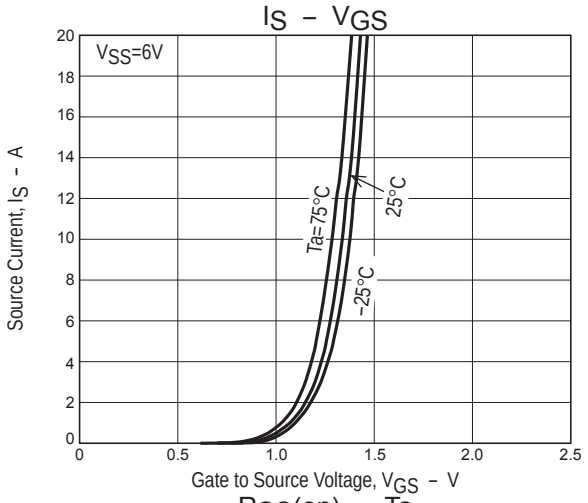
Test Circuit 7
$V_{F(S-S)}$

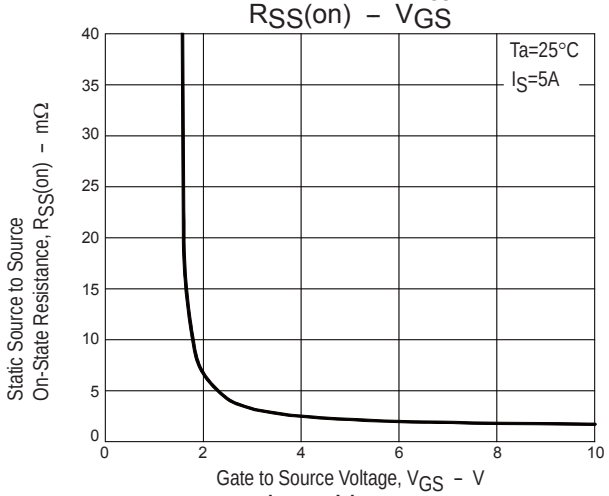


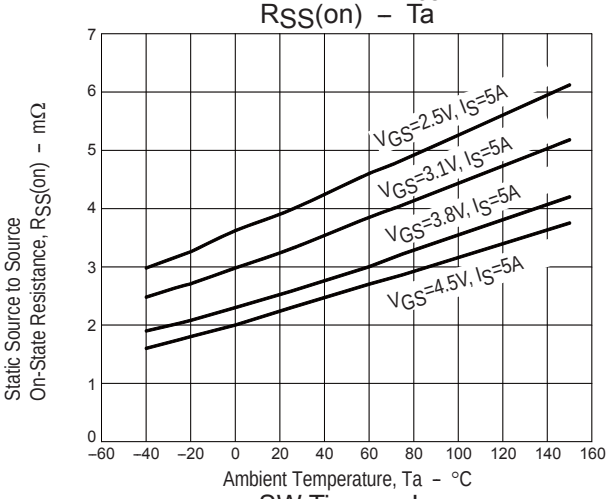
When FET1 is measured,+4.5V is added to V_{GS} of FET2.

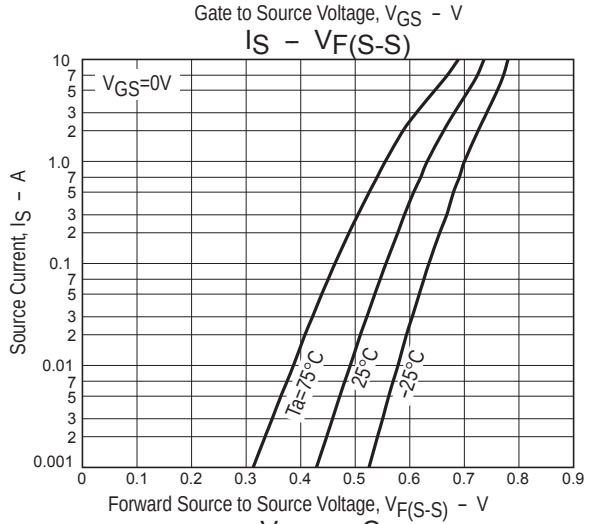
When FET2 is measured, the position of FET1 and FET2 is switched.

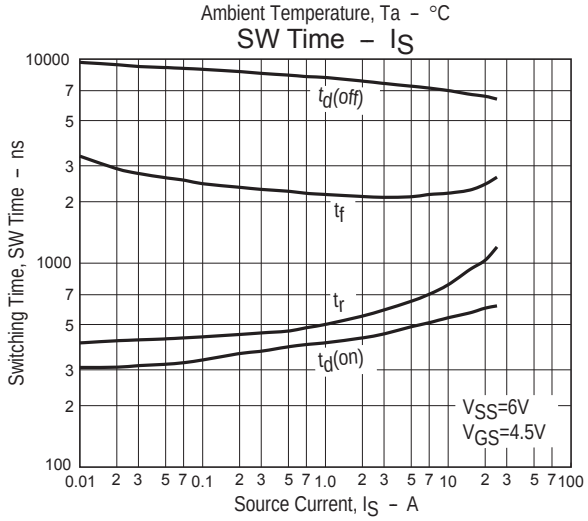

IS – VSS
Ta=25°C
10V
4.0V
3.1V
2.5V
1.5V
1.3V
VGS=1.0V
Source Current, IS – A
Source to Source Voltage, VSS – V

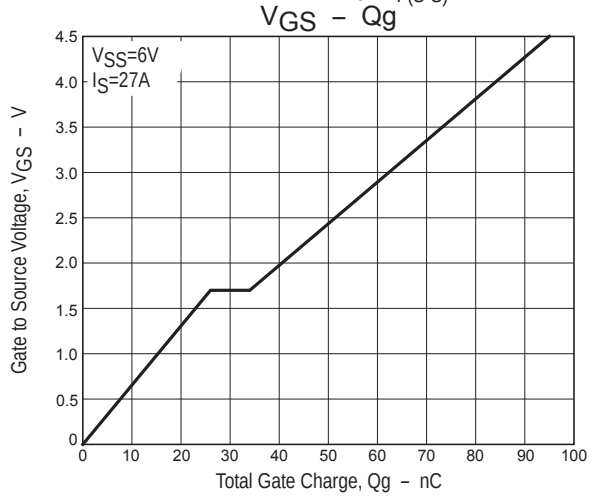

IS – VGS
VSS=6V
Ta=75°C
25°C
–25°C
Source Current, IS – A
Gate to Source Voltage, VGS – V

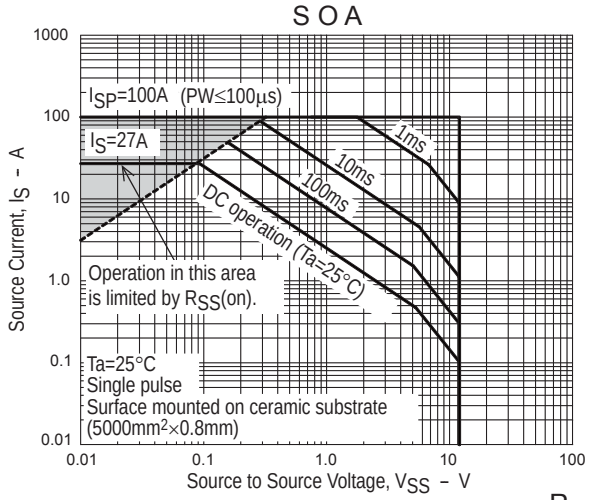

RSS(on) – VGS
Ta=25°C
IS=5A
Static Source to Source
On-State Resistance, RSS(on) – mΩ
Gate to Source Voltage, VGS – V

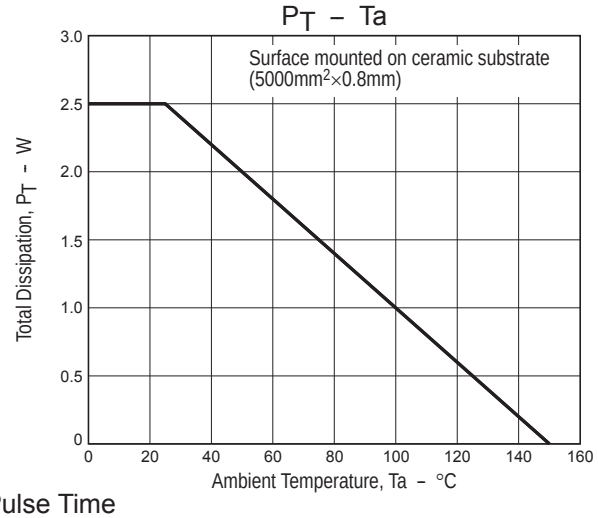

RSS(on) – Ta
VGS=2.5V, IS=5A
VGS=3.1V, IS=5A
VGS=3.8V, IS=5A
VGS=4.5V, IS=5A
Static Source to Source
On-State Resistance, RSS(on) – mΩ
Ambient Temperature, Ta – °C

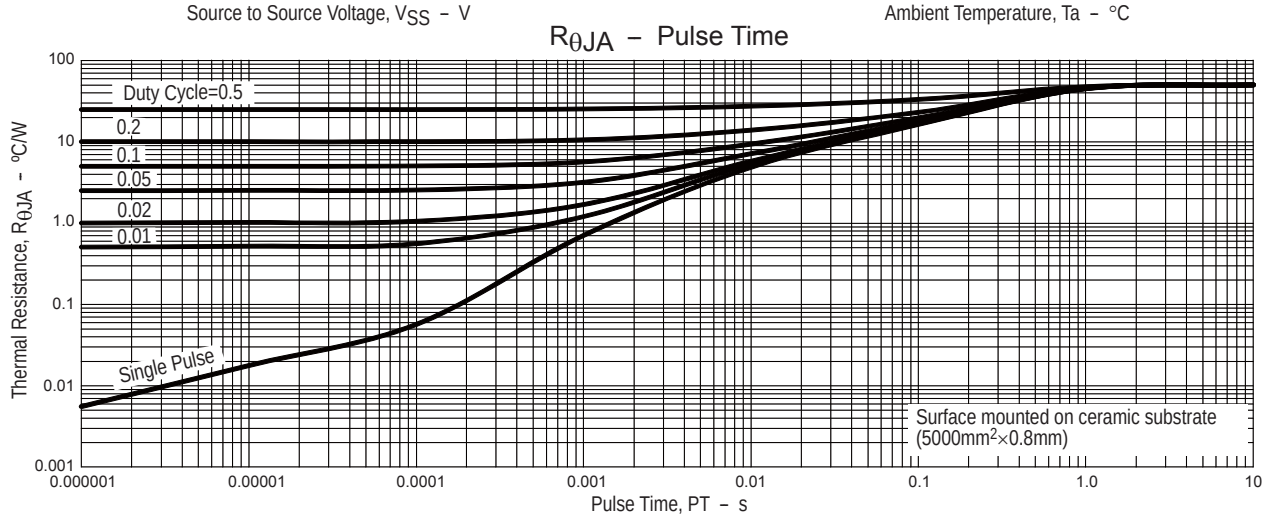

IS – VF(S-S)
VGS=0V
Ta=75°C
25°C
–25°C
Source Current, IS – A
Forward Source to Source Voltage, VF(S-S) – V


SW Time – IS
td(off)
tf
tr
td(on)
VSS=6V
VGS=4.5V
Switching Time, SW Time – ns
Source Current, IS – A


VGS – Qg
VSS=6V
IS=27A
Gate to Source Voltage, VGS – V
Total Gate Charge, Qg – nC

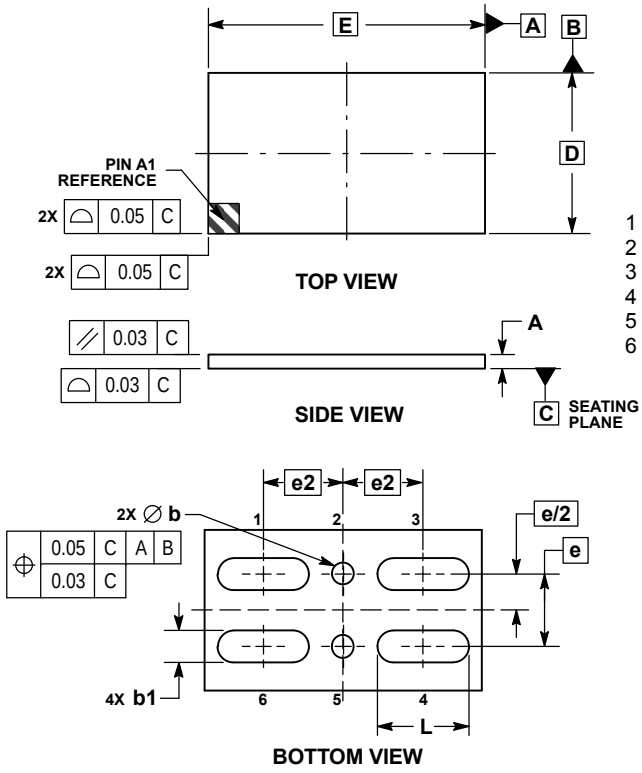

S O A
1000
100
10
1.0
0.1
0.01
Source Current, IS – A
ISP=100A (PW≤100μs)
IS=27A
1ms
10ms
100ms
DC operation (Ta=25°C)
Operation in this area
is limited by RSS(on).
Ta=25°C
Single pulse
Surface mounted on ceramic substrate
(5000mm2×0.8mm)
0.01
0.1
1.0
10
100
Source to Source Voltage, VSS – V


PT – Ta
3.0
2.5
2.0
1.5
1.0
0.5
0
Total Dissipation, PT – W
Surface mounted on ceramic substrate
(5000mm2×0.8mm)
0
20
40
60
80
100
120
140
160
Ambient Temperature, Ta – °C


RθJA – Pulse Time
100
10
1.0
0.1
0.01
0.001
Thermal Resistance, RθJA – °C/W
Duty Cycle=0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Surface mounted on ceramic substrate
(5000mm2×0.8mm)
0.000001
0.00001
0.0001
0.001
0.01
0.1
1.0
10
Pulse Time, PT – s

PACKAGE DIMENSIONS
unit : mm

WLCSP6, 1.77x3.05
CASE 567KS
ISSUE O

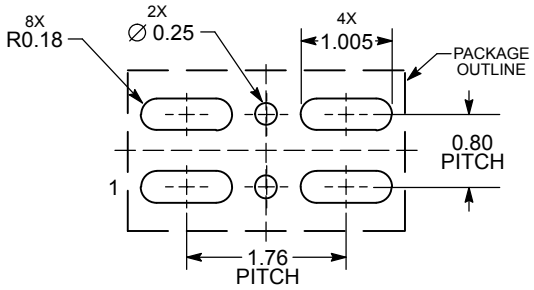


1 : Source1
2 : Gate1
3 : Source1
4 : Source2
5 : Gate2
6 : Source2

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.145
b	0.22	0.28
b1	0.32	0.38
D	1.77 BSC	
E	3.05 BSC	
e	0.80 BSC	
e2	0.8775 BSC	
L	0.975	1.035

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

Device	Marking	Package	Shipping (Qty / Packing)
EFC2J017NUZTDG	MS	WLCSP6, 1.77 × 3.05 (Pb-Free / Halogen Free)	5,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

Note on usage : Since the EFC2J017NUZ is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.