

74CBTLVD3861

10-bit level-shifting bus switch with output enable

Rev. 4 — 14 December 2011

Product data sheet

1. General description

The 74CBTLVD3861 is a 10-bit 3.3 V to 1.8 V level translating bus switch with one output enable (\overline{OE}) input. When \overline{OE} is LOW, the switch is closed and port A is connected to the B port. When \overline{OE} is HIGH, the switch is disabled.

To ensure the high-impedance OFF-state during power-up or power-down, \overline{OE} should be tied to the V_{CC} through a pull-up resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 3.0 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF} .

2. Features and benefits

- Supply voltage range from 3.0 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-B/JESD36 (3.0 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ CDM AEC-Q100-011 revision B exceeds 1000 V
- 4 Ω switch connection between two ports
- 3.3 V to 1.8 V level translation
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40°C to $+85^{\circ}\text{C}$ and -40°C to $+125^{\circ}\text{C}$

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3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74CBTLVD3861DK	−40 °C to +125 °C	SSOP24 ^[1]	plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT556-1
74CBTLVD3861PW	−40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74CBTLVD3861BQ	−40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

[1] Also known as QSOP24 package

4. Functional diagram

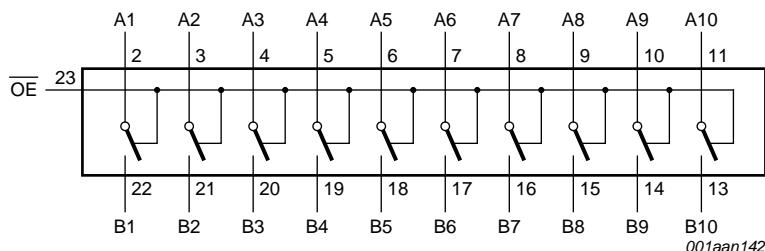


Fig 1. Logic symbol

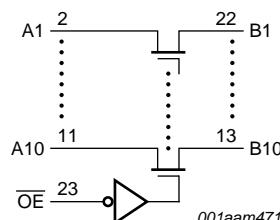


Fig 2. Logic diagram

5. Pinning information

5.1 Pinning

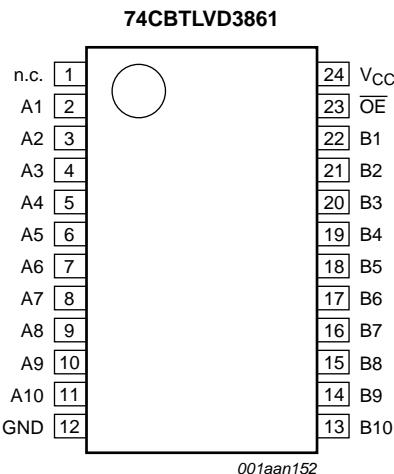


Fig 3. Pin configuration for TSSOP24 (SOT355-1)

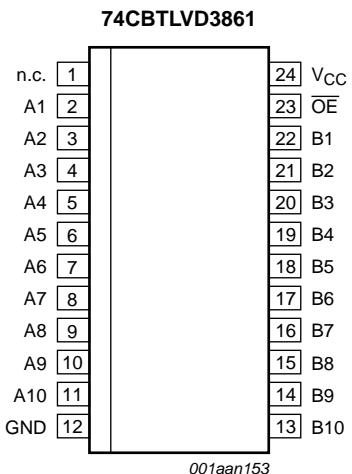
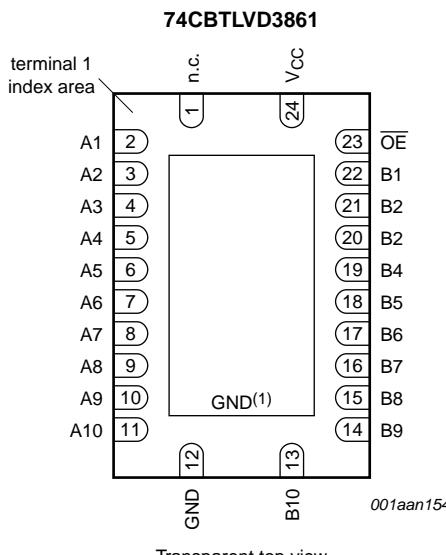


Fig 4. Pin configuration for SSOP24 (SOT556-1)



- (1) This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad however if it is soldered the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration for DHVQFN24 (SOT815-1)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
nc	1	not connected
A1 to A10	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	data input/output (A port)
GND	12	ground (0 V)
B1 to B10	22, 21, 20, 19, 18, 17, 16, 15, 14, 13	data input/output (B port)
OE	23	output enable input (active LOW)
V _{CC}	24	positive supply voltage

6. Functional description

Table 3. Function selection^[1]

Input	Input/output
OE	A _n , B _n
L	A _n = B _n
H	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		^[1] -0.5	+4.6	V
V _{SW}	switch voltage	enable and disable mode	^[1] -0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < -0.5 V	-50	-	mA
I _{SK}	switch clamping current	V _I < -0.5 V	-50	-	mA
I _{SW}	switch current	V _{SW} = 0 V to V _{CC}	-	±128	mA
I _{CC}	supply current		-	+100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[2] -	500	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SSOP24 and TSSOP24 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN24 package: P_{tot} derates linearly at 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		3.0	3.6	V
V_I	input voltage		0	3.6	V
V_{SW}	switch voltage	enable and disable mode	0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[1]	-	200 ns/V

[1] Applies to control signal levels.

9. Static characteristics

Table 6. Static characteristics

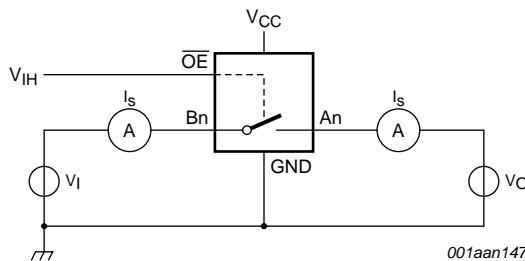
At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$			$T_{amb} = -40 \text{ }^{\circ}\text{C to } +125 \text{ }^{\circ}\text{C}$			Unit
			Min	Typ[1]	Max	Min	Max		
V_{IH}	HIGH-level input voltage	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	-	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	0.9	-	0.9	-	V
I_I	input leakage current	pin \overline{OE} ; $V_I = \text{GND to } V_{CC}$; $V_{CC} = 3.6 \text{ V}$	-	-	± 1	-	± 20	μA	
V_{pass}	pass voltage	$V_I = V_{CC}$; see Figure 8 to Figure 12	-	-	-	-	-	-	V
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 3.6 \text{ V}$; see Figure 6	-	-	± 1	-	± 20	μA	
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 3.6 \text{ V}$; see Figure 7	-	-	± 1	-	± 20	μA	
I_{OFF}	power-off leakage current	$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V}$	-	-	± 10	-	± 50	μA	
I_{CC}	supply current	$V_I = V_{CC}; I_O = 0 \text{ A}; V_{CC} = 3.6 \text{ V}; V_{SW} = \text{GND or } V_{CC}$	-	-	20	-	50	μA	
		$V_I = \text{GND}; I_O = 0 \text{ A}; V_{CC} = 3.6 \text{ V}; V_{SW} = \text{GND or } V_{CC}$	-	-	100	-	150	μA	
ΔI_{CC}	additional supply current	pin \overline{OE} ; $V_I = V_{CC} - 0.6 \text{ V}; V_{SW} = \text{GND or } V_{CC}; V_{CC} = 3.6 \text{ V}$	[2]	-	-	300	-	2000	μA
C_I	input capacitance	pin \overline{OE} ; $V_{CC} = 3.3 \text{ V}; V_I = 0 \text{ V to } 3.3 \text{ V}$	-	0.9	-	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance	$V_{CC} = 3.3 \text{ V}; V_I = 0 \text{ V to } 3.3 \text{ V}$	-	2.5	-	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	$V_{CC} = 3.3 \text{ V}; V_I = 0 \text{ V to } 3.3 \text{ V}$	-	9.0	-	-	-	-	pF

[1] All typical values are measured at $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

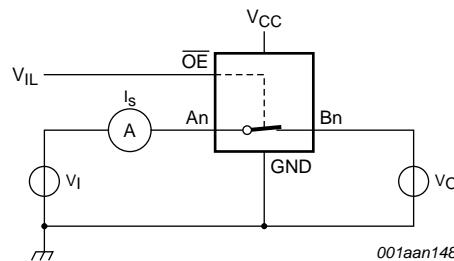
[2] One input at 3 V, other inputs at V_{CC} or GND.

9.1 Test circuits



$V_I = V_{CC}$ or GND and $V_O = GND$ or V_{CC} .

Fig 6. Test circuit for measuring OFF-state leakage current (one switch)



$V_I = V_{CC}$ or GND and $V_O = \text{open circuit}$.

Fig 7. Test circuit for measuring ON-state leakage current (one switch)

9.2 Typical pass voltage graphs

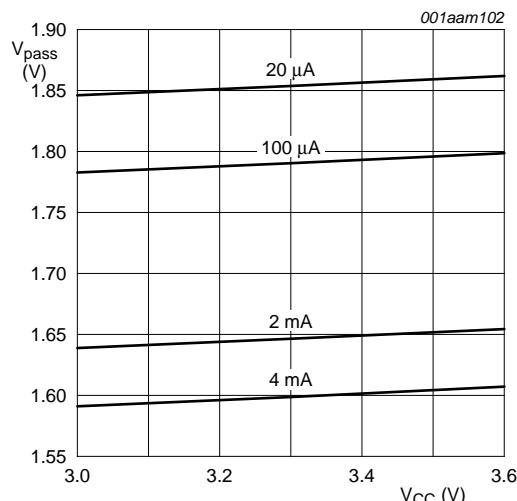


Fig 8. Pass voltage versus supply voltage; $T_{amb} = 125$ °C (typical)

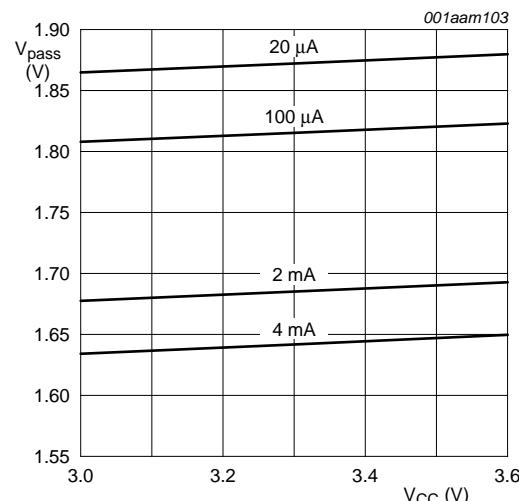


Fig 9. Pass voltage versus supply voltage; $T_{amb} = 85$ °C (typical)

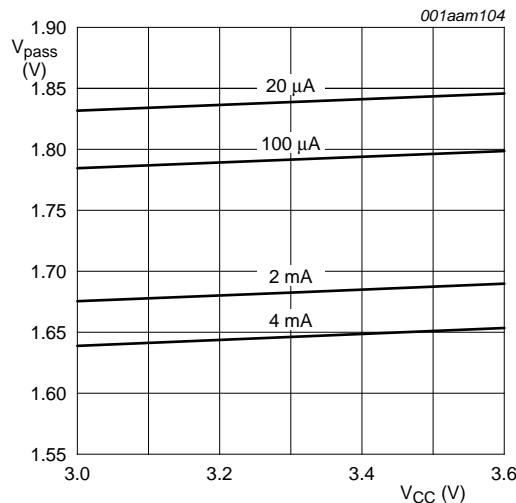


Fig 10. Pass voltage versus supply voltage;
 $T_{\text{amb}} = 25^{\circ}\text{C}$ (typical)

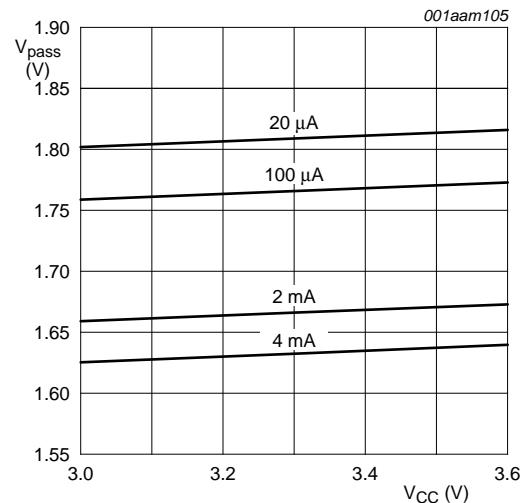


Fig 11. Pass voltage versus supply voltage;
 $T_{\text{amb}} = 0^{\circ}\text{C}$ (typical)

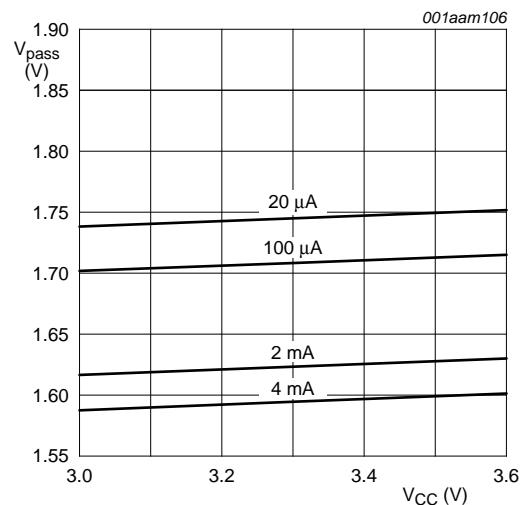


Fig 12. Pass voltage versus supply voltage; $T_{\text{amb}} = -40^{\circ}\text{C}$ (typical)

9.3 ON resistance

Table 7. Resistance R_{ON}

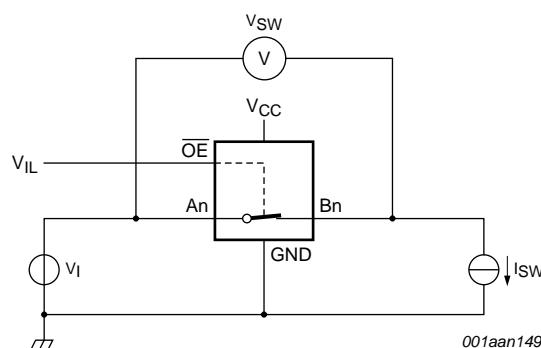
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 13](#).

Symbol	Parameter	Conditions	$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			$T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$			Unit
			Min	Typ ^[1]	Max	Min	Max		
R_{ON}	ON resistance	$V_{CC} = 3.0\text{ V}$ to 3.6 V	[2]						
		$I_{SW} = 64\text{ mA}; V_I = 0\text{ V}$	-	3.7	7.0	-	10.0	Ω	
		$I_{SW} = 24\text{ mA}; V_I = 0\text{ V}$	-	3.7	7.0	-	10.0	Ω	
		$I_{SW} = 15\text{ mA}; V_I = 1.2\text{ V}$	-	4.7	10.0	-	12.0	Ω	

[1] Typical values are measured at $T_{amb} = 25^{\circ}\text{C}$ and nominal V_{CC} .

[2] Measured by the voltage drop between the An and Bn terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (An or Bn) terminals.

9.4 ON resistance test circuit



$$R_{ON} = V_{SW} / I_{SW}.$$

Fig 13. Test circuit for measuring ON resistance (one switch)

10. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V; for test circuit see [Figure 16](#)

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	
t _{pd}	propagation delay	An to Bn or Bn to An; see Figure 14	[2][3]				
		V _{CC} = 3.0 V to 3.6 V	-	-	0.11	-	0.22 ns
t _{en}	enable time	OE to An or Bn; see Figure 15	[4]				
		V _{CC} = 3.0 V to 3.6 V	1.5	2.9	5.0	1.5	6.0 ns
t _{dis}	disable time	OE to An or Bn; see Figure 15	[5]				
		V _{CC} = 3.0 V to 3.6 V	0.8	3.3	7.0	0.8	8.0 ns

[1] All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC}.

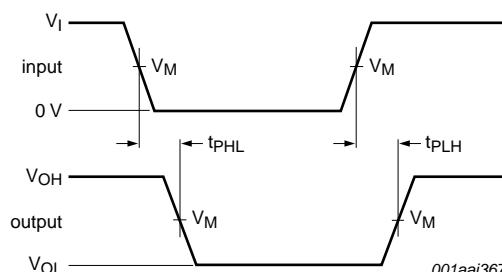
[2] The propagation delay is the calculated RC time constant of the on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).

[3] t_{pd} is the same as t_{PLH} and t_{PHL}.

[4] t_{en} is the same as t_{PZH} and t_{PZL}.

[5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

10.1 Waveforms



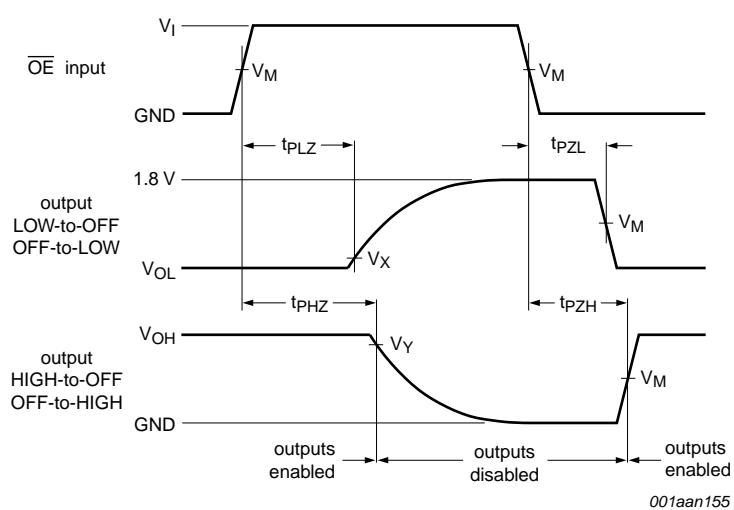
Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 14. The data input (An, Bn) to output (Bn, An) propagation delay times

Table 9. Measurement points

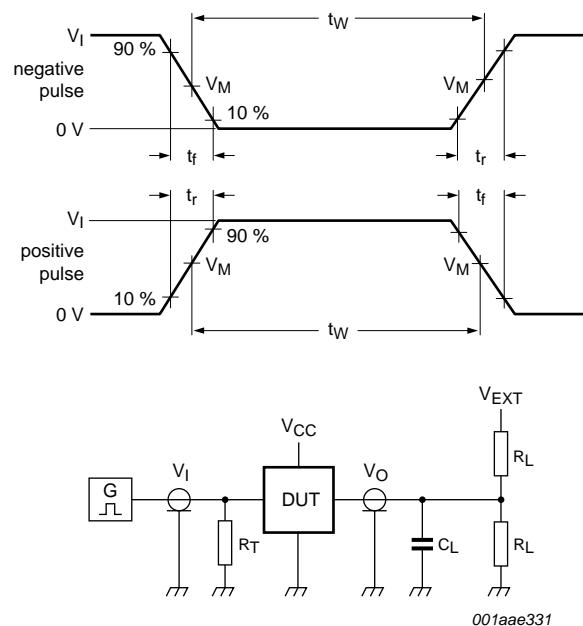
Supply voltage	Input			Output			
V _{CC}	V _M	V _I	t _r = t _f	V _M	V _X	V _Y	
3.0 V to 3.6 V	0.5V _{CC}	V _{CC}	≤ 2.0 ns	0.9 V	V _{OL} + 0.15 V	V _{OH} - 0.15 V	



Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 15. Enable and disable times



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 16. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V to 3.6 V	30 pF	1 k Ω	open	GND	3.6 V

10.2 Additional dynamic characteristics

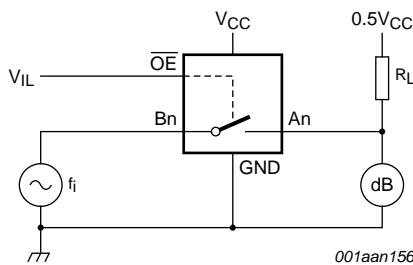
Table 11. Additional dynamic characteristics

$GND = 0 \text{ V}$.

Symbol	Parameter	Conditions	$T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$			Unit	
			Min	Typ	Max		
$f_{(-3\text{dB})}$	-3 dB frequency response	$V_{\text{CC}} = 3.3 \text{ V}$; $R_{\text{L}} = 50 \Omega$; see Figure 17	[1]	-	575	-	MHz

[1] f_i is biased at $0.5V_{\text{CC}}$.

10.3 Test circuit

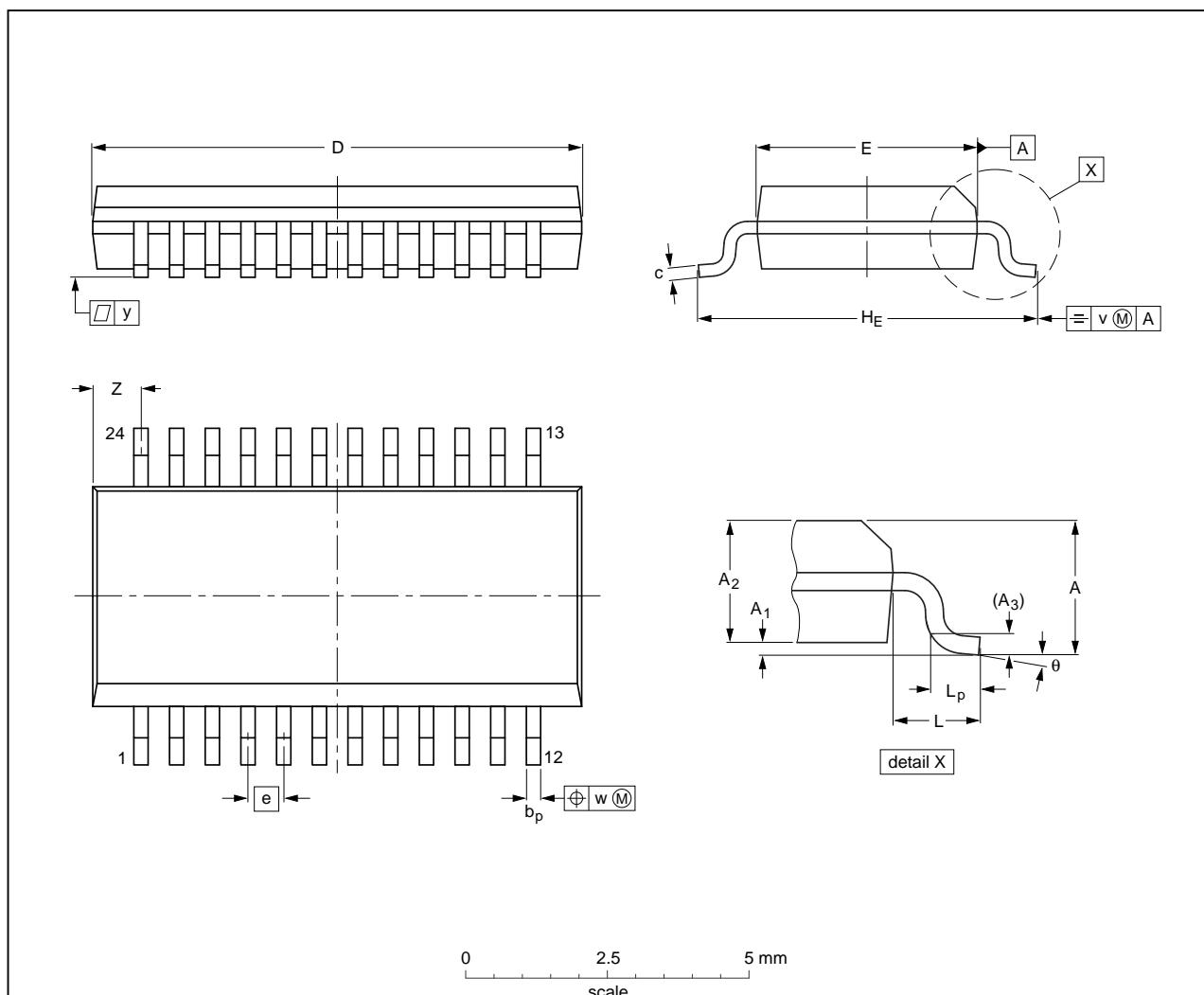


Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Fig 17. Test circuit for measuring the frequency response when channel is in ON-state

11. Package outline

SSOP24: plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm SOT556-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	8.8 8.6	4.0 3.8	0.635	6.2 5.8	1	0.89 0.41	0.25	0.18	0.1	1.05 0.66	8° 0°
inches	0.068	0.0098 0.0040	0.061 0.055	0.01	0.012 0.008	0.0098 0.0075	0.344 0.337	0.157 0.150	0.025	0.244 0.228	0.041	0.035 0.016	0.01	0.007	0.004	0.040 0.026	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm (0.008 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT556-1		MO-137			-99-12-27- 03-02-18

Fig 18. Package outline SOT556-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

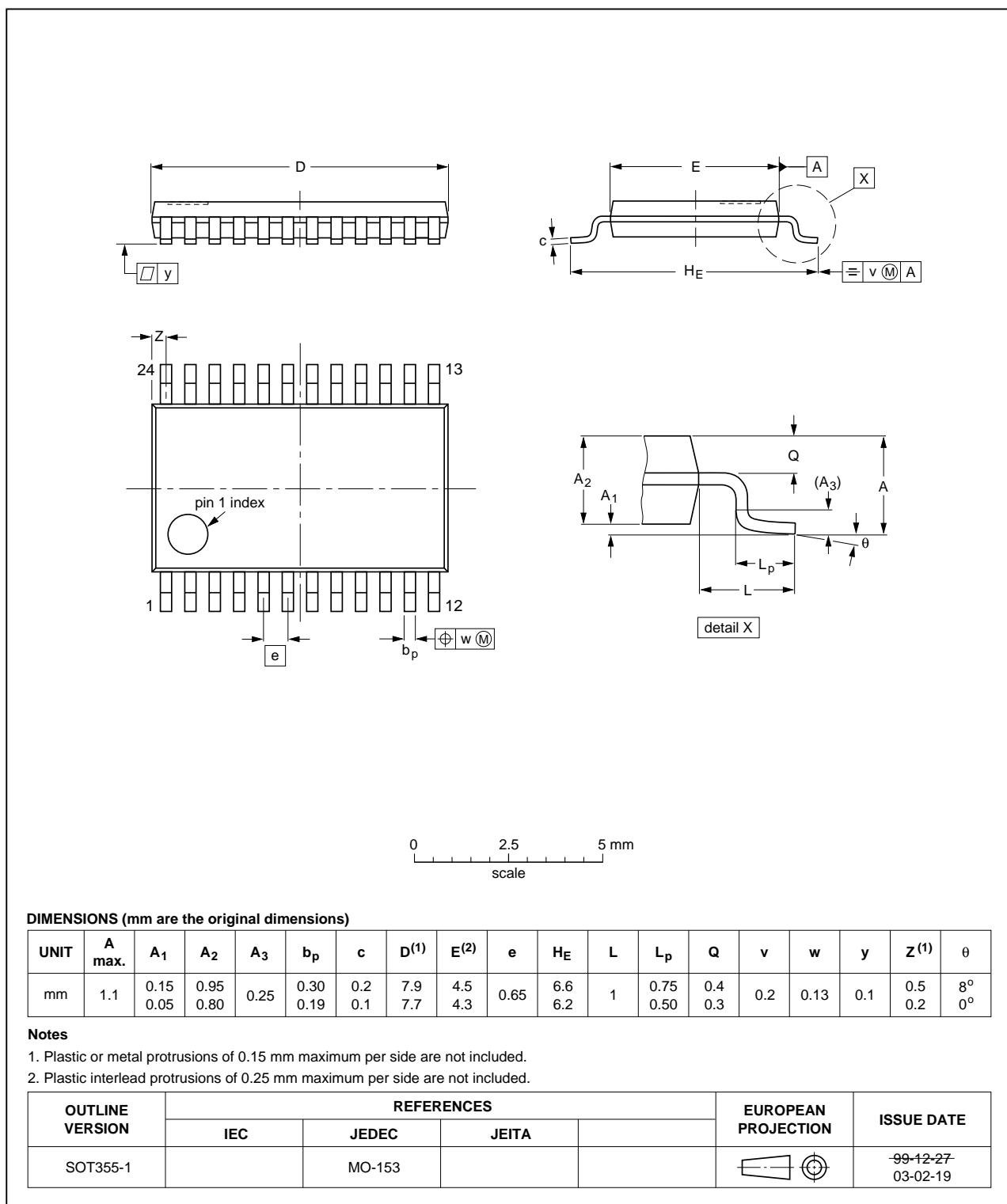


Fig 19. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package;
no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

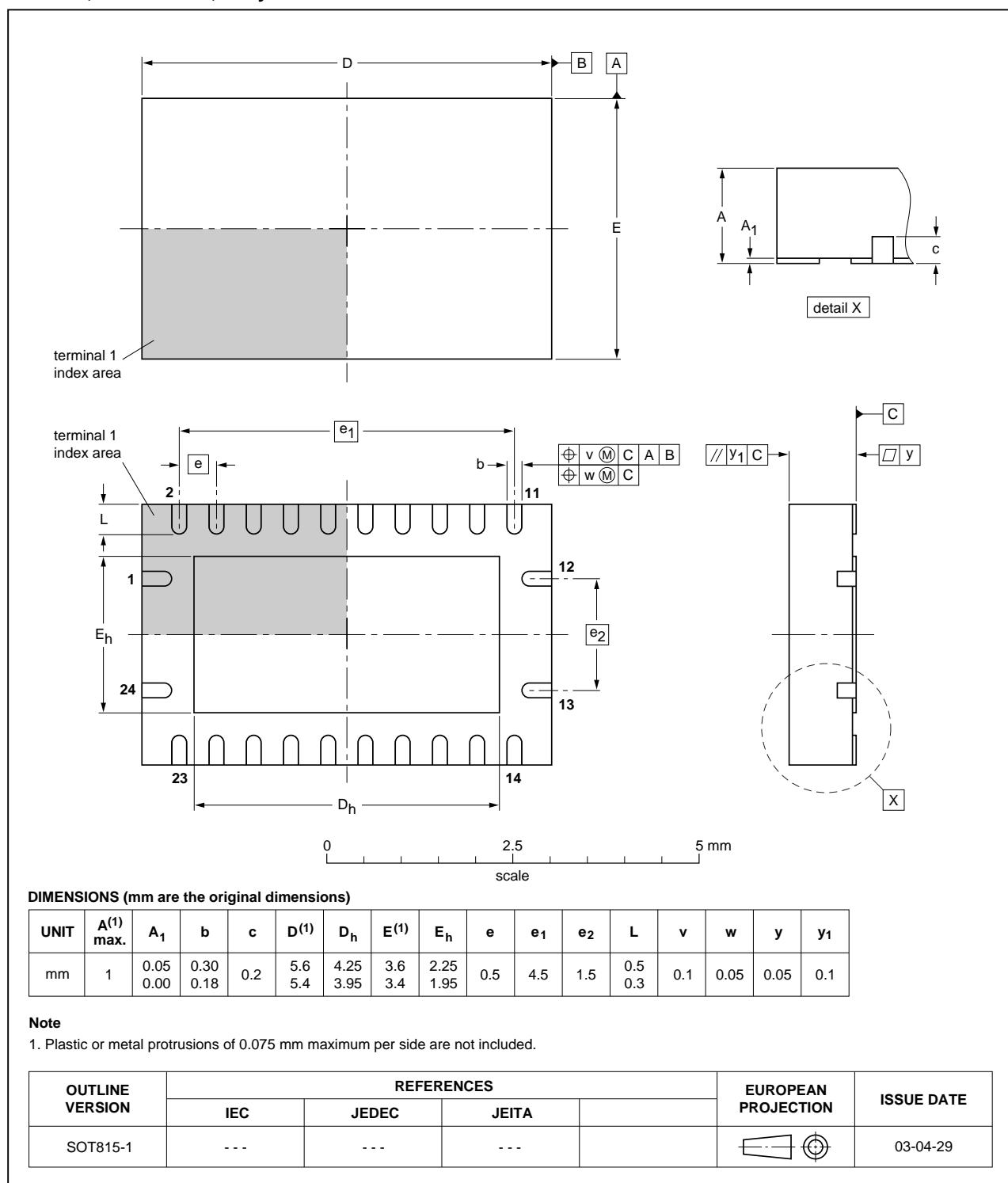


Fig 20. Package outline SOT815-1 (DHVQFN24)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLVD3861 v.4	20111214	Product data sheet	-	74CBTLVD3861 v.3
Modifications:		• Legal pages updated.		
74CBTLVD3861 v.3	20111020	Product data sheet	-	74CBTLVD3861 v.2
74CBTLVD3861 v.2	20110117	Product data sheet	-	74CBTLVD3861 v.1
74CBTLVD3861 v.1	20101206	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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