

# 74CBTLVD3861

10-bit level-shifting bus switch with output enable

Rev. 4 — 14 December 2011

Product data sheet

## 1. General description

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The 74CBTLVD3861 is a 10-bit 3.3 V to 1.8 V level translating bus switch with one output enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the switch is closed and port A is connected to the B port. When  $\overline{OE}$  is HIGH, the switch is disabled.

To ensure the high-impedance OFF-state during power-up or power-down,  $\overline{OE}$  should be tied to the  $V_{CC}$  through a pull-up resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire  $V_{CC}$  range from 3.0 V to 3.6 V.

This device is fully specified for partial power-down applications using  $I_{OFF}$ .

## 2. Features and benefits

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- Supply voltage range from 3.0 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
  - ◆ JESD8-B/JESD36 (3.0 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ CDM AEC-Q100-011 revision B exceeds 1000 V
- 4  $\Omega$  switch connection between two ports
- 3.3 V to 1.8 V level translation
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74CBTLVD3861DK	−40 °C to +125 °C	SSOP24 <sup>[1]</sup>	plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT556-1
74CBTLVD3861PW	−40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74CBTLVD3861BQ	−40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

[1] Also known as QSOP24 package

4. Functional diagram

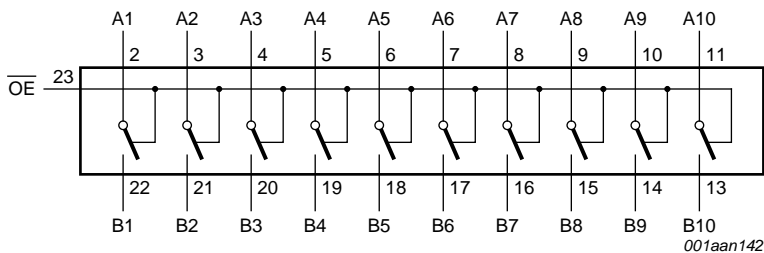


Fig 1. Logic symbol

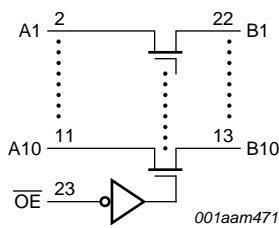


Fig 2. Logic diagram

5. Pinning information

5.1 Pinning

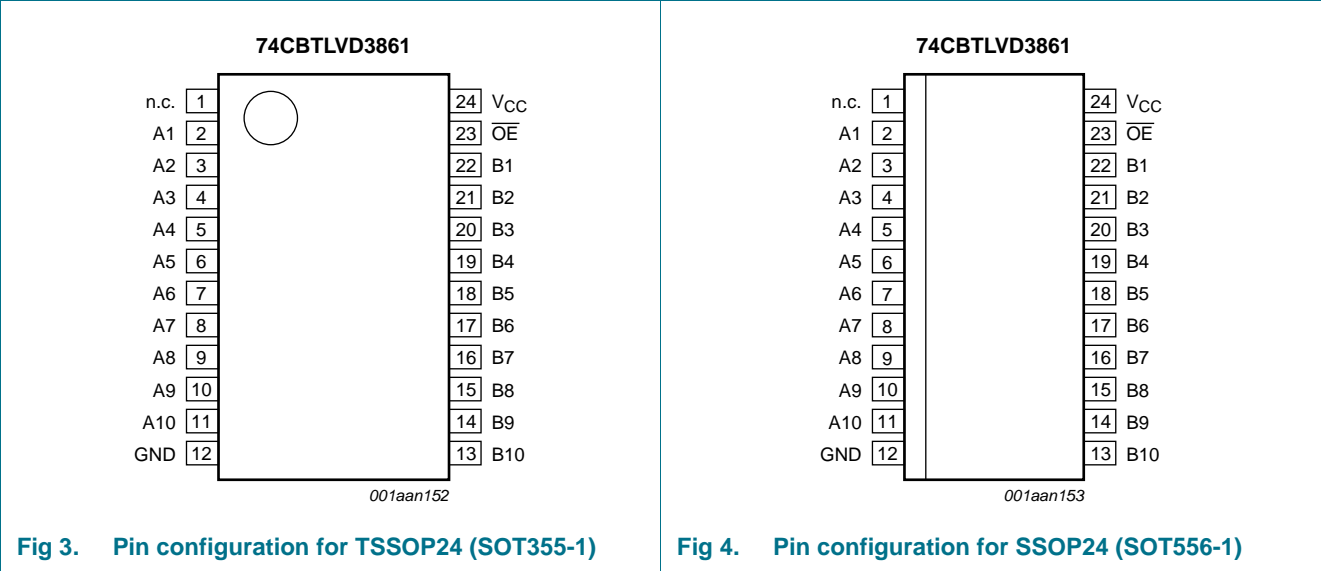


Fig 3. Pin configuration for TSSOP24 (SOT355-1)

Fig 4. Pin configuration for SSOP24 (SOT556-1)

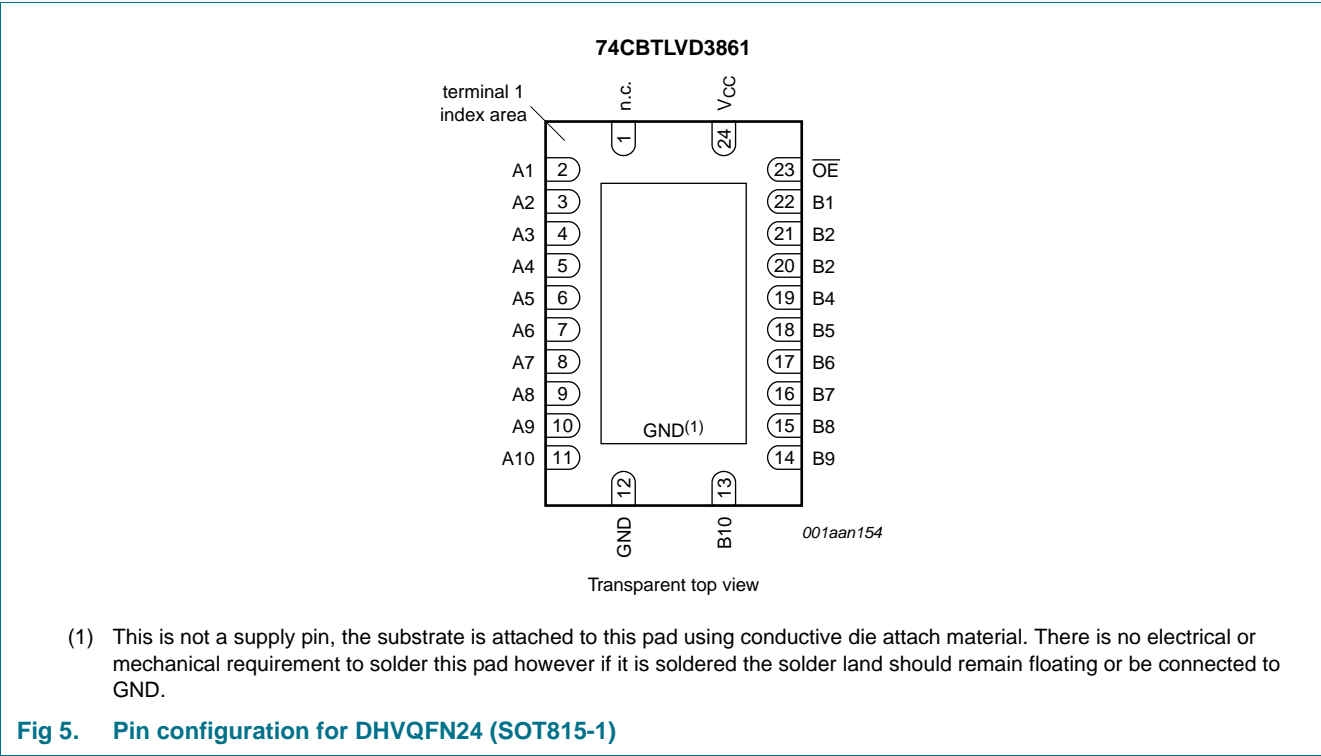


Fig 5. Pin configuration for DHVQFN24 (SOT815-1)

## 5.2 Pin description

**Table 2.** Pin description

Symbol	Pin	Description
nc	1	not connected
A1 to A10	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	data input/output (A port)
GND	12	ground (0 V)
B1 to B10	22, 21, 20, 19, 18, 17, 16, 15, 14, 13	data input/output (B port)
$\overline{\text{OE}}$	23	output enable input (active LOW)
V <sub>CC</sub>	24	positive supply voltage

## 6. Functional description

**Table 3.** Function selection<sup>[1]</sup>

Input	Input/output
$\overline{\text{OE}}$	An, Bn
L	An = Bn
H	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4.** Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
V <sub>I</sub>	input voltage		<sup>[1]</sup> -0.5	+4.6	V
V <sub>SW</sub>	switch voltage	enable and disable mode	<sup>[1]</sup> -0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	-50	-	mA
I <sub>SK</sub>	switch clamping current	V <sub>I</sub> < -0.5 V	-50	-	mA
I <sub>SW</sub>	switch current	V <sub>SW</sub> = 0 V to V <sub>CC</sub>	-	±128	mA
I <sub>CC</sub>	supply current		-	+100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	<sup>[2]</sup> -	500	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SSOP24 and TSSOP24 packages: P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.  
For DHVQFN24 package: P<sub>tot</sub> derates linearly at 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		3.0	3.6	V
$V_I$	input voltage		0	3.6	V
$V_{SW}$	switch voltage	enable and disable mode	0	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	[1] -	200	ns/V

[1] Applies to control signal levels.

## 9. Static characteristics

**Table 6. Static characteristics**

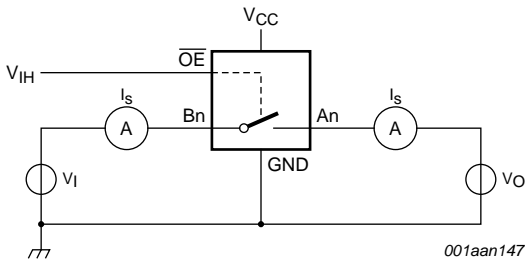
At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			$T_{amb} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ[1]	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	0.9	-	0.9	V
$I_I$	input leakage current	pin $\overline{OE}$ ; $V_I = \text{GND to }V_{CC}$ ; $V_{CC} = 3.6\text{ V}$	-	-	$\pm 1$	-	$\pm 20$	$\mu\text{A}$
$V_{pass}$	pass voltage	$V_I = V_{CC}$ ; see <a href="#">Figure 8</a> to <a href="#">Figure 12</a>	-	-	-	-	-	V
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 3.6\text{ V}$ ; see <a href="#">Figure 6</a>	-	-	$\pm 1$	-	$\pm 20$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 3.6\text{ V}$ ; see <a href="#">Figure 7</a>	-	-	$\pm 1$	-	$\pm 20$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 0\text{ V to }3.6\text{ V}$ ; $V_{CC} = 0\text{ V}$	-	-	$\pm 10$	-	$\pm 50$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ ; $I_O = 0\text{ A}$ ; $V_{CC} = 3.6\text{ V}$ ; $V_{SW} = \text{GND or }V_{CC}$	-	-	20	-	50	$\mu\text{A}$
		$V_I = \text{GND}$ ; $I_O = 0\text{ A}$ ; $V_{CC} = 3.6\text{ V}$ ; $V_{SW} = \text{GND or }V_{CC}$	-	-	100	-	150	$\mu\text{A}$
		pin $\overline{OE}$ ; $V_I = V_{CC} - 0.6\text{ V}$ ; $V_{SW} = \text{GND or }V_{CC}$ ; $V_{CC} = 3.6\text{ V}$	[2] -	-	300	-	2000	$\mu\text{A}$
$C_I$	input capacitance	pin $\overline{OE}$ ; $V_{CC} = 3.3\text{ V}$ ; $V_I = 0\text{ V to }3.3\text{ V}$	-	0.9	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance	$V_{CC} = 3.3\text{ V}$ ; $V_I = 0\text{ V to }3.3\text{ V}$	-	2.5	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	$V_{CC} = 3.3\text{ V}$ ; $V_I = 0\text{ V to }3.3\text{ V}$	-	9.0	-	-	-	pF

[1] All typical values are measured at  $T_{amb} = 25\text{ °C}$ .

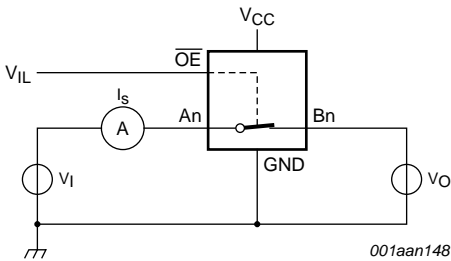
[2] One input at 3 V, other inputs at  $V_{CC}$  or GND.

9.1 Test circuits



$V_I = V_{CC}$  or GND and  $V_O =$  GND or  $V_{CC}$ .

Fig 6. Test circuit for measuring OFF-state leakage current (one switch)



$V_I = V_{CC}$  or GND and  $V_O =$  open circuit.

Fig 7. Test circuit for measuring ON-state leakage current (one switch)

9.2 Typical pass voltage graphs

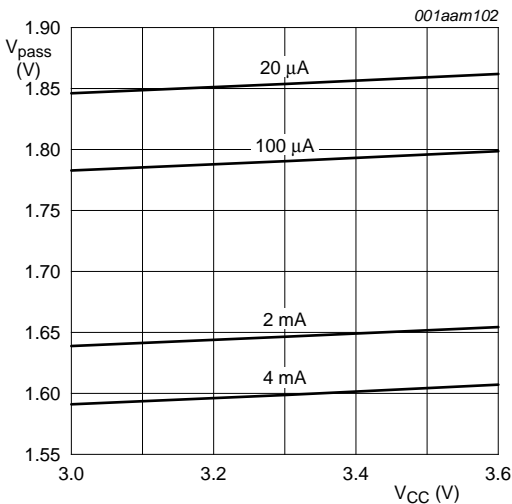


Fig 8. Pass voltage versus supply voltage;  
 $T_{amb} = 125\text{ °C}$  (typical)

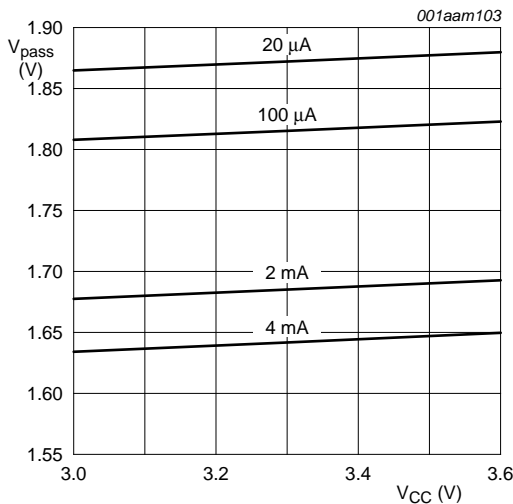


Fig 9. Pass voltage versus supply voltage;  
 $T_{amb} = 85\text{ °C}$  (typical)

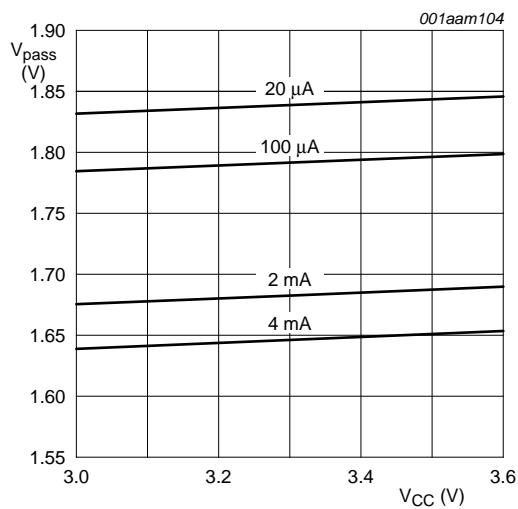


Fig 10. Pass voltage versus supply voltage; T<sub>amb</sub> = 25 °C (typical)

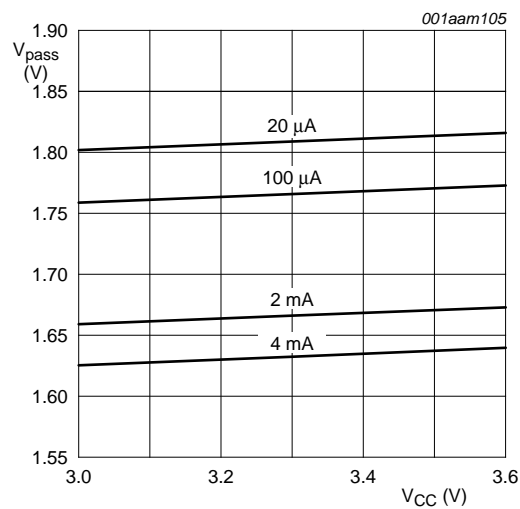


Fig 11. Pass voltage versus supply voltage; T<sub>amb</sub> = 0 °C (typical)

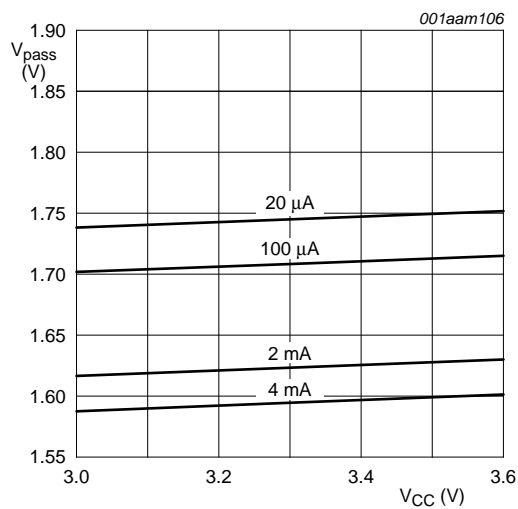


Fig 12. Pass voltage versus supply voltage; T<sub>amb</sub> = -40 °C (typical)

9.3 ON resistance

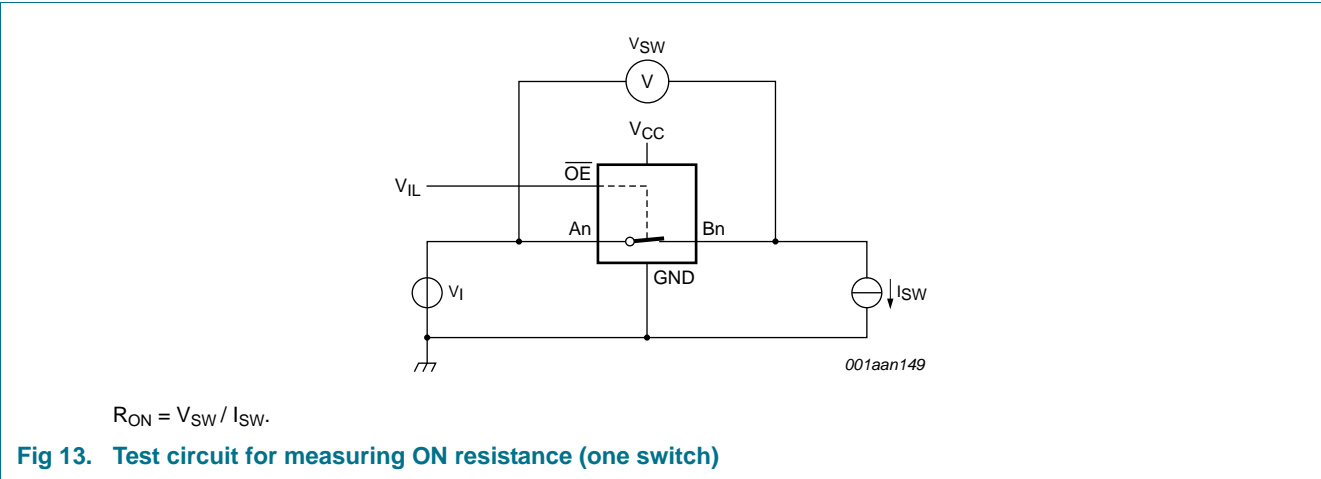
Table 7. Resistance R<sub>ON</sub>

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 13](#).

Symbol	Parameter	Conditions	T <sub>amb</sub> = −40 °C to +85 °C			T <sub>amb</sub> = −40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
R <sub>ON</sub>	ON resistance	V <sub>CC</sub> = 3.0 V to 3.6 V <a href="#">[2]</a>						
		I <sub>SW</sub> = 64 mA; V <sub>I</sub> = 0 V	-	3.7	7.0	-	10.0	Ω
		I <sub>SW</sub> = 24 mA; V <sub>I</sub> = 0 V	-	3.7	7.0	-	10.0	Ω
		I <sub>SW</sub> = 15 mA; V <sub>I</sub> = 1.2 V	-	4.7	10.0	-	12.0	Ω

- [1] Typical values are measured at T<sub>amb</sub> = 25 °C and nominal V<sub>CC</sub>.
- [2] Measured by the voltage drop between the An and Bn terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (An or Bn) terminals.

9.4 ON resistance test circuit





## 10. Dynamic characteristics

**Table 8. Dynamic characteristics**

$GND = 0\text{ V}$ ; for test circuit see [Figure 16](#)

Symbol	Parameter	Conditions	$T_{\text{amb}} = -40\text{ °C to }+85\text{ °C}$			$T_{\text{amb}} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$t_{\text{pd}}$	propagation delay	An to Bn or Bn to An; see <a href="#">Figure 14</a>  $V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	-	-	0.11	-	0.22	ns
$t_{\text{en}}$	enable time	$\overline{\text{OE}}$ to An or Bn; see <a href="#">Figure 15</a>  $V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	1.5	2.9	5.0	1.5	6.0	ns
$t_{\text{dis}}$	disable time	$\overline{\text{OE}}$ to An or Bn; see <a href="#">Figure 15</a>  $V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	0.8	3.3	7.0	0.8	8.0	ns

[1] All typical values are measured at  $T_{\text{amb}} = 25\text{ °C}$  and at nominal  $V_{\text{CC}}$ .

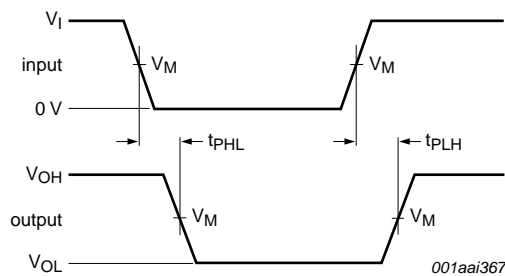
[2] The propagation delay is the calculated RC time constant of the on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).

[3]  $t_{\text{pd}}$  is the same as  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$ .

[4]  $t_{\text{en}}$  is the same as  $t_{\text{PZH}}$  and  $t_{\text{PZL}}$ .

[5]  $t_{\text{dis}}$  is the same as  $t_{\text{PHZ}}$  and  $t_{\text{PLZ}}$ .

### 10.1 Waveforms



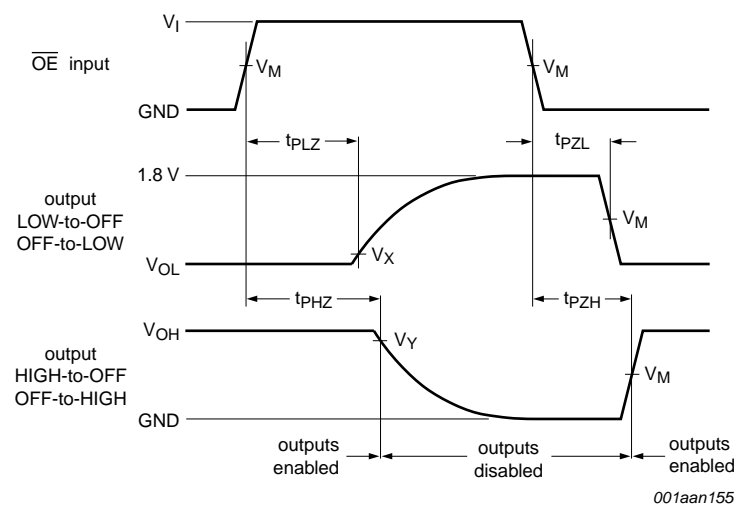
Measurement points are given in [Table 9](#).

Logic levels:  $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical output voltage levels that occur with the output load.

**Fig 14. The data input (An, Bn) to output (Bn, An) propagation delay times**

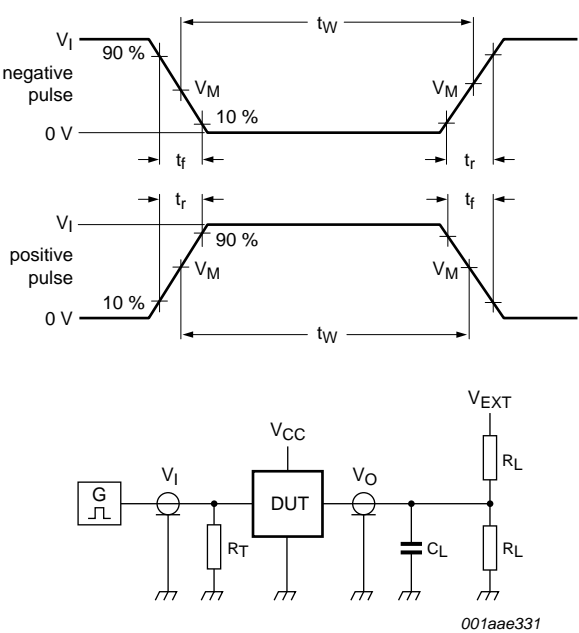
**Table 9. Measurement points**

Supply voltage	Input			Output		
$V_{\text{CC}}$	$V_{\text{M}}$	$V_{\text{I}}$	$t_{\text{r}} = t_{\text{f}}$	$V_{\text{M}}$	$V_{\text{X}}$	$V_{\text{Y}}$
3.0 V to 3.6 V	$0.5V_{\text{CC}}$	$V_{\text{CC}}$	$\leq 2.0\text{ ns}$	0.9 V	$V_{\text{OL}} + 0.15\text{ V}$	$V_{\text{OH}} - 0.15\text{ V}$



Measurement points are given in [Table 9](#).  
Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig 15. Enable and disable times



Test data is given in [Table 10](#).  
Definitions for test circuit:  
 $R_L$  = Load resistance.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.  
 $V_{EXT}$  = External voltage for measuring switching times.

Fig 16. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		$V_{EXT}$		
$V_{CC}$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
3.0 V to 3.6 V	30 pF	1 k $\Omega$	open	GND	3.6 V

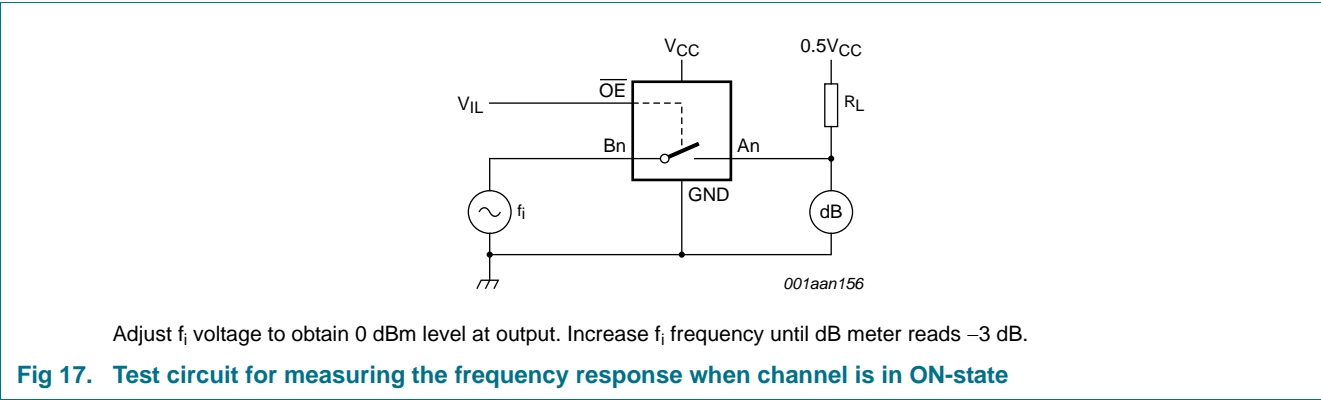
10.2 Additional dynamic characteristics

Table 11. Additional dynamic characteristics  
GND = 0 V.

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			Unit
			Min	Typ	Max	
f <sub>(-3dB)</sub>	-3 dB frequency response	V <sub>CC</sub> = 3.3 V; R <sub>L</sub> = 50 Ω; see <a href="#">Figure 17</a> <sup>[1]</sup>	-	575	-	MHz

[1] f<sub>i</sub> is biased at 0.5V<sub>CC</sub>.

10.3 Test circuit



11. Package outline

SSOP24: plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm SOT556-1

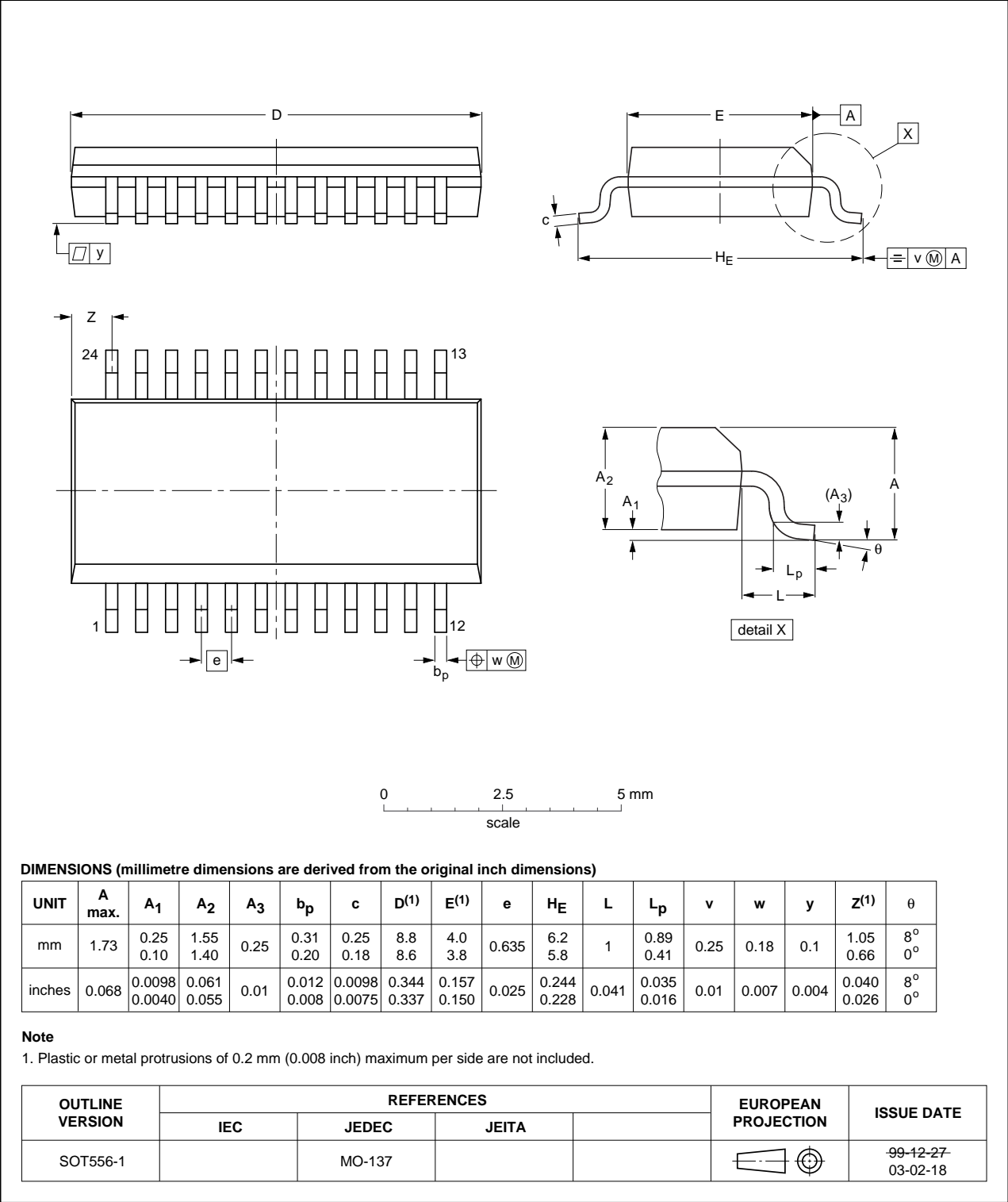


Fig 18. Package outline SOT556-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

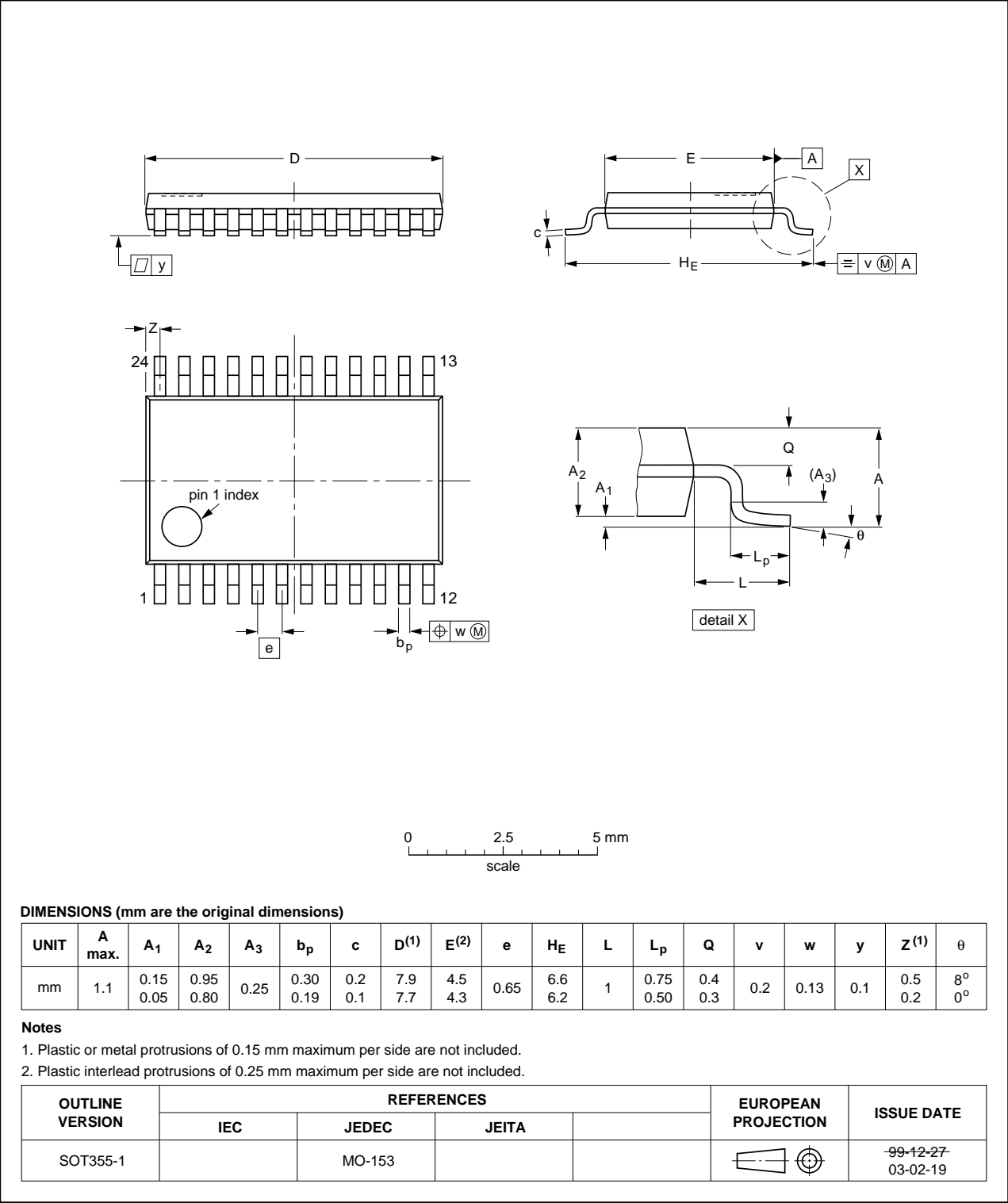


Fig 19. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package;  
no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

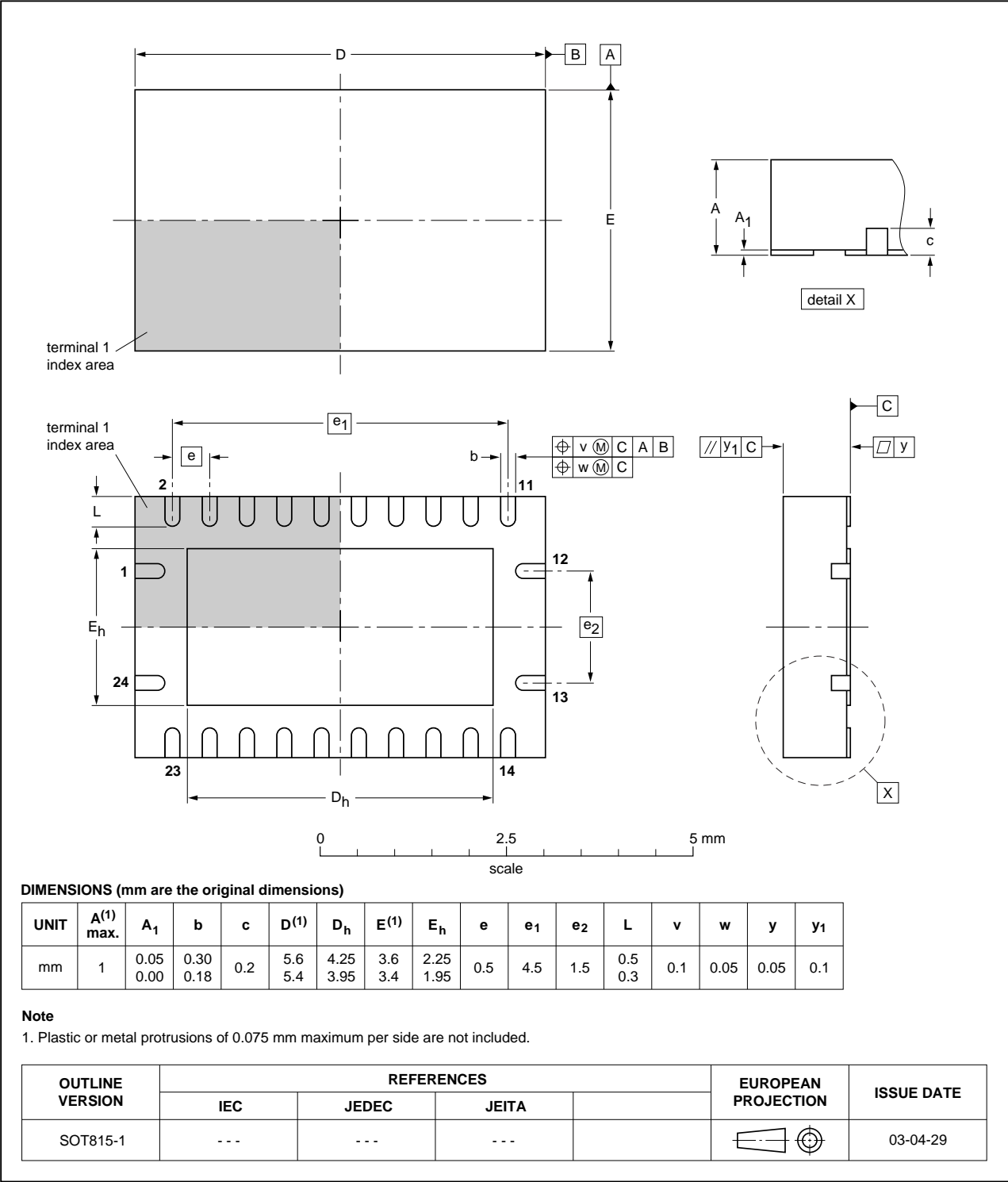


Fig 20. Package outline SOT815-1 (DHVQFN24)

## 12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

## 13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLVD3861 v.4	20111214	Product data sheet	-	74CBTLVD3861 v.3
Modifications:	• Legal pages updated.			
74CBTLVD3861 v.3	20111020	Product data sheet	-	74CBTLVD3861 v.2
74CBTLVD3861 v.2	20110117	Product data sheet	-	74CBTLVD3861 v.1
74CBTLVD3861 v.1	20101206	Product data sheet	-	-



## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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## 15. Contact information

For more information, please visit: <http://www.nexperia.com>

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