16-Bit Sigma-Delta ADC with Programmable Postprocessor

AD7725

FEATURES

Programmable Filtering:
- Any Characteristic up to 108 Tap FIR and/or IIR

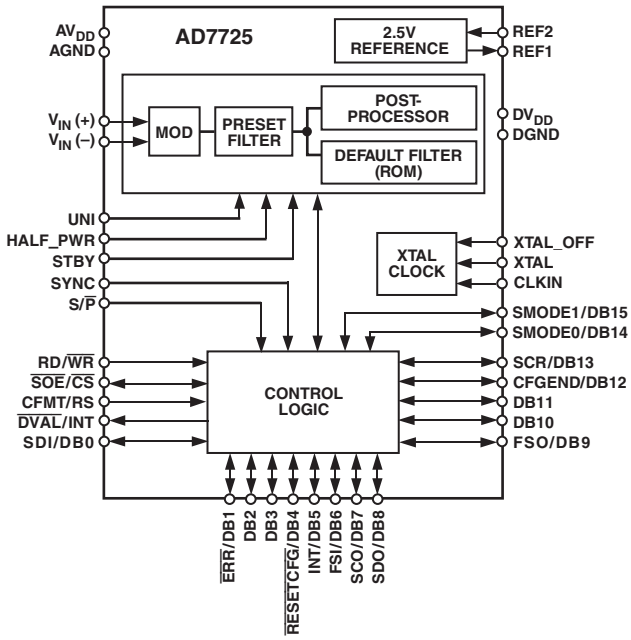
Polynomial Signal Conditioning up to 8th Order
Programmable Decimation and Output Word Rate
Flexible Programming Modes:
- Boot from DSP or External EPROM
- Parallel/Serial Interface

Internal Default Filter for Evaluation
14.4 MHz Max Master Clock Frequency
0 V to +4 V (Single-Ended) or ±2 V (Differential) Input Range
Power Supplies: AV_{DD}, DV_{DD}: 5 V ±5%
On-Chip 2.5 V Voltage Reference
44-Lead MQFP Package

TYPICAL APPLICATIONS

Radar
Sonar
Auxiliary Car Functions
Medical Communications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7725 is a complete 16-bit, sigma-delta analog-to-digital converter with on-chip, user-programmable signal conditioning. The output of the modulator is processed by three cascaded finite impulse response (FIR) filters, followed by a fully user-programmable postprocessor. The postprocessor provides processing power of up to 130 million accumulates (MAC) per second. The user has complete control over the filter response, the filter coefficients, and the decimation ratio.

The postprocessor permits the signal conditioning characteristics to be programmed through a parallel or serial interface. It is programmed by loading a user-defined filter in the form of a configuration file. This filter can be loaded from a DSP or an external serial EPROM. It is generated using a digital filter design package called Filter Wizard, which is available from the AD7725 section on the Analog Devices website. Filter Wizard allows the user to design different filter types and generates the appropriate configuration file to be downloaded to the postprocessor. The AD7725 also has an internal default filter for evaluation purposes.

It provides 16-bit performance for input bandwidths up to 350 kHz with an output word rate of 900 kHz maximum. The input sample rate is set either by the crystal oscillator or an external clock.

This part has an accurate on-chip 2.5 V reference for the modulator. A reference input/output function is provided to allow either the internal reference or an external system reference to be used as the reference source for the modulator.

The device is available in a 44-lead MQFP package and is specified over a –40°C to +85°C temperature range.

REV. 0

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AD7725—SPECIFICATIONS[1] (AV_{DD} = 5 V ±5%, AGND = AGND1 = AGND2 = DGND = 0 V, F_{CLKIN}[2] = 9.6 MHz, REF2 = 2.5 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Test Conditions/Comments	B Version Min	Typ	Max	Unit
DYNAMIC SPECIFICATIONS	When tested with the FIR filter in Figure 1. HALF_PWR = Logic High				
Bipolar Mode					
Signal to Noise[3]	Measurement Bandwidth = 0.5 × F_O[4]				
	2.5 V Reference	77	83		dB
	3 V Reference	79	85		dB
Total Harmonic Distortion[3, 5]			–94	–86	dB
Spurious Free Dynamic Range[3, 5]			–98	–89	dB
Unipolar Mode					
Signal to Noise[3]	Measurement Bandwidth = 0.5 × F_O[4]		83		dB
Total Harmonic Distortion[3, 5]			–94		dB
ANALOG INPUTS					
Full-Scale Input Span	$V_{IN}(+) - V_{IN}(-)$				
Bipolar Mode	Differential or Single-Ended Input			±4/5 × V_{REF2}	V
Unipolar Mode	Single-Ended Input	0		8/5 × V_{REF2}	V
Absolute Input Voltage	$V_{IN}(+)$ and/or $V_{IN}(-)$	AGND		AV_{DD}	V
Input Sampling Capacitance			2		pF
Input Sampling Rate, F_{CLKIN}				14.4[6]	MHz
CLOCK					
CLKIN Duty Ratio		45		55	%
REFERENCE					
REF1 Output Resistance			3.5		kΩ
Reference Buffer					
Offset Voltage	Offset between REF1 and REF2		±3		mV
Using Internal Reference					
REF2 Output Voltage		2.39	2.54	2.69	V
REF2 Output Voltage Drift			60		ppm/°C
Using External Reference					
REF2 Input Impedance	REF1 = AGND		8		kΩ
REF2 External Voltage Input[7]			2.5		V
STATIC PERFORMANCE					
Resolution		16			Bits
Differential Nonlinearity (DNL)[3]	Guaranteed Monotonic		±0.5	±1[8]	LSB
Integral Nonlinearity (INL)[3]			±2		LSB
DC CMRR			80		dB
Offset Error			±20		mV
Gain Error[3, 9]			±0.5		%FSR
LOGIC INPUTS (Excluding CLKIN)					
V_{INH}, Input High Voltage		2.0			V
V_{INL}, Input Low Voltage				0.8	V
CLOCK INPUT (CLKIN)					
V_{INH}, Input High Voltage		0.7 × DV_{DD}			V
V_{INL}, Input Low Voltage				0.3 × DV_{DD}	V

Parameter	Test Conditions/Comments	B Version Min	Typ	Max	Unit
ALL LOGIC INPUTS					
I_{IN}, Input Current	V_{IN} = 0 V to DV_{DD}			±10	μA
C_{IN}, Input Capacitance			10		pF
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	$\|I_{OUT}\|$ = 200 μA	4.0			V
V_{OL}, Output Low Voltage	$\|I_{OUT}\|$ = 1.6 mA			0.4	V
POWER SUPPLIES[10]					
AV_{DD}		4.75		5.25	V
AI_{DD}[11]	HALF_PWR = Logic High[12]		28	33	mA
DV_{DD}		4.75		5.25	V
DI_{DD}[13]	With the Filter in Figure 1.		84	90	mA
Power Consumption[14]	Standby Mode		30		mW

NOTES
[1]Operating Temperature Range is as follows: B Version: –40°C to +85°C.
[2]F_{CLKIN} is the CLKIN frequency.
[3]See Terminology section.
[4]F_O = Output Data Rate.
[5]When using the internal reference, THD and SFDR specifications apply only to input signals above 10 kHz with a 10 μF decoupling capacitor between REF2 and AGND2. At frequencies below 10 kHz, THD degrades to –80 dB and SFDR degrades to –83 dB.
[6]See Figures 23 and 24 for information regarding the number of filter taps allowed and the current consumption as the CLKIN frequency is varied.
[7]The AD7725 can operate with an external reference input in the range of 1.2 V to 3.15 V.
[8]Guaranteed by the design.
[9]Gain Error excludes reference error.
[10]All I_{DD} tests are done with the digital inputs equal to 0 V or DV_{DD}.
[11]Analog current does not vary as the CLKIN frequency and the number of filter taps used in the postprocessor is varied.
[12]If HALF_PWR is logic low, AI_{DD} will typically double.
[13]Digital current varies as the CLKIN frequency and the number of filter taps used in the postprocessor is varied. See Figures 23 and 24.
[14]Digital inputs static and equal to 0 or DV_{DD}.

Specifications subject to change without notice.

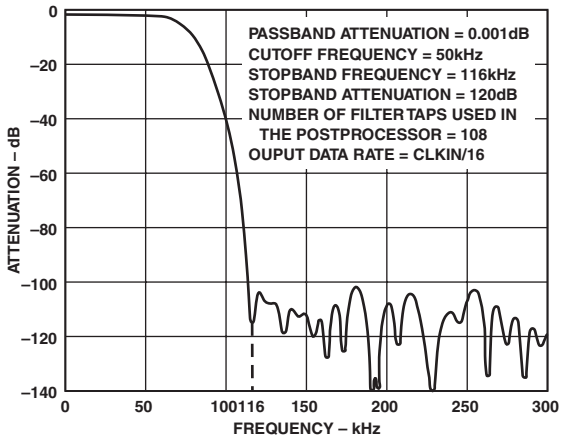

Figure 1. Digital Filter Characteristics Used for Specifications

Preset Filter, Default Filter, and Postprocessor Characteristics[1, 2]

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL FILTER RESPONSE					
PRESET FIR					
Data Output Rate				$F_{CLKIN}/8$	Hz
Stop-Band Attenuation		70			dB
Low-Pass Corner Frequency			$F_{CLKIN}/16$		Hz
Group Delay[3]			$133/(2 \times F_{CLKIN})$		s
Settling Time[3]			$133/F_{CLKIN}$		s
DEFAULT FILTER	Internal FIR Filter Stored in ROM				
Number of Taps				106	
Frequency Response					
0 kHz to $F_{CLKIN}/546.08$				±0.001	dB
$F_{CLKIN}/195.04$		–3			dB
$F_{CLKIN}/184.08$		–6			dB
$F_{CLKIN}/133.2$ to $F_{CLKIN}/2$				–120	dB
Group Delay[3]			$2141/(2 \times F_{CLKIN})$		s
Settling Time[3]			$2141/F_{CLKIN}$		s
Output Data Rate, F_O			$F_{CLKIN}/32$		Hz
POSTPROCESSOR CHARACTERISTICS					
Input Data Rate				$F_{CLKIN}/8$	Hz
Coefficient Precision[4]			24		Bits
Arithmetic Precision			30		Bits
No. of Taps Permitted				108	
Decimation Factor		2		256	
No. of Decimation Stages		1		5	
Output Data Rate		$F_{CLKIN}/4096$		$F_{CLKIN}/16$	Hz

NOTES
[1]These characteristics are fixed by the design.
[2]F_{CLKIN} is the CLKIN frequency.
[3]See Terminology.
[4]See the Configuration File Format section for more information.

TIMING SPECIFICATIONS[1, 2] (AV_{DD} = 5 V ±5%; DV_{DD} = 5 V ±5%; AGND = DGND = 0 V, REF2 = 2.5 V, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
CLKIN Frequency	f_{CLKIN}	1		14.4	MHz
CLKIN Period ($t_{CLK} = 1/f_{CLKIN}$)	t_1	0.07		1	µs
CLKIN Low Pulsewidth	t_2	0.45 × t_1		0.55 × t_1	
CLKIN High Pulsewidth	t_3	0.45 × t_1		0.55 × t_1	
CLKIN Rise Time	t_4	5			ns
CLKIN Fall Time	t_5	5			ns
CLKIN to SCO Delay	t_6		35	50	ns
SCO Period: SCR = 0	t_7		1		t_{CLK}
SCR = 1	t_7		2		t_{CLK}
SERIAL INTERFACE (DSP MODE ONLY)					
FSI Setup Time before SCO Transition	t_8	30			ns
FSI Hold Time after SCO Transition	t_9	0			ns
SDI Setup Time	t_{10}	30			ns
SDI Hold Time	t_{11}	0			ns
SERIAL INTERFACE (DSP AND BFR MODES)					
SCO Transition to FSO High Delay	t_{12}			20	ns
SCO Transition to FSO Low Delay	t_{13}			20	ns
SDO Setup before SCO Transition	t_{14}			10	ns
SDO Hold after SCO Transition	t_{15}	0			ns
SERIAL INTERFACE (EPROM MODE)					
SCO High Time	t_{16}			8	t_{CLK}
SCO Low Time	t_{17}			8	t_{CLK}
$\overline{SOE}$ Low to First SCO Rising Edge	t_{18}			20	t_{CLK}
Data Setup before SCO Rising Edge	t_{19}		22		ns
PARALLEL INTERFACE					
DATA WRITE					
RS Low to $\overline{CS}$ Low	t_{20}	15			ns
$\overline{WR}$ Setup before $\overline{CS}$ Low	t_{21}	15			ns
RS Hold after $\overline{CS}$ Rising Edge	t_{22}	0			ns
$\overline{CS}$ Pulsewidth	t_{23}	50			ns
$\overline{WR}$ Hold after $\overline{CS}$ Rising Edge	t_{24}	0			ns
Data Setup Time	t_{25}	10			ns
Data Hold Time	t_{26}	5			ns
DATA READ					
RS Low to $\overline{CS}$ Low	t_{27}	15			ns
RD Setup before $\overline{CS}$ Low	t_{28}	15			ns
RS Hold after $\overline{CS}$ Rising Edge	t_{29}	0			ns
RD Hold after $\overline{CS}$ Rising Edge	t_{30}	0			ns
Data Valid after $\overline{CS}$ Falling Edge[3]	t_{31}			30	ns
Data Hold after $\overline{CS}$ Rising Edge	t_{32}	10			ns
STATUS READ/INSTRUCTION WRITE					
$\overline{CS}$ Duty Cycle	t_{33}	1			t_{CLK}
Interrupt Clear after $\overline{CS}$ Low	t_{34}			15	ns
RD Setup to $\overline{CS}$ Low	t_{35}	15			ns
RD Hold after $\overline{CS}$ Rising Edge	t_{36}			0	ns
Read Data Access Time[3]	t_{37}			30	ns
Read Data Hold after $\overline{CS}$ Rising Edge	t_{38}	10			ns
Write Data Setup before $\overline{CS}$ Rising Edge	t_{39}	10			ns
Write Data Hold after $\overline{CS}$ Rising Edge	t_{40}	5			ns

NOTES
[1]Guaranteed by design.
[2]Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.
[3]Measured with the load circuit in Figure 2 and defined as the time required for the output to cross 0.8 V and 2.4 V.

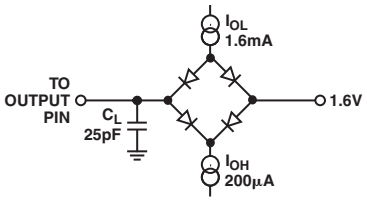

Figure 2. Load Circuit for Digital Output Timing Specifications

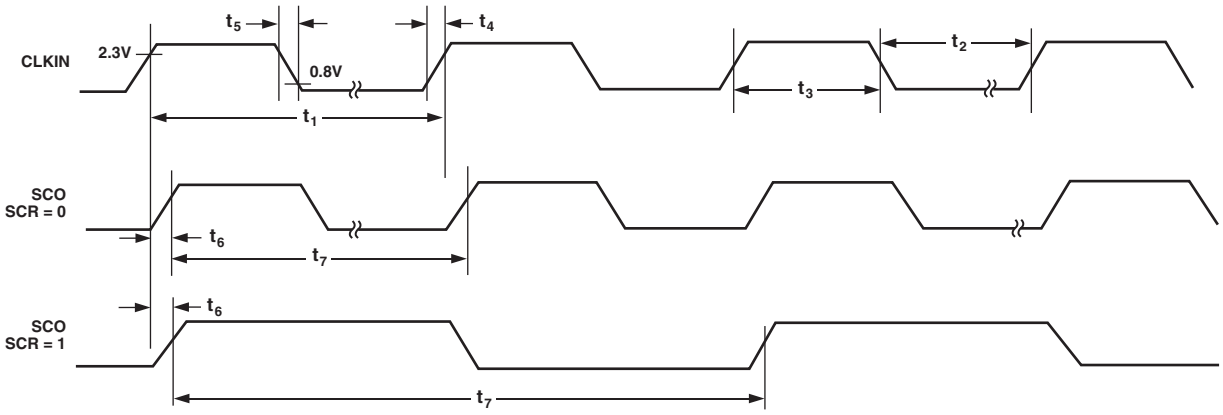

Figure 3. CLKIN to SCO Relationship

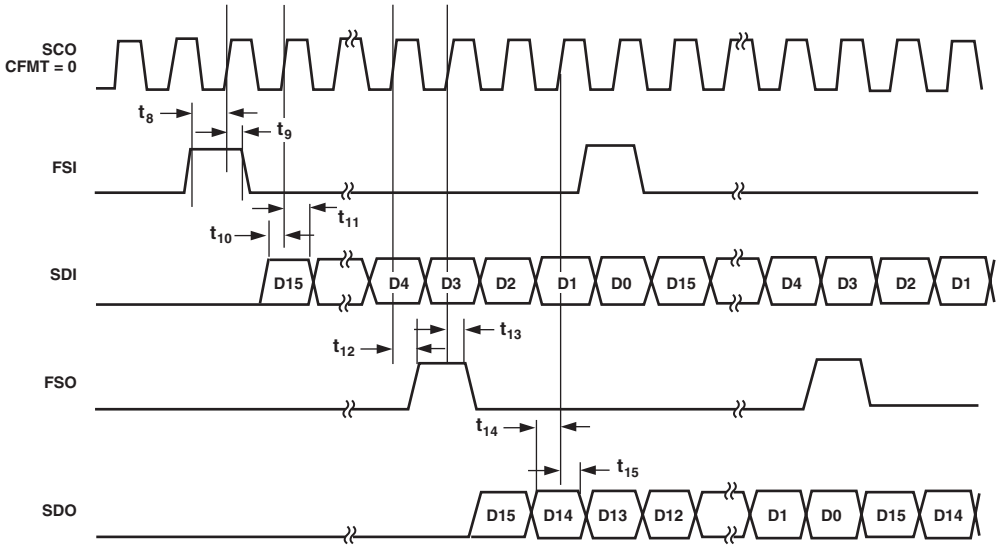

Figure 4. Serial Mode (DSP Mode and Boot from ROM (BFR) Mode). In BFR Mode, FSI and SDI Are Not Used.

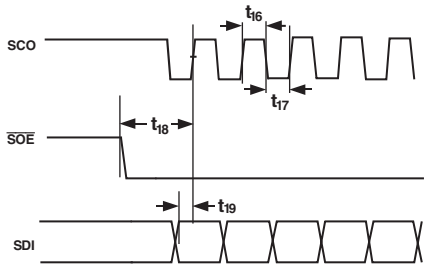

Figure 5. Serial Mode (EPROM Mode)

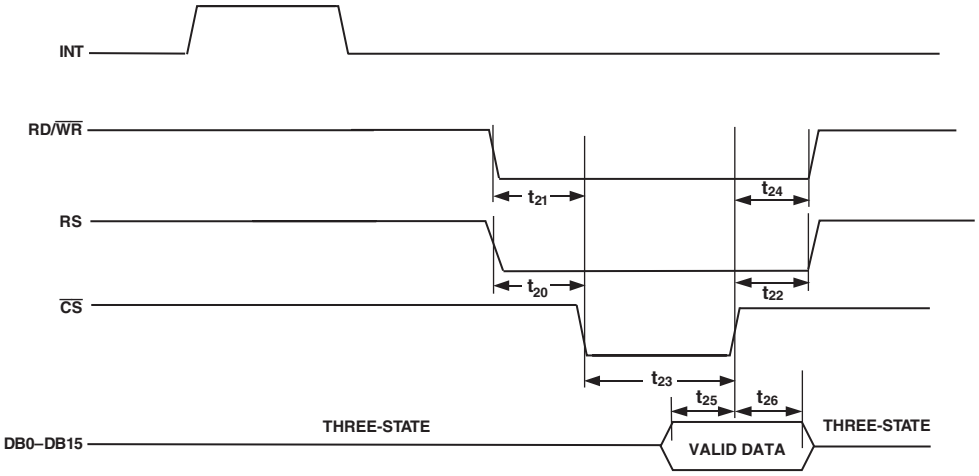

Figure 6. Parallel Mode (Writing Data to the AD7725)

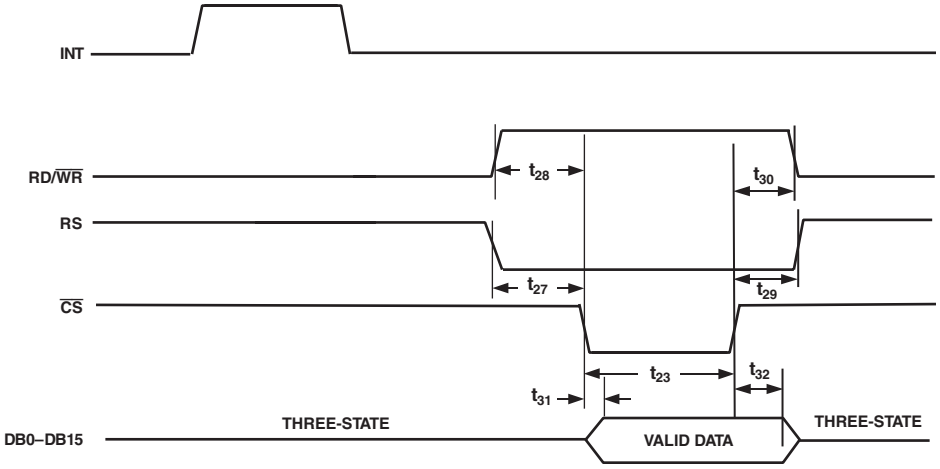

Figure 7. Parallel Mode (Reading Data to the AD7725)

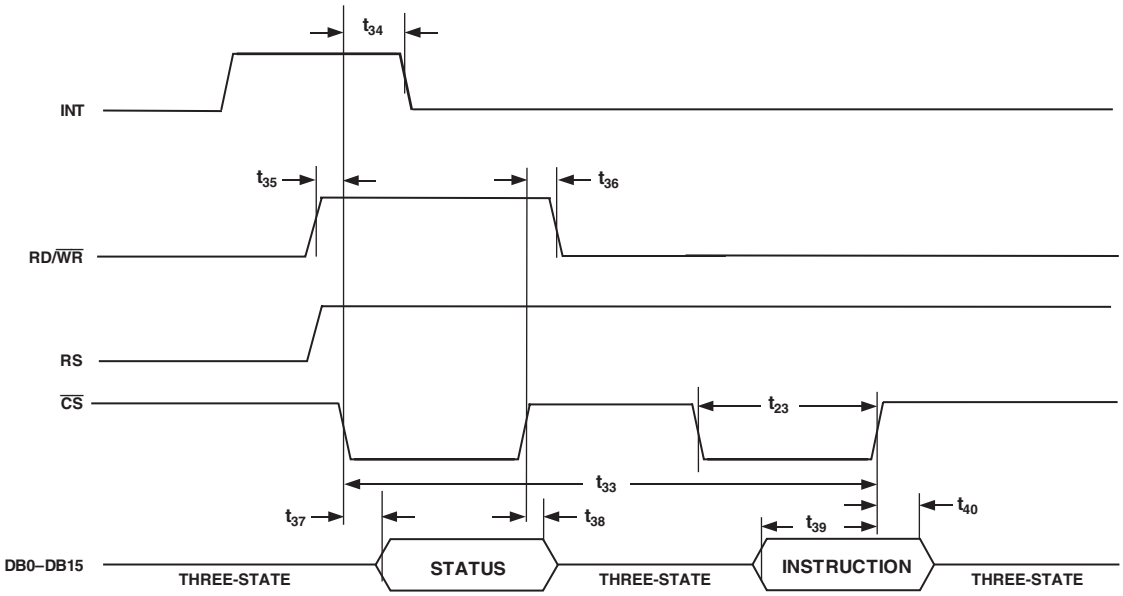

Figure 8. Parallel Mode (Reading the Status Register and Writing Instructions)

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

DV_{DD} to DGND ..... –0.3 V to +7 V
AV_{DD} to AGND ..... –0.3 V to +7 V
AV_{DD}, AV_{DD1} to DV_{DD} ..... –1 V to +1 V
AGND, AGND1 to DGND ..... –0.3 V to +0.3 V
Digital Inputs to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Digital Outputs to DGND ..... –0.3 V to DV_{DD} + 0.3 V
V_{IN}(+), V_{IN}(–) to AGND ..... –0.3 V to AV_{DD} + 0.3 V
REF1 to AGND ..... –0.3 V to AV_{DD} + 0.3 V
REF2 to AGND ..... –0.3 V to AV_{DD} + 0.3 V
REFIN to AGND ..... –0.3 V to AV_{DD} + 0.3 V
DGND, AGND ..... ±0.3 V
Input Current to Any Pin Except Supplies[2] ..... ±10 mA
I_{DD} (AI_{DD} + DI_{DD}) ..... 150 mA
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
θ_{JA} Thermal Impedance ..... 58° C/W
θ_{JC} Thermal Impedance ..... 20° C/W
Lead Temperature, Soldering
  Vapor Phase (60 sec) ..... 215°C
  Infrared (15 sec) ..... 220°C
ESD ..... 2 kV

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD7725BS	–40°C to +85°C	Plastic Quad Flatpack	S-44
EVAL-AD7725CB[2]		Evaluation Board	
EVAL-CONTROL BRD2[3]		Controller Board	

[1] S = Plastic Quad Flatpack (MQFP)

[2] This board can be used as a standalone evaluation board or in conjunction with the Evaluation Board Controller for evaluation/demonstration purposes. It is accompanied by software and technical documentation.

[3] Evaluation Board Controller. This board is a complete unit allowing a PC to control and communicate with all Analog Devices boards ending in the CB designator. To obtain the complete evaluation kit, the following needs to be ordered: EVAL-AD7725CB, EVAL-CONTROL BRD2, and a 12 V ac transformer. The Filter Wizard software can be downloaded from the Analog Devices website.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7725 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.