



SILEGO

SLG59H1127V

A 12 V, 15 mΩ, 4 A Integrated Power Switch with VIN Lockout Select and Power Good Output

General Description

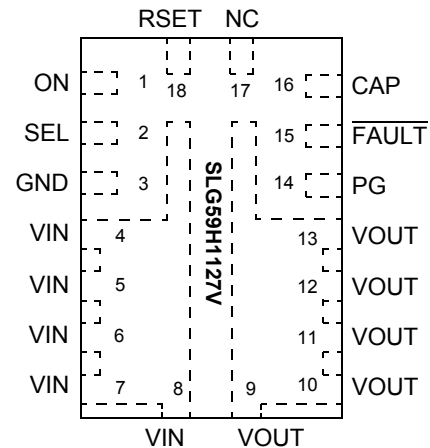
The SLG59H1127V is a high-performance, self-powered 15 mΩ NMOS power switch designed for all 4.5 to 12 V power rails up to 4A. Using a proprietary MOSFET design, the SLG59H1127V achieves a stable 15 mΩ $R_{DS(ON)}$ across a wide input voltage range. Using Silego's proprietary CuFET™ technology, the SLG59H1127V package also exhibits a low thermal resistance for high-current operation.

Designed to operate over a -40°C to 85°C range, the SLG59H1127V is available in a low thermal resistance, RoHS-compliant, 1.6 x 3.0 mm STQFN package.

Features

- Wide Operating Input Voltage: 4.5 V to 13.2 V
- Maximum Continuous Switch Current: 4 A
- Automatic nFET SOA Protection
- High-performance MOSFET Switch
 - Low $R_{DS(ON)}$: 15 mΩ at $V_{IN} = 12$ V
 - Low $\Delta R_{DS(ON)}/\Delta V_{IN}$: < 0.05 mΩ/V
 - Low $\Delta R_{DS(ON)}/\Delta T$: < 0.06 mΩ/°C
- Capacitor-adjustable Inrush Current Control
- Two stage Current Limit Protection:
 - Resistor-adjustable Active Current Limit
 - Internal Short-circuit Current limit
- Open-drain Power Good (PG) Signaling
- Open Drain FAULT Signaling
- Fast 4 kΩ Output Discharge
- Pb-Free / Halogen-Free / RoHS Compliant Packaging

Pin Configuration



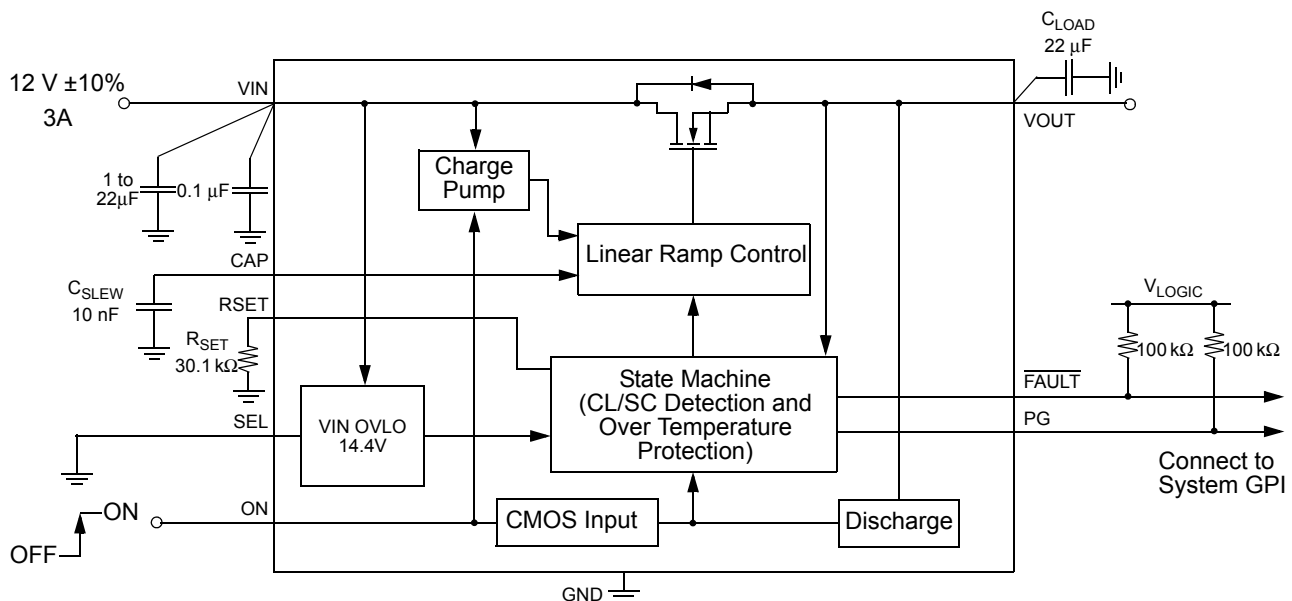
18-pin STQFN

1.6 x 3.0 mm, 0.40mm pitch
(Top View)

Applications

- Enterprise Computing & Telecom Equipment
 - 5V and 12V Point-of-Load Power Distribution
- PCI/PCIe Adapter Cards
- General-purpose High-voltage, Power-Rail Switching
- Multifunction Printers
- Fan Motor Control

Block Diagram and a 12V / 3 A Typical Application Circuit





Pin Description

Pin #	Pin Name	Type	Pin Description
1	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59H1127V's state machine. ON is an asserted HIGH, level-sensitive CMOS input with $V_{IL} < 0.3 \text{ V}$ and $V_{IH} > 0.9 \text{ V}$. As the ON pin input circuit does not have an internal pull-down resistor, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller – do not allow this pin to be open-circuited.
2	SEL	Input	Connect this pin to GND.
3	GND	GND	Pin 3 is the main ground connection for the SLG59H1127V's internal charge pump, its gate drive and current-limit circuits as well as its internal state machine. Therefore, use a short, stout connection from Pin 3 to the system's analog or power plane.
4-8	VIN	MOSFET	VIN supplies the power for the operation of the SLG59H1127V, its internal control circuitry, and the drain terminal of the nFET power switch. With 5 pins fused together at VIN, connect a 22 μF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VIN should be rated at 20 V or higher.
9-13	VOUT	MOSFET	Source terminal of n-channel MOSFET (5 pins fused for VOUT). Connect a 22 μF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VOUT should be rated at 20 V or higher.
14	PG	Output	An open-drain output, PG is asserted within TPG_{HIGH} when V_{OUT} is higher than the SLG59H1127's $PG_{TRIGGER}$ threshold. PG output becomes deasserted within TPG_{LOW} when V_{OUT} is less than the PG_{HYS} threshold. PG is not defined for $V_{IN} < 4 \text{ V}$.
15	$\overline{\text{FAULT}}$	Output	An open drain output, $\overline{\text{FAULT}}$ is asserted within $T\overline{\text{FAULT}}_{LOW}$ when a V_{IN} overvoltage, a current-limit, or an over-temperature condition is detected. $\overline{\text{FAULT}}$ is deasserted within $T\overline{\text{FAULT}}_{HIGH}$ when the fault condition is removed. Connect an 100 k Ω external resistor from the $\overline{\text{FAULT}}$ pin to local system logic supply.
16	CAP	Output	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the V_{OUT} slew rate and overall turn-on time of the SLG59H1127V. For best performance, the range for C_{SLEW} values are $10 \text{ nF} \leq C_{SLEW} \leq 20 \text{ nF}$ – please see typical characteristics for additional information. Capacitors used at the CAP pin should be rated at 10 V or higher. Please consult Applications Section on how to select C_{SLEW} based on V_{OUT} slew rate and loading conditions.
17	NC	NC	No Connect
18	RSET	Input	A 1%-tolerance, metal-film resistor between 18 k Ω and 95 k Ω sets the SLG59H1127V's active current limit. A 95 k Ω resistor sets the SLG59H1127V's active current limit to 1 A and a 18 k Ω resistor sets the active current limit to 5 A.

Ordering Information

Part Number	Type	Production Flow
SLG59H1127V	STQFN 18L FC	Industrial, -40 °C to 85 °C
SLG59H1127VTR	STQFN 18L FC (Tape and Reel)	Industrial, -40 °C to 85 °C



Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN} to GND	Power Switch Input Voltage to GND	Continuous	-0.3	--	16	V
		Maximum pulsed V_{IN} , pulse width <0.1s	--	--	18	V
V_{OUT} to GND	Power Switch Output Voltage to GND		-0.3	--	V_{IN}	V
ON, SEL, CAP, RSET, PG, and FAULT to GND	ON, SEL, CAP, RSET, PG, and FAULT Pin Voltages to GND		-0.3	--	7	V
T_S	Storage Temperature		-65	--	150	°C
ESD _{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD _{CDM}	ESD Protection	Charged Device Model	500	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Thermal Resistance; 1.6 x 3.0 mm 18L STQFN	Determined using 1 in ² , 1 oz. copper pads under each VIN and VOUT terminal and FR4 pcb material.	--	40	--	°C/W
		Determined using 0.25 in ² , 1 oz. copper pads under each VIN and VOUT terminal and FR4 pcb material.	--	77	--	°C/W
		Determined using 0.008 in ² , 1 oz. copper pads under each VIN and VOUT terminal and FR4 pcb material.	--	125	--	°C/W
MOSFET IDS _{CONT}	Continuous Current from VIN to VOUT	$T_J < 150^\circ\text{C}$	--	--	4	A
MOSFET IDS _{PEAK}	Peak Current from VIN to VOUT	Maximum pulsed switch current, pulse width < 1 ms	--	--	6	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

4.5 V ≤ V_{IN} ≤ 13.2 V; C_{IN} = 22 μF, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating Input Voltage		4.5	--	13.2	V
$V_{IN(OVLO)}$	V_{IN} Overvoltage Lockout Threshold	$V_{IN} \uparrow$; SEL = 0	13.5	14.4	15.2	V
$V_{IN(OVLOHYST)}$	V_{IN} Overvoltage Lockout Hysteresis		--	2	--	%
$V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout Threshold	$V_{IN} \downarrow$	2.4	--	3.8	V
I_Q	Quiescent Supply Current	ON = HIGH; $I_{DS} = 0$ A	--	0.5	0.6	mA
I_{SHDN}	OFF Mode Supply Current	ON = LOW; $I_{DS} = 0$ A	--	1	3	μA
RDS _{ON}	ON Resistance	$T_A = 25^\circ\text{C}$; $I_{DS} = 0.1$ A	--	15	18	mΩ
		$T_A = 85^\circ\text{C}$; $I_{DS} = 0.1$ A	--	22	24	mΩ



Electrical Characteristics (continued)

4.5 V ≤ V_{IN} ≤ 13.2 V; C_{IN} = 22 μF, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
MOSFET I _{DS}	Current from VIN to VOUT	Continuous	--	--	4	A
I _{LIMIT}	Active Current Limit, I _{ACL}	V _{OUT} > 0.5 V; R _{SET} = 30.1 kΩ	2.8	3.2	3.6	A
	Short-circuit Current Limit, I _{SCL}	V _{OUT} < 0.5 V	--	0.5	--	A
T _{ACL}	Active Current Limit Response Time		--	120	--	μs
R _{DSCHRG}	Output Discharge Resistance		3.5	4.4	5.3	kΩ
C _{LOAD}	Output Load Capacitance	C _{LOAD} connected from VOUT to GND	--	22	--	μF
T _{ON_Delay}	ON Delay Time	50% ON to 10% V _{OUT} ↑; V _{IN} = 4.5 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	--	0.4	0.5	ms
		50% ON to 10% V _{OUT} ↑; V _{IN} = 12 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	--	0.7	0.9	ms
T _{Total_ON}	Total Turn-on Time	50% ON to 90% V _{OUT} ↑	Set by External C _{SLEW} ¹			ms
		50% ON to 90% V _{OUT} ↑; V _{IN} = 4.5 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	--	1.6	2.1	ms
		50% ON to 90% V _{OUT} ↑; V _{IN} = 12 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	--	4	6	ms
V _{OUT(SR)}	V _{OUT} Slew rate	10% V _{OUT} to 90% V _{OUT} ↑	Set by External C _{SLEW} ¹			V/ms
		10% V _{OUT} to 90% V _{OUT} ↑; V _{IN} = 4.5 to 12 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	2.7	3.2	3.9	V/ms
T _{OFF_Delay}	OFF Delay Time	50% ON to V _{OUT} ↓; V _{IN} = 4.5 V to 12 V; R _{LOAD} = 100 Ω, No C _{LOAD}	--	15	--	μs
T _{FALL}	V _{OUT} Fall Time	90% V _{OUT} ↓ to 10% V _{OUT} ↓; V _{IN} = 4.5 V to 12 V; R _{LOAD} = 100 Ω, No C _{LOAD}	10.4	12.7	25	μs
T _{FAULT_LOW}	FAULT Assertion Time	Abnormal Step Load Current event to Fault ↓ I _{ACL} = 1 A; V _{IN} = 12 V; R _{SET} = 95 kΩ; switch in 10 Ω load;	--	80	--	μs
T _{FAULT_HIGH}	FAULT De-assertion Time	Delay to FAULT ↑ after fault condition is removed; I _{ACL} = 1 A; V _{IN} = 12 V; R _{SET} = 95 kΩ; switch out 10 Ω load	--	180	--	μs
FAULT _{VOL}	FAULT Output Low Voltage	I _{FAULT} = 1 mA	--	0.2	--	V
V _{PG(OL)}	PG Pin Output Low Voltage	V _{LOGIC} = 5 V, I _{PG(OL)} = -0.1 mA	--	--	0.4	V
V _{PG(OH)}	PG Pin Output High Voltage	V _{LOGIC} = 5 V, I _{PG(OH)} = 0.1 mA	V _{LOGIC} - 0.4	--	V _{LOGIC}	V
PG _{TRIGGER}	Power Good Threshold Voltage Level	V _{OUT} % of V _{IN}	86	90	94	%
PG _{HYS}	Power Good Hysteresis ↓	V _{OUT} ↓ % of V _{IN}	81	85	89	%
TPG _{HIGH}	PG Assertion Time	Delay to PG ↑ after PG _{TRIGGER} threshold is crossed.	1	1.25	1.5	ms
TPG _{LOW}	PG De-assertion Time	Delay to PG ↓ after PG _{TRIGGER} threshold is crossed.	--	7	--	μs
ON_V _{IH}	ON Pin Input High Voltage		0.9	--	5	V



Electrical Characteristics (continued)

4.5 V \leq V_{IN} \leq 13.2 V; C_{IN} = 22 μ F, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C

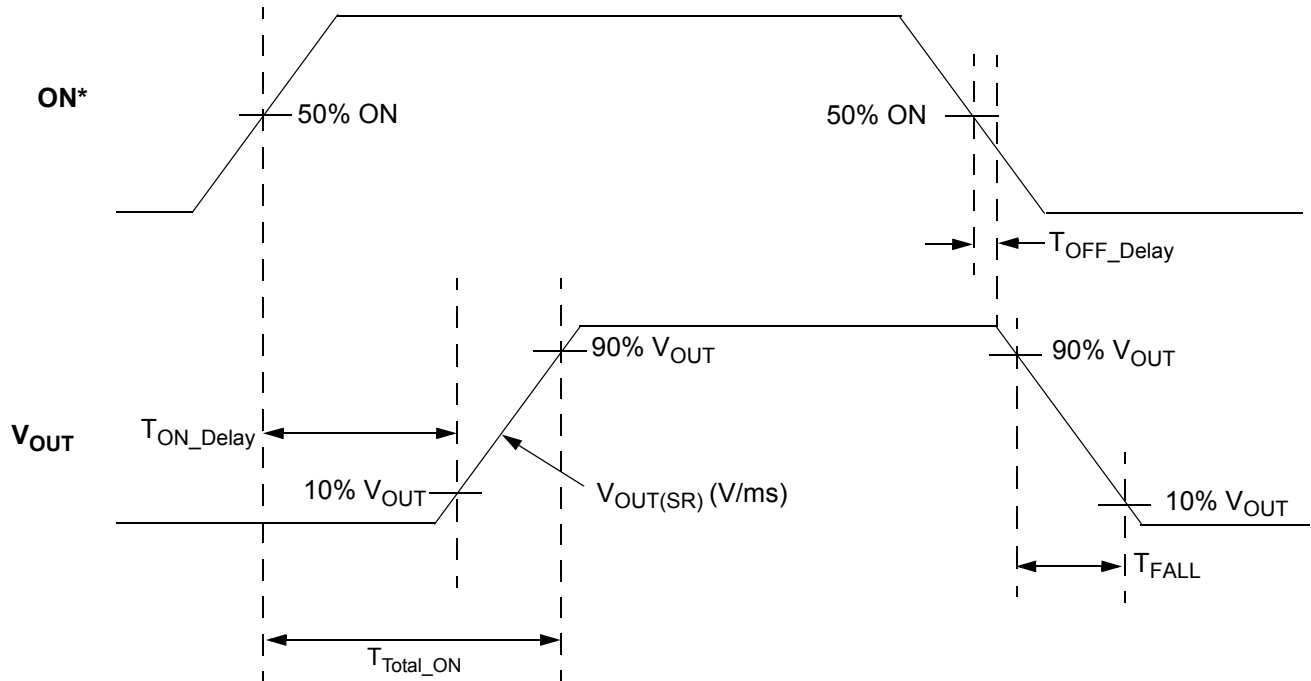
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
ON_V _{IL}	ON Pin Input Low Voltage		-0.3	0	0.3	V
SEL_V _{IH}	SEL pin Input High Voltage		1.65	--	4.5	V
SEL_V _{IL}	SEL pin Input Low Voltage		-0.3	--	0.3	V
I _{ON(Leakage)}	ON Pin Leakage Current	1V \leq ON \leq 5V or ON = GND	--	--	1	μ A
THERM _{ON}	Thermal Protection Shutdown Threshold		--	125	--	°C
THERM _{OFF}	Thermal Protection Restart Threshold		--	100	--	°C

Notes:

1. Refer to typical Timing Parameter vs. C_{SLEW} performance charts for additional information when available.

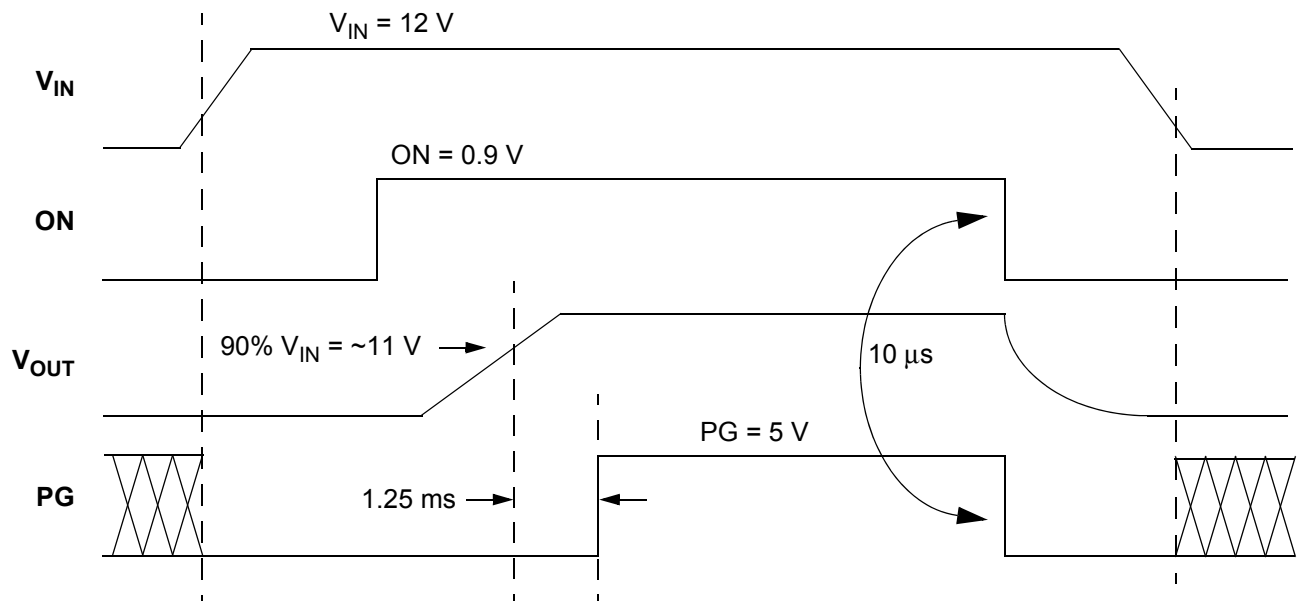


$T_{\text{Total_ON}}$, $T_{\text{ON_Delay}}$ and Slew Rate Measurement Timing Details



* Rise and Fall times of the ON signal are 100 ns

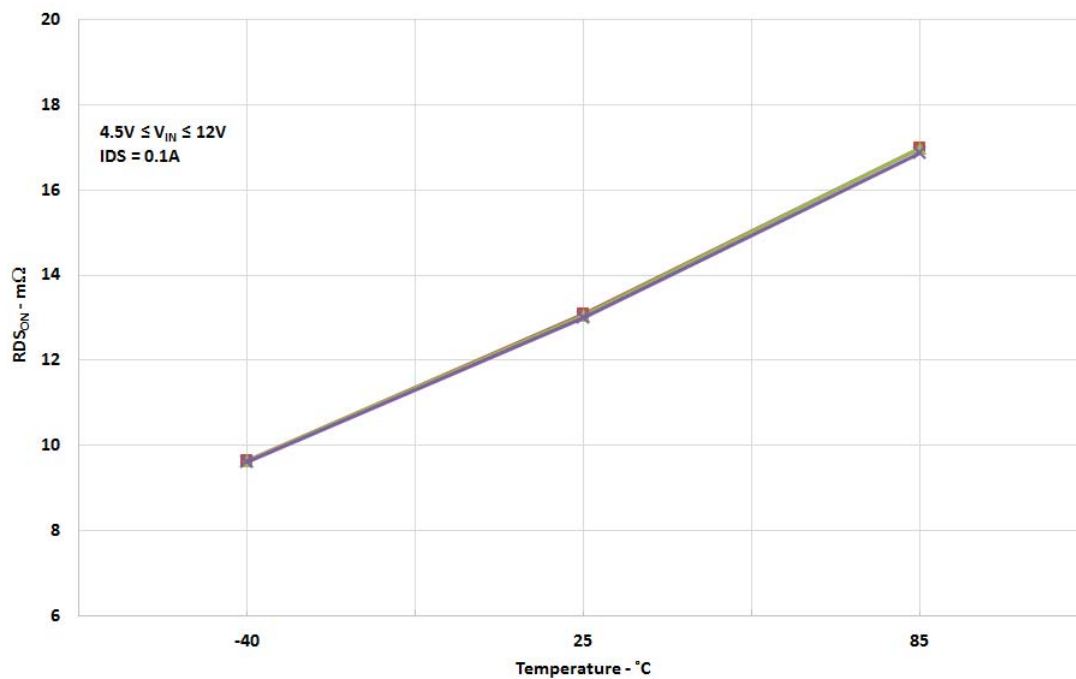
PG Timing Details



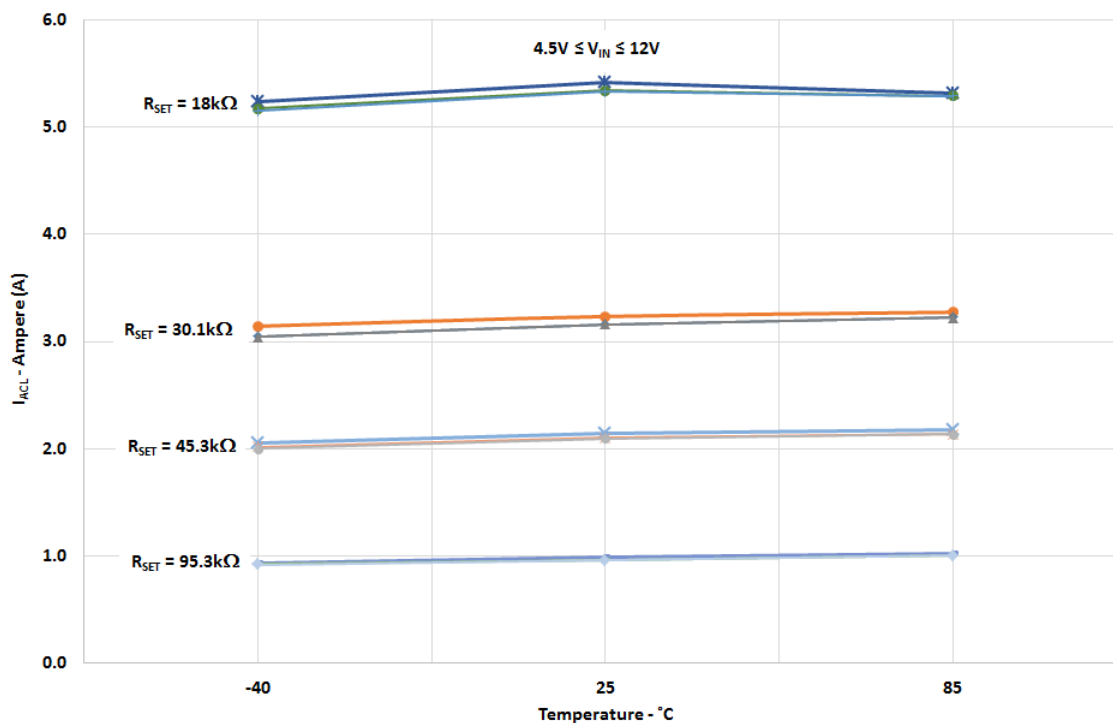


Typical Performance Characteristics

$R_{DS(on)}$ vs. Temperature and V_{IN}

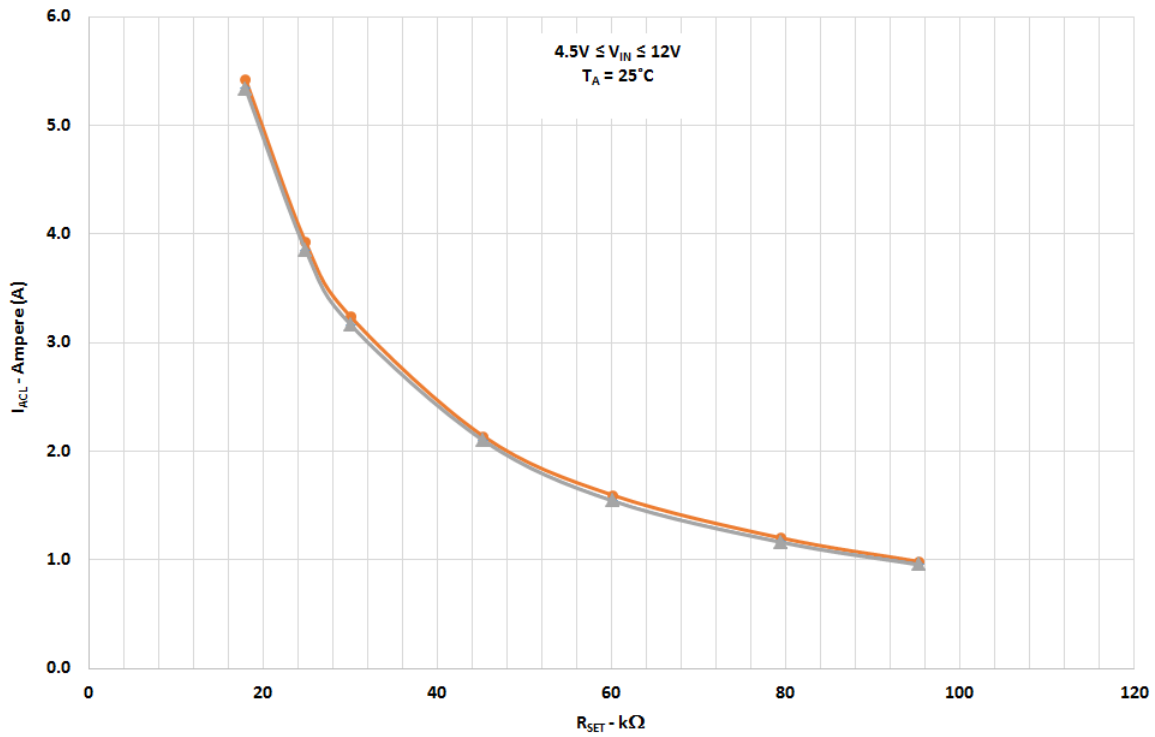


I_{ACL} vs. Temperature, R_{SET} , and V_{IN}

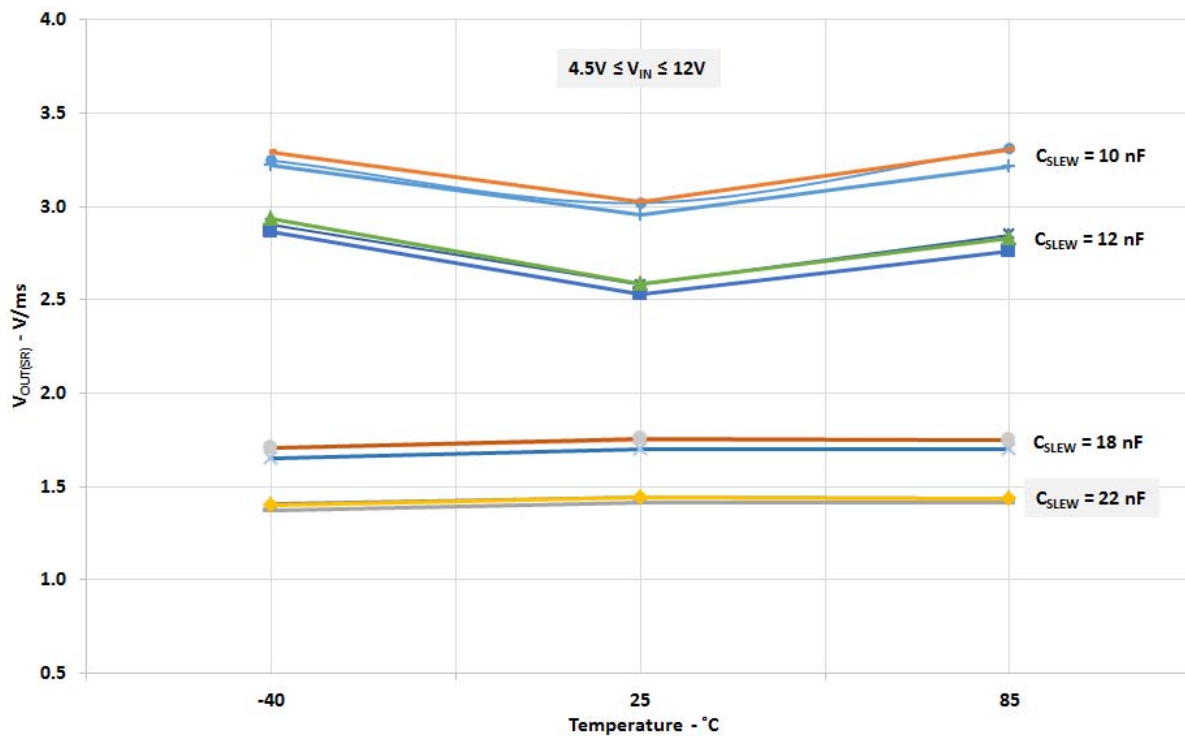




I_{ACL} vs. R_{SET} , Temperature, and V_{IN}

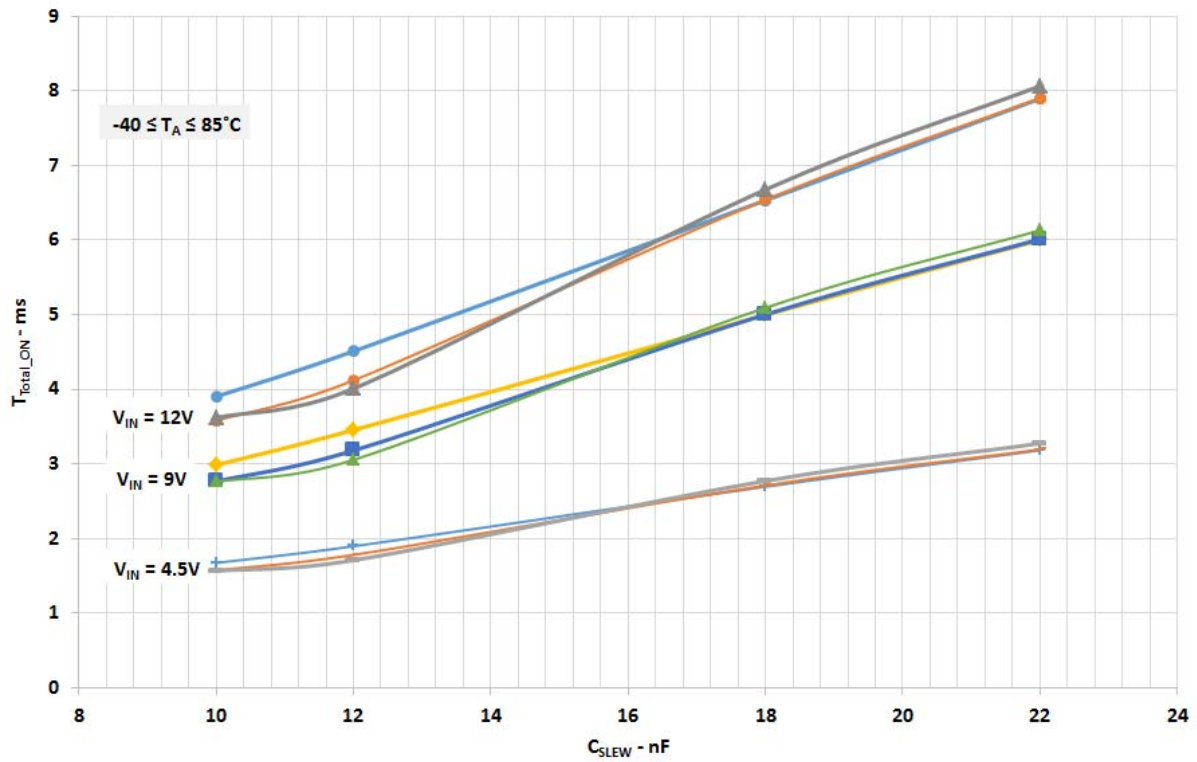


V_{OUT} Slew Rate vs. Temperature, V_{IN} , and C_{SLEW}





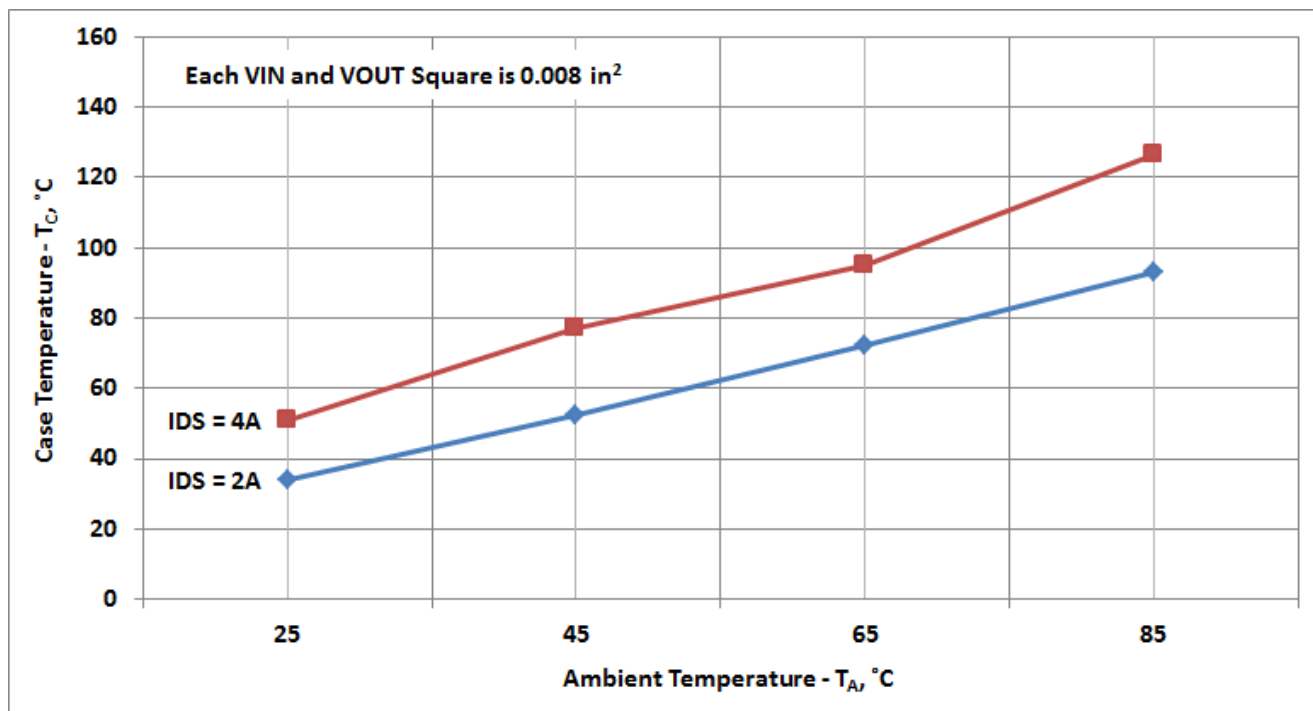
T_{Total_ON} vs. C_{SLEW} , V_{IN} , and Temperature



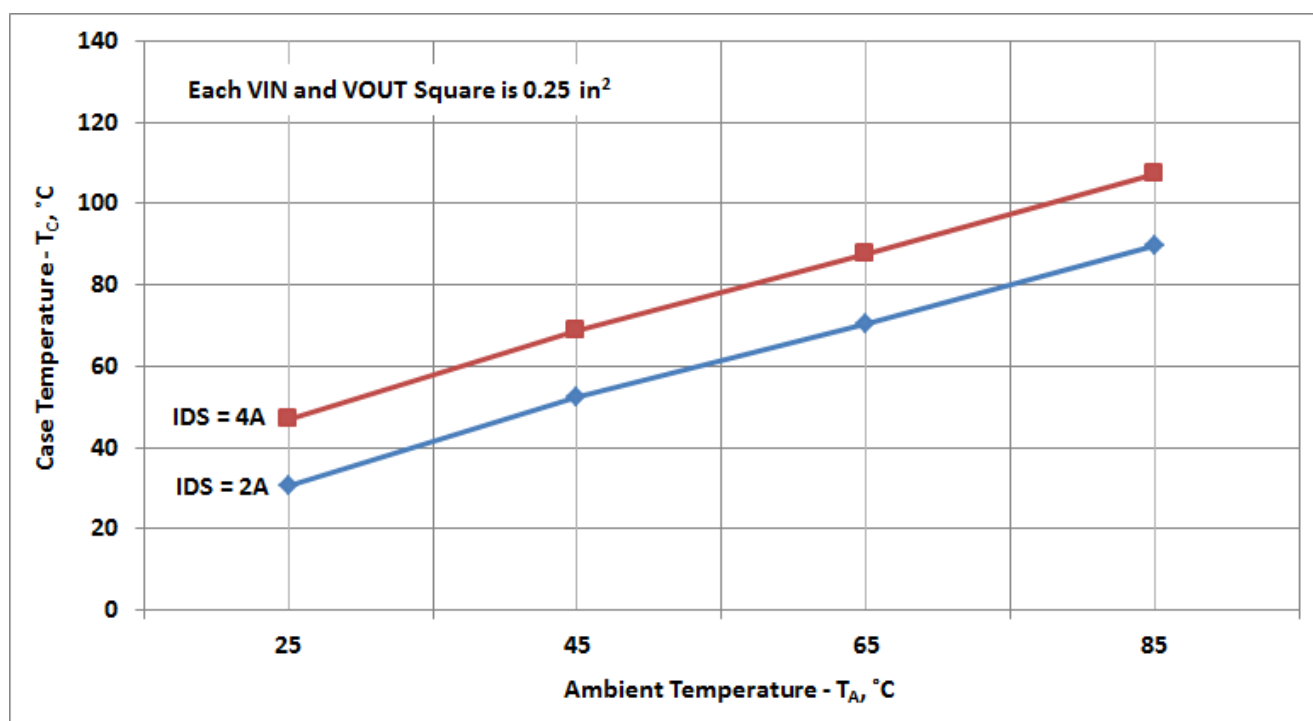


Case Measurement

Case Temperature vs. Ambient Temperature (each VIN and VOUT square is 0.008 in², no airflow)

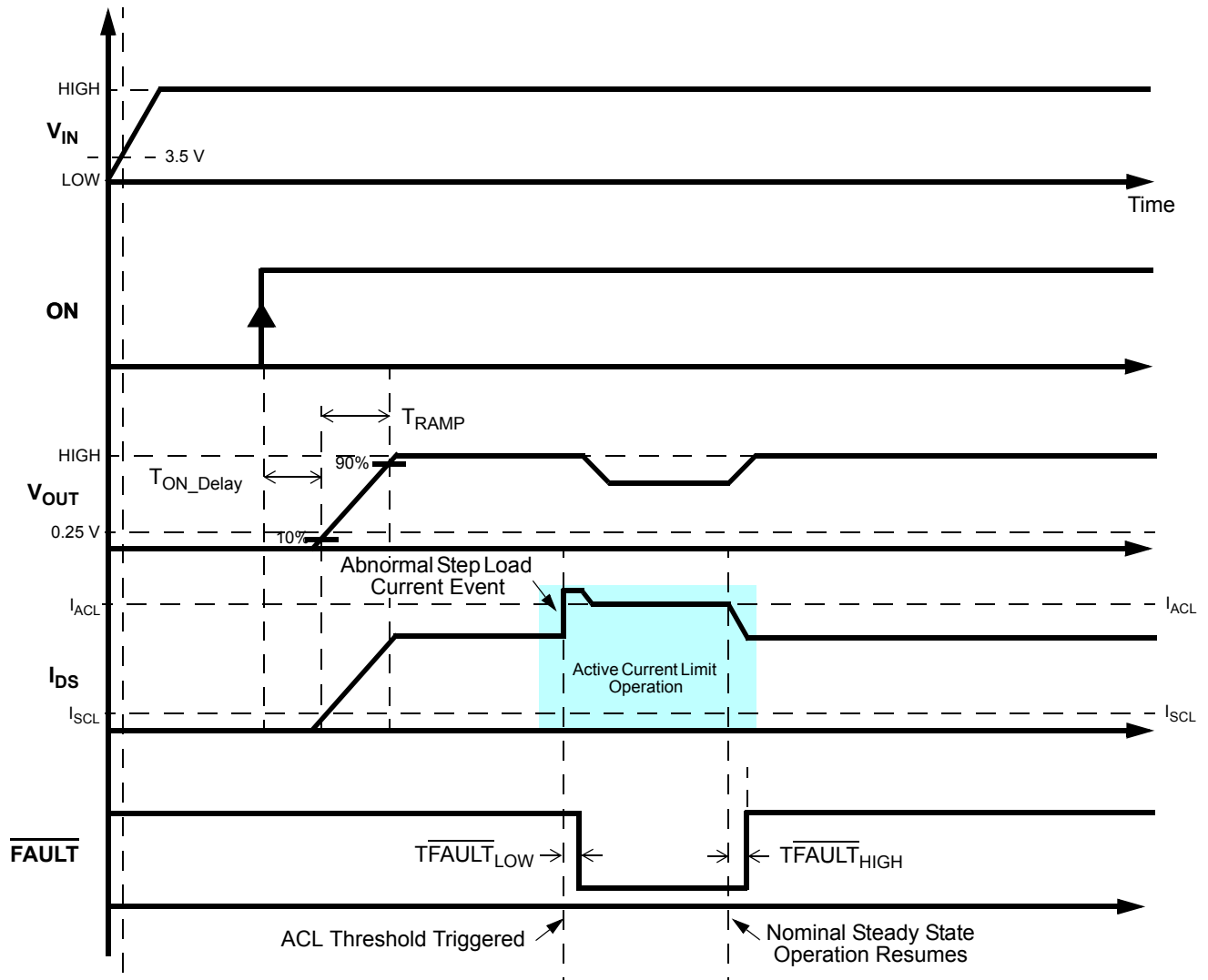


Case Temperature vs. Ambient Temperature (each VIN and VOUT square is 0.25 in², no airflow)



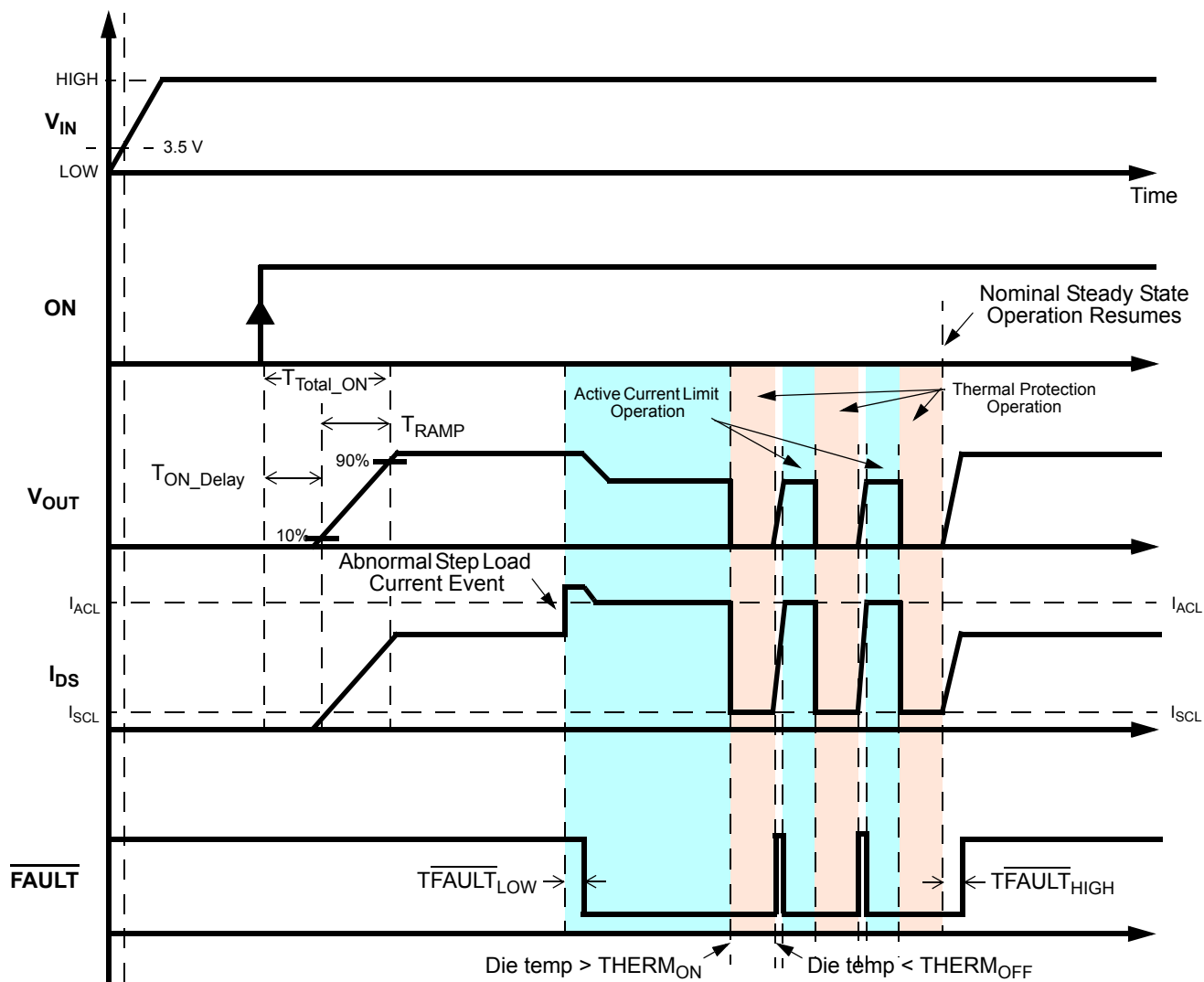


Timing Diagram - Basic Operation including Active Current Limit Protection



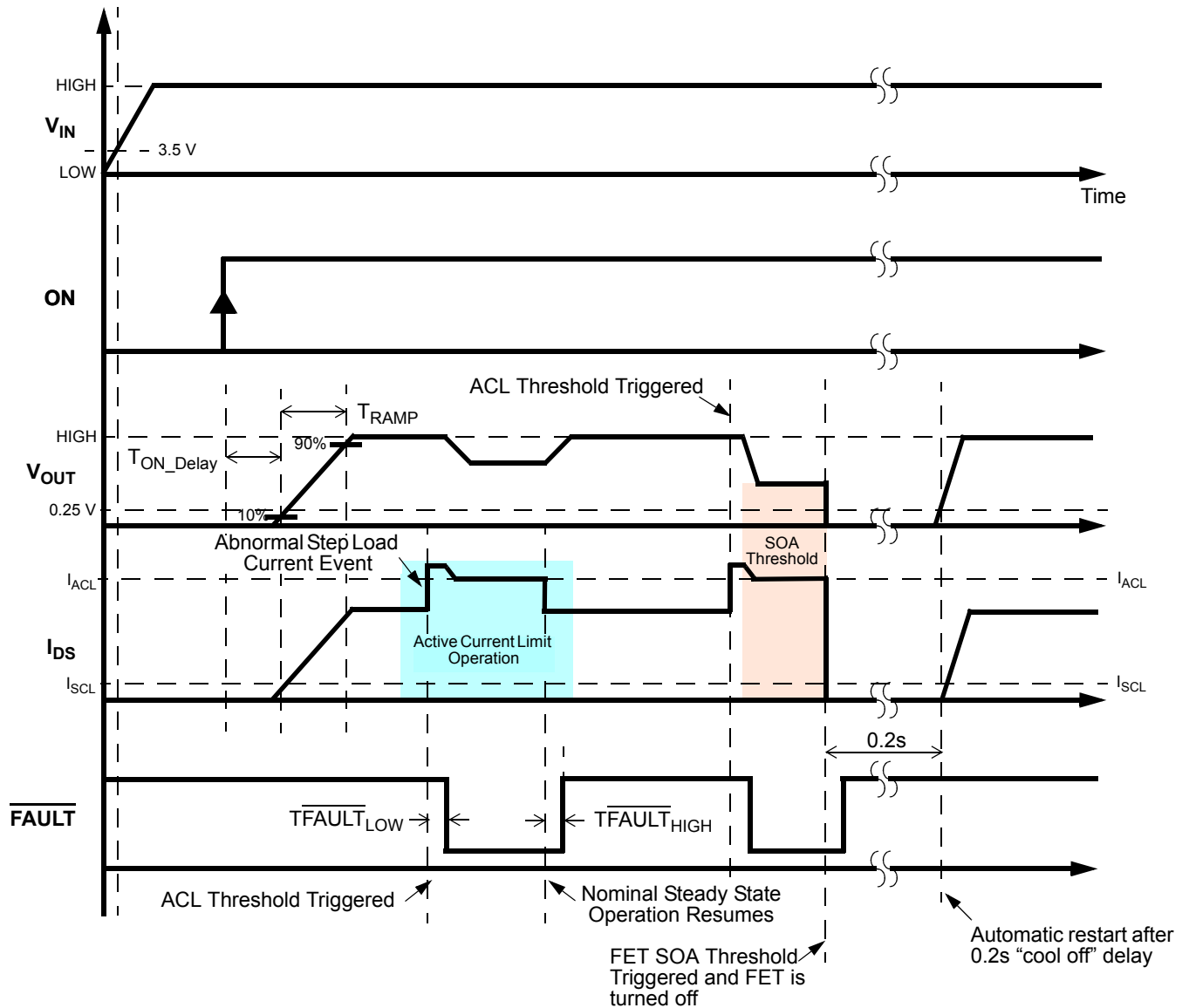


Timing Diagram - Active Current Limit & Thermal Protection Operation





Timing Diagram - Basic Operation including Active Current + Internal FET SOA Protection





SLG59H1127V Application Diagram

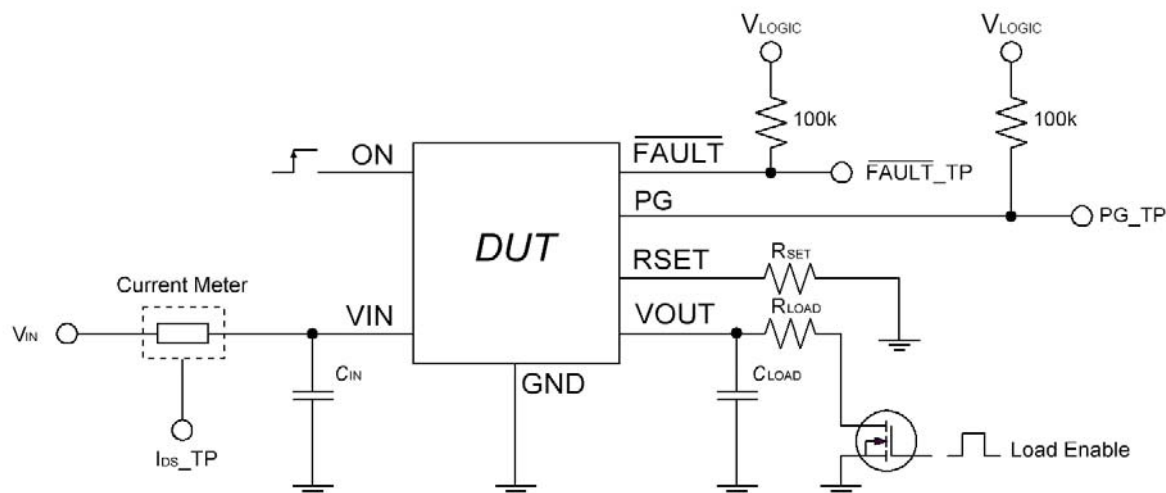


Figure 1. Test setup Application Diagram

Typical Turn-on Waveforms

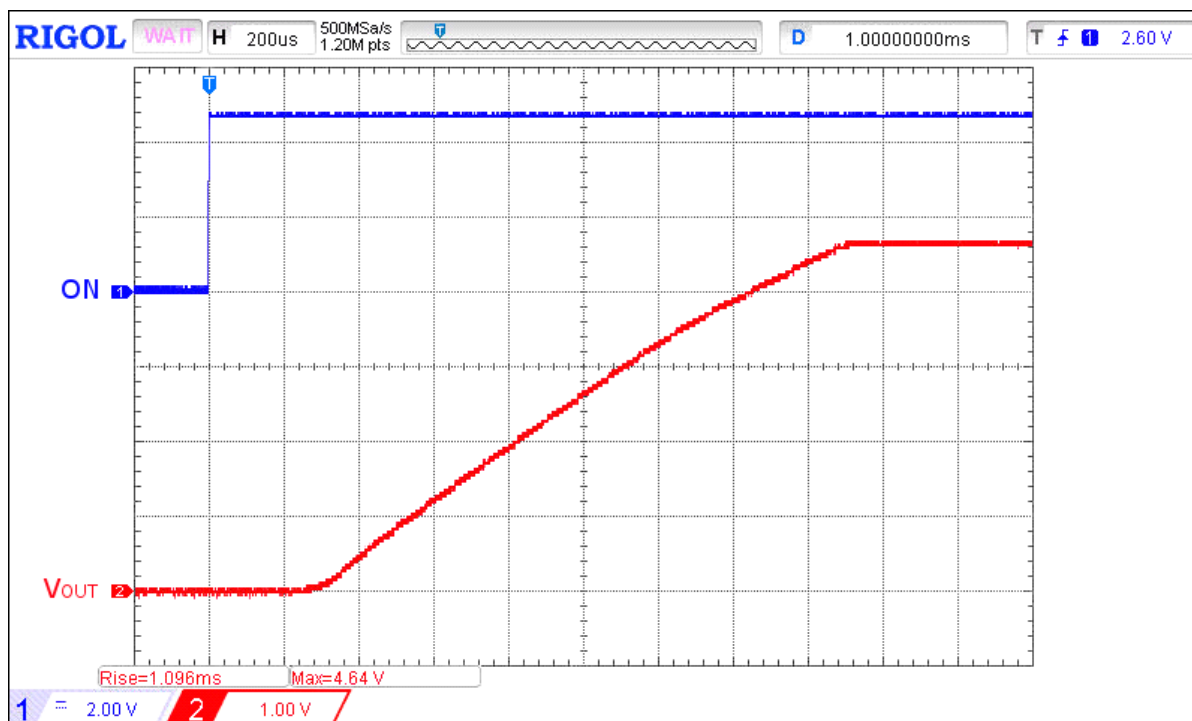


Figure 2. Typical Turn ON operation waveform for $V_{IN} = 4.5\text{ V}$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

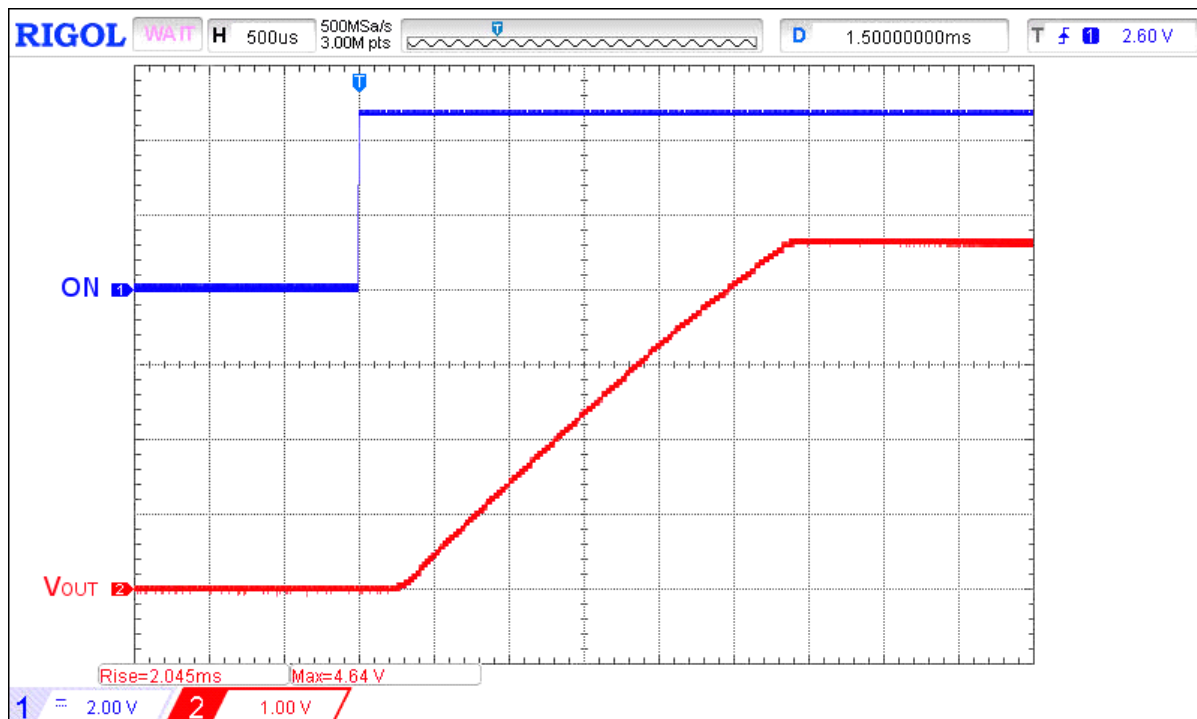


Figure 3. Typical Turn ON operation waveform for $V_{IN} = 4.5 \text{ V}$, $C_{SLEW} = 18 \text{ nF}$, $C_{LOAD} = 10 \text{ }\mu\text{F}$, $R_{LOAD} = 100 \text{ }\Omega$

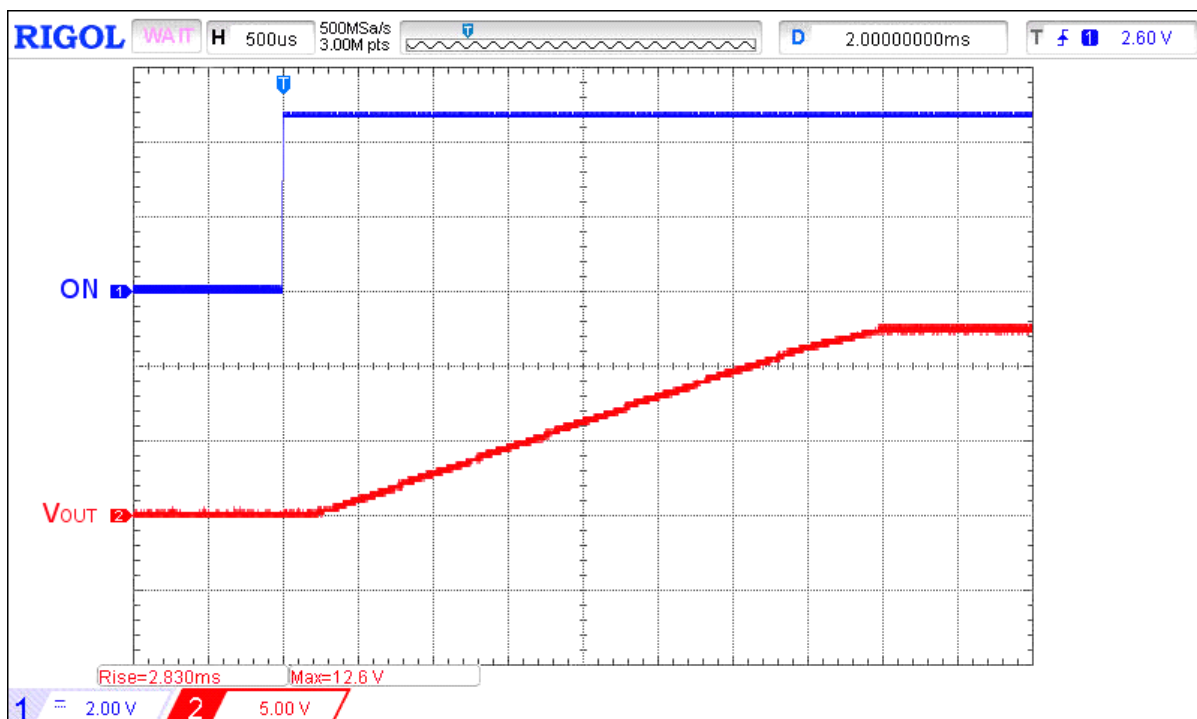


Figure 4. Typical Turn ON operation waveform for $V_{IN} = 12 \text{ V}$, $C_{SLEW} = 10 \text{ nF}$, $C_{LOAD} = 10 \text{ }\mu\text{F}$, $R_{LOAD} = 100 \text{ }\Omega$

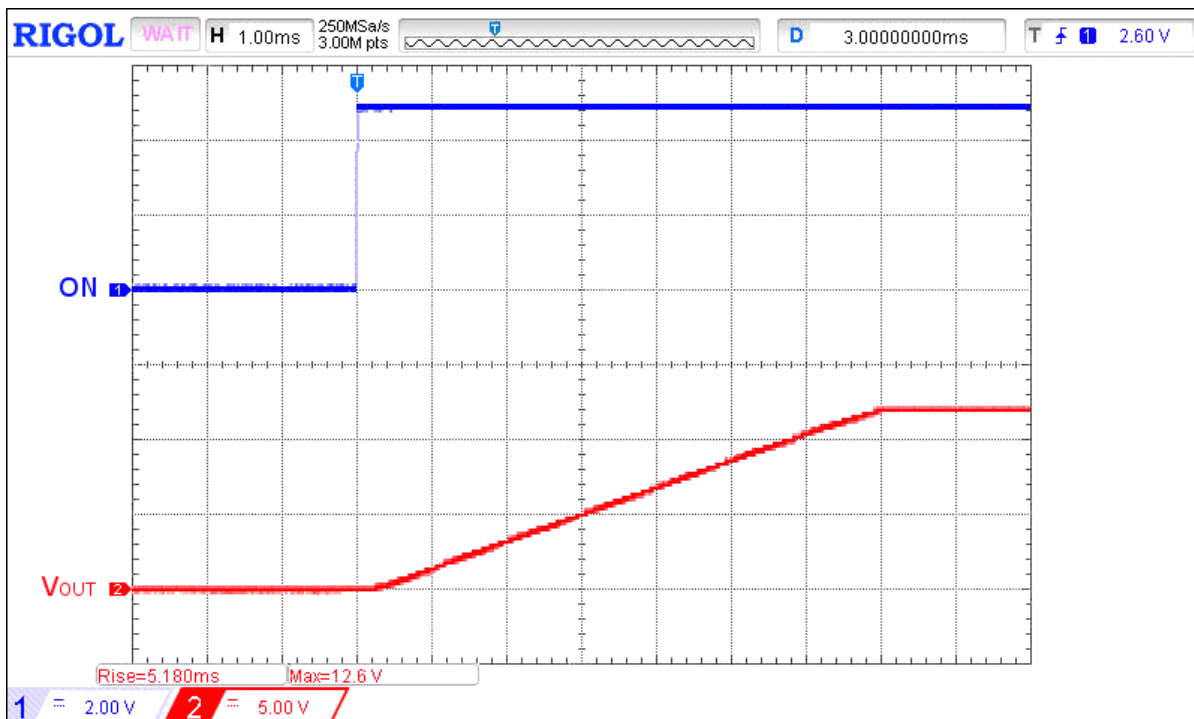


Figure 5. Typical Turn ON operation waveform for $V_{IN} = 12\text{ V}$, $C_{SLEW} = 18\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

Typical Turn-off Waveforms

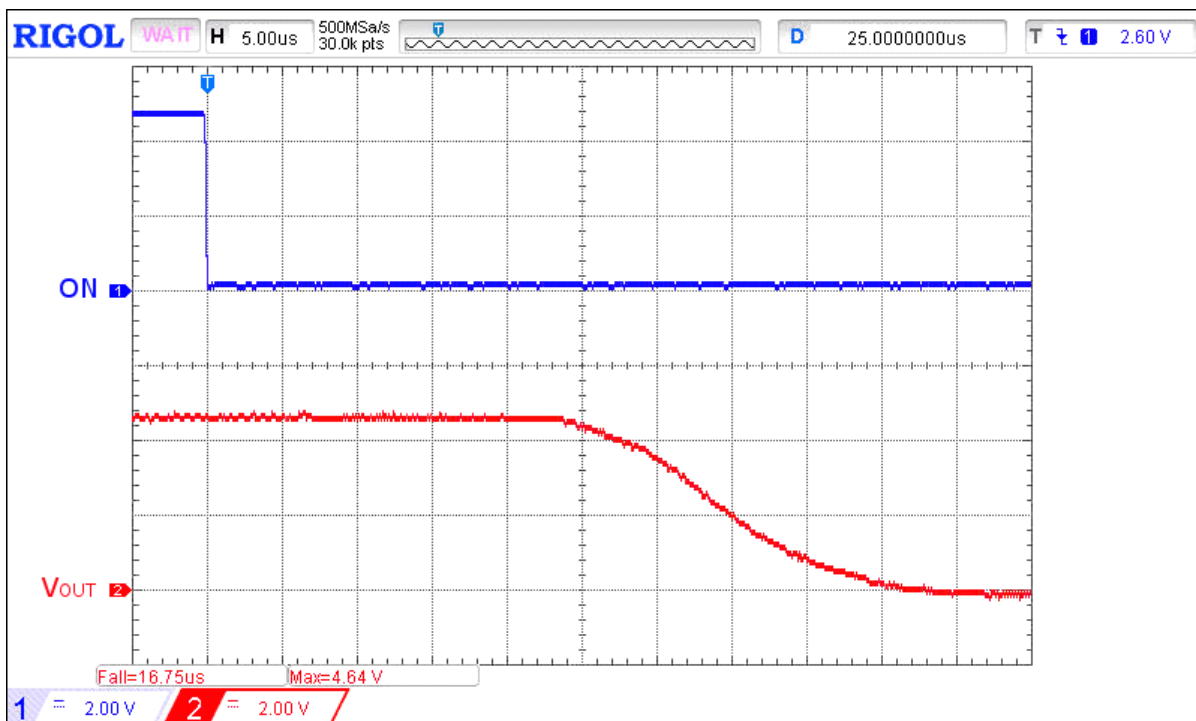


Figure 6. Typical Turn OFF operation waveform for $V_{IN} = 4.5\text{ V}$, $C_{SLEW} = 10\text{ nF}$, no C_{LOAD} , $R_{LOAD} = 100\text{ }\Omega$

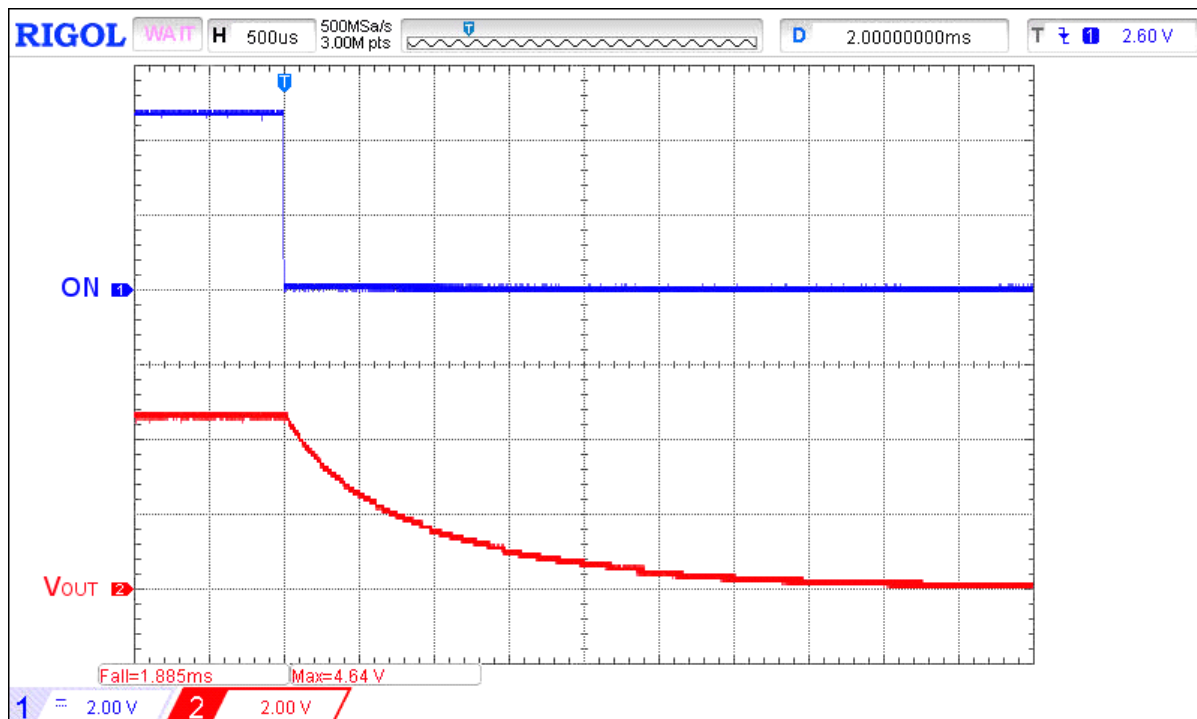


Figure 7. Typical Turn OFF operation waveform for $V_{IN} = 4.5\text{ V}$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

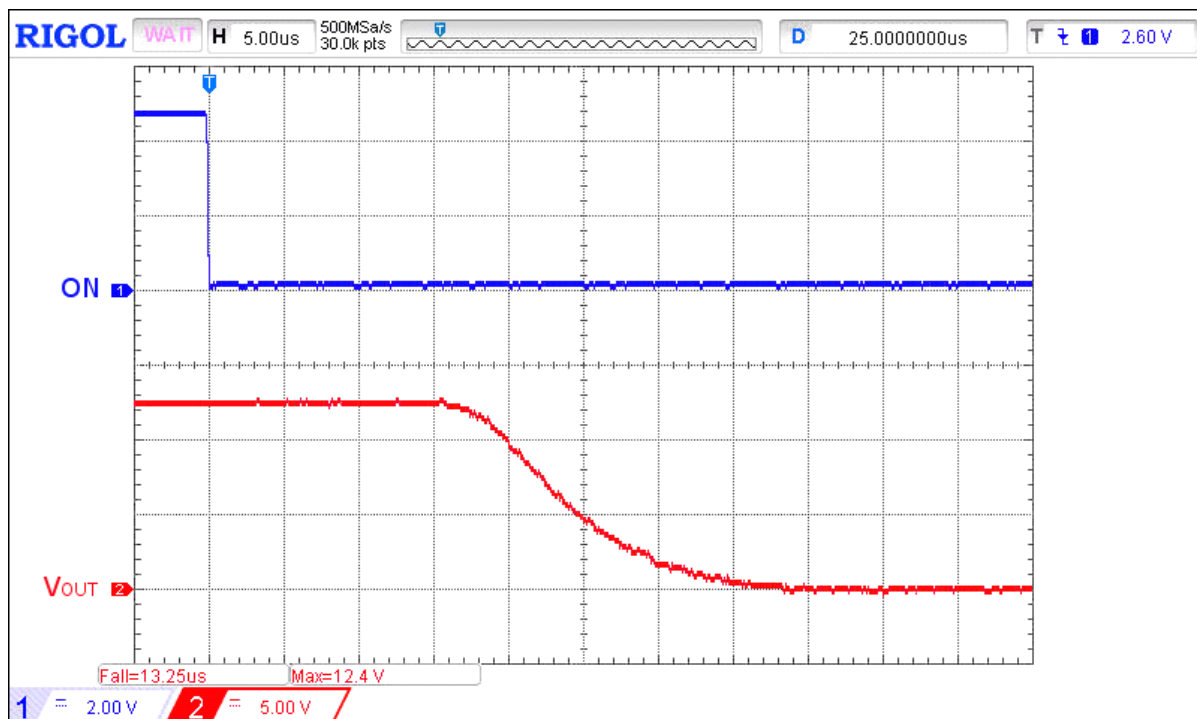


Figure 8. Typical Turn OFF operation waveform for $V_{IN} = 12\text{ V}$, $C_{SLEW} = 10\text{ nF}$, no C_{LOAD} , $R_{LOAD} = 100\text{ }\Omega$

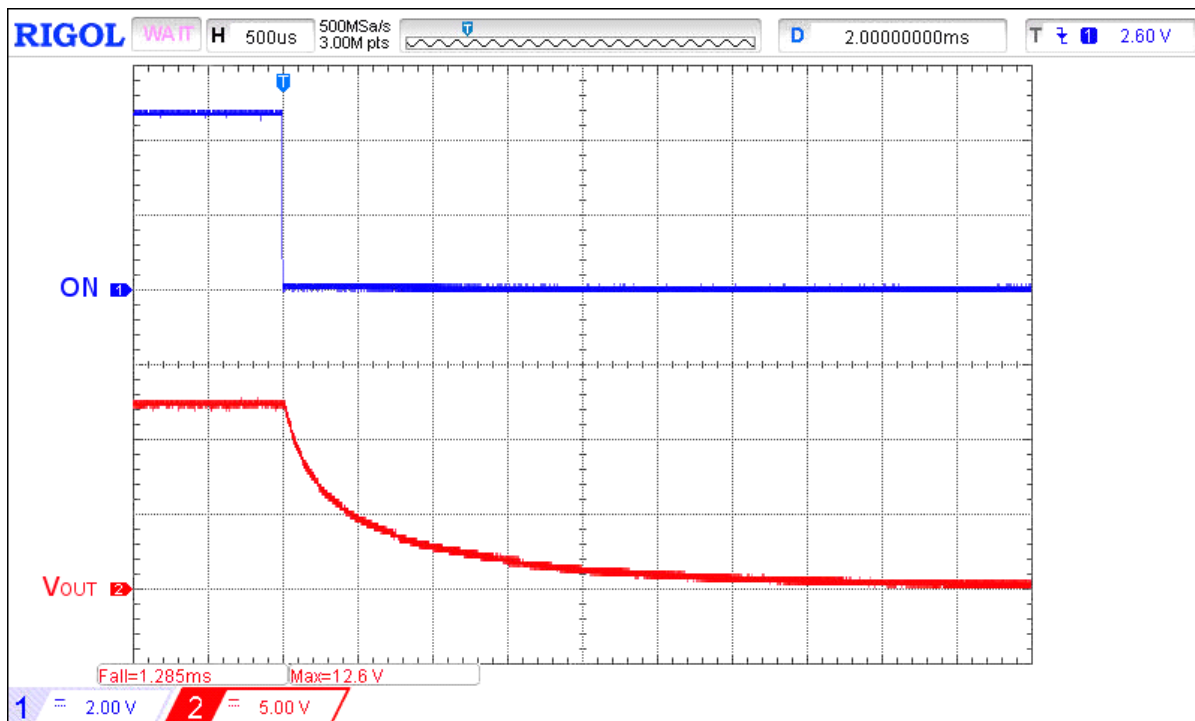


Figure 9. Typical Turn OFF operation waveform for $V_{IN} = 12\text{ V}$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

Typical ACL Operation Waveforms

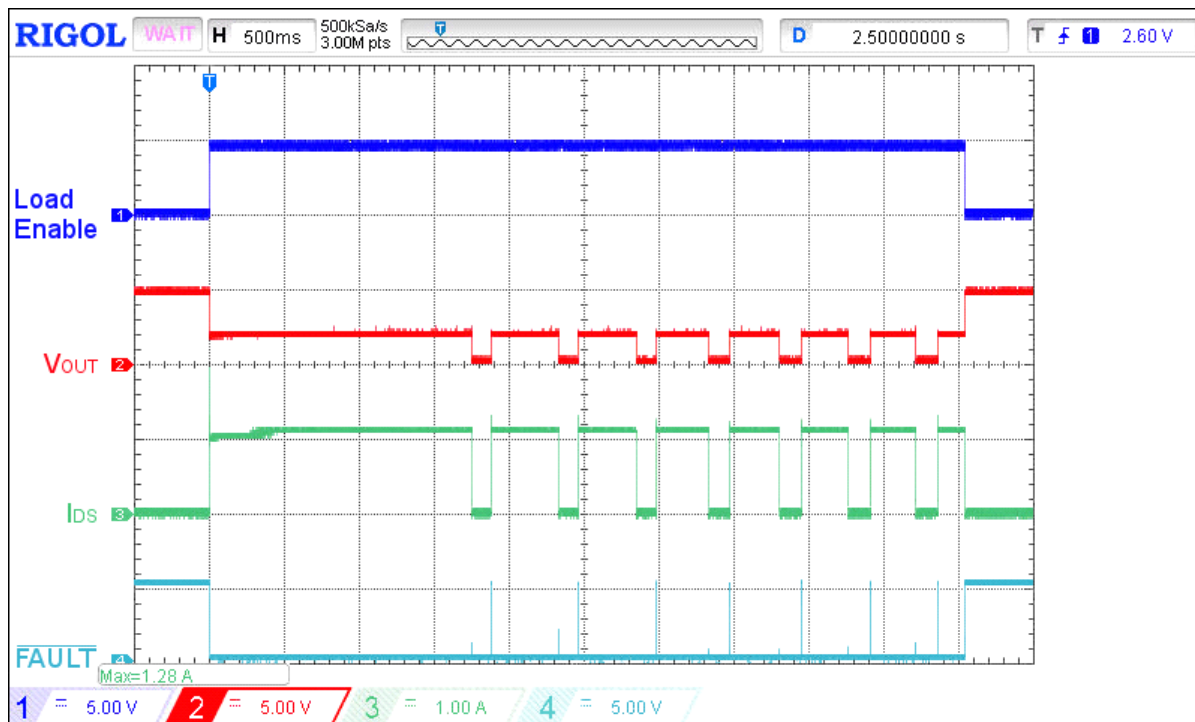


Figure 10. Typical ACL operation waveform for $V_{IN} = 4.5\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 95.3\text{ k}\Omega$

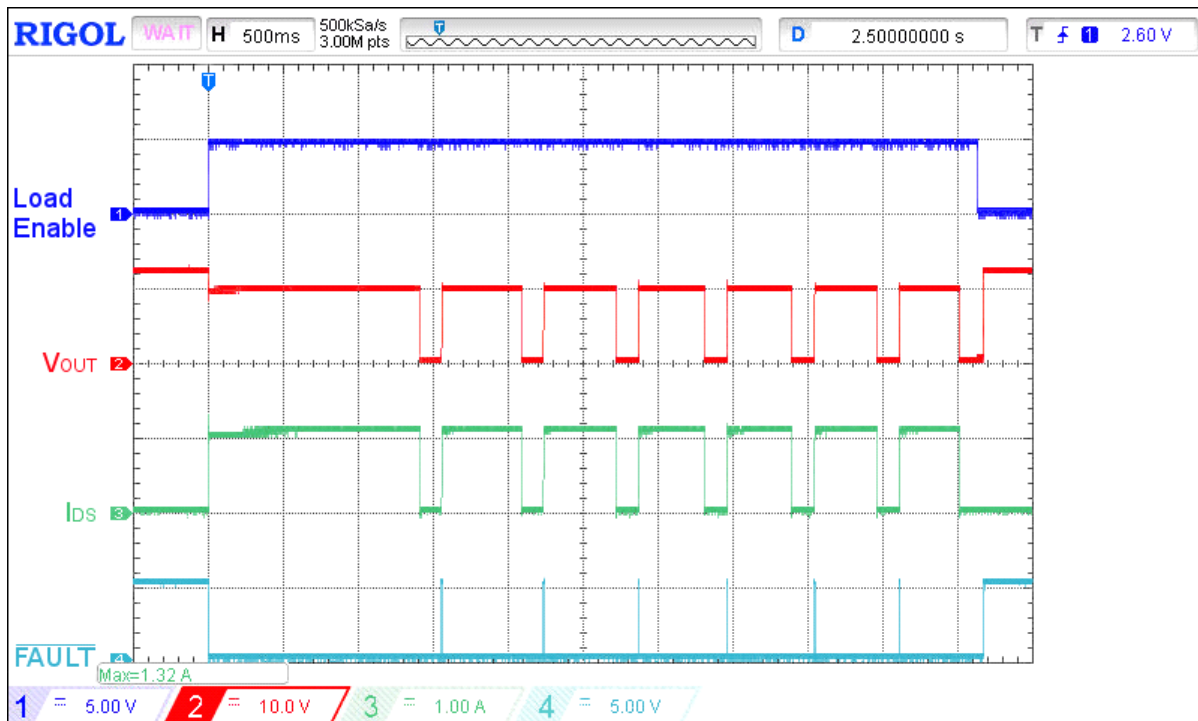


Figure 11. Typical ACL operation waveform for $V_{IN} = 12\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 95.3\text{ k}\Omega$

Typical FAULT Operation Waveforms

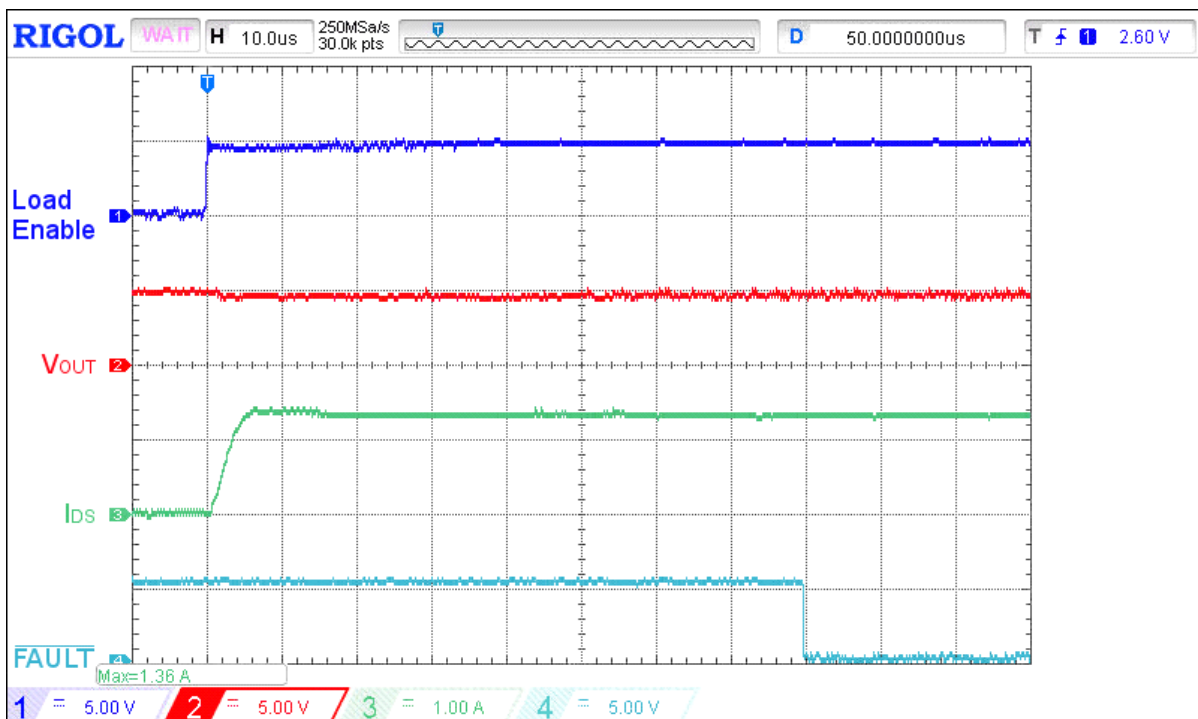


Figure 12. Typical FAULT assertion waveform for $V_{IN} = 4.5\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 95.3\text{ k}\Omega$, switch on $3.3\text{ }\Omega$ load

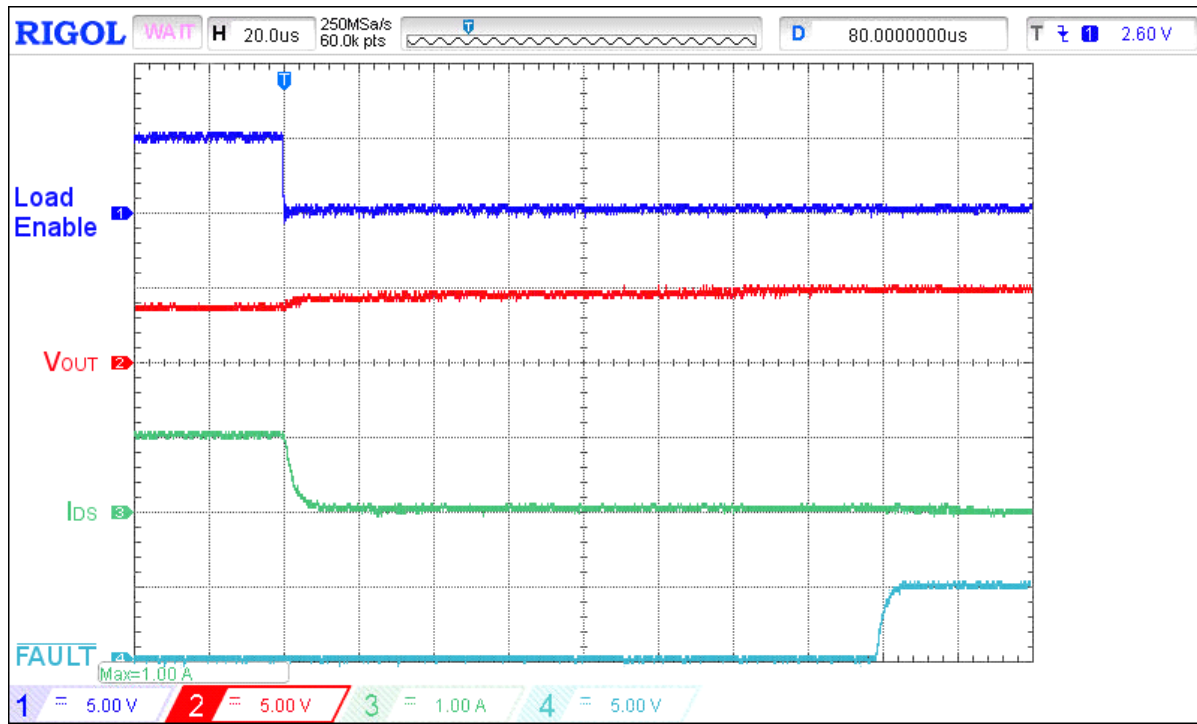


Figure 13. Typical $\overline{\text{FAULT}}$ de-assertion waveform for $V_{\text{IN}} = 4.5 \text{ V}$, $C_{\text{LOAD}} = 10 \mu\text{F}$, $I_{\text{ACL}} = 1 \text{ A}$, $R_{\text{SET}} = 95.3 \text{ k}\Omega$, switch out 3.3Ω load

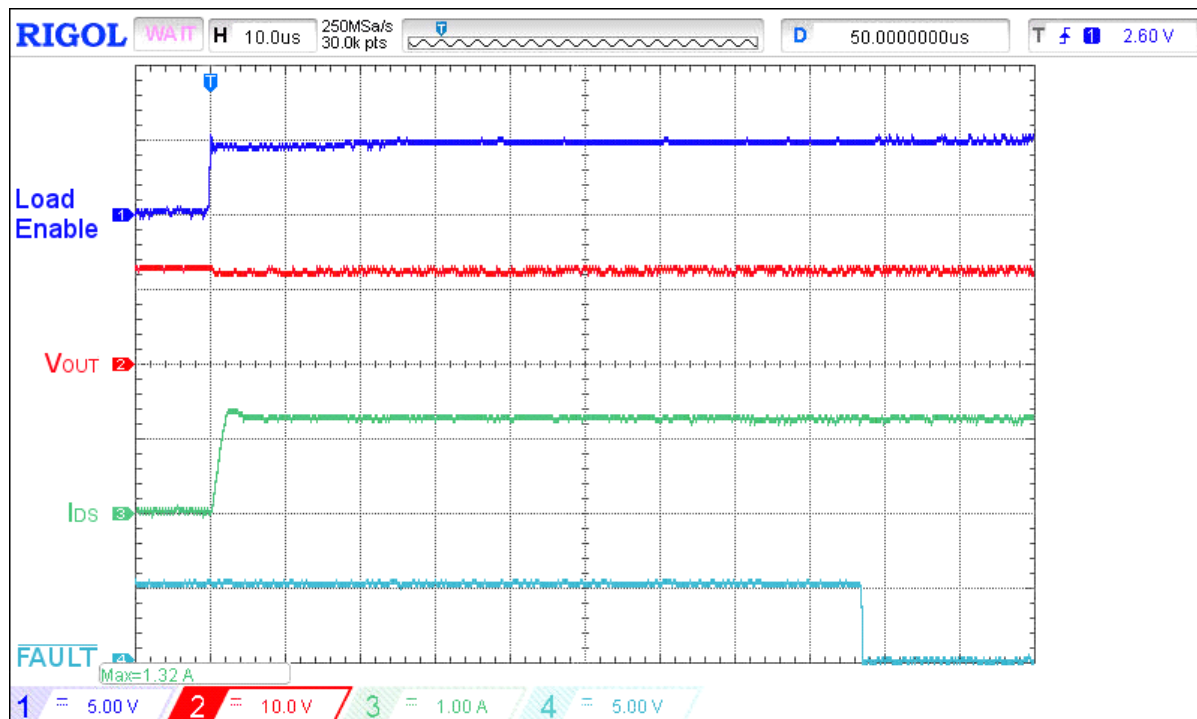


Figure 14. Typical $\overline{\text{FAULT}}$ assertion waveform for $V_{\text{IN}} = 12 \text{ V}$, $C_{\text{LOAD}} = 10 \mu\text{F}$, $I_{\text{ACL}} = 1 \text{ A}$, $R_{\text{SET}} = 95.3 \text{ k}\Omega$, switch on 10Ω load

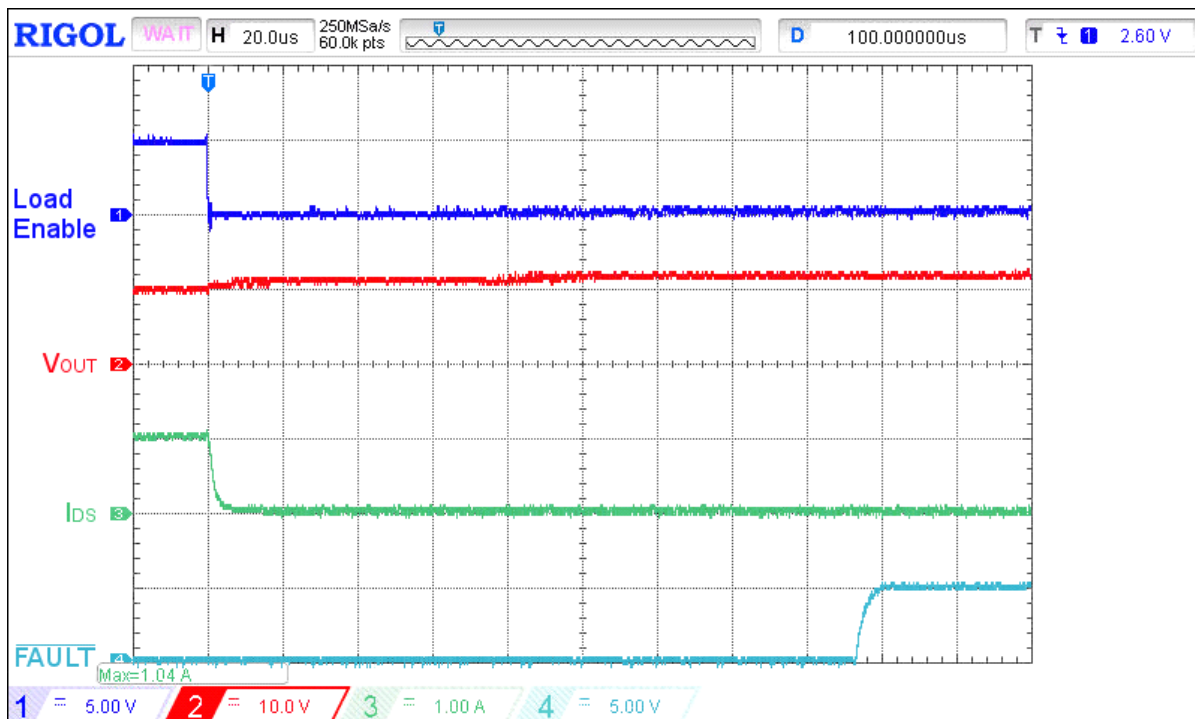


Figure 15. Typical FAULT de-assertion waveform for $V_{IN} = 12\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 95.3\text{ k}\Omega$, switch out $10\text{ }\Omega$ load

Typical Power Good Waveform

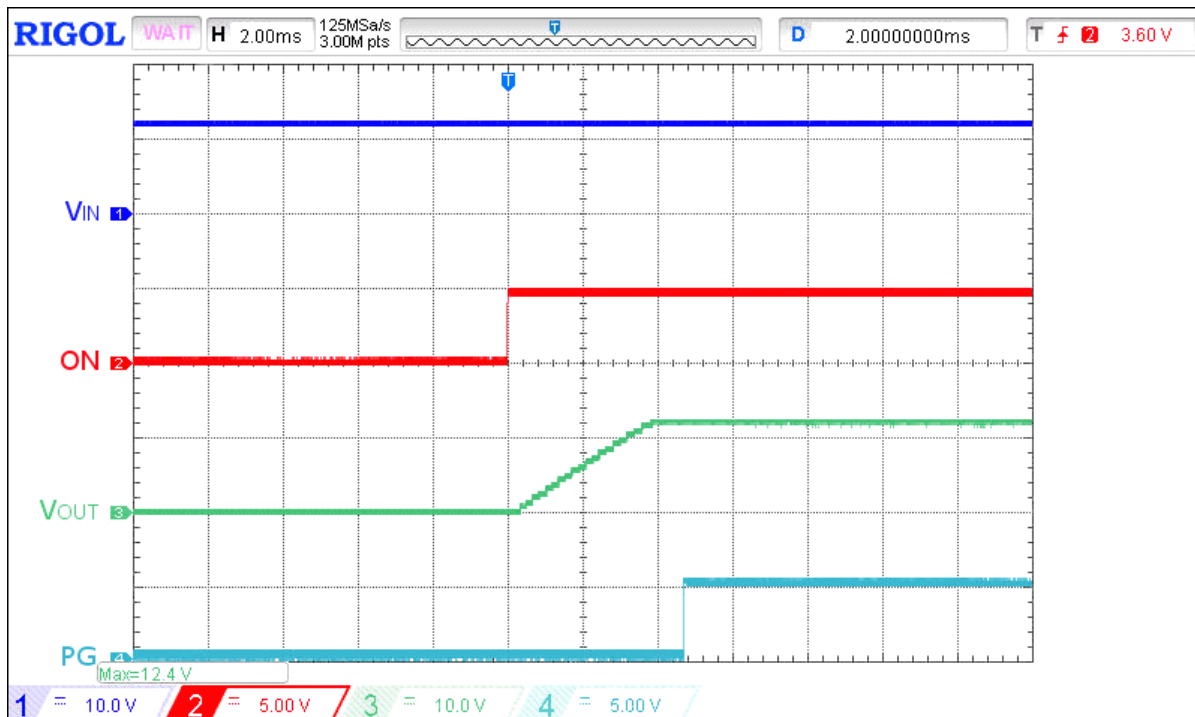


Figure 16. Typical Power Good operation waveform for $V_{IN} = 12\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, no R_{LOAD}



Typical SOA Waveforms

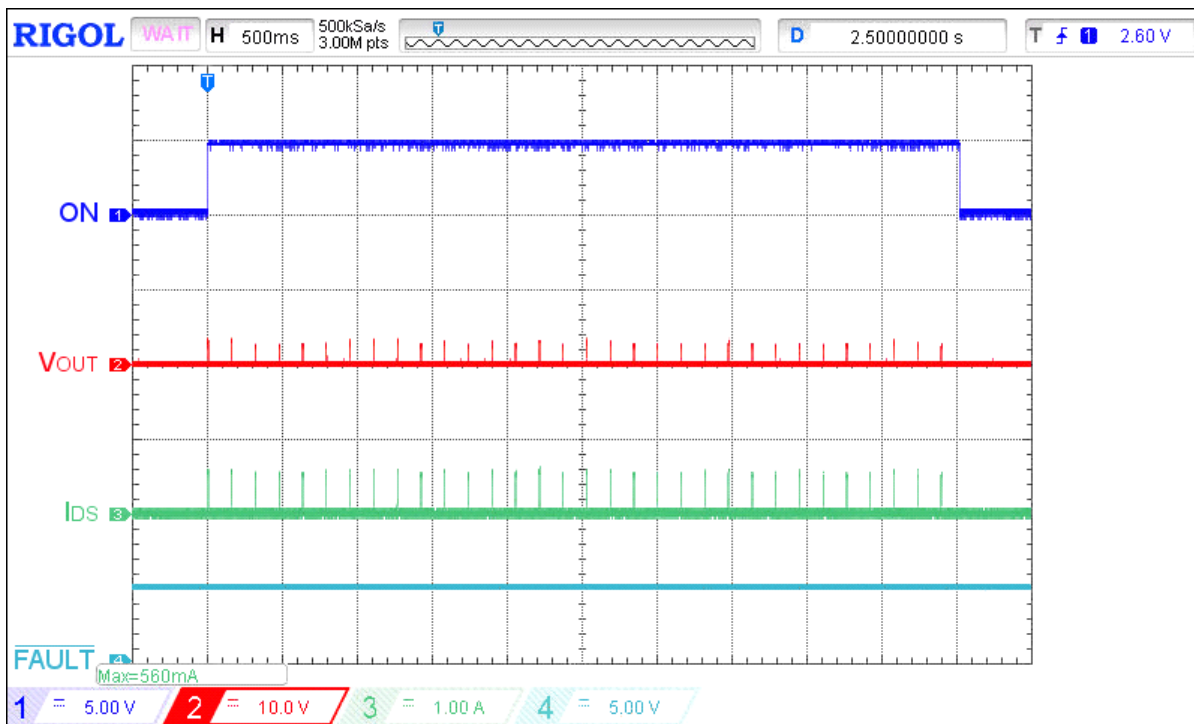


Figure 17. Typical SOA waveform during power up under heavy load for $V_{IN} = 12\text{ V}$,
 $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{SET} = 30.1\text{ k}\Omega$, $R_{LOAD} = 5\text{ }\Omega$

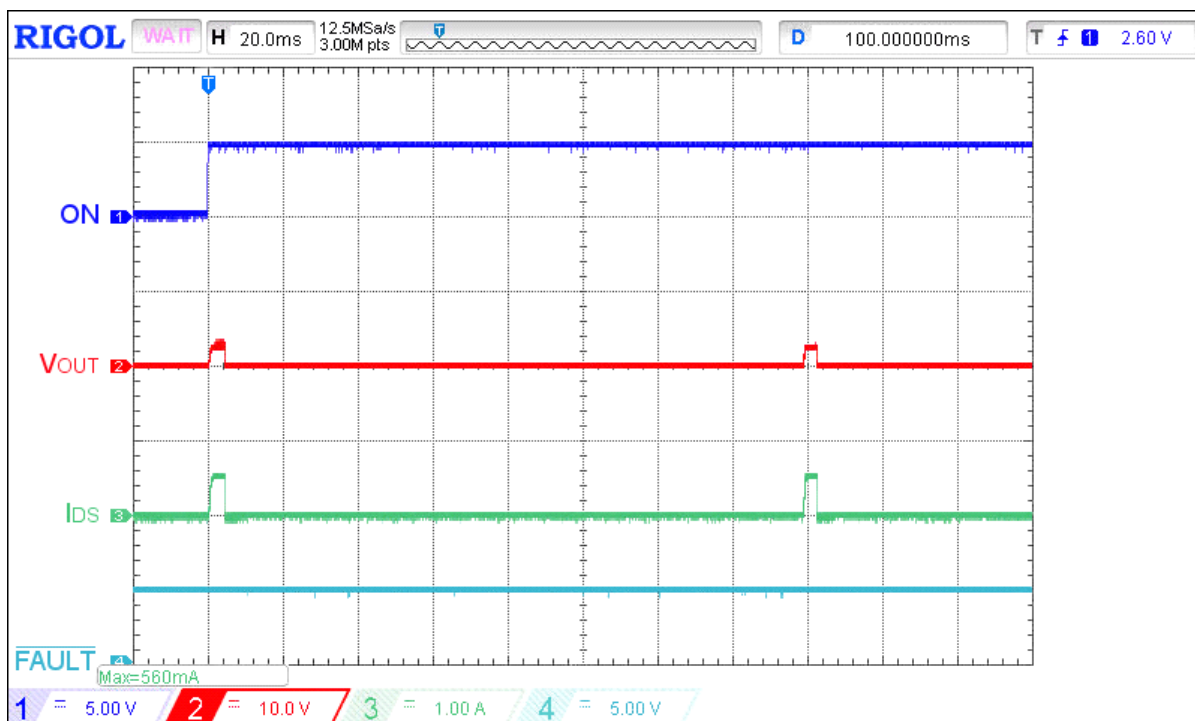


Figure 18. Extended typical SOA waveform during power up under heavy load for $V_{IN} = 12\text{ V}$,
 $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{SET} = 30.1\text{ k}\Omega$, $R_{LOAD} = 5\text{ }\Omega$



Applications Information

HFET1 Safe Operating Area Explained

Silego's HFET1 integrated power controllers incorporate a number of internal protection features that prevents them from damaging themselves or any other circuit or subcircuit downstream of them. One particular protection feature is their Safe Operation Area (SOA) protection. SOA protection is automatically activated under overpower and, in some cases, under overcurrent conditions. Overpower SOA is activated if package power dissipation exceeds an internal 5W threshold longer than 2.5 ms. HFET1 devices will quickly switch off (open circuit) upon overpower detection and automatically resume (close) nominal operation once overpower condition no longer exists.

One of the possible ways to have an overpower condition trigger SOA protection is when HFET1 products are enabled into heavy output resistive loads and/or into large load capacitors. It is under these conditions to follow carefully the "Safe Start-up Loading" guidance in the Applications section of the datasheet. During an overcurrent condition, HFET1 devices will try to limit the output current to the level set by the external R_{SET} resistor. Limiting the output current, however, causes an increased voltage drop across the FET's channel because the FET's $R_{DS_{ON}}$ increased as well. Since the FET's $R_{DS_{ON}}$ is larger, package power dissipation also increases. If the resultant increase in package power dissipation is higher/equal than 5 W for longer than 2.5 ms, internal SOA protection will be triggered and the FET will open circuit (switch off). Every time SOA protection is triggered, all HFET1 devices will automatically attempt to resume nominal operation after 160 ms.

Safe Start-up Condition

SLG59H1127V has built-in protection to prevent over-heating during start-up into a heavy load. Overloading the VOUT pin with a capacitor and a resistor may result in non-monotonic V_{OUT} ramping or repeated restarts (*Figure 17* and *Figure 18*). In general, under light loading on VOUT, V_{OUT} ramping can be controlled with C_{SLEW} value. The following equation serves as a guide:

$$C_{SLEW} = \frac{T_{RAMP}}{V_{IN}} \times 4.9 \mu A \times \frac{20}{3}$$

where

T_{RAMP} = Total rise time from 10% V_{OUT} to 90% V_{OUT}

V_{IN} = Input Voltage

C_{SLEW} = Capacitor value for CAP pin

When capacitor and resistor loading on VOUT during start up, the following tables will ensure V_{OUT} ramping is monotonic without triggering internal protection:

Safe Start-up Loading for $V_{IN} = 12 \text{ V}$ (Monotonic Ramp)			
Slew Rate (V/ms)	$C_{SLEW} \text{ (nF)}^3$	$C_{LOAD} \text{ (}\mu\text{F)}$	$R_{LOAD} \text{ (}\Omega)$
1	33.3	500	20
2	16.7	250	20
3	11.1	160	20
4	8.3	120	20
5	6.7	100	20

Note 3: Select the closest-value tolerance capacitor.



Setting the SLG59H1127V's Active Current Limit

R _{SET} (kΩ)	Active Current Limit (A) ⁴
95	1
45	2
30	3
18	5

Note 4: Active Current Limit accuracy is ±15% over voltage range and temperature range

Setting the SLG59H1127V's Input Overvoltage Lockout Threshold

As shown in the table below, SEL selects the V_{IN} overvoltage threshold at which the SLG59H1127V's internal state machine will turn OFF (open circuit) the power MOSFET if V_{IN} exceeds the selected threshold.

SEL	V _{IN(OVLO)} (Typ)
0	14.4 V

With an activated SLG59H1127V (ON=HIGH) and at any time V_{IN} crosses the programmed V_{IN} overvoltage threshold, the state machine opens the power switch and asserts the FAULT pin within T_{FAULT_LOW}.

In applications with a deactivated or inactive SLG59H1127V (V_{IN} > V_{IN(UVLO)} and ON=LOW) and if the applied V_{IN} is higher than the programmed V_{IN(OVLO)} threshold, the SLG59H1127V's state machine will keep the power switch open circuited if the ON pin is toggled LOW-to-HIGH. In these cases, the FAULT pin will also be asserted within T_{FAULT_LOW} and will remain asserted until V_{IN} resumes nominal, steady-state operation.

In all cases, the SLG59H1127V's V_{IN} undervoltage lockout threshold is fixed at V_{IN(UVLO)}.

Power Dissipation

The junction temperature of the SLG59H1127V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59H1127V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{DS}^2$$

where:

PD = Power dissipation, in Watts (W)

RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)

I_{DS} = MOSFET current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:

T_J = Junction temperature, in Celsius degrees (°C)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W)

T_A = Ambient temperature, in Celsius degrees (°C)



Power Dissipation (continued)

In current-limit mode, the SLG59H1127V's power dissipation can be calculated by taking into account the voltage drop across the power switch ($V_{IN} - V_{OUT}$) and the magnitude of the output current in current-limit mode (I_{ACL}):

$$PD = (V_{IN} - V_{OUT}) \times I_{ACL} \text{ or}$$
$$PD = (V_{IN} - (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)

V_{IN} = Input Voltage, in Volts (V)

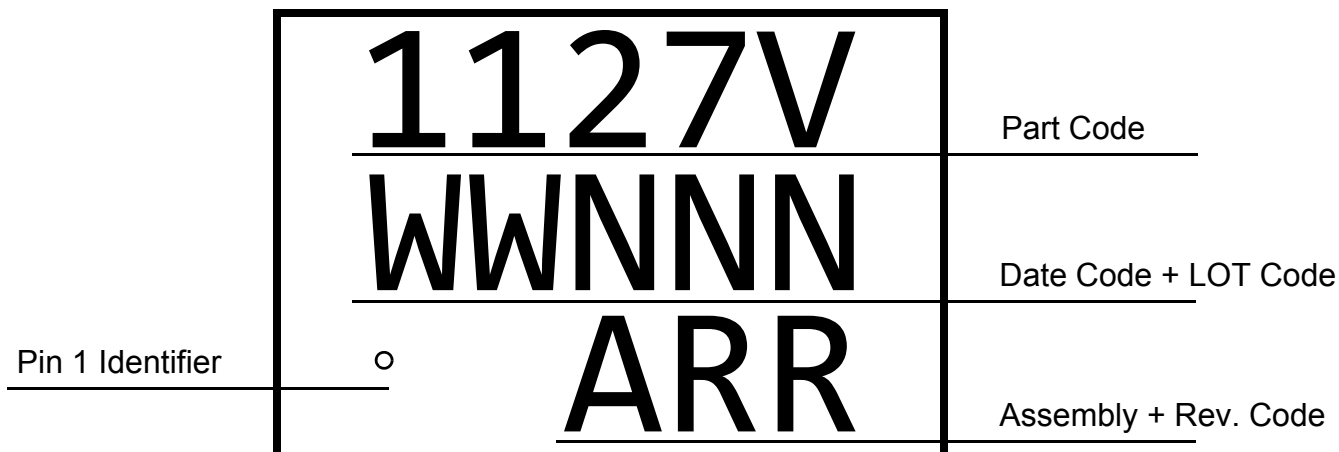
R_{LOAD} = Load Resistance, in Ohms (Ω)

I_{ACL} = Output limited current, in Amps (A)

$V_{OUT} = R_{LOAD} \times I_{ACL}$



Package Top Marking System Definition



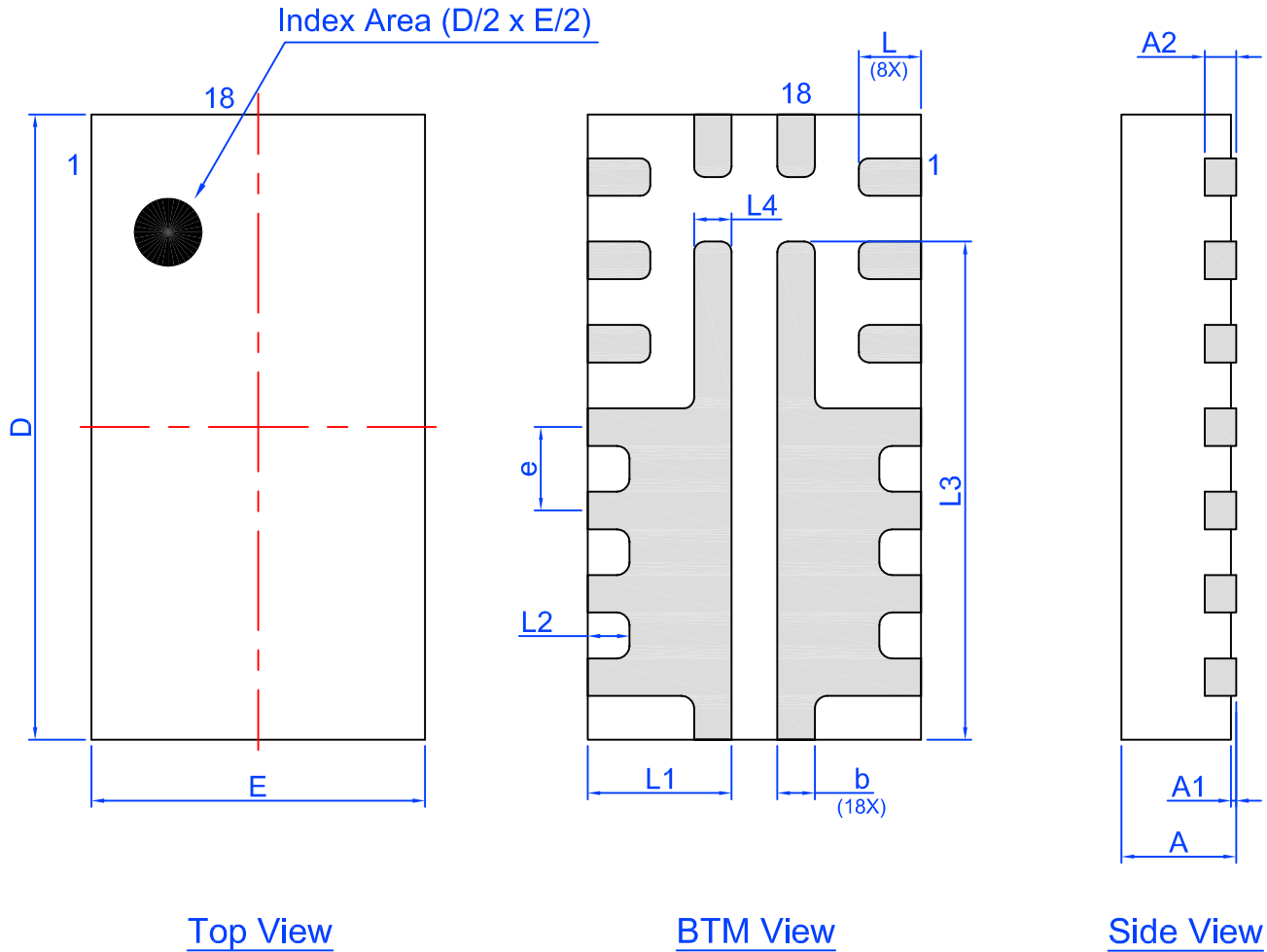
1127V - Part ID Field
WW - Date Code Field¹
NNN - Lot Traceability Code Field¹
A - Assembly Site Code Field²
RR - Part Revision Code Field²

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z



Package Drawing and Dimensions

18 Lead TQFN Package 1.6 x 3 mm (Fused Lead)
JEDEC MO-220, Variation WCEE




Unit: mm

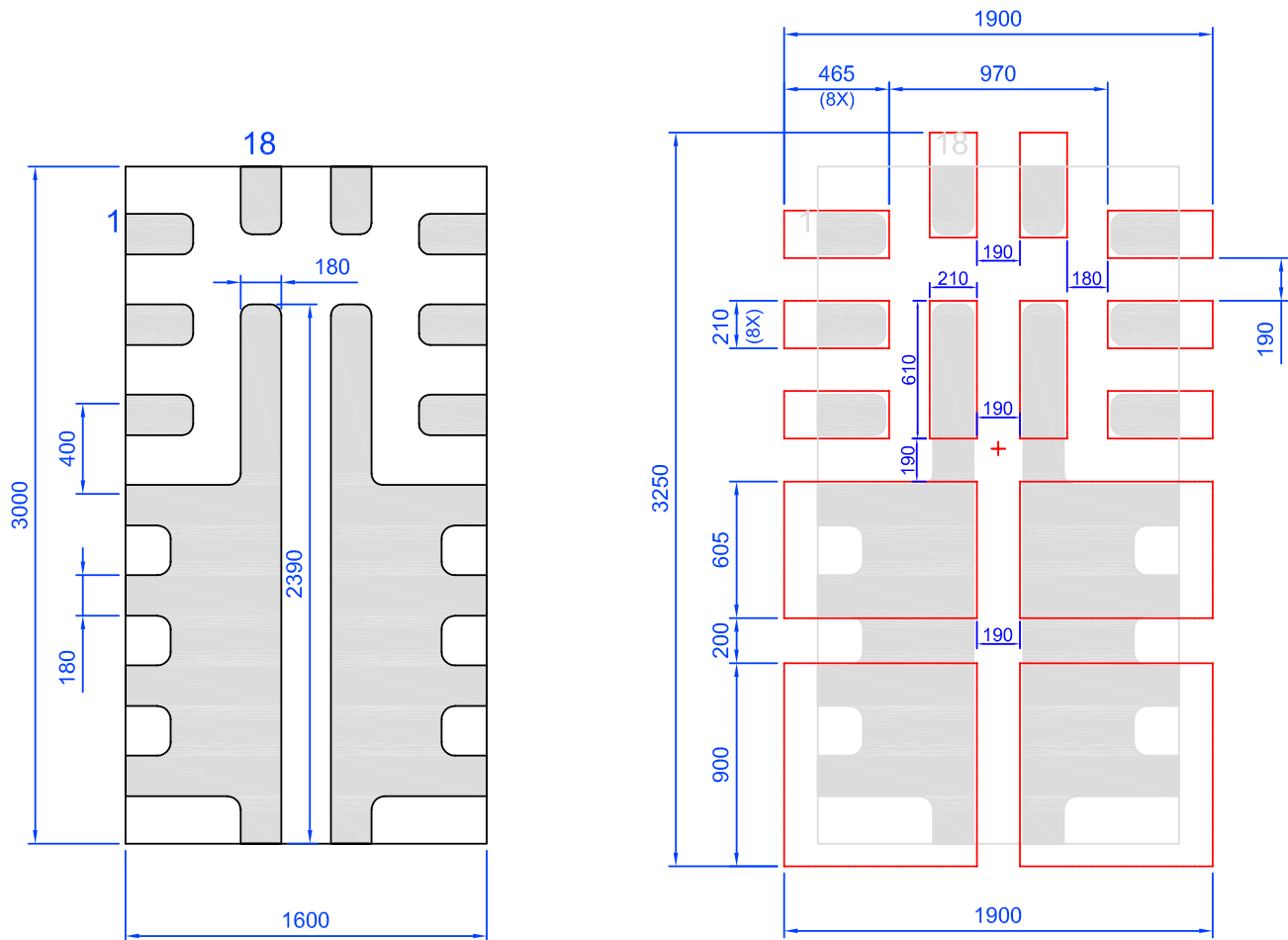
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.05	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.64	0.69	0.74
e	0.40 BSC			L2	0.15	0.20	0.25
L3	2.34	2.39	2.44	L4	0.13	0.18	0.23



SLG59H1127V 18-pin STQFN PCB Landing Pattern

 Exposed Pad
(PKG face down)

 Recommended Land Pattern
(PKG face down)



Note: All dimensions shown in micrometers (μm)

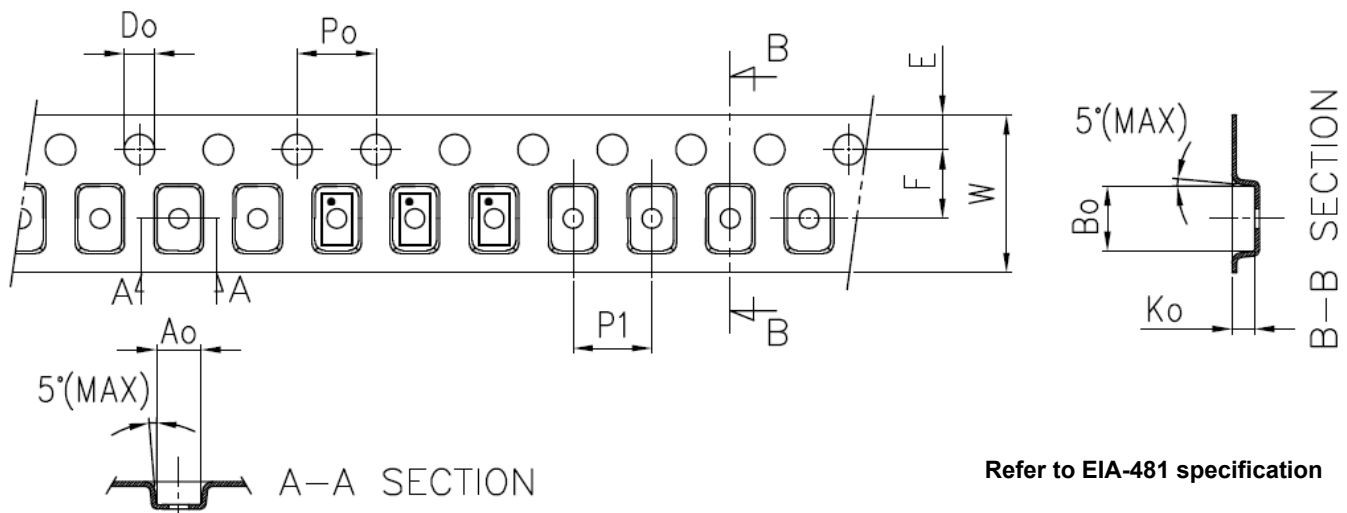


Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 18L 0.4P FC Green	18	1.6 x 3 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 18L 0.4P FC Green	1.78	3.18	0.76	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm³ (nominal). More information can be found at www.jedec.org.



SILEGO

SLG59H1127V

Revision History

Date	Version	Change
2/24/2017	1.00	Production Release