

74LV74-Q100

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 1 — 23 September 2013

Product data sheet

1. General description

The 74LV74-Q100 is a dual positive edge triggered, D-type flip-flop. It has individual data ($\overline{nD}$) inputs, clock ($\overline{nCP}$) inputs, set ($\overline{nSD}$) and ($\overline{nRD}$) inputs, and complementary $\overline{nQ}$ and $\overline{n\overline{Q}}$ outputs.

The set and reset are asynchronous active LOW inputs that operate independently of the clock input. Information on the data input is transferred to the $\overline{nQ}$ output on the LOW-to-HIGH transition of the clock pulse. The $\overline{nD}$ inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Direct interface with TTL levels (2.7 V to 3.6 V)
- ESD protection:
 - ◆ MIL-STD-883C, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV74D-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV74PW-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

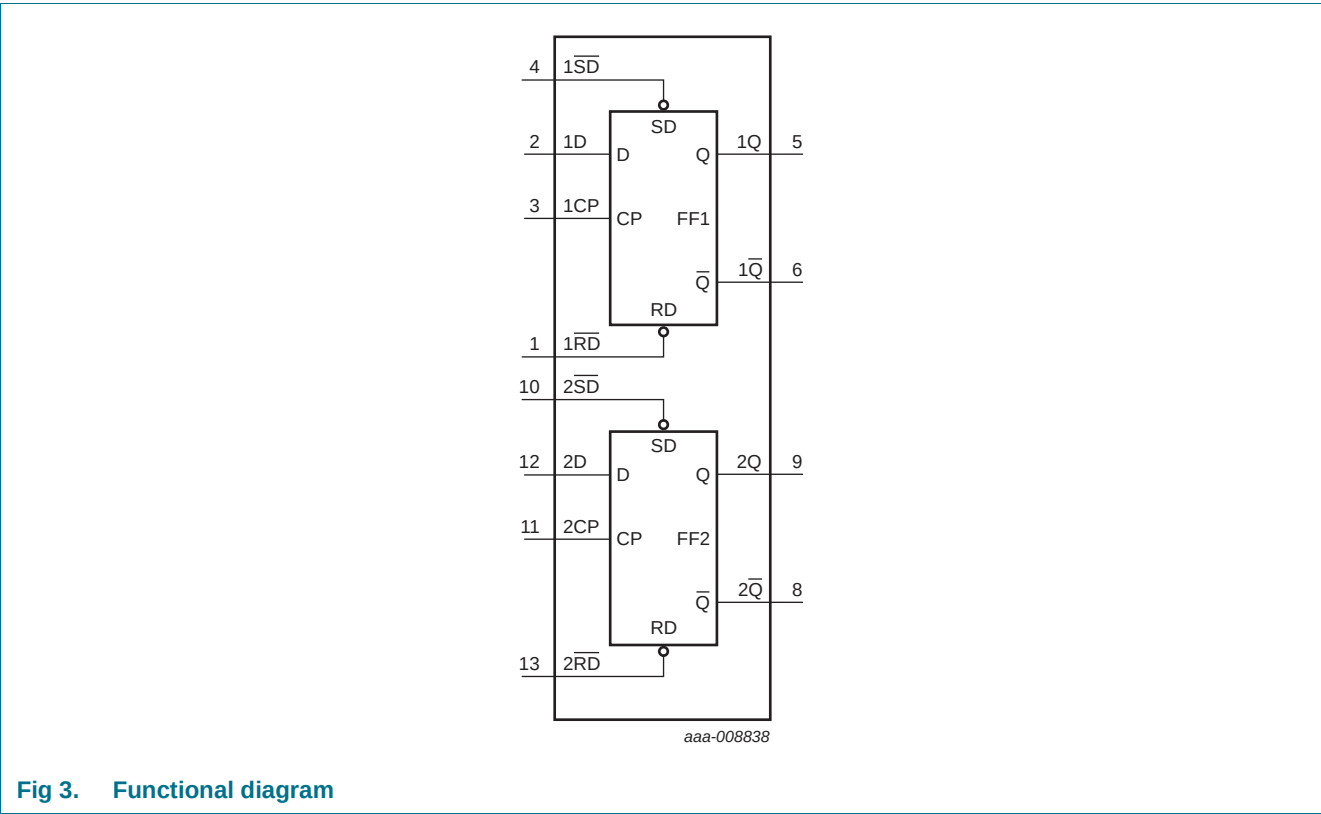
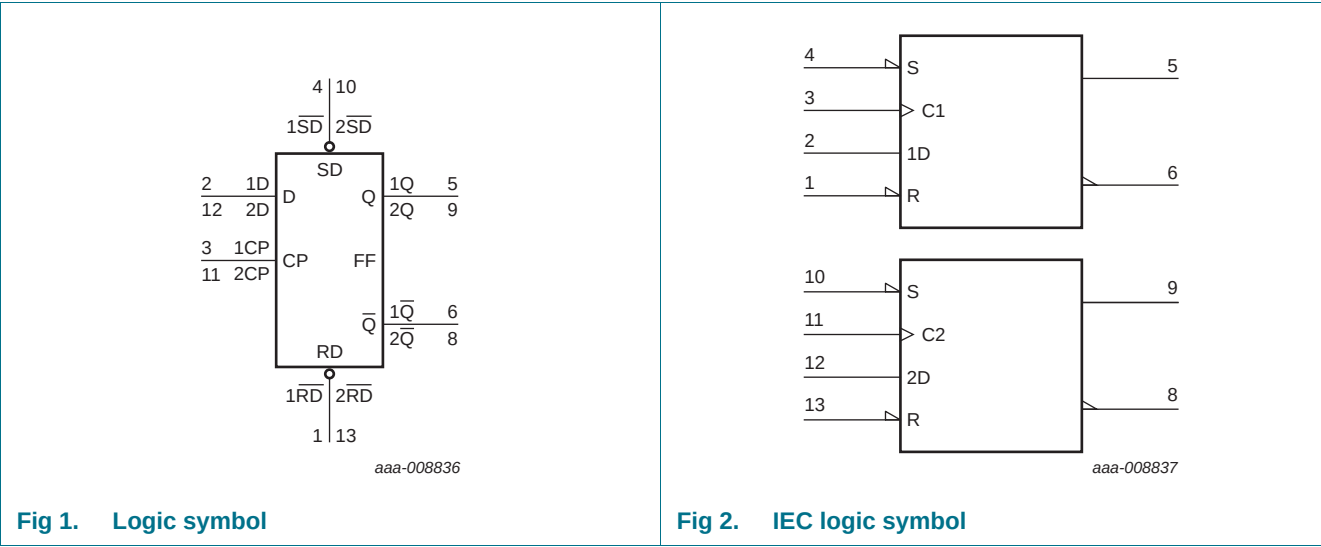
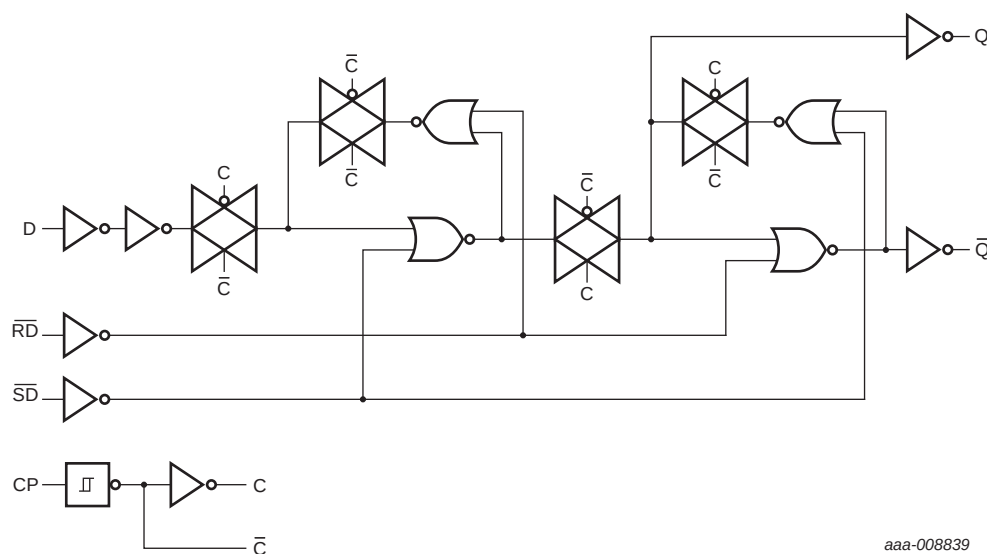


Fig 3. Functional diagram

**Fig 4. Logic diagram (one flip-flop)**

5. Pinning information

5.1 Pinning

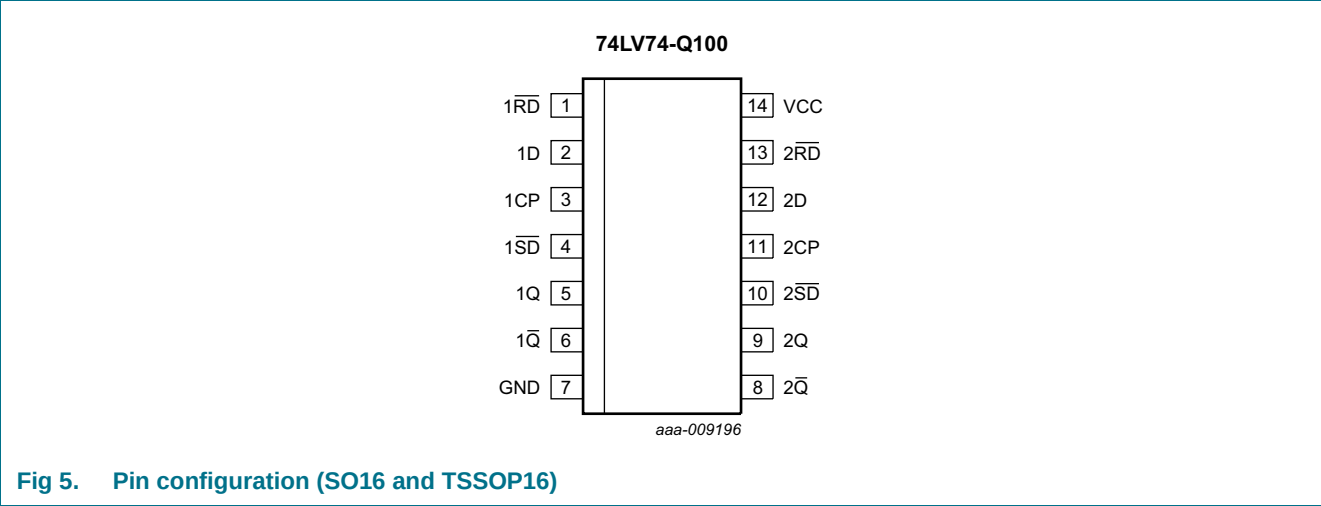


Fig 5. Pin configuration (SO16 and TSSOP16)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1RD	1	asynchronous reset-direct input (active-LOW)
1D	2	data inputs
1CP	3	clock input (LOW-to-HIGH), edge-triggered)
1SD	4	asynchronous set-direct input (active-LOW)
1Q	5	true flip-flop outputs
1Q	6	complement flip-flop outputs
GND	7	ground (0 V)
2Q	8	complement flip-flop outputs
2Q	9	true flip-flop outputs
2SD	10	asynchronous set-direct input (active-LOW)
2CP	11	clock input (LOW-to-HIGH), edge-triggered)
2D	12	data inputs
2RD	13	asynchronous reset-direct input (active-LOW)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table^[1]

Input				Output			
nSD	nRD	nCP	nD	nQ	nQ	Q _{n+1}	nQ _{n+1}
L	H	X	X	H	L	-	-
H	L	X	X	L	H	-	-
L	L	X	X	H	H	-	-
H	H	↑	L	-	-	L	H
H	H	↑	H	-	-	H	L

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 ↑ = LOW-to-HIGH clock transition;
 Q_{n+1} = state after the next LOW-to-HIGH CP transition

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	20	mA
V _I	input voltage		-0.5	+7	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0	-	±50	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	±50	mA
I _{GND}	ground current		-	±50	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		SO16 package	-	500	mW
		TSSOP16 package	-	400	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] P_{tot} derates linearly with 8 mW/K above 70 °C.
 [3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0 \text{ V to } 2.0 \text{ V}$	0	-	500	ns/V
		$V_{CC} = 2.0 \text{ V to } 2.7 \text{ V}$	0	-	200	ns/V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	-	100	ns/V
		$V_{CC} = 3.6 \text{ V to } 5.5 \text{ V}$	0	-	50	ns/V

[1] LV is guaranteed to function down to $V_{CC} = 1.0 \text{ V}$ (input levels GND or V_{CC}). DC characteristics are guaranteed from $V_{CC} = 1.2 \text{ V}$ to $V_{CC} = 5.5 \text{ V}$.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V _{CC} = 2.3 V to 2.7 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	0.7 × V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	-	0.3 × V _{CC}	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = –100 µA						
		V _{CC} = 1.2 V	-	1.2	-	-	-	
		V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		V _{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		V _{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		V _{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		standard outputs: V _I = V _{IH} or V _{IL}						
		V _{CC} = 3.0 V; I _O = –6 mA	2.40	2.82	-	2.20	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = 100 µA						
		V _{CC} = 1.2 V	-	0	-	-	-	
		V _{CC} = 2.0 V	-	0	0.2	-	0.2	V
		V _{CC} = 2.7 V	-	0	0.2	-	0.2	V
		V _{CC} = 3.0 V	-	0	0.2	-	0.2	V
		V _{CC} = 4.5 V	-	0	0.2	-	0.2	V
		standard outputs: V _I = V _{IH} or V _{IL}						
		V _{CC} = 3.0 V; I _O = 6 mA	-	0.25	0.40	-	0.50	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	20	-	80	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} – 0.6 V; V _{CC} = 2.7 V to 3.6 V	-	-	500	-	850	µA
C _I	input capacitance		-	3.5	-			pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V): for test circuit, see [Figure 8](#)

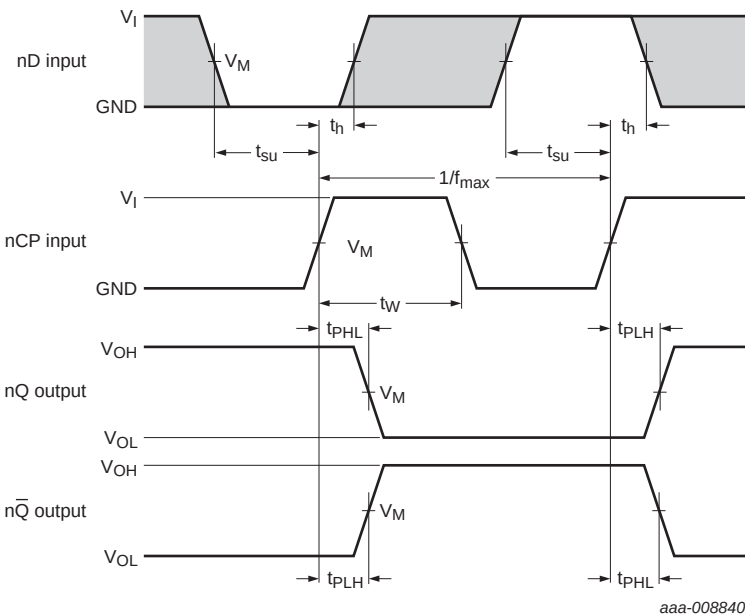
Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	nCP to nQ, n $\overline{Q}$; see Figure 6 ^[2]						
		$V_{CC} = 1.2\text{ V}$	-	70	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	24	44	-	56	ns
		$V_{CC} = 2.7\text{ V}$	-	18	28	-	41	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	-	13	26	-	33	ns
		$V_{CC} = 3.3\text{ V}; C_L = 15\text{ pF}$	-	11	-	-	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ^[4]	-	9.5	17	-	23	ns
		n $\overline{SD}$ to nQ, n $\overline{Q}$; see Figure 7						
		$V_{CC} = 1.2\text{ V}$	-	90	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	31	46	-	58	ns
		$V_{CC} = 2.7\text{ V}$	-	23	34	-	43	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	-	17	27	-	34	ns
		$V_{CC} = 3.3\text{ V}; C_L = 15\text{ pF}$	-	14	-	-	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ^[4]	-	12	19	-	24	ns
		n $\overline{RD}$ to nQ, n $\overline{Q}$; see Figure 7						
		$V_{CC} = 1.2\text{ V}$	-	90	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	31	46	-	58	ns
		$V_{CC} = 2.7\text{ V}$	-	23	34	-	43	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	-	17	27	-	34	ns
		$V_{CC} = 3.3\text{ V}; C_L = 15\text{ pF}$	-	14	-	-	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ^[4]	-	12	19	-	24	ns
t_w	pulse width	nCP input HIGH to LOW; see Figure 6						
		$V_{CC} = 2.0\text{ V}$	34	10	-	41	-	ns
		$V_{CC} = 2.7\text{ V}$	25	8	-	30	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	20	7	-	24	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ^[4]	15	6	-	18	-	ns
		n $\overline{SD}$ or n $\overline{RD}$ pulse width LOW; see Figure 7						
		$V_{CC} = 2.0\text{ V}$	34	10	-	41	-	ns
		$V_{CC} = 2.7\text{ V}$	25	8	-	30	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	20	7	-	24	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ^[4]	15	6	-	18	-	ns

Table 7. Dynamic characteristics ...continuedGND (ground = 0 V): for test circuit, see [Figure 8](#)

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{rec}	recovery time	nRD; see Figure 7						
		$V_{\text{CC}} = 1.2 \text{ V}$	-	5	-	-	-	ns
		$V_{\text{CC}} = 2.0 \text{ V}$	14	2	-	15	-	ns
		$V_{\text{CC}} = 2.7 \text{ V}$	10	1	-	11	-	ns
		$V_{\text{CC}} = 3.0 \text{ V to } 3.6 \text{ V}$	^[3] 8	1	-	9	-	ns
		$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$	^[4] 6	1	-	7	-	ns
t_{su}	set-up time	nD to nCP; see Figure 6						
		$V_{\text{CC}} = 1.2 \text{ V}$	-	10	-	-	-	ns
		$V_{\text{CC}} = 2.0 \text{ V}$	22	4	-	26	-	ns
		$V_{\text{CC}} = 2.7 \text{ V}$	12	3	-	15	-	ns
		$V_{\text{CC}} = 3.0 \text{ V to } 3.6 \text{ V}$	^[3] 8	2	-	10	-	ns
		$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$	^[4] 6	1	-	8	-	ns
t_{h}	hold time	nD to nCP; see Figure 6						
		$V_{\text{CC}} = 1.2 \text{ V}$	-	–10	-	-	-	ns
		$V_{\text{CC}} = 2.0 \text{ V}$	3	–2	-	3	-	ns
		$V_{\text{CC}} = 2.7 \text{ V}$	3	–2	-	3	-	ns
		$V_{\text{CC}} = 3.0 \text{ V to } 3.6 \text{ V}$	3	–2	-	3	-	ns
		$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$	3	–2	-	3	-	ns
f_{max}	maximum frequency	nCP; see Figure 6						
		$V_{\text{CC}} = 2.0 \text{ V}$	14	40	-	12	-	MHz
		$V_{\text{CC}} = 2.7 \text{ V}$	50	90	-	40	-	MHz
		$V_{\text{CC}} = 3.0 \text{ V to } 3.6 \text{ V}$	^[3] 60	100	-	48	-	MHz
		$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$	^[4] 70	110	-	56	-	MHz
C_{PD}	power dissipation capacitance	$V_{\text{I}} = \text{GND to } V_{\text{CC}}$	^[5] -	24	-	-	-	pF

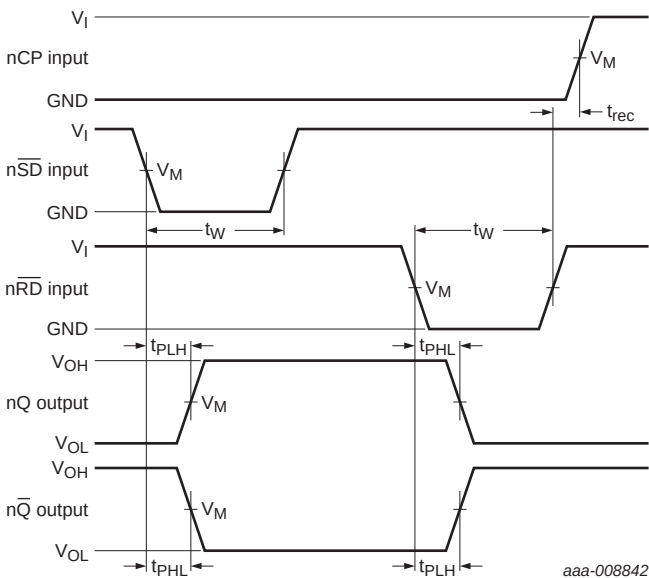
[1] Typical values are measured at $T_{\text{amb}} = 25 \text{ °C}$.[2] t_{pd} is the same as t_{PHL} and t_{PLH} .[3] Typical value measured at $V_{\text{CC}} = 3.3 \text{ V}$.[4] Typical values are measured at $V_{\text{CC}} = 5.0 \text{ V}$.[5] C_{PD} is used to determine the dynamic power dissipation $P_{\text{D}} = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_{\text{I}} + \Sigma (C_{\text{L}} \times V_{\text{CC}}^2 \times f_{\text{O}})$ (P_{D} in μW), where: f_{I} = input frequency in MHz; f_{O} = output frequency in MHz; $\Sigma (C_{\text{L}} \times V_{\text{CC}}^2 \times f_{\text{O}})$ = sum of outputs; C_{L} = output load capacitance in pF; V_{CC} = supply voltage in V.

11. Waveforms



Measurement points are given in Table 8.
The shaded areas indicate when the input is permitted to change for predictable output performance.

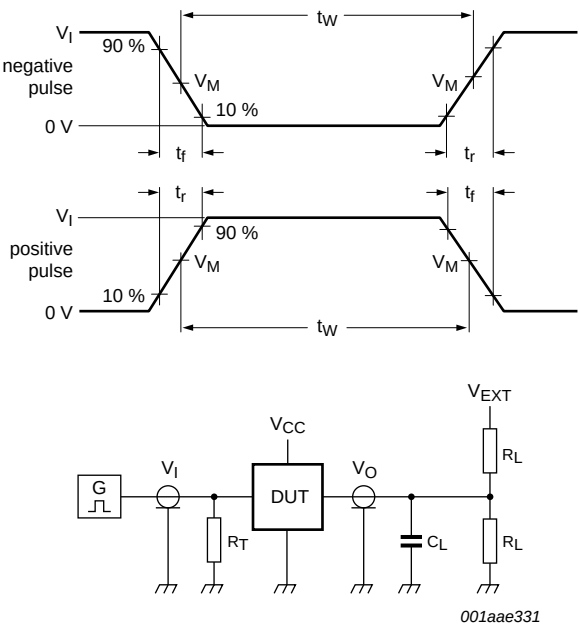
Fig 6. Clock pulse (nCP) to output (nQ, nQ̄) propagation delays, nCP pulse width and maximum frequency



Measurement points are given in Table 8.
Fig 7. Set (nSD) and reset (nRD) input to output (nQ, nQ̄) propagation delays, pulse widths and nRD to nCP recovery time

Table 8. Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _M
< 2.7 V	0.5V _{CC}	0.5V _{CC}
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	0.5V _{CC}	0.5V _{CC}



Test data is given in [Table 9](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V _{EXT}
	V _I	t _r , t _f	C _L	R _L	t _{PHL} , t _{PLH}
< 2.7 V	V _{CC}	2.5 ns	50 pF	1 kΩ	open
2.7 V to 3.6 V	2.7 V	2.5 ns	50 pF, 15 pF	1 kΩ	open
≥ 4.5 V	V _{CC}	2.5 ns	50 pF	1 kΩ	open

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

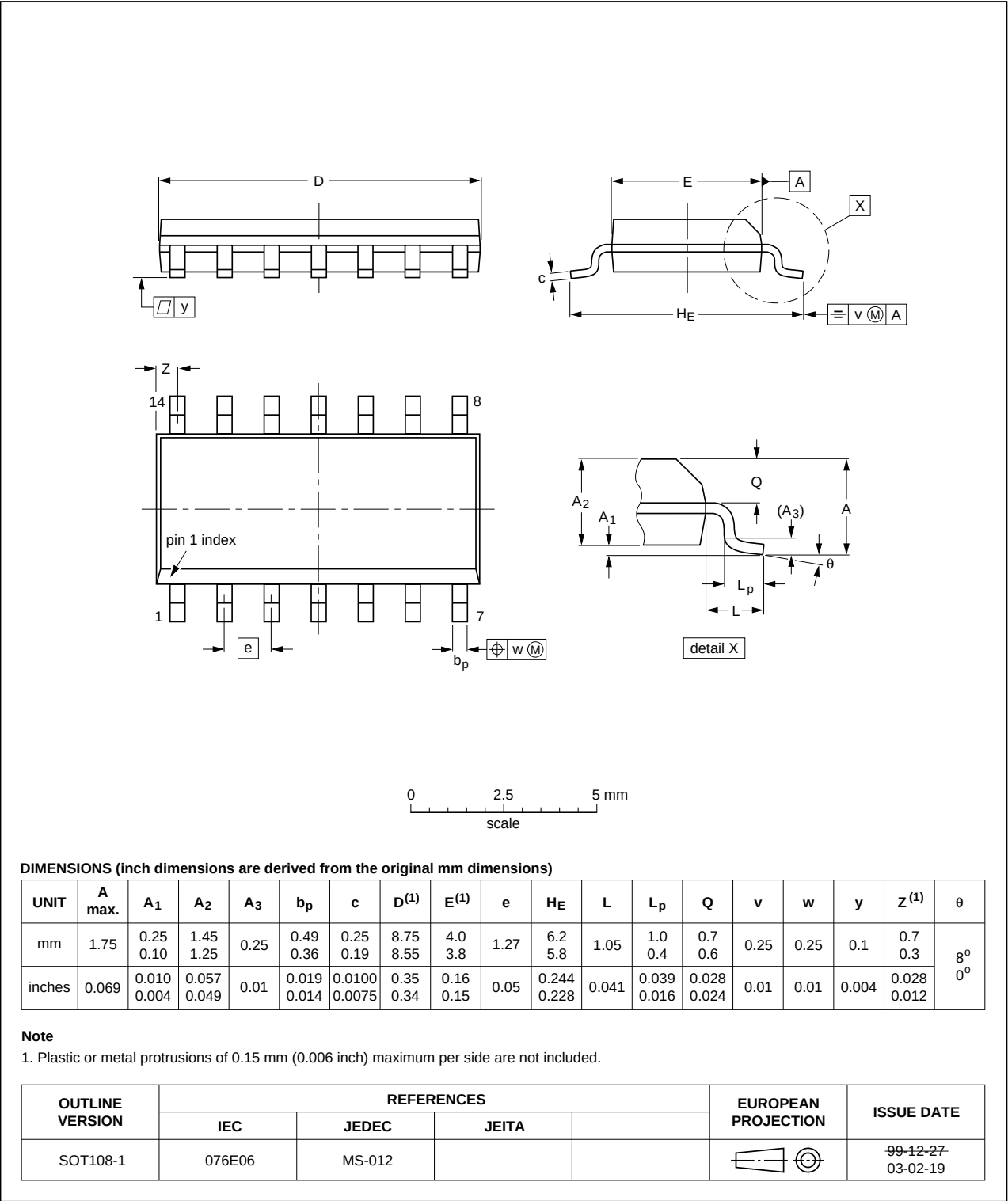


Fig 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

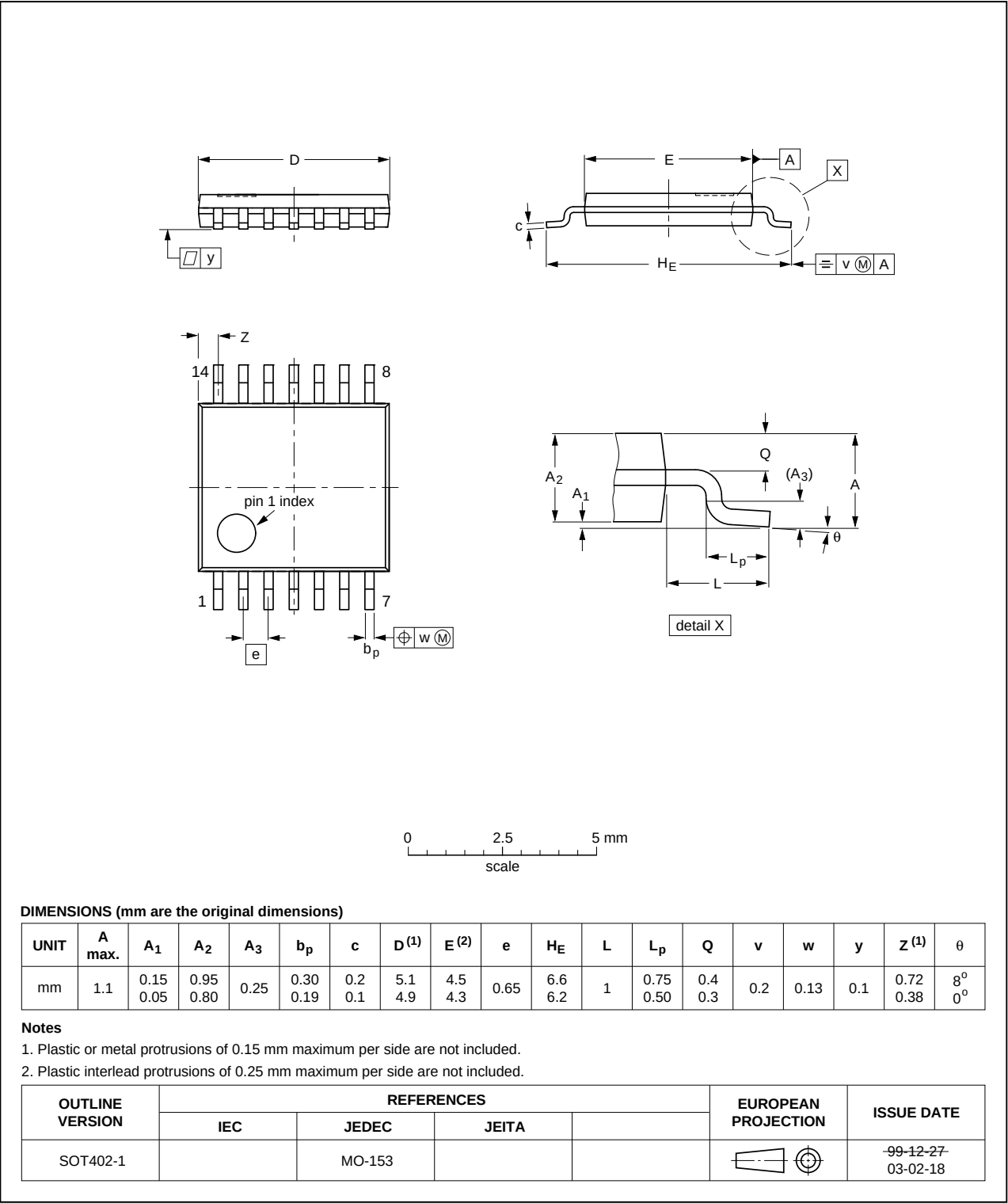


Fig 10. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV74_Q100 v.1	20130923	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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16. Contact information

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

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