

Dual 20V N-Channel Power MOSFET

GWS9294

The GWS9294 is a dual 20V, 12mΩ, N-channel power MOSFET used for Li-ion battery protection. It is offered in a 2mmx2mm MLPD with a very low thickness profile, 1mm maximum thickness. The device has extremely high power density, reducing the board size of the Li-ion battery power system. Designed for handheld devices with a high level of ESD protection.

PRODUCT SUMMARY			
$V_{(BR)DSS}$	$I_D = 250\mu A$	20V	Minimum
$r_{DS(ON)}$	$V_{GS} = 4.5V$	12mΩ	Typical

Features

- Monolithic dual MOSFET
- Low $r_{DS(ON)}$ in a small footprint
- Ultra low gate charge and figure of merit
- MLPD 2mmx2mm package
- Low thermal resistance

Applications

- Li-ion battery protection
- Portable devices, cell phones, PDA
- Rated for short-circuit and overcurrent protection
- Integrated gate diodes provide ESD protection of 2.5kV HBM

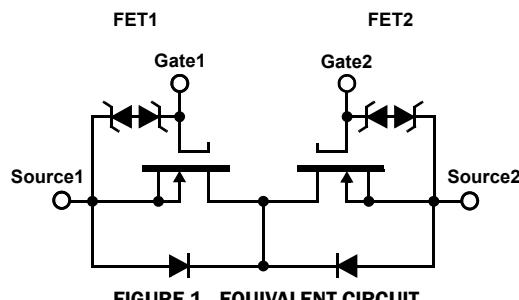


FIGURE 1. EQUIVALENT CIRCUIT

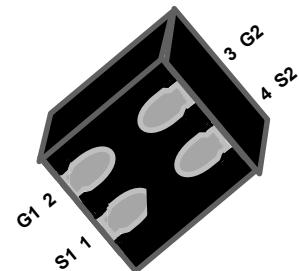
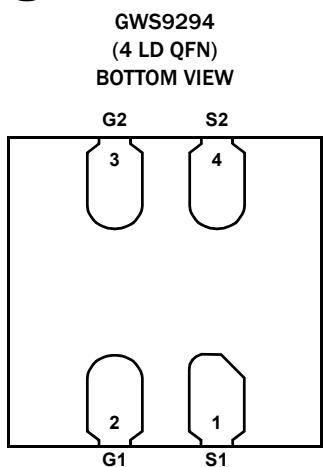


FIGURE 2. MLPD BOTTOM SIDE

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)
GWS9294	94	-55 to +150	4 Ld QFN

Pin Configuration



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1	S1	Source of FET1
2	G1	Gate of FET1
3	G2	Gate of FET2
4	S2	Source of FET2

Absolute Maximum Ratings [\(Note 1\)](#)

Drain-to-Source Voltage (V_{DS})	20V
Gate-to-Source Voltage (V_{GS})	$\pm 12V$
Drain Current (I_D) (Note 2)	
$T_A = +25^\circ C$	10.1A (10s), 6.5A (Steady State)
$T_A = +70^\circ C$	8.1A (10s), 5.2A (Steady State)
Drain Current ($R_{thjFoot}$)	
$T_F = +25^\circ C$	15A (Steady State)
Pulsed Drain Current (I_{PM})	60A
ESD Rating	
Human Body Model	2.5kV

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. $T_J = +25^\circ C$ unless otherwise noted.
2. Surface mounted on FR4 board.

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^\circ C/W$)	θ_{JF} ($^\circ C/W$)
$t \leq 10s$	35	
Steady State	85	16
Maximum Power Dissipation (P_D) (Note 2)		
$T_A = +25^\circ C$	3.6W (10s) 1.47W (Steady State)	
$T_A = +70^\circ C$	2.29W (10s) 0.94W (Steady State)	
Junction and Storage Temperature Range (T_J, T_{stg})	-55 $^\circ C$ to +150 $^\circ C$	
Pb-Free Reflow Profile	see TB493	

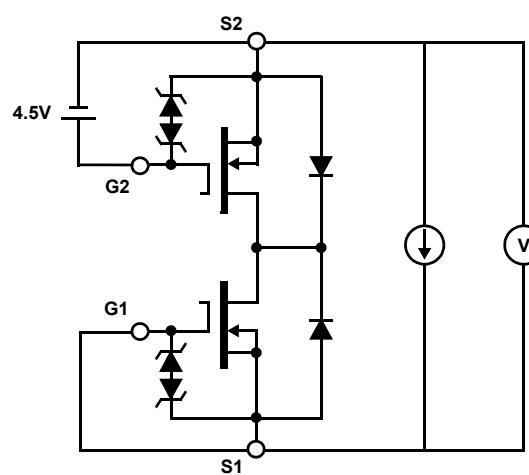
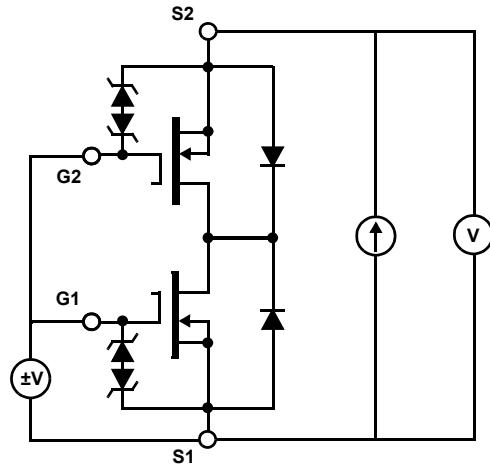
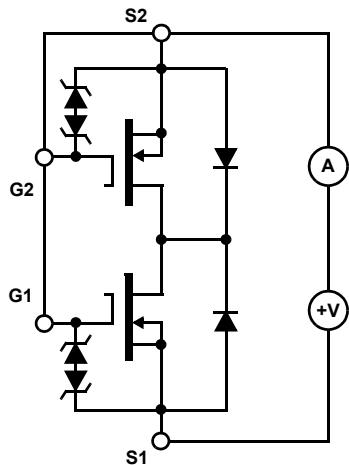
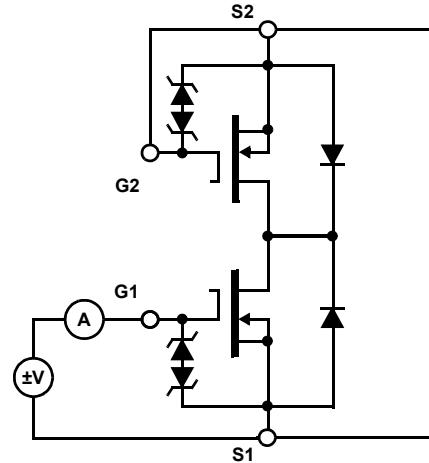
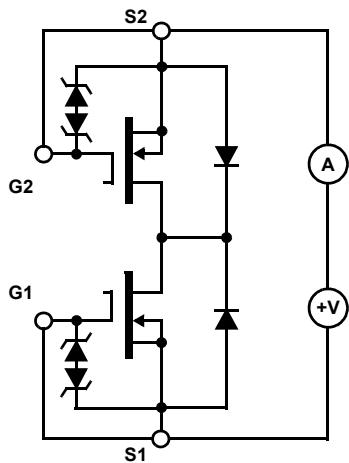
Electrical Characteristics $T_J = +25^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 3)	TYP (Note 4)	MAX (Note 3)	UNIT
STATIC						
$V_{(BR)SSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	20			V
I_{SSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0V, V_{DS} = 20V$			1	μA
I_{GSS}	Gate Body Leakage	$V_{DS} = 0V, V_{GS} = \pm 8V$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1mA$	0.5	0.6	1.5	V
$r_{DS(ON)}$	Drain-to-Source On-State Resistance (Note 5) (per MOSFET)	$V_{GS} = 4.5V, I_D = 6.5A$	6	12	13	$m\Omega$
		$V_{GS} = 4.0V, I_D = 6.5A$	7	13	14	$m\Omega$
		$V_{GS} = 3.1V, I_D = 6.0A$	8	14	18	$m\Omega$
		$V_{GS} = 2.5V, I_D = 5.5A$	9	16	20	$m\Omega$
$r_{SS(ON)}$	Source-to-Source On-State Resistance (Note 5) (both MOSFETs in series)	$V_{GS} = 4.5V, I_D = 6.5A$	12	24	26	$m\Omega$
		$V_{GS} = 4.0V, I_D = 6.5A$	13	25	28	$m\Omega$
		$V_{GS} = 3.1V, I_D = 6.0A$	16	28	35	$m\Omega$
		$V_{GS} = 2.5V, I_D = 5.5A$	17	32	40	$m\Omega$
V_{SD}	Source-to-Drain Diode Voltage	$V_{GS} = 0, I_S = 6.5A$	0.5	0.8	1	V
DYNAMIC						
Q_g	Total Gate Charge	$V_{DS} = 10V, I_D = 5.0A, V_{GS} = 4.0V$		11		nC
C_{iss}	Input Capacitance	$V_{DS} = 10V, V_{GS} = 0V, f = 1MHz$		900		pF
C_{oss}	Output Capacitance			300		pF
C_{rss}	Reverse Transfer Capacitance			150		pF

NOTES:

3. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
4. Typical values are for $T_A = +25^\circ C$.
5. Good Kelvin measurement required.

Test Circuit Examples for Measuring FET1 Key Parameters



Typical Performance Curves

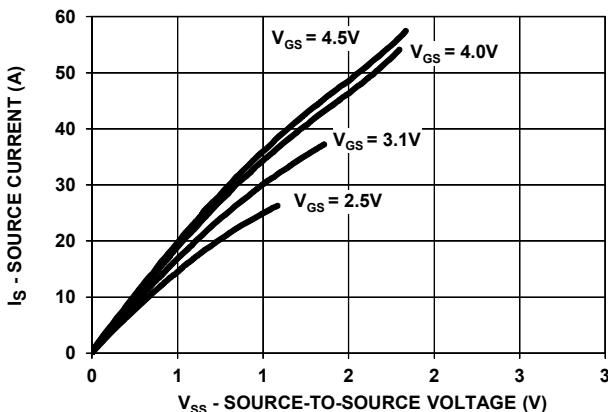


FIGURE 8. OUTPUT CHARACTERISTICS

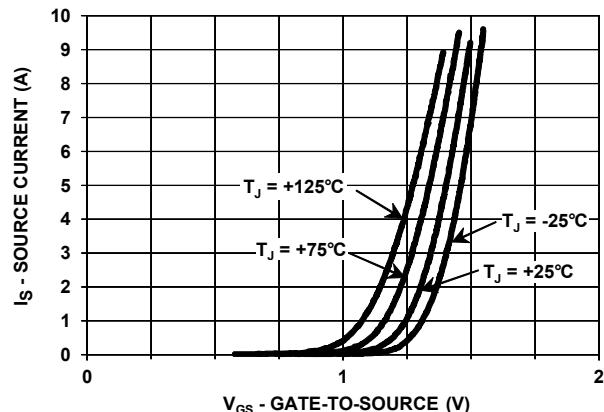


FIGURE 9. TRANSFER CHARACTERISTICS

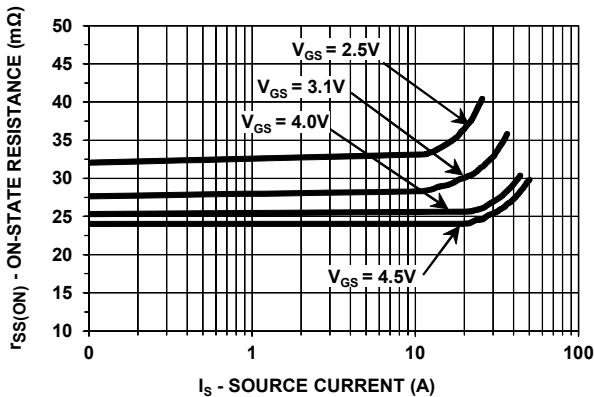


FIGURE 10. SOURCE-TO-SOURCE ON-STATE RESISTANCE vs SOURCE CURRENT

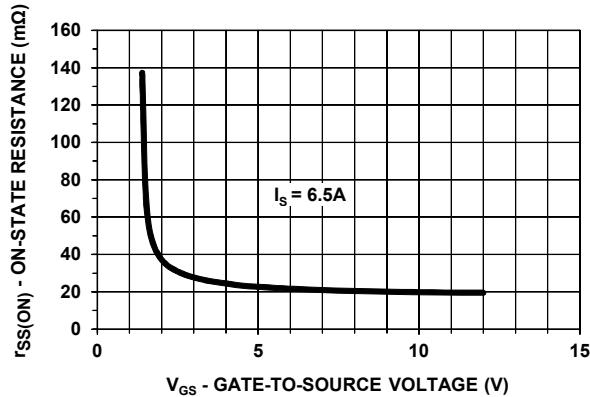


FIGURE 11. SOURCE-TO-SOURCE ON-STATE RESISTANCE vs GATE-TO-SOURCE VOLTAGE

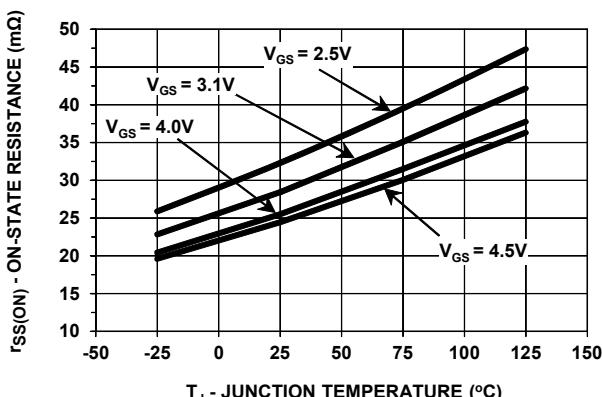


FIGURE 12. SOURCE-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

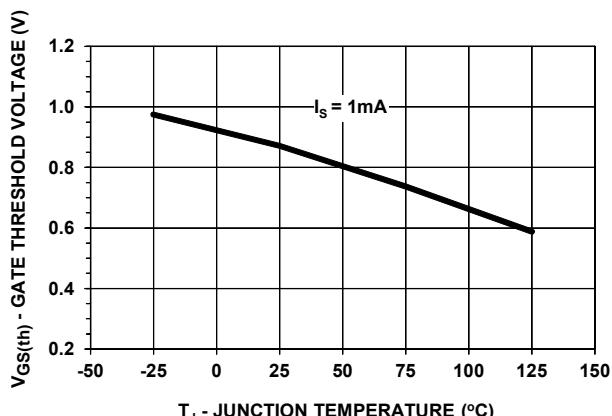


FIGURE 13. GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

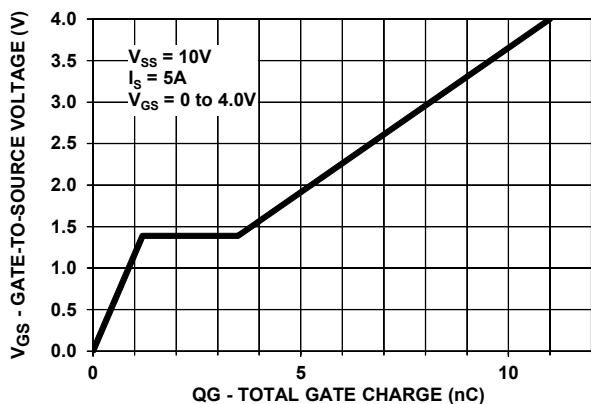


FIGURE 14. GATE CHARGE

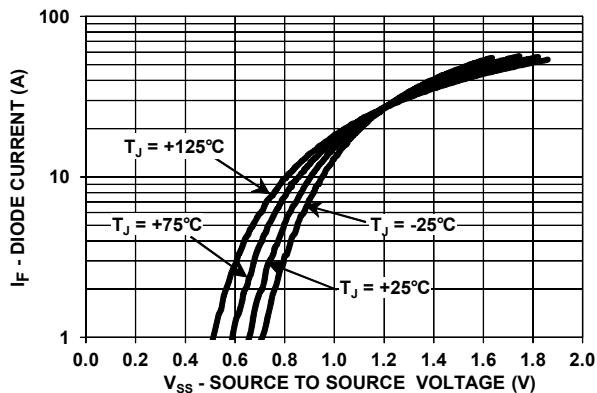


FIGURE 15. SOURCE-TO-SOURCE DIODE FORWARD VOLTAGE

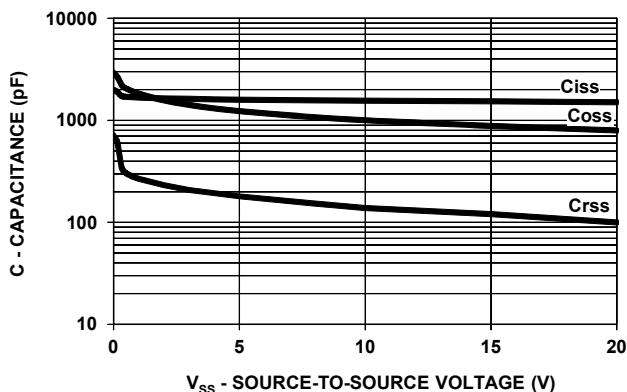


FIGURE 16. CAPACITANCE

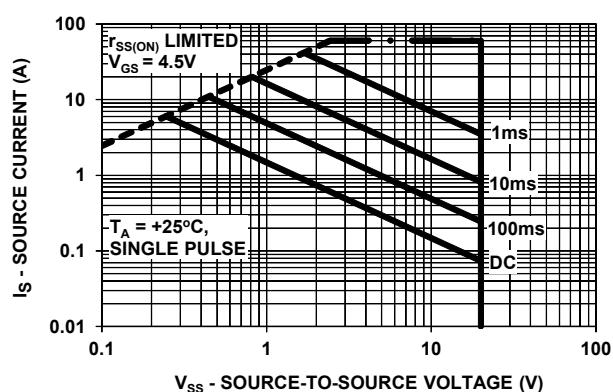


FIGURE 17. MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

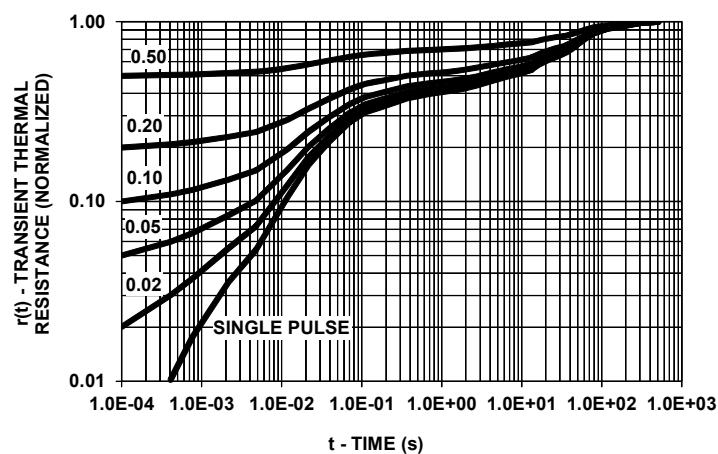


FIGURE 18. TRANSIENT THERMAL RESPONSE, JUNCTION-TO-AMBIENT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 22, 2015	FN8786.1	Added "Note 1. $T_J = +25^\circ\text{C}$ unless otherwise noted." to Abs Max on page 3.
October 30, 2015	FN8786.0	Initial release.

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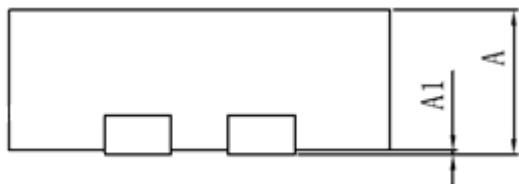
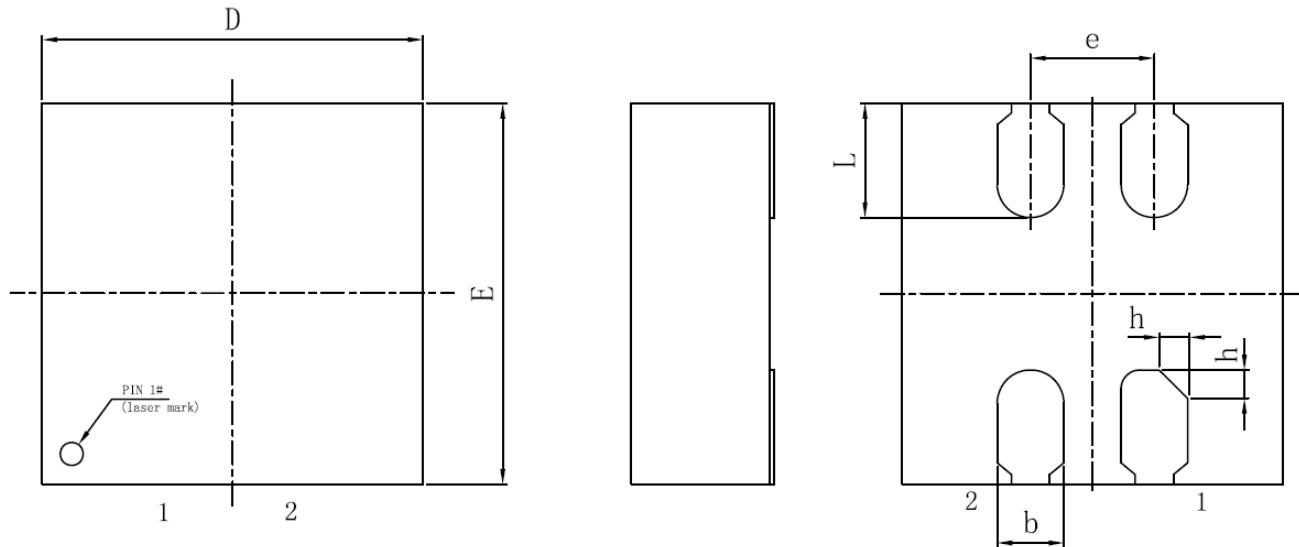
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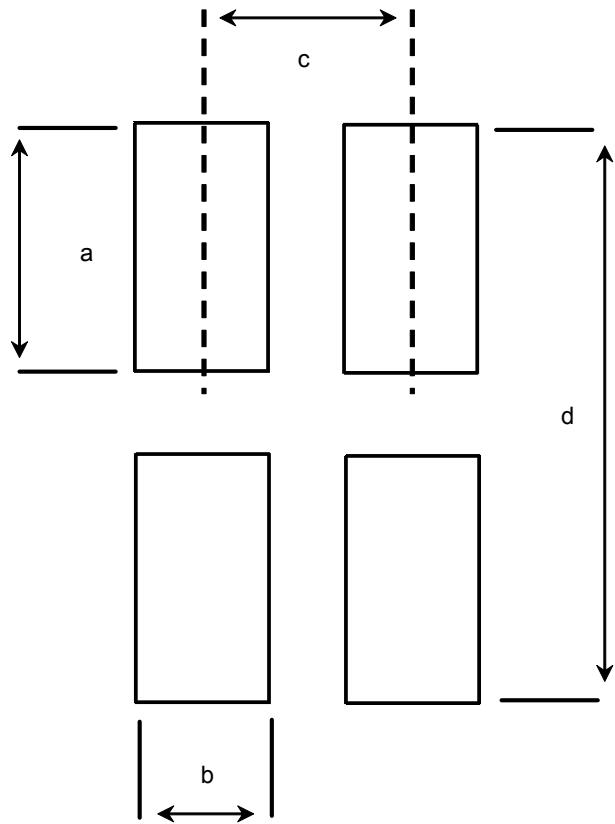
Package Outline and Dimensions



Pin	Node
1	Source 1
2	Gate 1
3	Gate 2
4	Source 2

Symbol	Min	Nom	Max
A	0.70		1.00
A1		0.02	0.05
b	0.275		0.400
D	2.00 BSC		
E	2.00 BSC		
e	0.65 BSC		
L	0.55	0.60	0.65
h	0.10	0.15	0.20

All dimensions in mm

Mounting Pad Layout and Dimensions

Symbol	Min	Nom	Max
a	0.788	0.838	0.888
b	0.358	0.381	0.404
c	0.65 BSC		
d	2.22	2.365	2.50

All dimensions in mm