Ethernet Switch

GSW140 (GSW140A3MC)
GSW140 (GSW140A3LC)

Data Sheet

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MaxLinear, Inc.
5966 La Place Court, Suite 100
Carlsbad, CA 92008
Tel.: +1 (760) 692-0711
Fax: +1 (760) 444-8598
www.maxlinear.com

Revision History

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Page	**Major changes since previous revision**
All	Removed MaxLinear Confidential from the document.
All	Removed the GSW140 (PEB7085M) and GSW140 (PEB7085MV12) devices.
14	**Section 1.1 Features**, **Interfaces** Removed mention of SGMII port from the PHY status indicating LEDs list.
55	**Section 3.2.8 Packet Insertion and Extraction** Removed mention of RMII interface from the first paragraph.
332	Updated **Table 70**, **Operating Range**.
344	Added **Section 5.5.10**, **Transformers (Magnetics)**.
346	Updated **Table 88**, **JEDEC Thermal Resistance PG-MRQFN-105 Package Parameters**.
348	Updated **Table 89**, **JEDEC Thermal Resistance LGA-105 Package Parameters**.
351	Updated **Literature References**.

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1 Product Overview

MaxLinear's Ethernet Switch GSW140 is a highly integrated, low-power, non-blocking six-port Gigabit Ethernet Switch with four tri-speed Ethernet PHYs, one four-speed SGMII interface, and one tri-speed RGMII interface. GSW140 uses a very small package, 8 mm x 8 mm, to minimize PCB size. There are two package variants available. For package details, see **Package Outline**.

Each Gigabit Ethernet (GbE) PHY supports 10BASE-Te, 100BASE-TX and 1000BASE-T standards and is characterized by low power consumption. Support of Energy-Efficient Ethernet allows for even further reduction in idle mode power consumption. Power saving at the system level is also possible with the Wake-on-LAN feature. A low-EMI line driver with integrated termination facilitates a simplified PCB design.

The 5th port of the GSW140 supports a four-speed (10/100/1000/2500 Mbps) SGMII interface to connect to an external PHY, SFP stick, or the MAC of an external chip.

The 6th port of the GSW140 supports a tri-speed (10/100/1000 Mbps) RGMII interface to connect to an external PHY or the MAC of an external chip.

The GSW140 is configurable via pin strapping, MDIO interface, UART interface, SPI interface, or optionally by connecting an external EEPROM.

In addition, the 7th 802.3 Gigabit Ethernet MAC is integrated for packet insertion and extraction. This allows an external controller to transmit and receive Ethernet packets via the management interface.

The GSW140 supports up to three LEDs per GbE PHY. Smart LED brightness control logic is integrated for power saving. LED brightness is either adjusted by a push button or varies dynamically depending on the intensity of the light measured by an external light sensor.

The 128 KB embedded packet storage SRAM is integrated and 9 KB jumbo frames are supported. The GSW140 integrates a 4K entry VLAN table for 802.1Q port-based, tag-based, and protocol based VLAN operation. It also supports double VLAN tagging, insertion, removal, and translation. The GSW140 features 2048 MAC addresses with 4-way hashing algorithm for address searching, auto-learning, and auto-aging.

Programmable parsing and a powerful classification engine allow future-proof designs that enable various data traffic types. The GSW140 supports IPv4 and IPv6 multicast forwarding, including IGMPv1/v2/v3 and MLD v1/v2 snooping.

The GSW140 features an advanced QoS architecture which prioritizes switch traffic for different classes of applications based on multiple fields of the packet. Multiple queues per port with strict or weighted round robin scheduling and rate shaping are supported. VLAN PCP and IP DSCP can be remarked. The GSW140 also supports Precise Time Stamping indication according to IEEE 1588v2 and IEEE 802.1AS.

Several degrees of application complexity are covered, from a basic stand-alone switch and set-top boxes to complex home gateways. The GSW140 is intended for Video/Audio applications in the Digital Home such as IP-TV, ADSL2+/VDSL2/PON IAD, Gateway, Wireless Router, Cable, Storage and HomePlug AV applications.

1.1 Features

This section provides an overview of the basic Gigabit Ethernet Switch GSW140 functionality.

Interfaces

- Four multiple speed Ethernet PHY interfaces, compliant with:
  - 10BASE-Te
  - 100BASE-TX
  - 1000BASE-T
  - Auto-MDIX
  - Auto-Downspeed
  - Auto-Negotiation with Next Page Support
  - Cable Diagnostics: Cable Open/Short Detection and Cable length estimation
  - Test Loops and Analog Self Test
  - Power Down Modes
  - 802.3az Energy-Efficient Ethernet
  - Support of Transformer-Less Ethernet for Backplane Applications
- One set of RGMII interface:
  - 10 Mbps, full and half duplex
  - 100 Mbps, full and half duplex
  - 1000 Mbps, full duplex
- One set of SGMII Interface:
  - Cisco* Serial-GMII Specification Rev 1.8 standard compliant operation at 1.25 Gbaud/s; extensions to achieve 3.125 GBaud/s by overclocking
  - 2.5 Gbps (one lane of XAUI conforming per 802.3, part 4, clause 47: 10 Gigabit Attachment Unit Interface (XAUI)) full duplex)
  - SerDes interface includes Clock and Data Recovery (CDR)
  - Multiple power-down modes
  - Programmable TX attenuation and amplification
  - Programmable flat-band RX equalization
  - Auto-calibration of RX and TX impedances
  - Test loop feature for debugging
  - 10 Mbps, full and half duplex
  - 100 Mbps, full and half duplex
  - 1000 Mbps, full duplex
  - 2500 Mbps, full duplex
- MDIO master interface to control external devices:
  - Support auto polling of external PHY devices registers
  - Support indirect access by command to external devices registers:
  - Support programmable MDC clock up to 17 MHz
- SPI master interface connecting to a serial external E2PROM:
  - Support programmable SPI clock up to 42 MHz
  - Supports automatic switch configuration from an external E2PROM memory
  - Support write access to E2PROM by an external controller
  - Supports different E2PROM sizes from 1 kbits to 1024 kbits
- SPI Slave, MDIO slave or UART interface to allow control from an external microcontroller:
  - Maximum MDIO interface clock: 25 MHz
  - Maximum SPI interface clock: 50 MHz
  - Minimum SPI interface clock: 2.5 MHz
  - UART baud rate from 4800 to 921600
- JTAG boundary scan, test and debug interface

  - Share pins with LED
- PHY status indicating LEDs:
  - Directly attached
  - Up to three LEDs per internal PHY port
  - Configurable LED functions per LED (link/activity, duplex/collision, link speed etc)
  - Steady/blinking indication
  - LED brightness controlled by an external push button
  - Up to 16 level LED brightness controlled by an external light sensor
- Twenty five general purpose IO: share pins with MDIO master interface, external interrupts, general purpose clock, SPI master interface, SPI slave interface, UART interface, MDIO slave, LED, JTAG functions.

Clocking

- Reference clock:
  - 25 MHz or 40 MHz
  - Crystal or direct input
- Two external clock outputs

Ethernet MACs

- Seven Ethernet MACs, complying with IEEE 802.3:
  - Four rates, that is, 10 Mbps, 100 Mbps, 1000 Mbps and 2500 Mbps operation speed
  - Half-duplex operation mode for 10 Mbps and 100 Mbps
  - Full-duplex operation mode for all speed
  - One dedicated Ethernet MAC is for packet insertion and extraction by an external controller via management interface
- Auto-negotiation for speed, duplex, flow control support, LPI support and link status
- Enhanced frame size support (“Jumbo frames”, programmable limit up to 9 Kbyte)
- Flow control:
  - Pause frame transmission/reception in full duplex mode
  - Forced collisions in half-duplex mode

Layer-2 Switching

- Store-and-forward architecture
- 1 Mbit on-chip segmented frame buffer
- 256 byte buffer segment size
- Up to 2048 MAC addresses:
  - Multiple-bucket HASH algorithm storage
  - Automatic learning and aging (1 s to 24 h)
  - Manual learning (static entries)
  - MAC learning limitation (configurable per port)
  - MAC port locking and spoofing detection (configurable per port)
  - MAC table freezing
- VLAN-unaware switching
- VLAN-aware switching:
  - Shared VLAN learning
  - Independent VLAN learning
  - Up to 4096 VLAN IDs
  - Port based VLAN
  - MAC based VLAN with automatic learning
  - Protocol-based VLAN based on flow classification result

  - Double VLAN or VLAN QinQ, addition/removal/translation of Service Tag VLAN ID and Customer Tag VLAN ID
  - Double VLAN or VLAN QinQ, port filtering based on both Service Tag VLAN ID and Customer Tag VLAN ID
- Multicast
  - Up to 64 multicast groups
  - Hardware IGMP mode: hardware based Join/Leave for IGMPv1/IGMPv2 mode, report suppression support
  - Software IGMP mode: IGMPv1/v2/v3 and MLDv1/v2 Snooping
  - Unknown IP multicast data stream forwarding or discard
  - Any Source Multicast and Source Specific Multicast forwarding

Layer-2/3/4 Flow Classification

- Multi-field parsing and classification, for example based on:
  - MAC source address
  - MAC destination address
  - Service Tag VLAN ID and Customer Tag VLAN ID
  - Ethertype
  - IPv4 header (DSCP, IP SA, IP DA)
  - IPv6 header (DSCP, IP SA, IP DA)
  - TCP source port/port range
  - TCP destination port/port range
  - UDP source port/port range
  - UDP destination port/port range
  - IGMP
  - MLD
  - ARP/RARP
  - ICMP
  - PPPoE, up to 16 session IDs
  - 64 ACL rules

Quality of Service

- Up to 32 CoS (Class of Service) queues
- Configurable egress queue scheduling
  - Strict priority
  - Weighted fair queueing, with configurable weights
  - Combination of strict priority and weighted fair queueing
- Flexible assignment of queues to egress ports
  - Multiple queues can be assigned to a single port (as far as available from the global pool of queues)
  - Maximum 16 queues per port
- Scalable egress rate shaping
  - 32 rate shapers
  - Up to 2 rate shapers can be assigned to a single queue (as far as available from global pool of rate shapers)
- Ingress traffic policing
  - 16 traffic policers
  - Standard single-rate Three Color Marker algorithm (srTCM)
  - Color-aware/-unaware operation
  - Policer can be assigned based on ingress port, egress port and flow classification result
  - Remarking, Drop or Flow Control for non-conforming traffic
- Flexible QoS handling based on any flow classification result, for example (but not limited to)
  - Service TAG VLAN PCP (Priority Code Point)
  - Customer TAG VLAN PCP (Priority Code Point)
  - IP DSCP

  - Ingress port
  - Source/destination IP address
  - TCP/UDP port/port range
- Service Tag VLAN PCP and DEI remarking
- Customer Tag VLAN PCP remarking
- DSCP remarking
- Congestion management
  - WRED algorithm (Weighted Random Early Discard)
  - Buffer reservation
  - Ingress port congestion based flow control
  - Ingress port metering based flow control
  - Three drop precedences
  - Configurable thresholds
- AVB support
  - Supports Precise Time Stamping indication according to IEEE P802.3bf for support of IEEE 1588v2, and IEEE 802.1AS
  - Rate shaper can work either at Token Bucket Mode or Credit Based Mode

Security

- Access Control List (ACL)
  - Use L2/L3/L4 flow classification results
  - Blacklist
  - Whitelist
- Access control actions
  - Accept
  - Discard
  - Redirect
  - Port Filtering
  - Cross-state forwarding
  - Cross-VLAN forwarding
  - QoS classification
  - VLAN Service Tag VLAN ID and Custom VLAN ID translation
- Broadcast, unknown multicast and unknown unicast storm control
- Authentication support (IEEE 802.1X Port Authentication)

Other Features

- Spanning Tree/Rapid Spanning Tree and 16 STP instances per port
- Port trunking of any two ports
- Port mirroring
- 802.3az Energy-Efficient Ethernet
- Wake-on-LAN
  - Detection of “magic packets”
  - Check WoL password (optional)
  - Wake-up interrupt to external device
- Special Tag
  - Provides in-band packet control and status communication with an internal or external controller
- RMON counters
- Boundary Scan

Power Supply

- Supply voltage domains
  - 3.3 V for digital PAD except RGMII PAD
  - 3.3 V for analog GPHY and SerDes
  - 1.1 V for digital core
  - 1.1 V for analog GPHY and SerDes
  - 3.3 V or 2.5 V for digital RGMII PAD

1.2 Applications

The following figures show application examples.

Figure 1 and **Figure 2** show standalone switch applications with a SFP port. The main advantage for the SFP port is the flexibility for putting it in the network. SFP stands for "small form-factor pluggable" and is a hot-swappable input/output device that plugs into a Gigabit Ethernet port or slot, linking the port with the network. An optional external EEPROM is used for switch configuration. **Figure 1** shows an optional low cost brightness sensor integrated to allow the LED brightness to be controlled by the Gigabit Ethernet Switch to save the system power consumption. **Figure 2** shows an optional brightness on/off switch integrated to allow the LED brightness to be controlled by the switch button to save the system power consumption.

Figure 3 shows an application of home gateway. An external SoC can manage the switch via management interface (eg. UART, SPI or MDIO interface). The 2.5 Gbps SGMII interface allows the high throughput rate between Ethernet LAN ports and SoC. In addition, another LAN/WAN type interface can be build (for example MoCA, Wi-Fi, Ethernet etc) and connected to the router/gateway SoC via a RGMII interface.

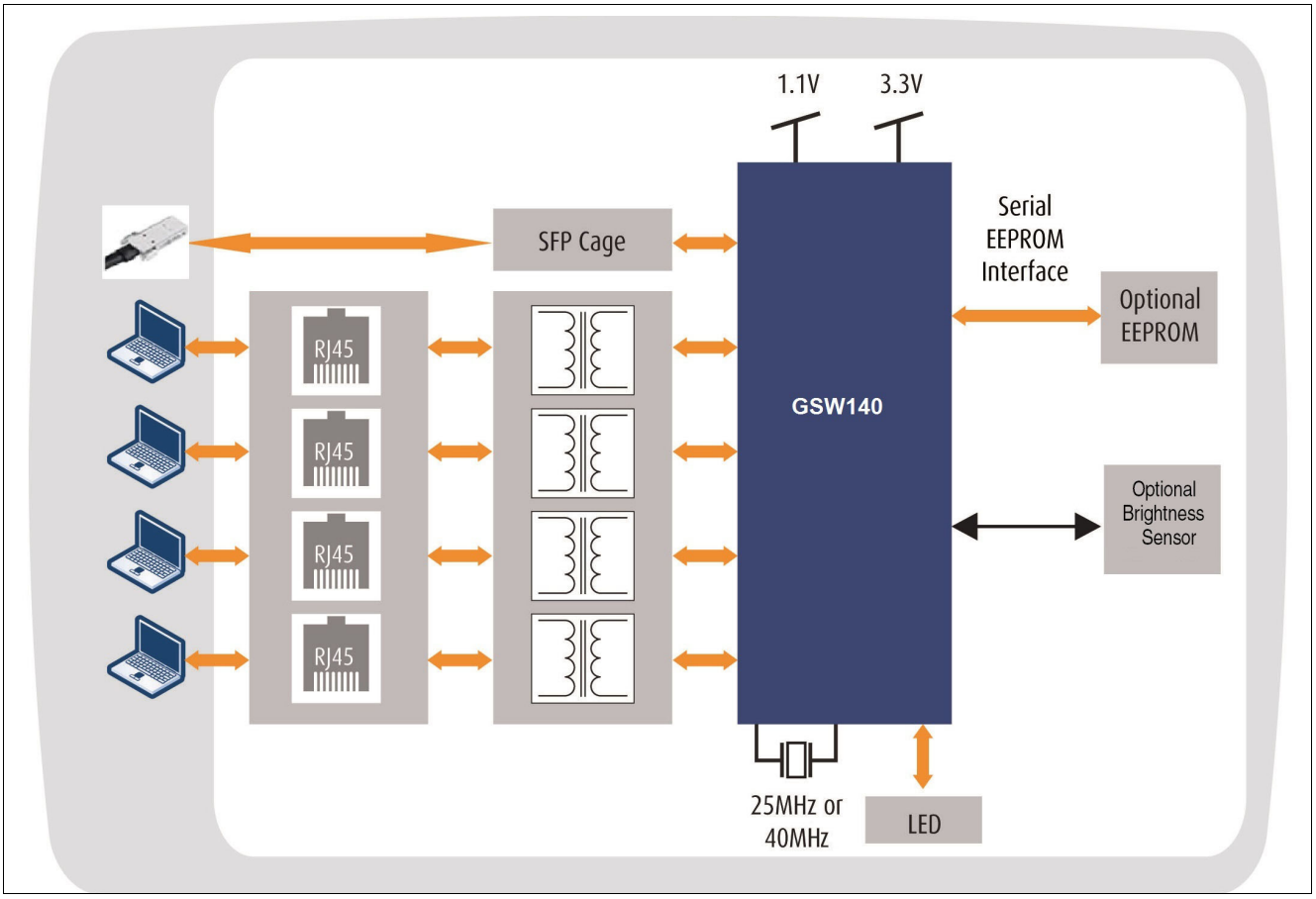


Figure 1 Standalone Desktop Switch with an Optional Brightness Sensor

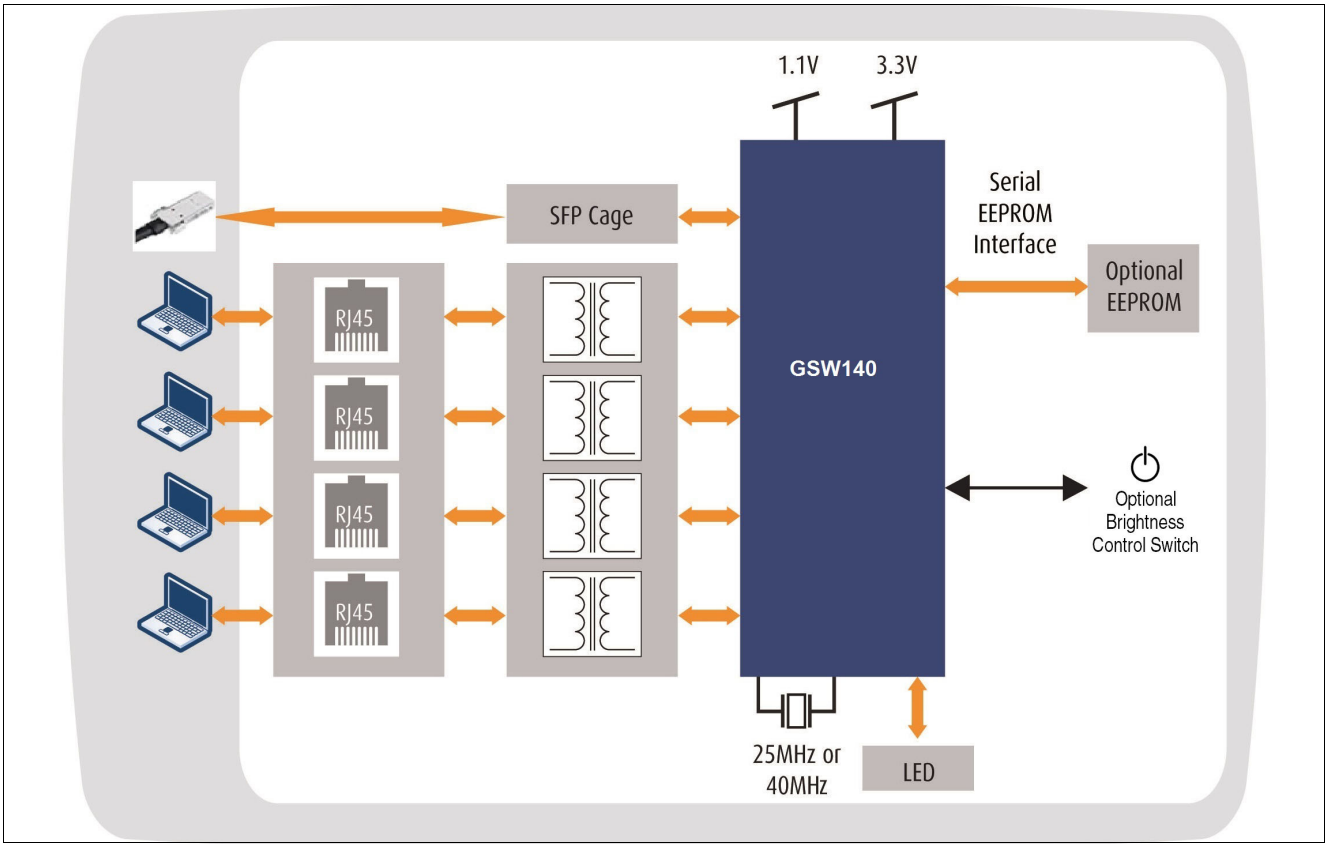


Figure 2 Standalone Desktop Switch with an Optional Brightness Control Switch

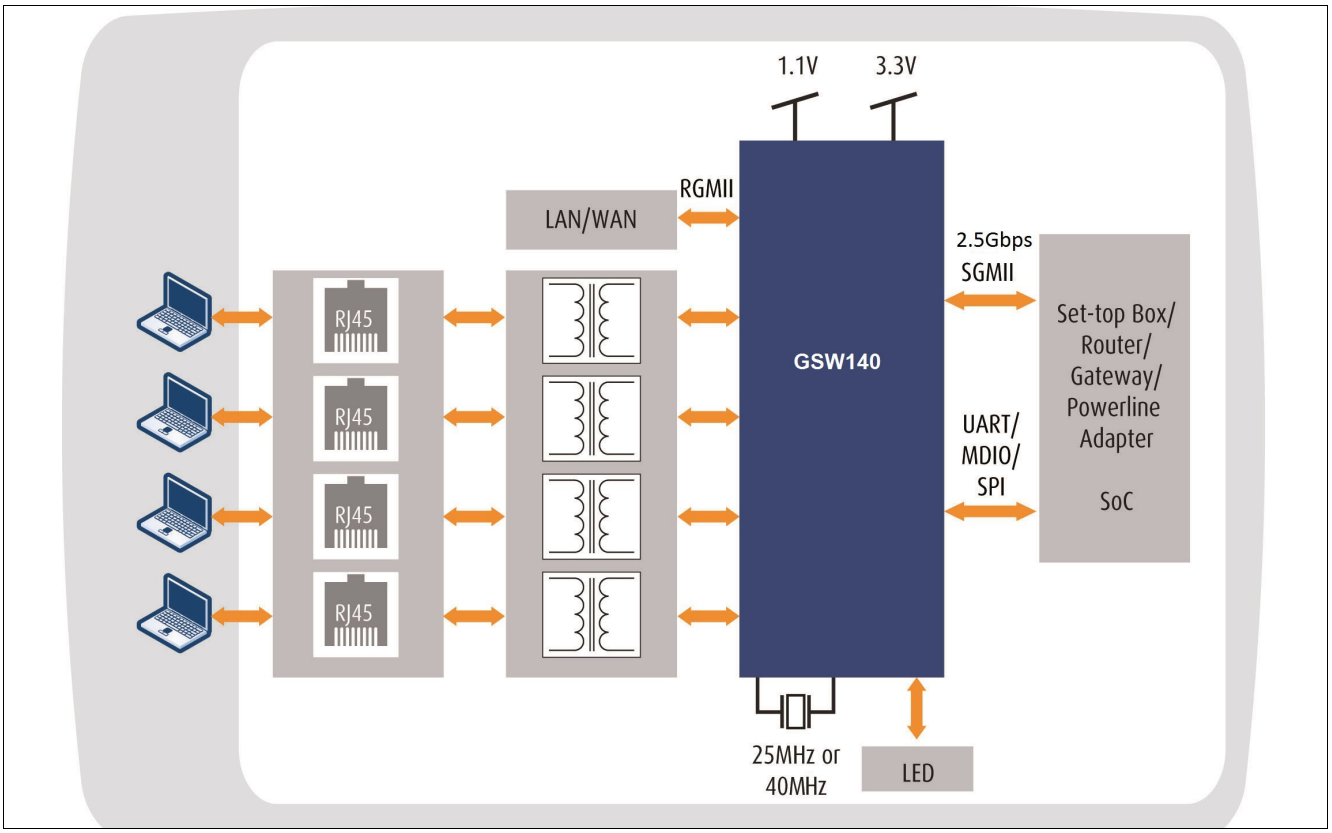


Figure 3 Home Gateway

1.3 Block Diagram

Figure 4 shows the block diagram.

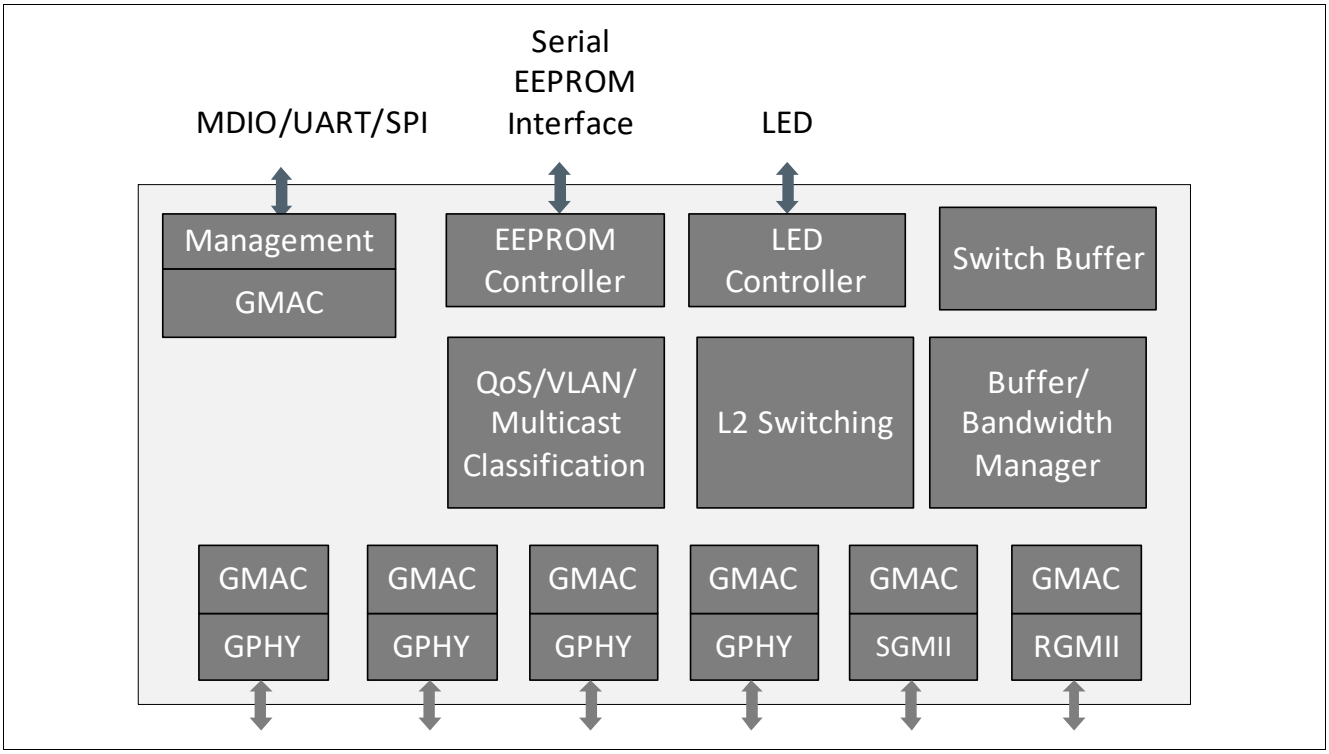


Figure 4 Block Diagram

2 External Signals

This chapter describes the signal mapping to the package.

2.1 Logic Symbol

Figure 5 gives a global overview of the device's external interfaces.

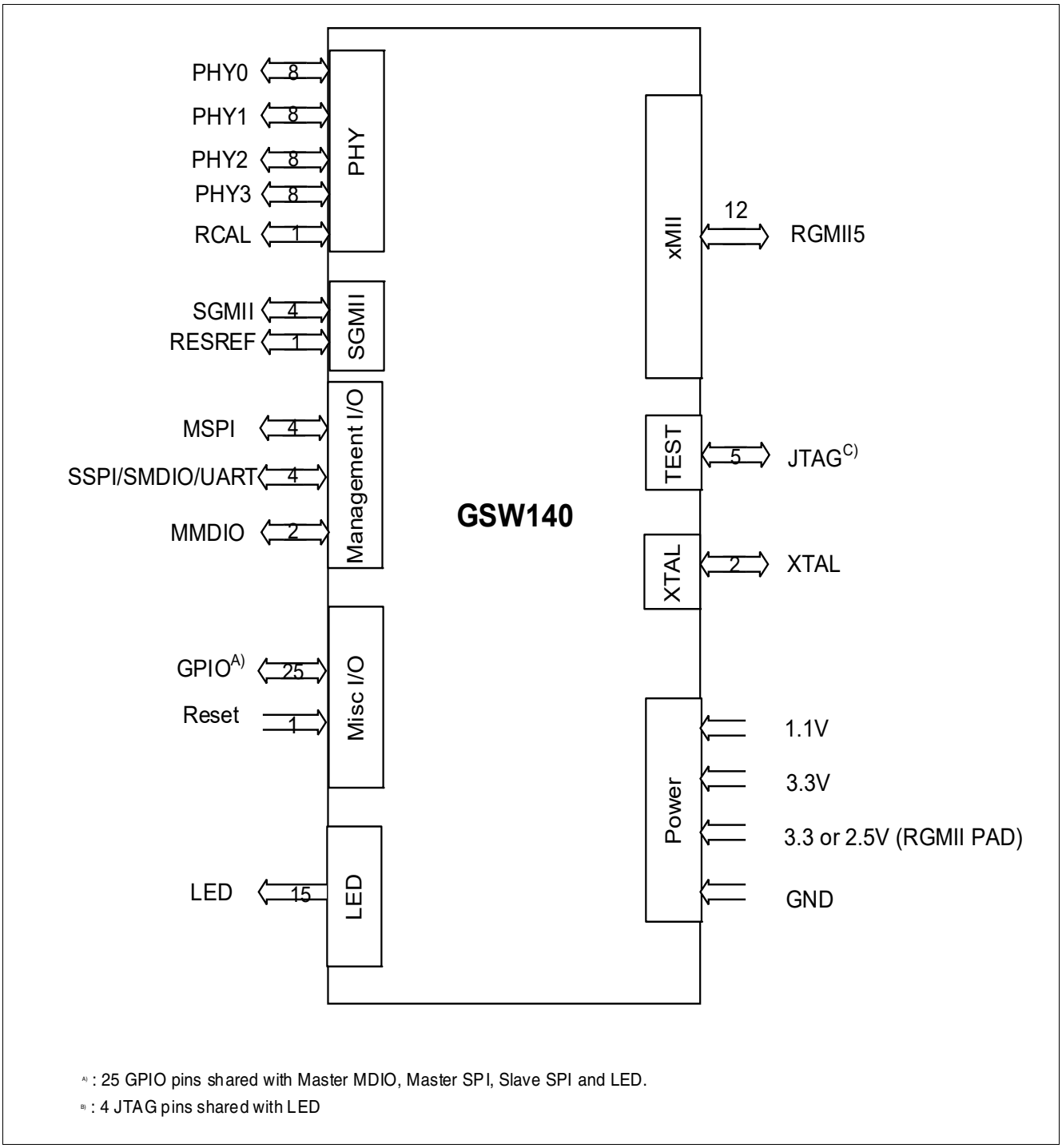


Figure 5 GSW140 Logic Symbol

2.2 External Signal Description

This section provides in detail the pin diagrams, abbreviations for pin types and buffer types, as well as the table of input and output signals.

2.2.1 Pin Diagram

Figure 6 shows the pin layout of the package.

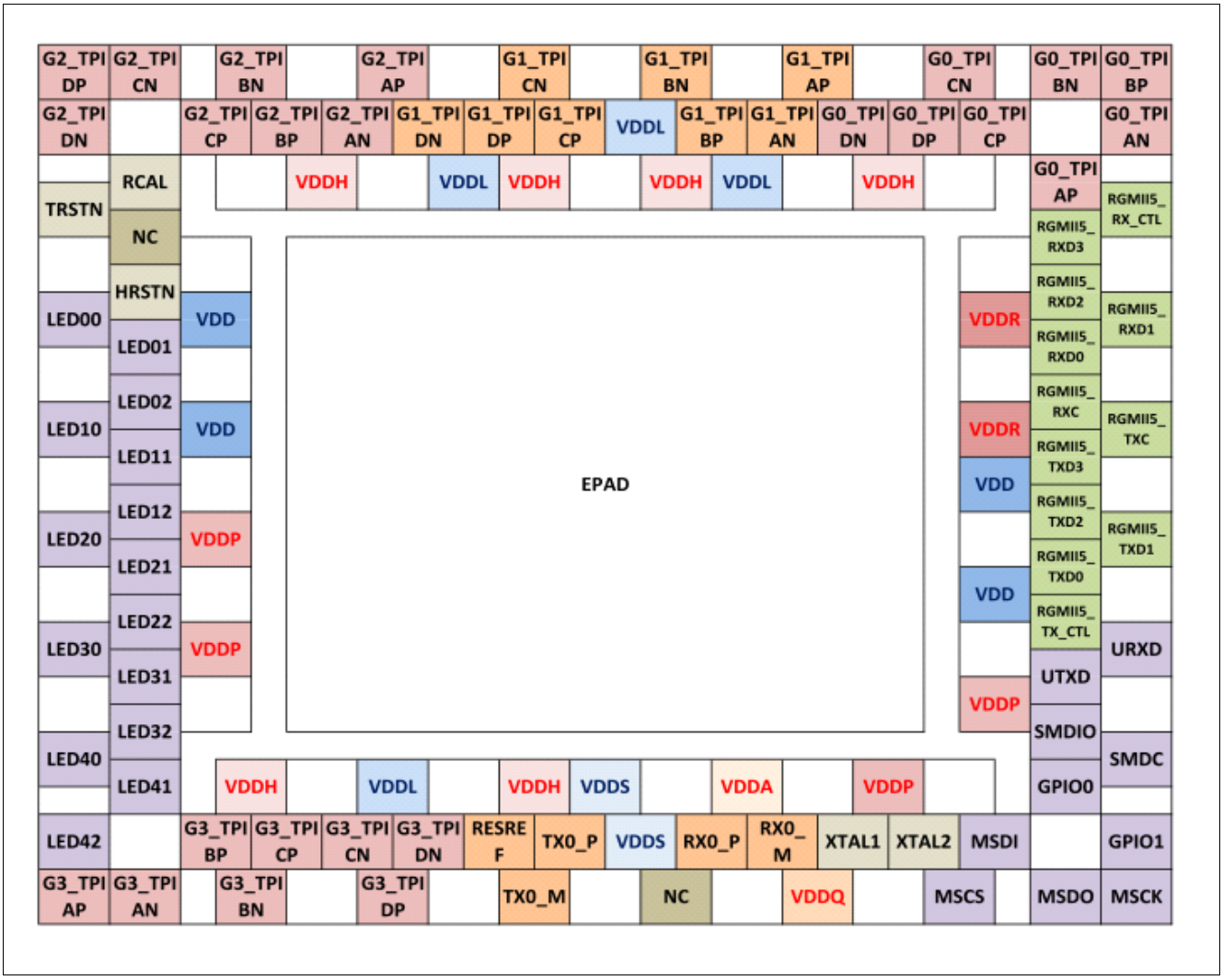


Figure 6 Pin Layout

2.2.2 Abbreviations

Table 1 and Table 2 summarize abbreviations used in the signal tables.

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Input-only, digital levels
O	Output-only, digital levels
I/O	Bidirectional input/output signal, digital levels
Prg	Bidirectional pad, programmable to operate either as input or output, digital levels
AI	Input-only, analog levels
AO	Output-only, analog levels
AI/O	Bidirectional, analog levels
PWR	Power
GND	Ground

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
LVTTL n	LVTTL characteristics, n = A, B, or C (driver strength)
LVTTL n PU m	LVTTL characteristics with weak pull-up device; n = A, B, or C (driver strength); m = A, B, or C (pull-up strength)
LVTTL n PD m	LVTTL characteristics with weak pull-down device; n = A, B, or C (driver strength); m = A, B, or C (pull-down strength)
LVTTL n OD	LVTTL characteristics with open-drain characteristic, n = A, B, or C (driver strength)
LVTTL n PP	LVTTL characteristics with push-pull characteristic, n = A, B, or C (driver strength)
I^2C	I^2C bus characteristics, open drain, see the AC/DC specification for details.
A	Analog characteristics, see the AC/DC specification for details.

2.2.3 Input/Output Signals

Table 3 to Table 8 show a detailed description of all pins.

2.2.3.1 Ethernet Media Interface

Table 3 Ethernet Media Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
Ethernet Port 0 Ethernet Media Interface				
B36	**G0_TPIAP**	AI/AO	A	**Port 0 Transmit/Receive Positive/Negative Connect directly to XFMR without any pull-down terminators, such as resistors or capacitors, required**
A39	**G0_TPIAN**	AI/AO	A	
D4	**G0_TPIBP**	AI/AO	A	
A40	**G0_TPIBN**	AI/AO	A	
B37	**G0_TPICP**	AI/AO	A	
A41	**G0_TPICN**	AI/AO	A	
B38	**G0_TPIDP**	AI/AO	A	
B39	**G0_TPIDN**	AI/AO	A	
Ethernet Port 1 Ethernet Media Interface				
A43	**G1_TPIAP**	AI/AO	A	**Port 1 Transmit/Receive Positive/Negative Connect directly to XFMR without any pull-down terminators, such as resistors or capacitors, required**
B40	**G1_TPIAN**	AI/AO	A	
B41	**G1_TPIBP**	AI/AO	A	
A45	**G1_TPIBN**	AI/AO	A	
B43	**G1_TPICP**	AI/AO	A	
A47	**G1_TPICN**	AI/AO	A	
B44	**G1_TPIDP**	AI/AO	A	
B45	**G1_TPIDN**	AI/AO	A	
Ethernet Port 2 Ethernet Media Interface				
A49	**G2_TPIAP**	AI/AO	A	**Port 2 Transmit/Receive Positive/Negative Connect directly to XFMR without any pull-down terminators, such as resistors or capacitors, required**
B46	**G2_TPIAN**	AI/AO	A	
B47	**G2_TPIBP**	AI/AO	A	
A51	**G2_TPIBN**	AI/AO	A	
B48	**G2_TPICP**	AI/AO	A	
A52	**G2_TPICN**	AI/AO	A	
D1	**G2_TPIDP**	AI/AO	A	
A1	**G2_TPIDN**	AI/AO	A	

Table 3 Ethernet Media Interface Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
Ethernet Port 3 Ethernet Media Interface				
D2	**G3_TPIAP**	AI/AO	A	**Port 3 Transmit/Receive Positive/Negative Connect directly to XFMR without any pull-down terminators, such as resistors or capacitors, required**
A14	**G3_TPIAN**	AI/AO	A	
B13	**G3_TPIBP**	AI/AO	A	
A15	**G3_TPIBN**	AI/AO	A	
B14	**G3_TPICP**	AI/AO	A	
B15	**G3_TPICN**	AI/AO	A	
A17	**G3_TPIDP**	AI/AO	A	
B16	**G3_TPIDN**	AI/AO	A	
Ethernet Port Calibration				
B1	**RCAL**	AI/AO	A	**Calibration for all GPHY Ethernet Ports**

2.2.3.2 SGMII Interface

Table 4 SGMII Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
B20	**RX0_P**	AI	HD	**Differential SGMII Data Input Pair** These are the negative and positive signals respectively of the differential input pair of the SGMII SerDes interface. The pair samples a 1.25/3.125 GT/s differential data signal. These pins must be AC-coupled. Due to the integrated CDR, no external transmission peer source-synchronous clock is required. These pins must be AC-coupled.
B21	**RX0_M**	AI	HD	
B18	**TX0_P**	AO	HD	**Differential SGMII Data Output Pair** These are the negative and positive signals respectively of the differential output pair of the SGMII SerDes interface. The pair samples a 1.25/3.125 GT/s differential data signal.
A19	**TX0_M**	AO	HD	
B17	**RESREF**	AO	A	**Pad to connect external tuning resistor**

2.2.3.3 Ethernet Media Independent Interface

Attention: The pin functionality in Table 5 highlighted in bold indicates the pin name.

Table 5 Ethernet Media Independent Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
Ethernet Port 5 Media Independent Interface				
A34	**RGMII5_TXC**	O	PD	RGMII Transmit Clock for pins RGMII5_TX*
B29	**RGMII5_TXD0**	O		RGMII Transmit Data Bit 0
A32	**RGMII5_TXD1**	O		RGMII Transmit Data Bit 1
B30	**RGMII5_TXD2**	O		RGMII Transmit Data Bit 2
B31	**RGMII5_TXD3**	O		RGMII Transmit Data Bit 3
B28	**RGMII5_TX_CTL**	O		RGMII Transmit Control
B32	**RGMII5_RXC**	I	PD	RGMII Receive Clock for pins RGMII5_RX*
B33	**RGMII5_RXD0**	I	PD	RGMII Receive Data Bit 0
A36	**RGMII5_RXD1**	I	PD	RGMII Receive Data Bit 1
B34	**RGMII5_RXD2**	I	PD	RGMII Receive Data Bit 2
B35	**RGMII5_RXD3**	I	PD	RGMII Receive Data Bit 3
A38	**RGMII5_RX_CTL**	I	PD	RGMII Receive Control

2.2.3.4 LED/UART/JTAG Interface

The LED interface is used to connect the external LEDs for Ethernet status indication of the Ethernet PHY interfaces. The single and dual color LEDs are supported. There are three LEDs per port. The JTAG interface shares the pins with the LED interface.

Attention: The pin functionality in Table 6 highlighted in bold indicates the pin name.

Table 6 LED Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
LED Signals				
A4	GPIO16	Prg	Prg	**General Purpose IO 16** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED00	O		**LED0 for Port 0** LED control output, freely configurable, drives single-color or dual color LEDs.
A6	GPIO17	Prg	Prg	**General Purpose IO 17** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED10	O		**LED0 for Port 1** LED control output, freely configurable, drives single-color or dual color LEDs.
	TDO	O		**JTAG Serial Test Data Output** JTAG test data output
A8	GPIO18	Prg	Prg	**General Purpose IO 18** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED20	O		**LED0 for Port 2** LED control output, freely configurable, drives single-color or dual color LEDs.
	TDI	I	PU	**JTAG Serial Test Data Input**
A10	GPIO19	Prg	Prg	**General Purpose IO 19** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED30	O		**LED0 for Port 3** LED control output, freely configurable, drives single-color or dual color LEDs.
	TMS	I	PU	**JTAG Test Mode Select**
A12	GPIO20	Prg	Prg	**General Purpose IO 20** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	TCK	I	PU	**JTAG Test Clock** The signals TDI, TDO and TMS are synchronous subject to this JTAG test clock. *Note: When JTAG Controller is held in reset state, i.e. Gigabit Ethernet Switch operates in normal mode, this clock pin does not have to be clocked.*

Table 6 LED Interface Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
B4	GPIO21	Prg	Prg	**General Purpose IO 21** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED01	O		**LED1 for Port 0** LED control output, freely configurable, drives single-color or dual-color LEDs.
B6	GPIO22	Prg	Prg	**General Purpose IO 22** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED11	O		**LED1 for Port 1** LED control output, freely configurable, drives single-color or dual-color LEDs.
B8	GPIO23	Prg	Prg	**General Purpose IO 23** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED21	O		**LED1 for Port 2** LED control output, freely configurable, drives single-color or dual-color LEDs.
B10	GPIO24	Prg	Prg	**General Purpose IO 24** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	LED31	O		**LED1 for Port 3** LED control output, freely configurable, drives single-color or dual-color LEDs.
B12	GPIO25	Prg	Prg	**General Purpose IO 25** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
B5	GPIO26	Prg	Prg	**General Purpose IO 26** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pin-strapping information during reset.*
	LED02	O		**LED0 for Port 0** LED control output, freely configurable, drives dual-color or single color LED.
	LIGHT	I/O		**Light Sensor Input** Light Sensor Input
B7	GPIO27	Prg	Prg	**General Purpose IO 27** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pin-strapping information during reset.*
	LED12	O		**LED0 for Port 1** LED control output, freely configurable, drives dual-color or single color LED.

Table 6 LED Interface Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
B9	GPIO28	Prg	Prg	**General Purpose IO 28** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pin-strapping information during reset.*
	LED22	O		**LED0 for Port 2** LED control output, freely configurable, drives dual-color or single color LED.
B11	GPIO29	Prg	Prg	**General Purpose IO 29** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pin-strapping information during reset.*
	LED32	O		**LED0 for Port 3** LED control output, freely configurable, drives dual-color or single color LED.
A13	GPIO30	Prg	Prg	**General Purpose IO 30** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pin-strapping information during reset.*
	LED42	I/O		**Brightness Control** This pin is used for the brightness control switch input.
A2	**TRSTN**	I	PD	**JTAG Test Reset** *Note: The integrated pull-down resistor holds the TAP controller in its reset state when the pin is left open. This is a difference to the JTAG specification given by IEEE 1149.1.*

2.2.3.5 Management Interfaces

Five types of serial management interfaces are provided: the SPI master, SPI slave, MDIO slave, MDIO master and UART interfaces.

Attention: The pin functionality in Table 7 highlighted in bold indicates the pin name.

Table 7 Management Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
MDIO Master Interface				
B25	**GPIO0**	Prg	Prg	**General Purpose IO 0** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	GPC0			**General Purpose Clock 0** General Purpose clock for Synchronous Ethernet or external devices.
	EXINT0			**External Interrupt 0** The output characteristic can be selected to be open drain or push-pull.
	MMDIO	I/O		**MDIO Master Data Input/Output** Serial data input and output according to IEEE 802.3, clause 22.
A27	**GPIO1**	Prg	Prg	**General Purpose IO 1** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	GPC1			**General Purpose Clock 1** General Purpose clock for Synchronous Ethernet or external devices.
	EXINT1			**External Interrupt 1** The output characteristic can be selected to be open drain or push-pull.
	MMDC	O		**MDIO Master Clock Output** Serial clock output according to IEEE 802.3, clause 22.
SPI Slave, MDIO Slave Interface and UART Interface				
A30	GPIO2	Prg	Prg	**General Purpose IO 2** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	SSDI	I		**SPI Slave Data Input** SPI interface data input
	URXD	I		**UART Data Input** UART interface data input
B27	GPIO3	Prg	Prg	**General Purpose IO 3** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pin-strapping information during reset.*
	SSDO	O		**SPI Slave Data Output** SPI interface data output.
	UTXD	O		**UART Data Output** UART interface data output.

Table 7 Management Interface Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
A28	GPIO4	Prg	Prg	**General Purpose IO 4** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	SSCK	I		**SPI Slave Clock** SPI interface clock.
	SMDC	I		**MDIO Slave Clock** The external controller provides the serial clock of up to 25 MHz on this input.
	LIGHT	I/O		**Light Sensor Input** Light Sensor Input.
B26	GPIO5	Prg	Prg	**General Purpose IO 5** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	SSCS	I		**SPI Slave Chip Select** SPI interface chip select.
	SMDIO	I/O		**MDIO Slave Data Input/Output** The external controller uses this signal to address internal registers and to transfer data to and from the internal registers.
	PWLED	O		**Power LED** LED for indicating power up.
SPI Master interface				
B24	GPIO6	Prg	Prg	**General Purpose IO 6** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull.
	MSDI	I		**SPI Master Data Input** SPI interface data input.
	LIGHT	I/O		**Light Sensor Input** Light Sensor Input.
A26	GPIO7	Prg	Prg	**General Purpose IO 7** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pin-strapping information during reset.*
	MSDO	O		**SPI Master Data Output** SPI interface data output
	PWLED	O		**Power LED** LED for indicating power up
D3	GPIO8	Prg	Prg	**General Purpose IO 8** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pin-strapping information during reset.*
	MSCK	O		**SPI Master Clock** SPI interface clock

Table 7 Management Interface Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
A25	GPIO9	Prg	Prg	**General Purpose IO 9** It can be selected as input or output mode. The output characteristic can be selected to be open drain or push-pull. *Note: This pin reads in pin-strapping information during reset.*
	MSCS	O		**SPI Master Chip Select** SPI interface chip select. Active low signal.

2.2.3.6 Miscellaneous Signals

Attention: The pin functionality in Table 8 highlighted in bold indicates the pin name.

Table 8 Miscellaneous Signals

Pin No.	Name	Pin Type	Buffer Type	Function
Reset and Clocking				
B22	**XTAL1**	AI	A	**Crystal: Oscillator Input** A crystal must be connected between XTAL1 and XTAL2. Additional Load Capacitances must tie both pins to the GND.
	CLK	I		**Clock: Clock Input** Direct clock input.
B23	**XTAL2**	AO	A	**Crystal: Oscillator Output** A crystal must be connected between XTAL1 and XTAL2. Additional Load Capacitances must tie both pins to the GND.
B3	**HRSTN**	I	PU	**Hardware Reset** Asynchronous active low device reset
A21, B2	**NC**	-	-	**Not Connected** Must be connected to ground

2.2.3.7 Power Supply

This section specifies the power supply pins.

Table 9 Power Supply Pins

Pin No.	Name	Pin Type	Buffer Type	Function
C10, C14, C31, C34, C36, C39	**VDDH**	PWR		**High-Voltage Domain Supply** This is the group of supply pins for the high voltage domain. It supplies the Line-Driver in the PMA of the Gigabit Ethernet Switch. This supply must provide a nominal voltage of V_{DDH}=*3.3 V* with a worst case tolerance ±5% at the corners, respectively.
C6, C8, C19, C21	**VDDP**	PWR		**Pad-Voltage Domain P Supply** This is the group of supply pins for the pad-supply of the Gigabit Ethernet Switch (excluding RGMII). This supply must provide a nominal voltage of V_{DDP}=*3.3 V* with a worst case tolerance ±5% at the corners, respectively.
C26, C28	**VDDR**	PWR		**Pad Voltage Domain R Supply** This is the group of supply pins for the RGMII pad-supply of the Gigabit Ethernet Switch. This supply must provide a nominal voltage of V_{DDR}=*3.3 V* or *2.5 V* with a worst case tolerance ±5% at the corners, respectively.
B42, C12, C33, C37	**VDDL**	PWR		**Low-Voltage Domain Supply** This is the group of supply pins for the low voltage domain. It supplies mixed signal blocks in the PMA of the Gigabit Ethernet Switch. This supply must provide a nominal voltage of V_{DDL}=*1.1 V* with a worst case tolerance ±5%.
C17	**VDDA**	PWR		**XO Pad-Voltage Domain P Supply** This is the group of supply pins for the pad-supply of the ROPLL and XO. This supply must provide a nominal voltage of V_{DDSP}=*3.3 V* with a worst case tolerance ±5% at the corners, respectively.
C15, B19	**VDDS**	PWR		**SGMII Low-Voltage Domain Supply** This is the group of supply pins for the low voltage domain of the SGMII interface. It supplies mixed signal blocks in the PMA of the SGMII interface. This supply must provide a nominal voltage of V_{DDSL}=*1.1 V* with a worst case tolerance ±5%.
A23	**VDDQ**	PWR		**Fusing Domain Supply** This is the group of supply pins for the fusing logic. This supply must provide a nominal voltage of V_{DDQ}=*2.5 V* with a worst case tolerance ±5%. When fusing is not enabled, this pin can be left floating or tied to ground.
C2, C4, C23, C25	**VDD**	PWR		**Core-Voltage Domain Supply** This is the group of supply pins for the core voltage domain. It supplies the digital core blocks of the Gigabit Ethernet Switch. This supply must provide a nominal voltage of V_{DDC}=*1.1 V* with a worst case tolerance ±5%.
EPAD[1)]	**VSS**	GND		**General Device Ground**

1) The EPAD is the exposed pad at the bottom of the package. This pad must be properly connected to the ground plane of the PCB.

3 Functional Description

This chapter includes the functional description.

3.1 Clock and Reset

This section describes the clock and reset.

3.1.1 Clock Generation Unit

A single clock source connects to the system, the internal clock circuit generates all required clocks through the internal PLL circuits. The clock source must be 25 MHz or 40 MHz, selected via pin strapping of pin UTXD.

3.1.2 General Purpose Clock Output

There are two general purpose clocks supported. General purpose clock share the pins with other functions.

The general purpose clock output has frequency of 125/N MHz, where N is configurable via register **SYSCLK_CONF** field **CLK250_DIV**.

3.1.3 Reset Generation Unit

There are the following reset sources that can bring chip or partial of chip into reset:

- Hardware Reset Input
- Global Software Reset
- Module Software Reset

Hardware input resets all hardware modules and loads pin-strapping information into the register. Hardware input reset is the most thorough reset among the reset choices. Driving HRSTN pin low causes an asynchronous reset of the entire device. HRST pin high deasserts the reset. The configuration input pin(s) are sampled and latched at the rising edge of HRSTN signal. Hardware reset resets all logics in digital and analog domains.

Global software reset (SRST) is issued by the external controller or by boot loader to reset the whole chip. A global software reset does not latch boot strapping information again. The following registers are not affected by global software reset.

- All clock generation configuration registers
- Pin-strapping registers

Individual module software Reset is another type of reset. When the software detects a condition which requires the individual module to be reset, a software reset can be performed by writing to a special register, the Reset Request register. Write ‘1’ to **RST_REQ** register to assert software reset and write ‘0’ to **RST_REQ** register to de-assert software reset. The duration of reset is controlled by the software. There is an additional self-clearing reset for 1st GPHY Macro (GHY0 Macro).

3.1.4 Power Up Sequence

VDDP/VDDH/VDDA must be up before VDDL/VDDS/VDD.

3.2 Management Interface Functional Description

This section includes the Management Interface functional description.

3.2.1 Management Interface Subsystem Features

The Management Interface Subsystem supports the following features:

- Four concurrent types of management interface:
  - MDIO slave interface or SPI slave interface (share pins with GPIO)
  - UART interface or SPI slave interface (share pins with GPIO)
  - SPI master interface (share pins with GPIO)
  - MDIO master interface (share pins with GPIO)
- MDIO master interface to control PHY devices
  - Support auto polling of internal and external PHY devices registers
  - Support indirect access by command to internal and external PHY devices registers
  - Support programmable MDC clock up to 17 MHz
- SPI master interface connecting to a serial EEPROM
  - Support clock up to 42 MHz
  - Supports automatic switch configuration from external EEPROM memory
  - Support write access to EEPROM by an external controller
  - Supports different EEPROM sizes from 1 Kbit to 1024 Kbit
- SPI slave interface to allow control by an external master (such as router or microcontroller)
  - Maximum SPI interface clock 50 MHz and Minimum SPI interface clock is 2.5 MHz
- MDIO slave to allow control by an external master (such as router or microcontroller)
  - Maximum MDIO interface clock 25 MHz
- UART interface connecting to serial terminal
  - Support various baud rate: 4800, 9600, 19200, 38400, 57600, 115200 (default), 230400, 460800, 921600
  - Supports 8-bit data frame, LSB first
  - Support even parity and no parity mode
  - Support 1 or 2 stop bits
  - Support single read access and single write access via serial terminal
  - Support access abort via special characters

3.2.2 MDIO Master Module

The Management Data Input/Output (MDIO) master module provides the register interface to access external or internal PHY registers. The access is triggered by an internal bus master access or by an automatic PHY status polling function. See **Figure 8** for details.

This interface is used to configure the internal and external PHYs and to read status information (speed, duplex, pause, EEE capability). Access to the MDIO master registers automatically starts a serial access to the internal or external component that is addressed by the PHY address given with the command.

The interface uses the serial protocol defined by IEEE 802.3, clause 22. Up to 32 external devices can be addressed through a 5-bit PHY address (PHYADR). Each of these devices can have up to 32 16-bit registers, selected by a 5-bit register address (REGADR). PHY and register address are given in the command word. Each data transfer covers a 16-bit data word.

High Speed Operation

The MDIO master interface configuration is through **MMDC_CFG_1**. The standard MDIO protocol uses a clock rate of 3.4 MHz on MDC, which is also the default setting. To speed up the data exchange, the clock generated on MDC can be increased (when the connected PHY supports this). See the **AC Characteristics** for details.

MDIO Master Interface Address Assignment

The MDIO address for PHY can be configured through **PHY_ADDR_0**/1/2/3/4/5.

Table 10 Default Master MDIO Address Assignment

	Default Address	Configuration Register
Port 0 Internal PHY	0	**PHY_ADDR_0**
Port 1 Internal PHY	1	**PHY_ADDR_1**
Port 2 Internal PHY	2	**PHY_ADDR_2**
Port 3 Internal PHY	3	**PHY_ADDR_3**
Port 4 External PHY	4	**PHY_ADDR_4**
Port 5 External PHY	5	**PHY_ADDR_5**

Automatic Polling State Machine

An automatic polling state machine is implemented to dynamically read the internal and external PHY registers which reflect the status of the link, the link speed, duplex mode, pause capabilities and 802.3az EEE capabilities. When the automatic polling state machine is enabled on a port (through **MMDC_CFG_0**), the PHY status is read out and corresponding MAC module is configured accordingly.

When MDIO Master interface is accessed by the management action (using the dedicated indirect MDIO register access) it has the higher priority over the auto-polling state machine.

When the MDIO auto-polling state machine is disabled, the link speed, link duplex mode, link status, the pause settings and 802.3az EEE settings hold the previous polled values and can also be configured by the explicit management action.

Figure 7 shows the port loop of the auto-polling FSM. The auto-polling FSM goes sequentially over all ports enabled for auto-polling and applies the auto-polling main loop. The gap between each auto polling main loop is programmable via register **MMDC_CFG_0** field **GAP**. Ports disabled for auto-polling are skipped. The polling sequence is repeated constantly in an infinite loop.

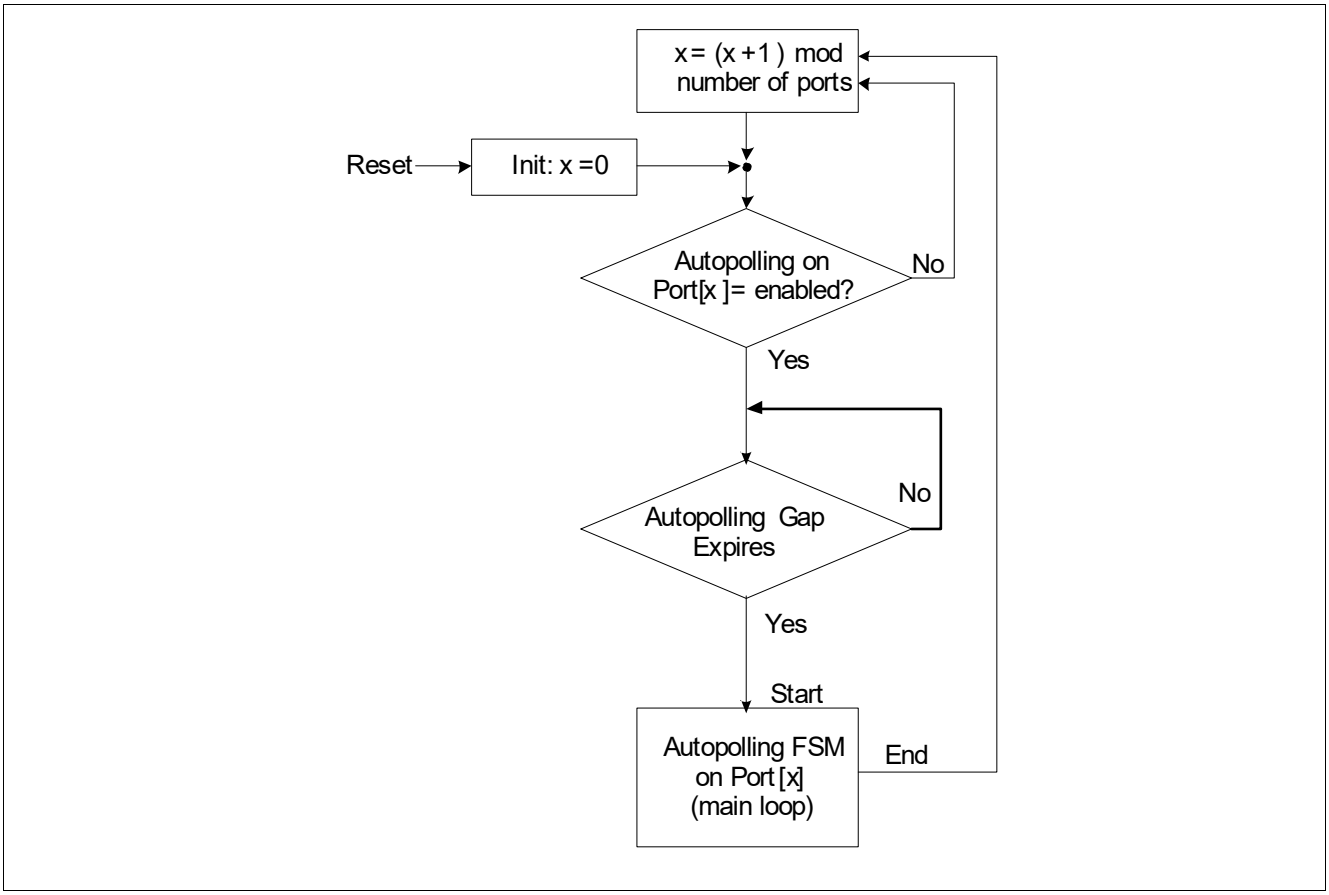


Figure 7 Auto-polling FSM - Port Loop

Figure 8 describes the main loop of the auto-polling state machine. The state machine reads the PHYs registers in the following sequence:

1. Read REG0 and check when the PHY is connected. When the value of the register is all ones, no PHY is assumed to be connected and PHY Inactive status is reported.
2. PHY support of the auto-negotiation (ANEG) is checked in Bit 12 of the REG0. When the PHY does not support ANEG, duplex and speed are based on REG0 settings. Link is based on the bit 2 of REG1. Pause capability is set to the maximum (support symmetric and asymmetric pause).
3. Bit 5 of the REG1 is checked for ANEG status. When ANEG is not complete - current FSM cycle for this port breaks and the Link Status reported as zero. Status of this port is checked again in the next round.
4. When ANEG is complete, the FSM branches based on the bit 8 in REG1. In case there is no extended status supported, the attached PHY is a FE PHY. In case extended status is supported (REG1.8=1_B) the PHY is GE PHY.
5. For FE PHY, REG5 (partner) and REG4 (local) are fetched for the speed/duplex/pause auto-negotiation result.
6. For GE PHY REG10 (partner) and REG9 (local) are fetched in addition to the FE abilities. REG15 bit 12 to 15 are checked for the 1000BASE-X or 1000BASE-T capability.
7. When bit 1 in REG6 for GE PHY does not indicate reception of the next page, the PHY considered to perform parallel detection and speed/duplex/pause is based on the REG4 and REG5 as in the FE PHY case.
8. EEE capability and advertising registers are fetched.
9. Auto resolution function is applied in the end, based on the fetched result and appropriate status info is reported to the MAC module.

Note: When automatic polling is enabled, PHY status registers are regularly read. This causes the latching status bits to be reset. When the software must read out the latched status information, the automatic polling must be disabled.

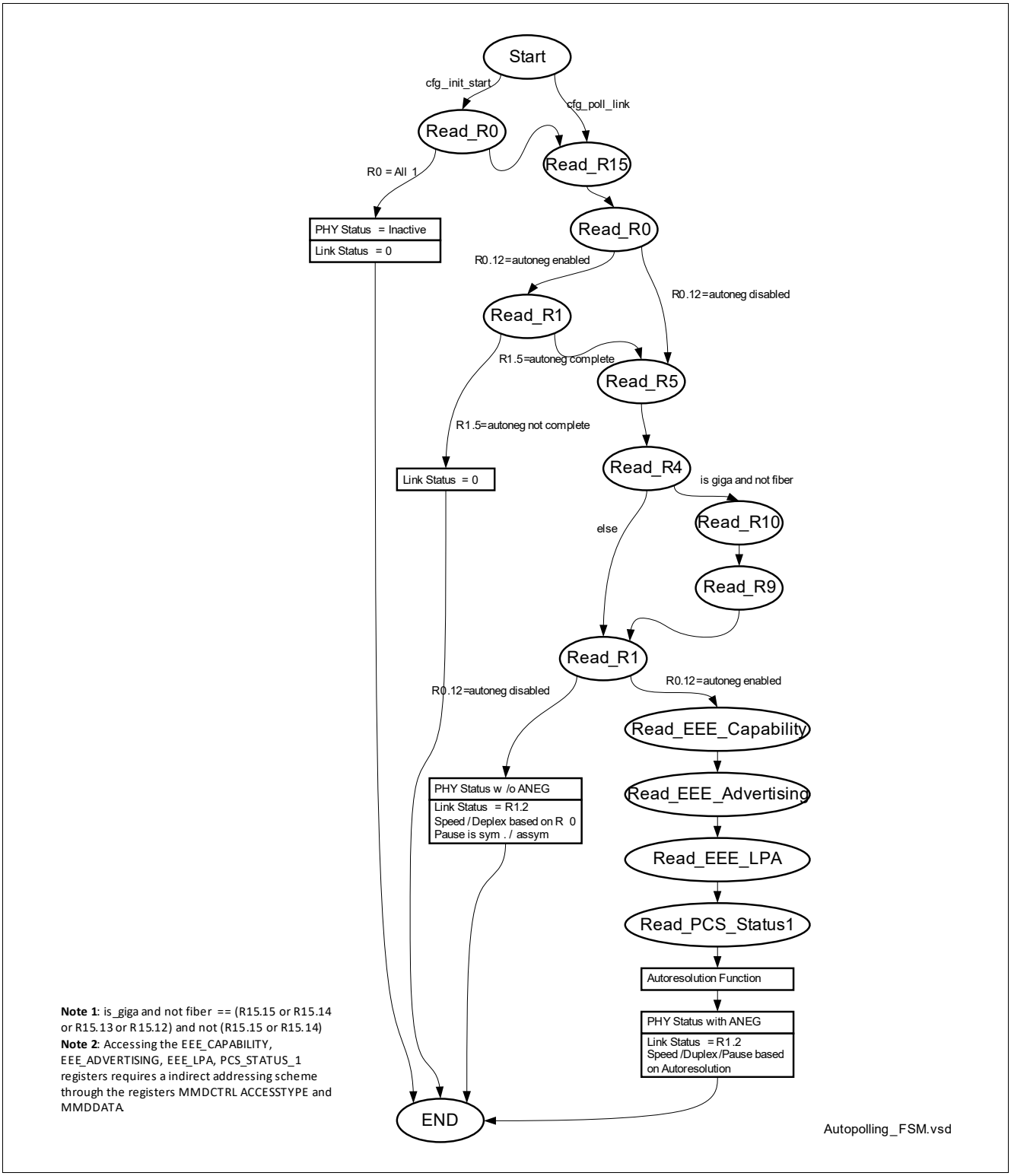


Figure 8 Auto Polling FSM - Main Loop

MDIO Master Indirect Access

When MDIO Master interface is accessed by the management action (using the dedicated indirect MDIO register access through **MMDIO_CTRL**, **MMDIO_READ** and **MMDIO_WRITE**). It has the higher priority over the auto-polling state machine.

Only single access is supported.

Single Read Access:

Reading data from a PHY register through indirect access is performed in following steps:

The first step can be skipped for the following consecutive access.

1. Read status **MMDIO_CTRL**.
2. When **MMDIO_CTRL.MBUSY** is 0_B, write “operation mode”, “target PHY address” and “target register address” to **MMDIO_CTRL**.
   a) **OP** = 10_B (read)
   b) **PHYAD** = Target PHY Address
   c) **REGAD** = Target Register Address
3. Read status **MMDIO_CTRL**.
4. When **MMDIO_CTRL.MBUSY** is 0_B, read data from **MMDIO_READ**.
   a) **RDATA**= [result from target register]

Single Write Access:

Writing data to a PHY register through indirect access is performed in following steps:

1. Read status **MMDIO_CTRL**.
2. When **MMDIO_CTRL.MBUSY** is 0_B, write the target data to **MMDIO_WRITE**.
   a) **WDATA** = [data to be written]
3. Write “operation mode”, “target PHY address” and “target register address” to **MMDIO_CTRL**.
   a) **OP** = 01_B (write)
   b) **PHYAD** = Target PHY Address
   c) **REGAD** = Target Register Address

3.2.3 MDIO Slave Module

An external controller can be connected to the switch’s slave MDIO interface. **Figure 9** shows the chip behaves as MDIO slave similar to an PHY. Via indirect addressing the external controller is able to access all internal registers. MDIO Slave module is a master of internal bus. Read and write requests of MDIO slave are translated to read and write requests to internal bus.

For the access to the external or internal PHYs, the chip serves as a proxy for the external controller. The external controller must write the PHY address, the PHY register address, the command (read/write) and the corresponding data into internal registers. Based on the information which has been written, the information is translated into an MDIO frame and sent via the MDIO master interface to the destination PHY.

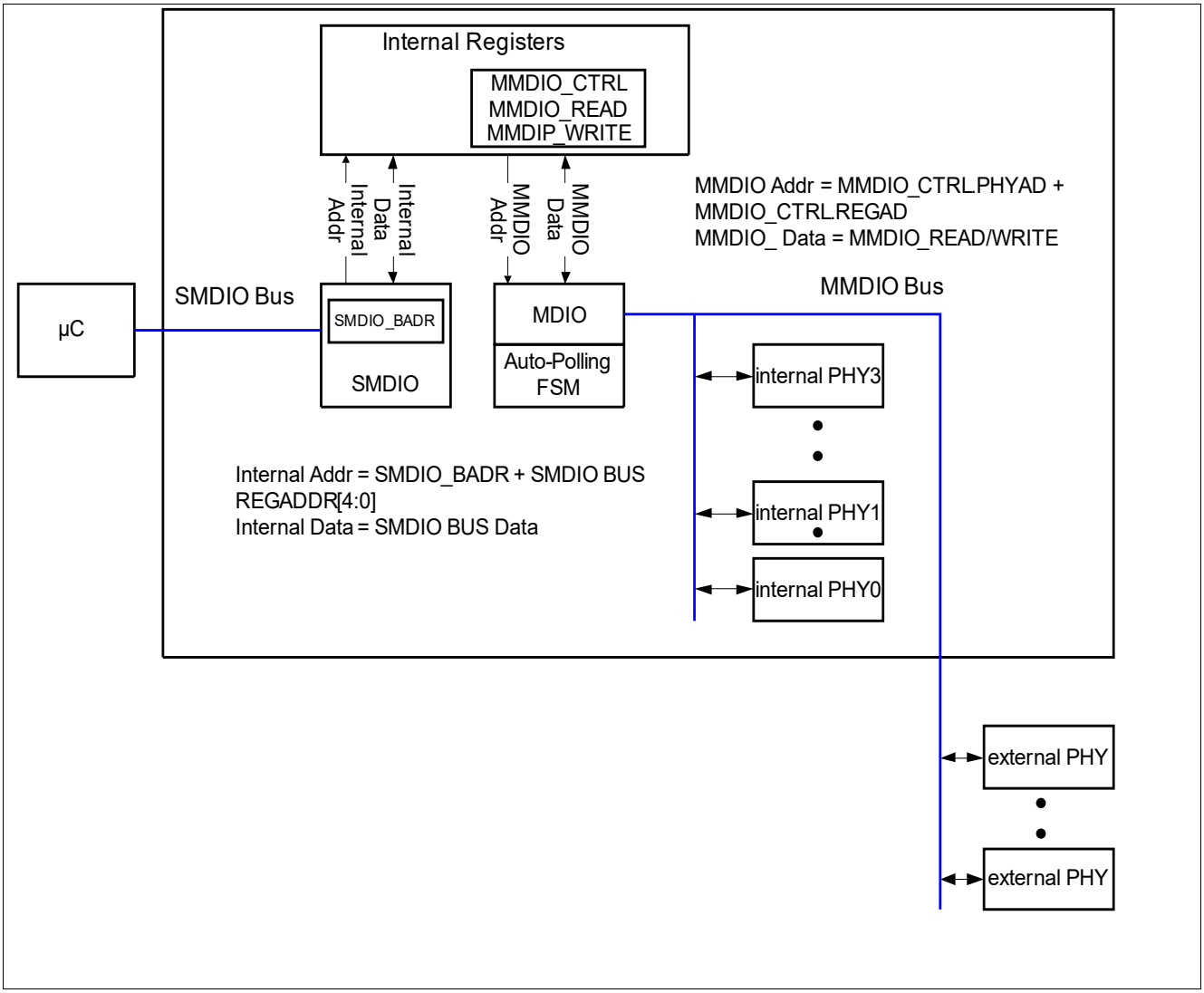


Figure 9 MDIO Proxy in Switching Mode

When other devices in the system must be configured through MDIO, they must either be connected to the MDIO master interface or, when connected to the MDIO slave interface, must be configured so that no addressing conflict arises.

The interface can uses the standard MDIO protocol which provides vendor-specific registers in the upper 5-bit REGADR range. Within this range there are certain registers which allow an indirect access to multiple internal configuration and status registers.

The standard MDIO protocol requires a 32-bit preamble at the beginning of each read or write access. To speed up the data exchange, the preamble can be reduced down to 1 bit for the second and following subsequent accesses.

The standard MDIO protocol uses a clock rate of 2.5 MHz on MDC. To speed up the data exchange, the clock applied on SMDC can be increased to maximum 25 MHz. See the **AC Characteristics** for details.

The bus protocol used for the MDIO slave interface is the same as defined for MDIO master interface. **Table 10** shows the PHY address (PHYADR) range usage. The internal registers are read or written in single or sequential access mode. In sequential access mode, multiple accesses are possible to registers located at subsequent internal addresses.

The SMDIO address used for indirect access is configurable through pin strapping. The SMDIO address are reconfigured via **SMDIO_CFG.ADDR**.

After hardware reset, MDIO slave interface is enabled. MDIO slave interface is multiplexed with SPI slave interface. MDIO and SPI slave cannot be enabled at the same time. When both are enabled, MDIO slave interface is used. When both interfaces are disabled and all the 4 pins used for MDIO slave and SPI slave are input only.

Single Read Access

Reading data from an internal register through indirect access is performed in following steps:

The first step can be skipped for consecutive access.

1. Write Base Address Register **SMDIO_BADR**.
   a) OPCODE[1:0] = 01_B (write)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 11111_B (Address of Target Base Address Register)
   d) DATA[15:0] = [Value of Target Base Address]
2. Read Target Data.
   a) OPCODE[1:0] = 10_B (read)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 00000 - 11110_B (Target Offset Address)
   d) DATA[15:0] = [Read Data from Target]

Multiple Read Access

Reading data from an internal register through indirect access can also access the same register multiple times or the consecutive register within a range. This can be used, for example, to read from a FIFO-style memory through a single register address or to poll a register for a certain value. The sequence is as follows:

1. Write Base Address Register **SMDIO_BADR**.
   a) OPCODE[1:0] = 01_B (write)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 11111_B (Address of Target Base Address Register)
   d) DATA[15:0] = [Value of Target Base Address]
2. Read Target Data.
   a) OPCODE[1:0] = 10_B (read)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 00000 - 11110_B (Target Offset Address)
   d) DATA[15:0] = [Read Data from Target]
3. Repeat Step 2 when the target register address is within offset 0 to 30 from the target base address.

Single Write Access

Writing data to an internal register through indirect access is performed in following steps:

1. Write Base Address Register **SMDIO_BADR**.
   a) OPCODE[1:0] = 01_B (write)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 11111_B (Address of Target Base Address Register)
   d) DATA[15:0] = [Value of Target Base Address]
2. Write Target Data.
   a) OPCODE[1:0] = 01_B (write)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 00000 - 11110_B (Target Offset Address)
   d) DATA[15:0] = [Write data To Target]

Multiple Write Access

Writing data to an internal register through indirect access can also access the same register multiple times or the consecutive register within a range. This can be used, for example, to write a FIFO-style memory through a single register address or to write a register for a certain value. The sequence is as follows:

1. Write Base Address Register.
   a) OPCODE[1:0] = 01_B (write)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 11111_B (Address of Target Base Address Register)
   d) DATA[15:0] = [Value of Target Base Address]
2. Write Target Data.
   a) OPCODE[1:0] = 01_B (read)
   b) PHYADR[4:0] = SMDIO Address
   c) REGADR[4:0] = 00000 - 11110_B (Target Offset Address)
   d) DATA[15:0] = [Write Data to Target]
3. Repeat Step 2 when the target register address is within offset 0 to 30 from the target base address.

3.2.4 SPI Master Module

It supports the following functions:

- Configuration download from an external serial EEPROM after hardware or global software reset is triggered.
- Configuration upload to an external serial EEPROM during run time after initialization is done.

Operation

External or internal controller can control SPI master interface via SPI access registers. Operation relies on regular interrupt asserted at the boundary of 8-bit transactions. SPI interrupt indicates that data out buffer is ready to be written and data in carries the valid data and is ready for reading.

Operation Configuration:

- First set **MSPI_OP.MDSEL** to 1_B.
- Wait until **MSPI_OP.MDSTA** = 1_B.
- Do single or multiple manual access.

Single Read Access Operation:

- Write address to **MSPI_DIN01**/**MSPI_DIN23**.
- Configure **MSPI_MANCTRL.SIZE** = number of bytes and **MSPI_MANCTRL.START** to 1_B.
- Wait for SPI interrupt **MSPI_ISR.DONE** = 1_B.
- Write 1_B to **MSPI_ISR.DONE** to clear interrupt.
- Read **MSPI_DOUT01**/**MSPI_DOUT23**/**MSPI_DOUT45**/**MSPI_DOUT67**.

Single Write Access Operation:

- Configure **MSPI_DIN01**/**MSPI_DIN23**/**MSPI_DIN45**/**MSPI_DIN67**.
- Configure **MSPI_MANCTRL.SIZE** = number of bytes and **MSPI_MANCTRL.START** to 1_B.
- Wait for SPI interrupt **MSPI_ISR.DONE** = 1_B.
- Write 1_B to **MSPI_ISR.DONE** to clear interrupt.

3.2.5 SPI Slave Access

The Gigabit Ethernet Switch may work as an SPI slave. An external controller manages the Gigabit Ethernet Switch via SPI slave interface.

The SPI Slave module is a master of internal bus. Read and write requests of SPI are translated to read and write requests to internal bus.

The SPI Slave follows the 16-bit/24-bit serial EEPROM-like protocols (for WRITE/READ respectively). **Figure 10** shows the timing diagrams.

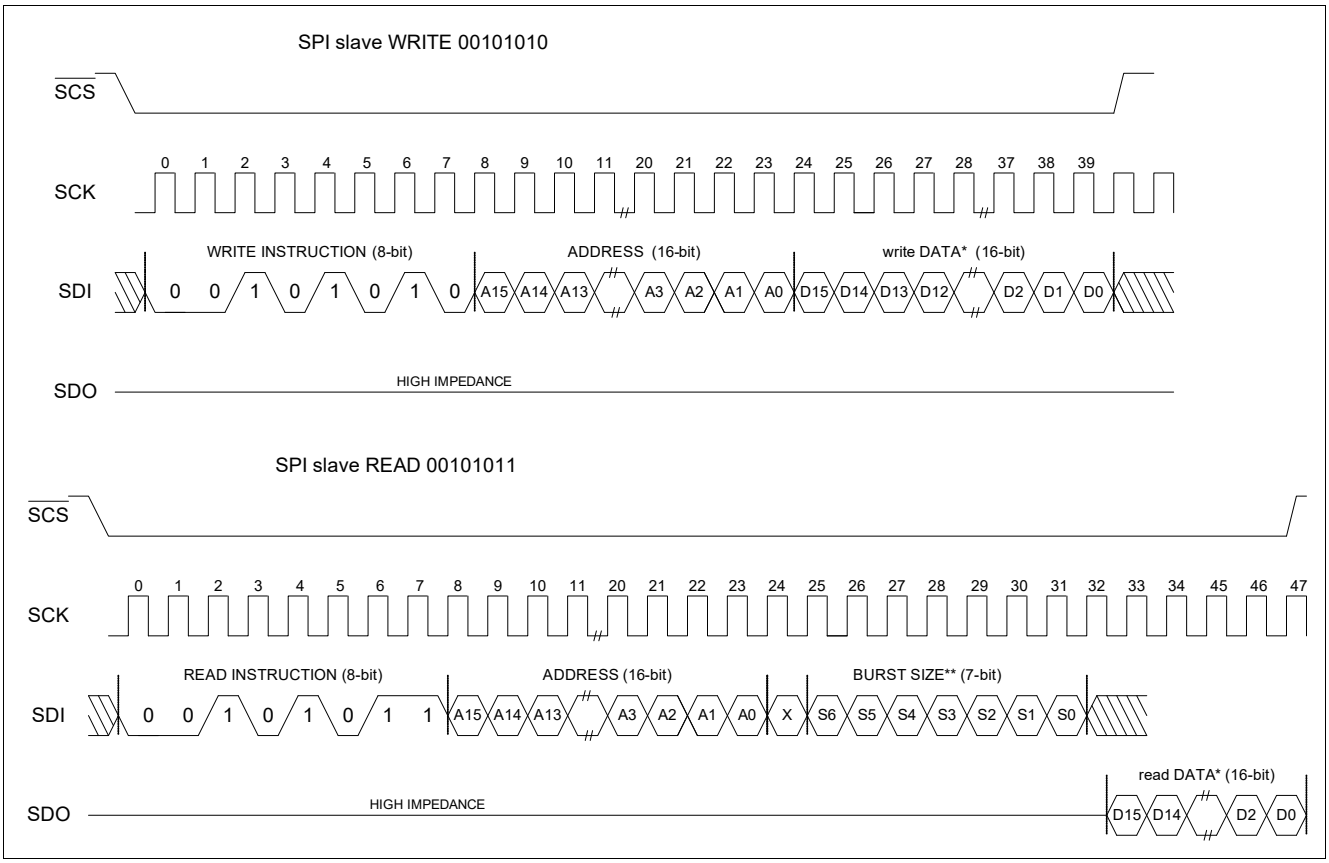


Figure 10 SPI Slave Access

The maximal SCK frequency of 50 MHz and the minimum SCK frequency of 2.5 MHz is supported.

Two major synchronization techniques are used:

- In SDI direction, special preamble like "001010" is used to adjust sampling edge to middle of the stable region. Preamble is part of READ or WRITE command.
- In SDO direction, delay is adjustable in steps of 4ns from rising or falling edge of SCK.
  - delay is (3+ **SSPI_CFG.DRVDLY**)*4ns when **SSPI_CFG.DRVDLY** /= 0
  - delay is 4*4ns when **SSPI_CFG.DRVDLY** = 0
- SDO can also be driven up to 2 SCK cycles earlier than the sequence defined in **Figure 10**.
  - When **SSPI_CFG.REFCYC** = 0, SDO is driven 2 SCK cycles earlier than the sequence defined in **Figure 10**.
  - When **SSPI_CFG.REFCYC** = 1, SDO is driven 1 SCK cycles earlier than the sequence defined in **Figure 10**.
  - When **SSPI_CFG.REFCYC** = 2, SDO is driven as the sequence defined in **Figure 10**.
  - When **SSPI_CFG.REFCYC** = 3, SDO is driven 1 SCK cycles after than the sequence defined in **Figure 10**.
- When **SSPI_CFG.SDIEGSEL** is set to 0, SDI is latched with the rising edge of SCK (for example in case when the master is driving SDI with the falling edge of SCK).
- When **SSPI_CFG.SDIEGSEL** is set to 1, SDI is latched with the falling edge of SCK (for example in case when the master is driving SDI with the rising edge of SCK).

3.2.6 UART Access

UART supports connection to internal bus of chip via a standard com terminal emulator running on UNIX or Windows. UART module is a master of internal bus. Read and write requests of UART are translated to read and write requests to internal bus. Three commands supported are:

```
> r address16
> w address16 write_data16
> m address16 write_data16 enable_data16
```

The UART module echoes the commands as is, ignoring any character that does not match the command format. The return value of r address16 command includes read_data16 on a new line.

The format of address16, write_data16 and enable_data16 are four consecutive hexadecimal digits between 0000_H and $FFFF_H$ or $FFFF_H$. The returned read_data16 is same format in lower case.

After chip reset, UART is in line monitoring state, searching line for valid byte. This must be preceded by at least 12 consecutive ones, (IDLE). When first error-free byte is detected, UART module responds by sending a system message:

System ready! Use:r/w <addr> <data>

followed by prompt sequence:

‘\r\n’ and ‘>’

where the ‘\r’ ASCII(13) can be disabled by setting **UART_CFG.CRDIS**=1 and the ‘\n’ ASCII(10) can be disabled by setting **UART_CFG.LFDIS**=1 to adjust new line sequence to different platforms (UNIX, MAC, Windows)

The default prompt character ‘>’ can be changed by **UART_PROMPT.Promt0** and **UART_PROMPT.Promt1**. Up to two prompt characters are supported. Setting the character to zero disables this character.

In addition to 3 commands, the character ‘#’ can be used as a first character of the line and the rest of the line is ignored. The character ‘#’ and following characters are not echoed. In line comment, following the valid command, is ignored as invalid character sequence and no other special handling is required.

When using UART from terminal, the basic editing facilities are provided using ‘\b’ ‘backspace’ character, ASCII(8). ‘b’ erases a single character on the current line that is echoed. Ignored characters cannot be erased. Multiple ‘b’ characters can erase the line up to the prompt. Prompt is not erased.

Any command can be aborted by DEL ASCII(127) or ESC(27) characters. The indication of abort of a command is done by ‘$’ character. Abort of empty line is not indicated by ‘$’ character.

The following baud rates are supported: 4800, 9600, 19200, 38400, 57600, 115200 (default), 230400, 460800, 921600. The baud rate is programmed via **UART_BD** and **UART_FDIV**. **UART_BD** is the whole part of divider and **UART_FDIV** is the fractional part of the divider.

Only 8-bit data format is supported. Parity can be enabled or disabled (default) via **UART_CFG.PAREN**. Even parity is supported. In receive direction any number of stop bits is supported. In transmit direction, the number of stop bits is configured via **UART_CFG.STOP**.

3.2.7 Boot Loader Description

The device supports the following boot modes:

- Wait for external master (via SPI Slave, MDIO slave or UART) configuration and trigger
- Self-start mode (External EEPROM not attached)
- SPI master EEPROM mode (External EEPROM attached)

The boot mode is determined by pin strapping. See **Pin Strapping** for details.

Wait For External Master Procedure (PS_NOWAIT = 0_B)

When pin strapping indicates that boot mode is “wait for external master”, boot loader only configures slave interface according to pin strapping. External master must configure and enable Gigabit Ethernet Switch core operation.

Self-start Mode Procedure (PS_NOWAIT = 1_B)

When pin strapping indicates that boot mode is not “wait for external master” and no EEPROM is attached, boot loader configures the registers according to the pin-strapping values shown in **Table 11** and **Table 12**.

Table 11 shows the registers configuration for self-start mode: standalone unmanaged switch sub-mode when PS_OP_MD = 01_B.

Table 11 Registers Configuration for Self-start Mode: Standalone Unmanaged Switch Sub-Mode

Register	Field	Description	Note
GPHY0_GPS	Bit 1 to 0	= PS_SUBTYPE_MD[4:3]	LED Display Mode
GPHY1_GPS	Bit 1 to 0	= PS_SUBTYPE_MD[4:3]	LED Display Mode
GPHY2_GPS	Bit 1 to 0	= PS_SUBTYPE_MD[4:3]	LED Display Mode
GPHY3_GPS	Bit 1 to 0	= PS_SUBTYPE_MD[4:3]	LED Display Mode
GPIO_ALTSEL0	Bit 5 to 4	$=11_B$	Enable PWLED alternate function on GPIO7 Enable Light alternate function on GPIO6
GPIO_ALTSEL1	Bit 5 to 4	$=11_B$	Enable PWLED alternate function on GPIO7 Enable Light alternate function on GPIO6
GPIO_PUDEN	Bit 5 to 4	$=00_B$	Disable PWLED and LIGHT pin pull up and pull down
GPIO_OUT	Bit 5	$= 1_B$	Turn on Power LED
GPIO_DRIVE0_CFG	Bit 5	$= 1_B$	Change PWLED drive strength to 12 mA
GPIO2_ALTSEL0	All field	Depends on LED mode of pin strapping	Configured according to **Table 13**
GPIO2_PUDEN	All field	Depends in LED mode of pin strapping	Configured according to **Table 13**
GPIO2_DRIVE1_CFG	All field	Depends in LED mode of pin strapping	Configured according to **Table 13**
MII_CFG_5	Bit 14:13	When PS_SUBTYPE_MD[0] is 1_B: $=10_B$	Enable RGMII5 interface according to pin strap
PHY_ADDR_5	All fields	When PS_SUBTYPE_MD[2] is 1_B and PS_SUBTYPE_MD[0] is 1_B: $= 32A5_H$	For RGMII5 interface, force link on, speed is 1 Gbps, full duplex, pause enable according to pin strap.

Table 11 Registers Configuration for Self-start Mode: Standalone Unmanaged Switch Sub-Mode

Register	Field	Description	Note
GSWIP PCE_PCTRL_2 for Port 3	All Field	$=0001_H$	Enable higher priority for port 3
GSWIP PCE_PCTRL_2 for Port 4	All Field	$=0001_H$	Enable higher priority for port 4
BM_WRED_GTH_0	All Fields	$=0100_H$	Global watermark is 256 segments. Remaining 256 segments are for buffer reservation
BM_WRED_GTH_1	All Fields	$=0100_H$	Global watermark is 256 segments. Remaining 256 segments are for buffer reservation
PCE_PMAP_2	All Fields	$=006F_H$	Only port 4 is disabled
PCE_PMAP_3	All Fields	$=006F_H$	Only port 4 is disabled
MAC_CTRL_4 (for each port)	All Fields	$=1494_H$	Enable EEE LPI Mode for each port
SDMA_PFCTHR8 (for each port)	All Fields	$=0018_H$	Configure backpressure watermark for each port
SDMA_PFCTHR9 (for each port)	All Fields	$=001E_H$	Configure backpressure watermark for each port
SDMA_FCTHR1	All Fields	$=03FF_H$	Configure tail drop watermark
SDMA_FCTHR2	All Fields	$=03FF_H$	Configure tail drop watermark
SDMA_FCTHR3	All Fields	$=03FF_H$	Configure tail drop watermark
SDMA_FCTHR4	All Fields	$=03FF_H$	Configure tail drop watermark
Buffer Reservation for each queue	All Fields	$=001E_H$	Buffer Reservation for each queue is 30 segments
WRED green min/max for each queue	All Fields	$=03FF_H$	Configure WRED green min/max for each queue
Queue weight for each queue	All Fields	$=FFFF_H$	Enable strict priority
GSWIP_CFG	All Fields	$=8000_H$	Enable GSWIP and all ports

Table 12 shows the registers configuration for self-start mode: managed switch sub-mode when PS_OP_MD = $1x_B$.

Table 12 Registers Configuration for Self-start Mode: Managed Switch Sub-Mode

Register	Field	Description	Note
Following Configurations when PS_OP_MD is “11”			
SMDIO_CFG	Bit 8 to 4	When PS_SUBTYPE_MD[1:0] is 0: = 0_H When PS_SUBTYPE_MD[1:0] is 1: = 4_H When PS_SUBTYPE_MD[1:0] is 2: = 10_H When PS_SUBTYPE_MD[1:0] is 3: = $1F_H$	Configure SMDIO Address
Following Configurations when PS_OP_MD is “10”			
SSPI_CFG	Bit 15	=~PS_SUB_MD[0]	SDO Driving Edge Selection
SSPI_CFG	Bit 14	=~PS_SUB_MD[1]	SDI Sampling Edge Selection
SSPI_CFG	Bit 0	$=1_B$	Enable SSPI
GPIO_ALTSEL0	Bit 5 to 2	$=1111_B$	Change GPIO to alternate function SSPI
GPIO_ALTSEL1	Bit 5 to 2	$=0000_B$	Change GPIO to alternate function SSPI
Configurations when PS_OP_MD is “1X”			
MII_CFG_5	Bit 14:13	$=10_B$	Enable RGMII5 interface
PHY_ADDR_5	All fields	= $32A5_H$	For RGMII5 interface, force link on, speed is 1 Gbps, full duplex, pause enable
PCDU_5	Bit 9:7	When PS_SUBTYPE_MD[4] is 1_B: = 4	Setting RGMII RX delay to 2ns
PCDU_5	Bit 2:0	When PS_SUBTYPE_MD[3] is 1_B: = 4	Setting RGMII TX delay to 2ns
PHY_ADDR_4	All fields	= $32A4_H$	Force Port 4 link speed to 1 Gbps or above, pause enable, link on, full duplex
NCO_CTRL	Bit 3:1	When PS_SUBTYPE_MD[2] is 1_B $=111_B$	Set SGMII to 2.5 Gbps Mode according to pin strapping
RST_REQ	All field	= $0F_H$	Remove reset for SGMII.
SGMII_PHY_HWBU_CTRL	All Fields	$=0009_H$	Activate hardware bring up FSM
SGMII_PHY_STATUS	All Fields	Read wait until bit [11:7] =7	Check whether HWFSM was brought up correctly
SGMII_TBI_TBICTL	All Fields	$=0033_H$	Initialize TBI module keep TBI module enabled
SGMII_TBI_TBICTL	All Fields	$=0032_H$	Put TBI module out of init state and keep TBI module enabled
SGMII_PCS_TXB_CTL	All Fields	$=0003_H$	Initialize TX BUFFER

Table 12 Registers Configuration for Self-start Mode: Managed Switch Sub-Mode (cont'd)

Register	Field	Description	Note
SGMII_PCS_TXB_CTL	All Fields	$=0001_H$	TX BUFFER running
SGMII_PCS_RXB_CTL	All Fields	$=0003_H$	Initialize RX BUFFER
SGMII_PCS_RXB_CTL	All Fields	$=0001_H$	RX BUFFER running
SGMII_TBI_ANEGCTL	All Fields	$=00F0_H$	RX BUFFER running
SGMII_TBI_LPSTAT	All Fields	$=0021_H$	Force to full duplex and 1 or 2.5 Gbps speed
BM_WRED_GTH_0	All Fields	$=0100_H$	Global watermark is 256 segments. Remaining 256 segments are for buffer reservation
BM_WRED_GTH_1	All Fields	$=0100_H$	Global watermark is 256 segments. Remaining 256 segments are for buffer reservation
MAC_CTRL_4 (for each port)	All Fields	$=1494_H$	Enable EEE LPI Mode for each port
SDMA_PFCTHR8 (for each port)	All Fields	$=0018_H$	Configure backpressure watermark for each port
SDMA_PFCTHR9 (for each port)	All Fields	$=001E_H$	Configure backpressure watermark for each port
SDMA_FCTHR1	All Fields	$=03FF_H$	Configure tail drop watermark
SDMA_FCTHR2	All Fields	$=03FF_H$	Configure tail drop watermark
SDMA_FCTHR3	All Fields	$=03FF_H$	Configure tail drop watermark
SDMA_FCTHR4	All Fields	$=03FF_H$	Configure tail drop watermark
Buffer Reservation for each queue	All Fields	$=001E_H$	Buffer Reservation for each queue is 30 segments
WRED green min/max for each queue	All Fields	$=03FF_H$	Configure WRED green min/max for each queue
Queue weight for each queue	All Fields	$=FFFF_H$	Enable strict priority
GSWIP_CFG	All Fields	$=8000_H$	Enable GSWIP and all ports

Table 13 LED Status VS LED Mode

LED Mode	LEDx0	LEDx1	LEDx2	Configuration
0	10 Mbps link activity Blinking frequency: 4 Hz Single color or dual color	100 Mbps Link Activity Blinking frequency: 4 Hz Single color or dual color	1000 Mbps link activity Blinking frequency: 4 Hz Single color or dual color	**GPIO2_ALTSEL0**= $7FFF_H$ **GPIO2_PUDEN** = 4000_H **GPIO2_DRIVE1_CFG** = $7FFF_H$
1	Link Single color or dual color	Activity Blinking depends on packet rate Single color or dual color	GPIO	**GPIO2_ALTSEL0**= $43FF_H$ **GPIO2_PUDEN** = $7C00_H$ **GPIO2_DRIVE1_CFG** = $03FF_H$
2	Link activity Blinking frequency: 4 Hz Single color or dual color	100 Mbps Single color or dual color	1000 Mbps Single color or dual color	**GPIO2_ALTSEL0**= $7FFF_H$ **GPIO2_PUDEN** = 4000_H **GPIO2_DRIVE1_CFG** = $7FFF_H$
3	10 Mbps or 100 Mbps link activity Blinking frequency: 4 Hz Single color or dual color	1000 Mbps link activity Blinking frequency: 4 Hz Single color or dual color	GPIO	**GPIO2_ALTSEL0**= $43FF_H$ **GPIO2_PUDEN** = $7C00_H$ **GPIO2_DRIVE1_CFG** = $03FF_H$

EEPROM Detection Procedure (PS_NOWAIT = 1_B)

Boot loader configures the registers in the same way as Self-start mode procedure first (as shown in **Self-start Mode Procedure (PS_NOWAIT = 1_B)**. After that, SPI master uses default low speed clock and 24-bit address mode to start. It uses SPI master manual mode and start to read the first six addresses of EEPROM. When the value in **MSPI_DIN23** = $010101XX010101XX_B$, then most likely valid flash is attached. The address mode (**ADDRMD** in MSPI_CFG) is set to the lower 2 bits of **MSPI_DIN23**. After that, with the new addressing mode, read address 6 and 7 of the EEPROM. When the value of the address 6 is 10101010_B, then it is confirmed that the flash is detected. Configure SPI master clock frequency (**CLKDIV** in **MSPI_CFG**) to the value in the address 7 of the EEPROM. Finally the configuration in EEPROM is executed by boot loader.

EEPROM Applications

Connecting an external EEPROM is intentionally used to enable customers implementing systems without any management entity or STA. In such a system there is no STA driving the management interface and thus neither control nor configuration information is transferred as such. Also it is not possible to configure all functionality of the Gigabit Ethernet Switch solely using the pin-strapping interface. In such applications, the external EEPROM provides a low cost and efficient solution to store the whole configuration information required to be loaded by the Gigabit Ethernet Switch during startup.

The Gigabit Ethernet Switch supports EEPROM devices by means of SPI master interface.

In the simplest application the EEPROM is only used to store the configuration information of the Gigabit Ethernet Switch. This configuration is loaded by the Gigabit Ethernet Switch directly after reset or power-up when an EEPROM has been detected.

EEPROM Content

Table 21 shows the EEPROM contents, which include EEPROM type record and configuration content records.

The start address for EEPROM type record is 0. There are 8 bytes in EEPROM type record. **Table 14** shows the format of EEPROM type record.

The start address for EEPROM configuration content record is 8.

Table 21 shows the overall EEPROM content format.

Table 15 to Table 20 define configuration content record. It consists of multiple access blocks. For each access block, there are the following elements:

- Number of configuration entries. When it is 0, this is the last access block and no valid configuration for the last access block. When it is non-0, it represents the number of configuration entries in the current access block.
- Access Type
  - When it is 0000_H, then the current access type is incremental access type. Only the address for the first access entry is stored in the EEPROM. See Table 15.
  - When it is $FFFF_H$, then the current access type is single access without write enable type. The address for each access entry is stored in the EEPROM. See Table 16.
  - When it is 6666_H, then the current access type is single access with write enable type. The address and the write enable for each access entry is stored in the EEPROM. This requires read-modify-write operation for each access entry. See Table 17.
  - When it is 9999_H, then the current access type is “run self-start mode configuration”. The configuration is listed in **Self-start Mode Procedure (PS_NOWAIT = 1_B)**. See Table 18.
  - When it is 5555_H, then the current access type is wait until true access. Boot loader polls a 16-bit register until its value after mask matches with the expected data. See Table 19.
  - When it is $AAAA_H$, then the current access type is conditional jump access. Boot load reads a 16-bit register, when its value after mask matches with the expected data, boot loader jumps to a new location. The new location relative offset to the current address is programmable in the block. See Table 20.
- Optional: 16-bit Bus Address
- Single or Multiple 16-bit Data to be written or read
- Optional: 16-bit mask for read or enable for write
- Optional: The offset of the next address from the current address

Table 14 EEPROM Type Record

Address[1]	Content								Comment
	7	6	5	4	3	2	1	0	
0	0	1	0	1	0	1	EEPROM Address Mode		Identify EEPROM and EEPROM Address Mode EEPROM Address Mode: **Constants** 00_B **9-bit** SPI master interface is in 9-bit address mode. 01_B **16-bit** SPI master interface is in 16/17-bit address mode. 10_B **24-bit** SPI master interface is in 24-bit address mode. 11_B **24H-bit** SPI master interface is in 24-bit high speed address mode.
1	0	1	0	1	0	1	EEPROM Address Mode		
2	0	1	0	1	0	1	EEPROM Address Mode		
3	0	1	0	1	0	1	EEPROM Address Mode		
4	1	0	1	0	1	0	1	0	Check Value
5	CLKDIV								Master SPI Clock is 62.5 MHz/(CLKDIV+1)
6	0	0	0	0	0	0	0	0	
7	0	0	0	0	0	0	0	0	

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode.

Table 15 Configuration Content Record: Incremental Access Format

Address[1]	Content								Comment
	7	6	5	4	3	2	1	0	
Incremental Access Format									
0	NOCE[15:8]								Number of Configuration Entries. A value of 00_H corresponds to 0 entry. A value of $FFFF_H$ corresponds to 65535 entries.
1	NOCE[7:0]								
2	0	0	0	0	0	0	0	0	0000_H = Incremental Access Type
3	0	0	0	0	0	0	0	0	
4	ADDR(0)[15:8]								PDI Bus Address and Configuration-Data for Entry 0
5	ADDR(0)[7:0]								
6	DATA(0)[15:8]								
7	DATA(0)[7:0]								
8	DATA(1)[15:8]								PDI Bus Configuration-Data Word for Entry 1
9	DATA(1)[7:0]								
...	...								...
6+2*(NOCE-1)	DATA(NOCE-1)[15:8].								PDI Bus Configuration-Data Word for Entry #NOCE -1
7+2*(NOCE-1)	DATA(NOCE-1)[7:0]								

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode.

Table 16 Configuration Content Record: Single Access without Write Enable Format

Address[1]	Content								Comment
	7	6	5	4	3	2	1	0	
Single Access Without Write Enable Format									
0	NOCE[15:8]								Number of Configuration Entries. A value of 00_H corresponds to 0 entry. A value of $FFFF_H$ corresponds to 65535 entries.
1	NOCE[7:0]								
2	1	1	1	1	1	1	1	1	$FFFF_H$ = Single Access Without Write Enable Type
3	1	1	1	1	1	1	1	1	
4	ADDR(0)[15:8]								PDI Bus Address and Configuration-Data for Entry 0
5	ADDR(0)[7:0]								
6	DATA(0)[15:8]								
7	DATA(0)[7:0]								
8	ADDR(1)[15:8]								PDI Bus Address and Configuration-Data for Entry 1
9	ADDR(1)[7:0]								
10	DATA(1)[15:8]								
11	DATA(1)[7:0]								
...	...								...

Table 16 Configuration Content Record: Single Access without Write Enable Format (cont'd)

Address[1]	Content								Comment
	7	6	5	4	3	2	1	0	
4 + 4*(NOCE-1)	ADDR(NOCE-1)[15:8]								PDI Bus Address and Configuration-Data for Entry #NOCE-1
5 + 4*(NOCE-1)	ADDR(NOCE-1)[7:0]								
6 + 4*(NOCE-1)	DATA(NOCE-1)[15:8]								
7 + 4*(NOCE-1)	DATA(NOCE-1)[7:0]								

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode.

Table 17 Configuration Content Record: Single Write Access with Write Enable Format

Address[1]	Content								Comment
	7	6	5	4	3	2	1	0	
Single Access With Write Enable Format									
0	NOCE[15:8]								Number of Configuration Entries. A value of 00_H corresponds to 0 entry. A value of $FFFF_H$ corresponds to 65535 entries.
1	NOCE[7:0]								
2	0	1	1	0	0	1	1	0	6666_H = Single Access With Write Enable Type
3	0	1	1	0	0	1	1	0	
4	ADDR(0)[15:8]								PDI Bus Address, Configuration-Data and Write Enable for Entry 0 This requires read-modify-write. Write Enable **Constants** 0_B **DIS** Don't Modify the Bit. 1_B **EN** Modify the Bit.
5	ADDR(0)[7:0]								
6	DATA(0)[15:8]								
7	DATA(0)[7:0]								
8	WE(0)[15:8]								
9	WE(0)[7:0]								
10	ADDR(1)[15:8]								PDI Bus Address, Configuration-Data and Write Enable for Entry 1 This requires read-modify-write. Write Enable **Constants** 0_B **DIS** Don't Modify the Bit. 1_B **EN** Modify the Bit.
11	ADDR(1)[7:0]								
12	DATA(1)[15:8]								
13	DATA(1)[7:0]								
14	WE(1)[15:8]								
15	WE(1)[7:0]								
...	...								...
4 + 6*(NOCE-1)	ADDR(NOCE-1)[15:8]								PDI Bus Address, Configuration-Data and Write Enable for Entry #NOCE-1 This requires read-modify-write. Write Enable **Constants** 0_B **DIS** Don't Modify the Bit. 1_B **EN** Modify the Bit.
5 + 6*(NOCE-1)	ADDR(NOCE-1)[7:0]								
6 + 6*(NOCE-1)	DATA(NOCE-1)[15:8]								
7 + 6*(NOCE-1)	DATA(NOCE-1)[7:0]								
8 + 6*(NOCE-1)	WE(NOCE-1)[15:8]								
9 + 6*(NOCE-1)	WE(NOCE-1)[7:0]								

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode.

Table 18 Configuration Content Record: Run Self-start Mode Configuration Format

Address[1]	Content								Comment
	7	6	5	4	3	2	1	0	
Run Self Start Mode Configuration Format									
0	NOCE[15:8]								Any Value /= 0
1	NOCE[7:0]								
2	1	0	0	1	1	0	0	1	9999_H = Run Self Start Mode Configuration
3	1	0	0	1	1	0	0	1	

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode.

Table 19 Configuration Content Record: Wait Until True Format

Address[1]	Content								Comment
	7	6	5	4	3	2	1	0	
Wait Until True Access Format									
0	NOCE[15:8]								Any Value /= 0
1	NOCE[7:0]								
2	0	1	0	1	0	1	0	1	5555_H = Wait Until True Access
3	0	1	0	1	0	1	0	1	
4	ADDR[15:8]								Register Address
5	ADDR[7:0]								
6	DATA[15:8]								Expected Data
7	DATA[7:0]								
8	MASK[15:8]								Comparison Mask **Constants** 0_B **DIS** Don't Compare. 1_B **EN** Compare.
9	MASK[7:0]								

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode.

Table 20 Configuration Content Record: Conditional Jump Access Format

Address[1]	Content								Comment
	7	6	5	4	3	2	1	0	
Conditional Jump Access Format									
0	NOCE[15:8]								Any Value /= 0
1	NOCE[7:0]								
2	1	0	1	0	1	0	1	0	$AAAA_H$ = Conditional Jump Access
3	1	0	1	0	1	0	1	0	
4	ADDR[15:8]								Register Address
5	ADDR[7:0]								
6	DATA[15:8]								Expected Data
7	DATA[7:0]								

Table 20 Configuration Content Record: Conditional Jump Access Format (cont'd)

Address[1)]	Content								Comment
	7	6	5	4	3	2	1	0	
8	MASK[15:8]								Comparison Mask **Constants** 0_B **DIS** Don't Compare. 1_B **EN** Compare.
9	MASK[7:0]								
A	OFFSET[15:8]								Next Address = Next EEPROM Address of OFFSET[7:0] + OFFSET[15:0]*2 OFFSET is a signed integer.
B	OFFSET[7:0]								

1) This is the byte-wise EEPROM address. This scheme is independent of the used address mode.

Table 21 EEPROM Content Format

Address Range	Content	Comment
0 to 7	EEPROM Type Record	Identify EEPROM Address Mode and Speed
8 to ...	Configuration Content Record	Boot loader

Pin Strapping

This section describes the configuration of the device by means of pin strapping. As can be seen, the pin strapping functionality shares the LED pins, SPI and TDO signals.

Internal pull up for the pin strapping must be disabled after reset.

Table 22 and **Table 23** list the pin-strapping mapping.

All GPIO pins are sampled at the rising edge of HRSTN and stored in registers PS0 and PS1. These two registers can only be reset by hardware reset.

PLL must be released from reset state some cycles after the rising edge of HRSTN (so that pin strapping occurs and be stable before PLL is released).

Table 22 Functional Mode Pin Strapping

Pin Strap	Description
PS0(3): UTXD	PS_XTAL
PS0(7): MSDO	PS_OP_MD1
PS0(8): MSCK	PS_SUBTYPE_MD3
PS0(9): MSCS	PS_SUBTYPE_MD4
PS1(10): LED02	PS_NOWAIT
PS1(11): LED12	PS_OP_MD0
PS1(12): LED22	PS_SUBTYPE_MD0
PS1(13): LED32	PS_SUBTYPE_MD1
PS1(14): LED42	PS_SUBTYPE_MD2

Table 23 Pin Strapping Description

Pin Strapping Signals	Description
PS_XTAL	**XTAL Frequency** This is to specify the frequency of XTAL. 0_B **40 MHz** 40 MHz 1_B **25 MHz** 25 MHz
PS_NOWAIT	**No Wait for External Master Trigger** This is to specify whether the boot loader waits for the external master to trigger the start. 0_B **WAIT** Boot loader waits for external master to trigger the start of GPHY and GSWIP. 1_B **NOWAIT** Boot loader starts GPHY and GSWIP after the initialization is done.
PS_OP_MD	**Operation Mode** This is to specify the chip operation mode. 00_B **OPMD0** Reserved 01_B **OPMD1** Standalone Unmanaged Switch. 10_B **OPMD2** Managed Switch with SPI Slave Interface. 11_B **OPMD3** Managed Switch with MDIO Slave Interface.
PS_SUBTYPE_MD	**SUB Type Mode** See **Table 24**.

Table 24 SUBTYPE Mode Configuration

Operation Mode	SUBTYPE Mode
OPMD1: Standalone Unmanaged Switch	PS_SUBTYPE_MD[4:3]: 00_B **MD0** LED Display Mode 0 01_B **MD1** LED Display Mode 1 10_B **MD2** LED Display Mode 2 11_B **MD3** LED Display Mode 3
	PS_SUBTYPE_MD[2]: 0_B **AUTO** Auto-polling to determine RGMII5 link status. 1_B **FORCE** Force RGMII5 link speed to 1G, full duplex and on.
	PS_SUBTYPE_MD[1]: Reserved
	PS_SUBTYPE_MD[0]: 0_B **DIS** Disable RGMII5 interface. 1_B **EN** Enable RGMII5 interface.

Table 24 SUBTYPE Mode Configuration (cont'd)

Operation Mode	SUBTYPE Mode
OPMD2: Managed Switch with SPI Slave Interface	PS_SUBTYPE_MD[4]: 0_B **RXDLY0** RGMII Path RX Delay is 0 ns. 1_B **RXDLY2** RGMII Path RX Delay is 2 ns.
	PS_SUBTYPE_MD[3]: 0_B **TXDLY0** RGMII Path TX Delay is 0 ns. 1_B **TXDLY2** RGMII Path TX Delay is 2 ns.
	PS_SUBTYPE_MD[2]: 0_B **1G** SGMII Interface is 1 Gbps, MAC mode and Auto-neg disabled. 1_B **2.5G** SGMII Interface is 2.5 Gbps, MAC mode and Auto-neg disabled.
	PS_SUBTYPE_MD[1]: SSPI SDI Edge Select 0_B **RISE** Sample at rising edge 1_B **FALL** Sample at falling edge
	PS_SUBTYPE_MD[0] SSPI SDO Edge Select 0_B **RISE** Drive at rising edge 1_B **FALL** Drive at falling edge
OPMD3: Managed Switch with MDIO Slave Interface	PS_SUBTYPE_MD[4]: 0_B **RXDLY0** RGMII Path RX Delay is 0 ns. 1_B **RXDLY2** RGMII Path RX Delay is 2 ns.
	PS_SUBTYPE_MD[3]: 0_B **TXDLY0** RGMII Path TX Delay is 0 ns. 1_B **TXDLY2** RGMII Path TX Delay is 2 ns.
	PS_SUBTYPE_MD[2]: 0_B **1G** SGMII interface is 1 Gbps, MAC mode and Auto-neg disabled. 1_B **2.5G** SGMII Interface is 2.5 Gbps, MAC mode and Auto-neg disabled.
	PS_SUBTYPE_MD[1:0]: 00_B **0** SMDIO Address is 0. 01_B **4** SMDIO Address is 4. 10_B **16** SMDIO Address is 16. 11_B **31** SMDIO Address is 31.

3.2.8 Packet Insertion and Extraction

An external controller is able to insert and extract the packets to/from the switch via port 6 of Gigabit Ethernet switch. When packet insertion/extraction mode is enabled (**PIE** = 1_B), switch port 6 is connected to packet insertion/extraction module. This mode allows external CPU to insert/extract management/control packets without using RGMII interface.

In packet insertion/extraction mode, port 6 must be configured to 1000 Mbps, full duplex and pause disable mode. The link ok must be forced on.

For TX direction (packet extraction), when there is a new packet available, an interrupt is asserted. Interrupt status is cleared automatically when an external controller read **PKT_EXT_READ** register. When the AVAIL value is '1', then the data byte in the current read is the first byte of the packet and the data byte in the previous read is the last byte of the previous packet. When TXEN value of the read access is 0_B, then the data byte in the previous read is the last byte of the packet.

An external controller can flush the rest of the packet after reading the packet header in packet extraction direction.

Packet Insertion Programming Sequence

- Write **PKT_INS**:
  - **INSCMD** = 1_B
  - **RXVD** = 0_B or 1_B depending when injecting interframe gap (**RXVD**=0_B) or other types of data (including preamble, SFD and packet data, **RXVD**=1_B).
  - **RXD** = the byte to be written.
- Repeat the above step for all the bytes in a packet (including IPG, Preamble, SFD). At least one interframe gap must be inserted so that the MAC can identify the end of packet and the start of the packet. At least one cycle between the two writes to **PKT_INS** must be met.

Packet Extraction Read Programming Sequence

- Wait for interrupt.
- Read **PKT_EXT_READ** register.
- When **TXEN** is 1_B, then the data byte is valid. When **TXEN** is 0_B, then the data byte is not valid.
- When the previous read **TXEN** = 0_B, the current read **TXEN** = 1_B and the current read **AVAIL** = 1_B, then current read data byte is the first byte of the packet (including preamble and SFD).
- When the previous read **TXEN** = 1_B and the current read **TXEN** = 0_B or current read **AVAIL** = 1_B, then the previous read data byte is the last byte of the packet.
- Repeat reading until **TXEN** = 0_B or current read **AVAIL** = 1_B (EOP or SOP is detected). At least one cycle between the read reads to **PKT_EXT_READ** must be met.

Packet Extraction Flush Programming Sequence

- Write **PKT_EXT_CMD** to issue flush command (**FLUSH** = 1_B).
- Wait for interrupt and check whether **AVAIL** in **PKT_EXT_CMD** is set for the next new packet.

3.3 LED Controller Function Description

3.3.1 LED

LED pin 10, 20, 30 and TCK are multiplexed with JTAG interface. When TRSTN = ‘0’, these 4 pins are used for GPIO/LED pins. When TRSTN = ‘1’, these 4 pins are used for JTAG interface.

3.3.2 LED Display

Each GPHY has 3 LEDs. The 3rd LED are used for pin strapping in the boot loader. All of them can be used as single color LED or dual color LED. When dual color LED is required in system, it is recommended to use the 3rd LED as one of the dual color LED to ease the pin-strapping circuit. The 3rd LED are used for pin strapping in the Boot ROM code.

Power LED is always in single color mode and multiplexed with GPIO pin. The value of power LED is directly configurable via GPIO output register.

For each LED in single color mode, it is either connecting external LED to ground or connecting external LED to power as shown in **Figure 11**. It is configurable per LED to one of the mode via **LED_MD_CFG**. For dual color LED, the corresponding field must be set to 0_B. When LED is configured to power mode, then internal LED signal is inverted before feeding to the LED PAD. When LED is configured to power mode, both push-pull and open drain mode are supported via GPIO programming registers.

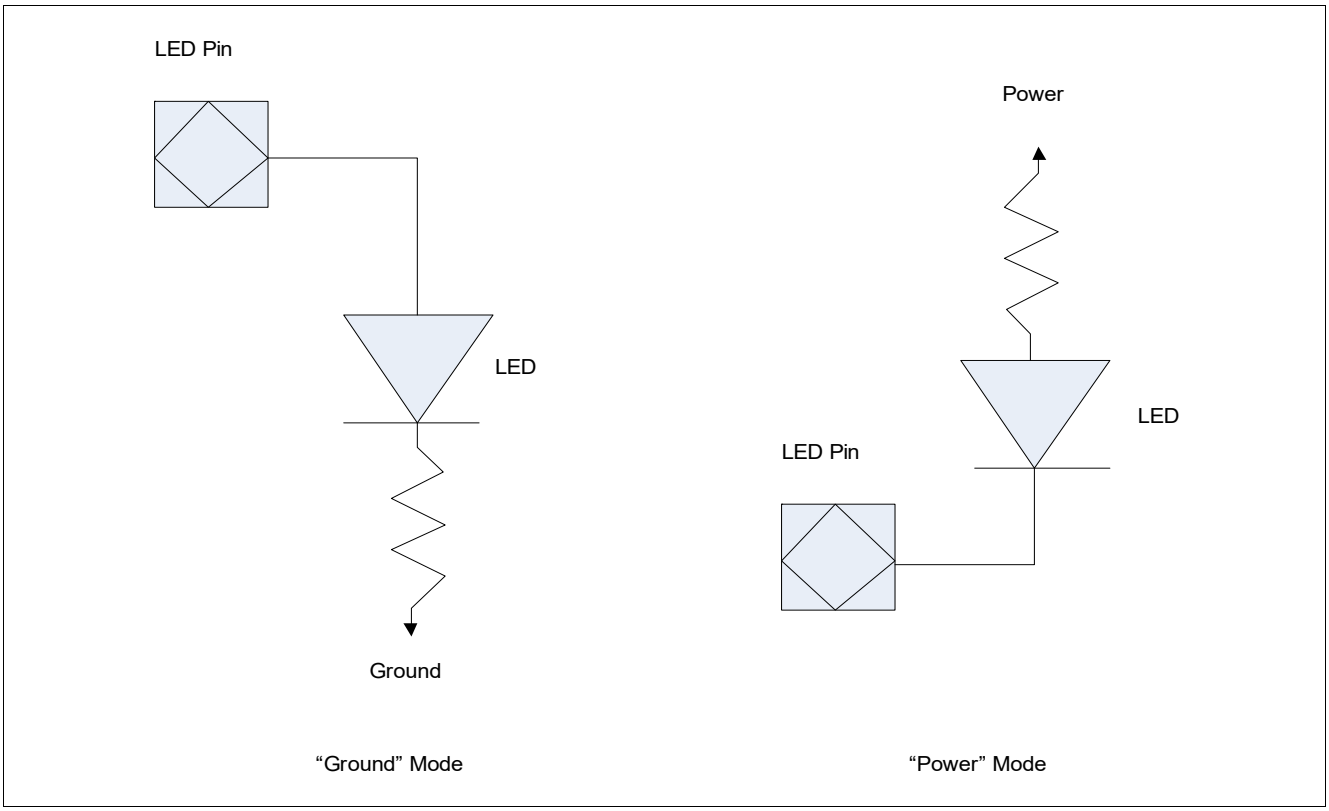


Figure 11 LED Display Mode

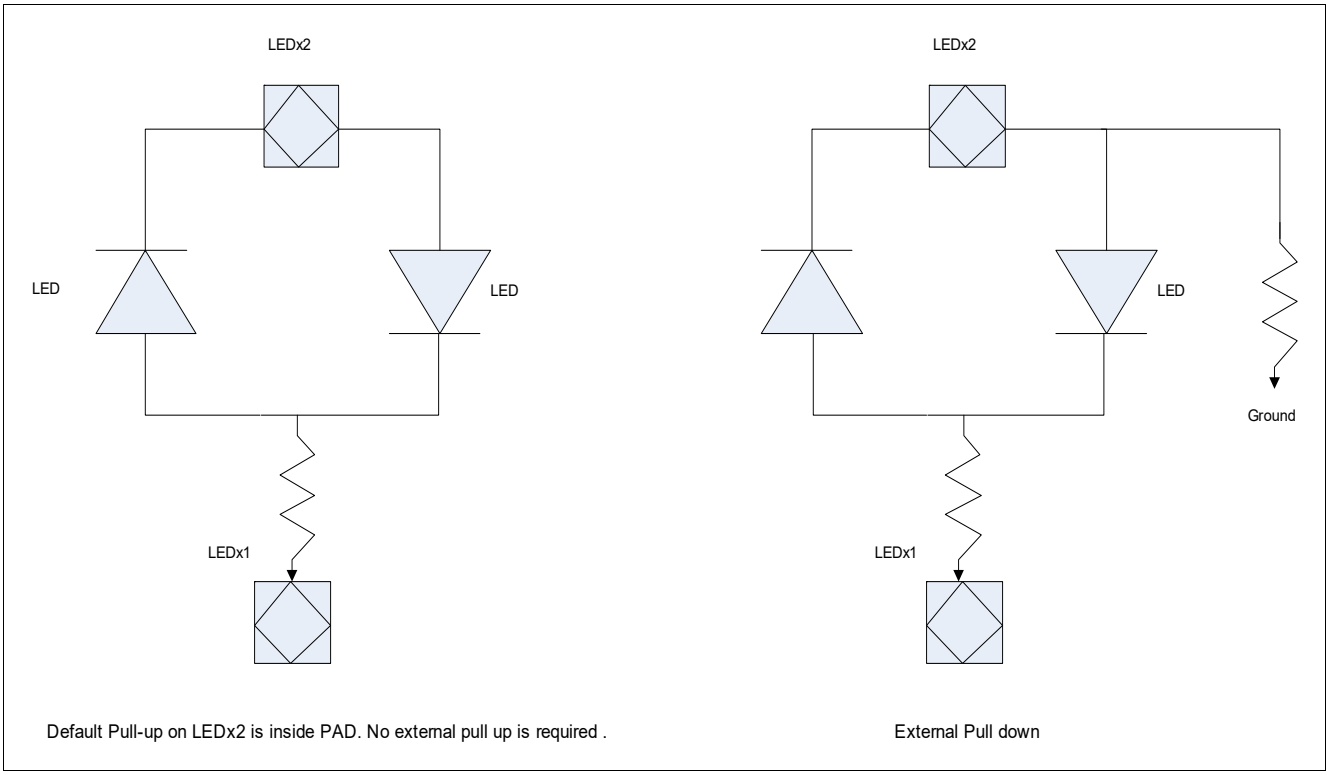


Figure 12 Pin Strapping on Dual Color LED

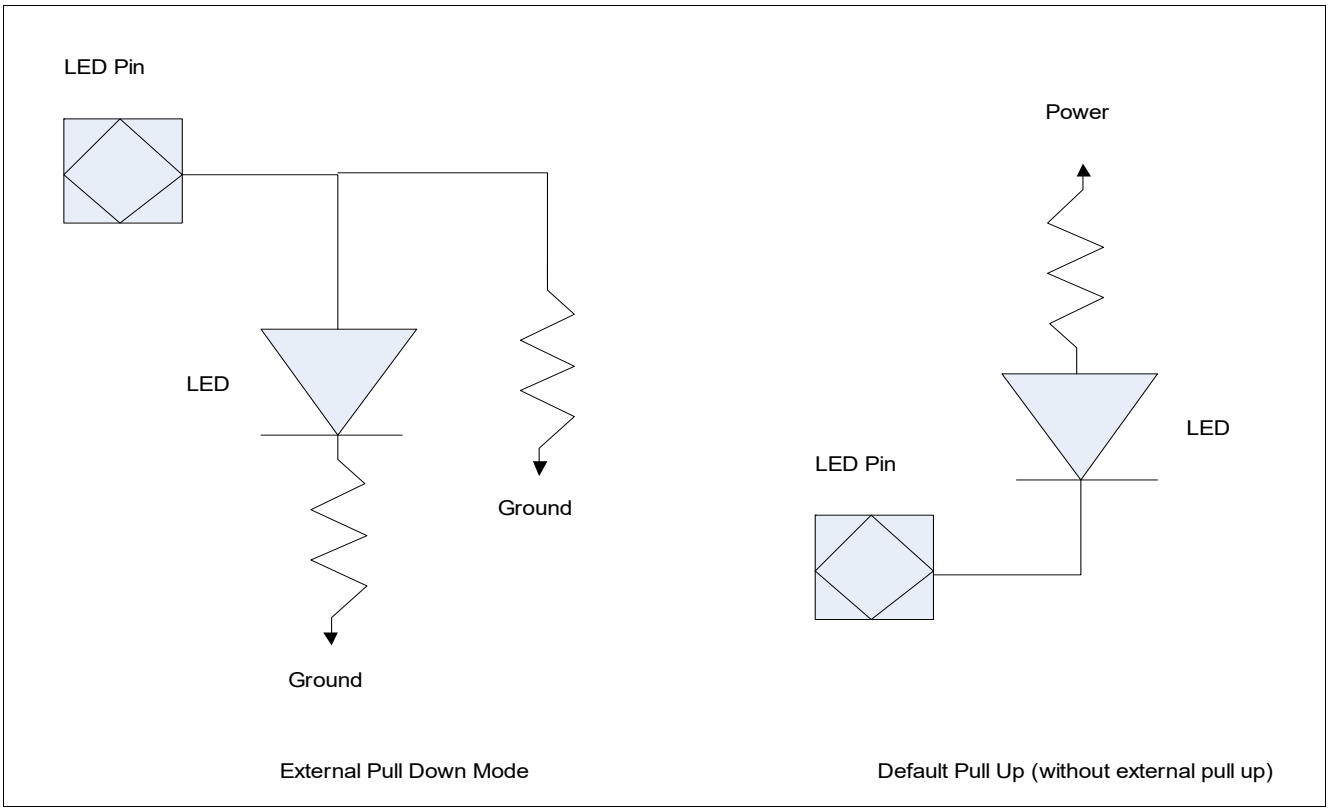


Figure 13 Pin Strapping on Single Color LED

3.3.3 LED Brightness Control

There are two brightness control mode. Either one of them can be used. The selection is determined by board design. They must not be used simultaneously.

- 2 Level Brightness Switch Mode
- 16 Level Light Sensor Control Mode

Brightness Control

This block controls the brightness of the LED by way of controlling the time duration the LED is ON/OFF, and due to persistence of the eye, LED brightness is perceived. When LED is off, the output is disabled. When LED is on, the output is enabled. Brightness control controls the LED output enable directly.

Figure 14 shows the brightness control frequency is 100Hz. Each period is divided into 64 slots. LED brightness control is enabled/disabled via **LED_BRT_CTRL.EN**.

When LED brightness control is disabled, LED is enabled in all 64 slots.

When LED brightness control is enabled, LED is enabled for consecutive n slots. n is determined by brightness level configured. LED output is disabled in the 64th slot. LED42 pin is in input mode during 64th slot and used to detect the rising/falling edge of external brightness switch input.

Figure 14 LED Brightness Control By Controlling LED Output Enable/Disable

2 Level Brightness Switch Mode

LED42 pin is sampled at slot 63 to detect the toggling. The LED brightness is switched between two configurable brightness level (**LED_BRT_CTRL.MAXLEVEL**, **LED_BRT_CTRL.MINLEVEL**).

This can be enabled/disabled via **LED_BRT_CTRL.2SEWN**. When 2 level brightness switch mode is disabled, the brightness level is configured via **LED_BRT_CTRL.MAXLEVEL**.

The spike on LED42 pin is filtered. Only when the value are stable for two consecutive sample after a change, the edge is considered as detected. The brightness must start with **LED_BRT_CTRL.MAXLEVEL**. When LED42 pin is pulled up at pin strapping, then the falling edge of the sampling triggers the brightness toggle. When LED42 pin is pulled down, then the rising edge of the sampling triggers the brightness level toggle. The falling edge or rising edge trigger is selected via **LED_BRT_CTRL.EDGE**.

When 2 level brightness switch control is disabled on system board, LED42 pin is either pull up or down externally (depending on pin strap option) to allow there is a constant, untoggled level on LED42 during the sample slot.

When 2 level LED brightness switch control is enabled on system board, an external recess switch is required to connect to LED42 pin.

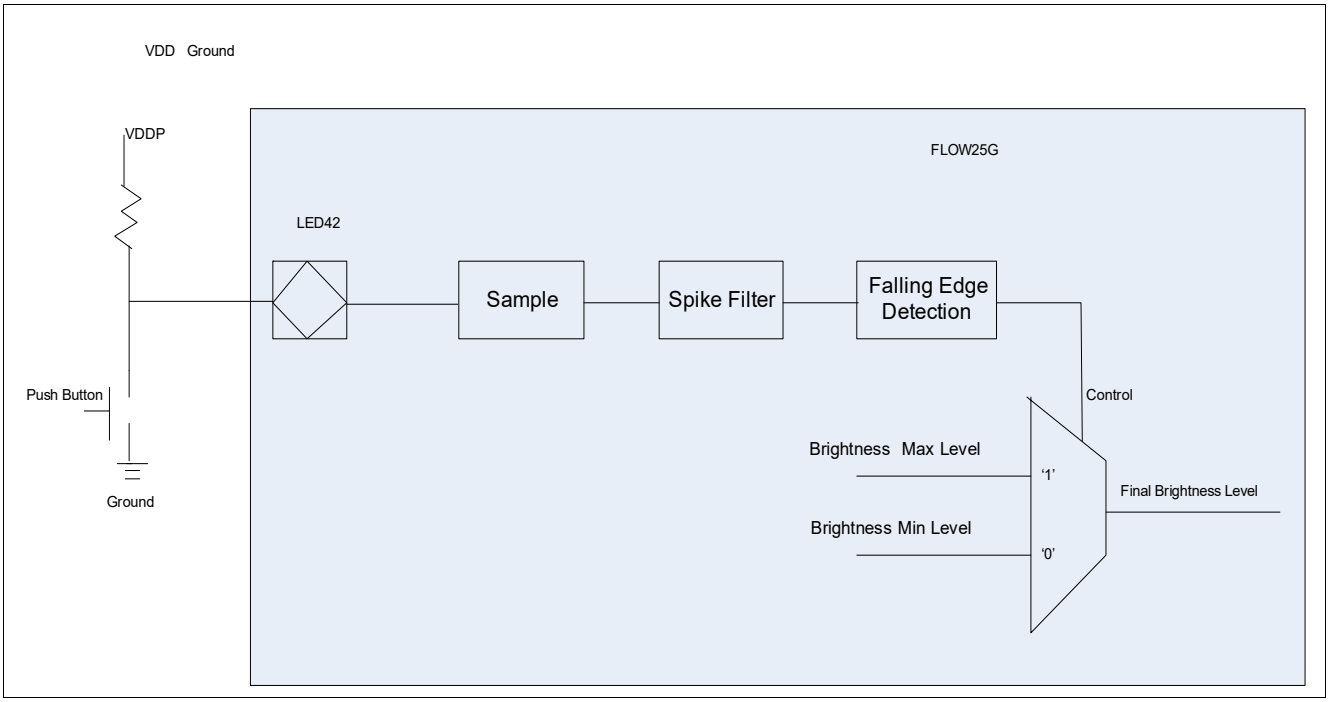


Figure 15 Direct 2 Level LED Control Enable on System Board (with Pull-Up)

16 Level Light Sensor Control Mode

In this mode, the brightness of LED dynamically varies depending on the light intensity. The light intensity is measured by a light sensor. This approach uses a constant current source (Visible Light Detector) and capacitor. The time it takes for the capacitor to charge to the given threshold voltage is linearly proportional to the charging current. The current is proportional to LUX value. One of GPIO pin is used for this purpose.

The sensing is repeated periodically. The period of the sensoring is programmable via **LED_LSENS_CTRL.PERIOD**. For each period, there are 256 slots. The first few slots are for discharging circuit. The number of slots for discharging is configurable via **LED_LSENS_CTRL.TD**. After the discharging, the rising edge of the GPIO pin is detected. The number of slots from the end of discharging to the slot when the rising edge is detected (t - td) is used to determine the light condition. There are 16 level of light condition, this 16 level light condition is converted to a 16-bit brightness level. Only when the difference between the sensed brightness level and the current brightness level is more than 1 (exception is when sensed brightness level is 1 and 15), the brightness is adjusted. Only 1 brightness level (+/-) can be adjusted from the current value. The brightness level must be within the range configured within **LED_BRT_CTRL.MINLEVEL**, **LED_BRT_CTRL.MAXLEVEL**.

When both **LED_BRT_CTRL.2SEWN** and **LED_LSENS_CTRL.SENS** are enabled, the final brightness level is the smaller value of the value determined by sensoring logic and by the 2 Level LED switch logic.

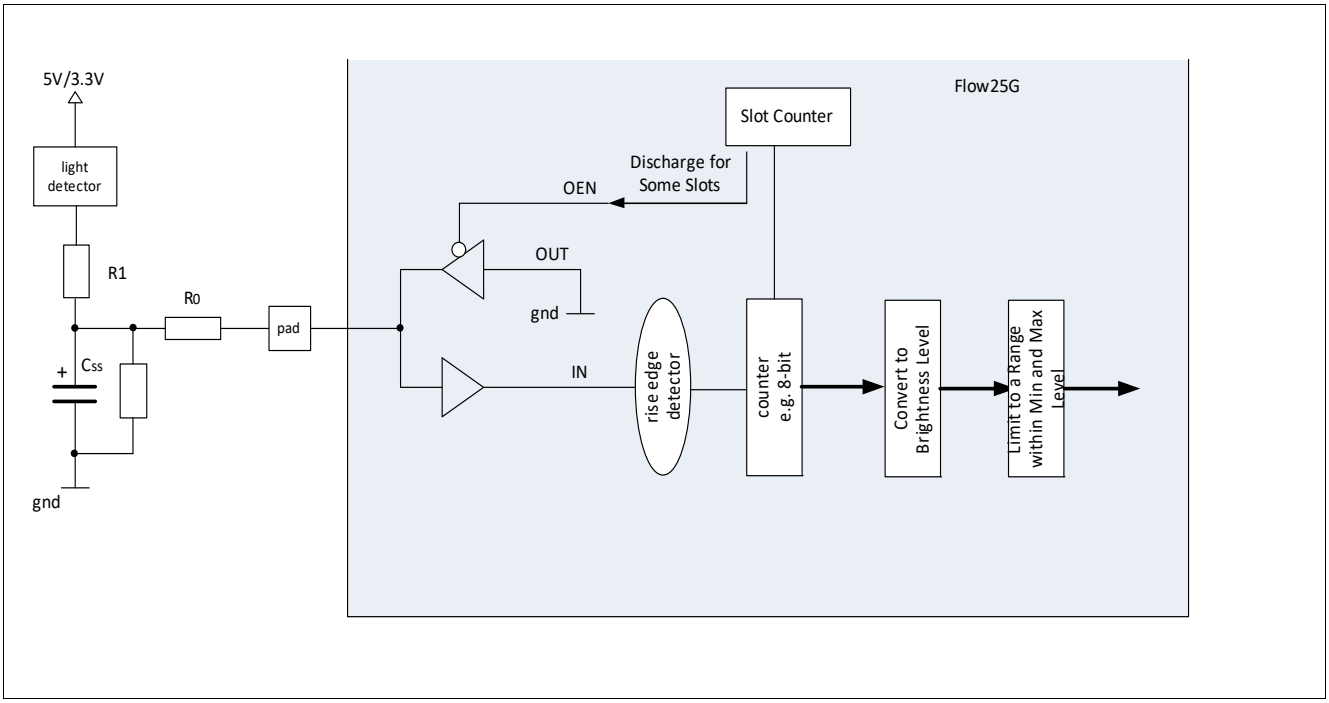


Figure 16 Light Sensing System

3.4 General Purpose Input Output Function Description

Figure 17 shows a general block diagram of a GPIO pin. Each GPIO pin is equipped with a number of control and data bits, enabling very flexible usage of the line.

Each GPIO pin can be configured for input or output operation. In input mode (default after reset), the output driver is switched off (high-impedance). The actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt-Trigger device and can be read via the read only register GPIO_IN. In output mode, the output driver is activated and drives the value supplied through the multiplexer to the port pin. Switching between input and output mode is accomplished through the GPIO_DIR register, which enables or disables the output driver.

The output multiplexer in front of the output driver enables the port output function to be used for different purposes. When the pin is used as general purpose output, the multiplexer is switched by software to the Output Data Register GPIO_OUT. Software can set or clear the bit in GPIO_OUT, and therefore it can directly influence the state of the port pin. When the on-chip peripheral units use the pin for output signals, alternate output lines can be switched via the multiplexer to the output driver circuitry.

Latch GPIO_IN is provided for input functions of the on-chip peripheral units. Its input is connected to the output of the input Schmitt-Trigger. Further, an input signal can be connected directly to the various inputs of the peripheral units (AltDataIn). The function of the input line from the pin to the input latch GPIO_IN and to AltDataIn is independent of the port pin operates as input or output. This means that when the port is in output mode, the level of the pin can be read by software via latch GPIO_IN or a peripheral can use the pin level as an input. This offers additional advantages in an application.

- Each GPIO pin can also be programmed to activate an internal weak pull-up or pull-down device. Register GPIO_PUDSEL selects whether a pull-up or the pull-down device is activated while register GPIO_PUDEN enables or disables the pull devices.
- The data written to the output register GPIO_OUT by software can be used as input data to an on-chip peripheral. This enables, for example, peripheral tests via software without external circuitry. Examples for this can be the triggering of a timer count input, generating an external interrupt, or simulating the incoming serial data stream to a serial port receive input via software.

- When the pin is used as an output, the actual logic level at the pin can be examined through reading latch GPIO_IN and compared against the applied output level (either applied through software via the output register GPIO_OUT, or via an alternate output function of a peripheral). This can be used to detect some electrical failures at the pin caused through external circuitry. In addition, software supported arbitration schemes can be implemented in this way using the open-drain configuration and an external wired-And circuitry. Collisions on the external communication lines can be detected when a logic 1 is output, but a logic 0 is seen when reading the pin value via the input latch GPIO_IN.
- The output data from a peripheral applied to the pin via an alternate output function can be read through software or used by the same or another peripheral as input data. This enables testing of peripheral functions or provides additional connections between on-chip peripherals via the same pin without external wires.

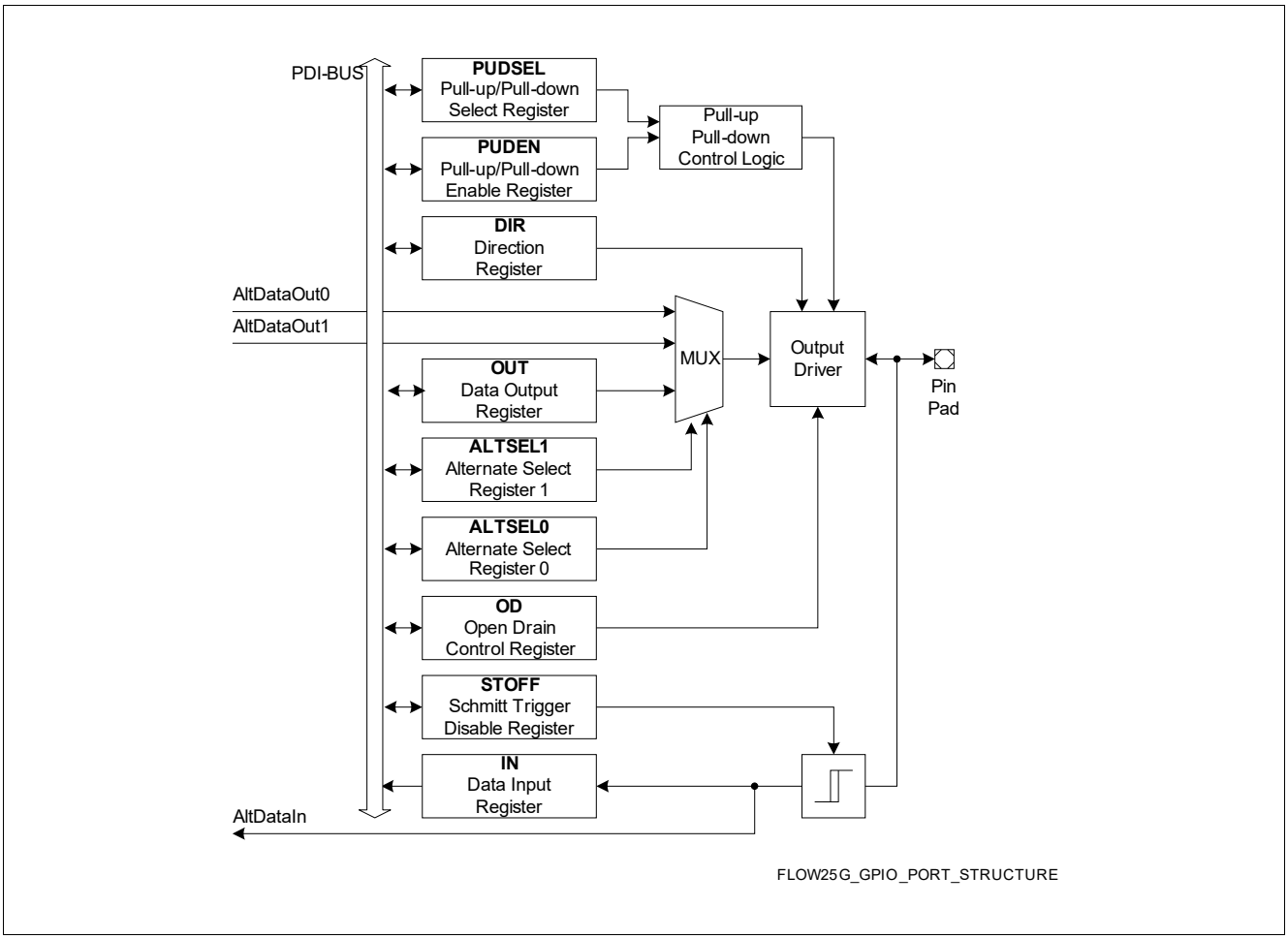


Figure 17 General Port Structure

The GPIO pins share with other alternative functions as shown in **Table 6** and **Table 7**.

3.5 Gigabit Ethernet PHY Functional Description

3.5.1 Features

- Supports Energy-Efficient Ethernet (EEE):
  - 10BASE-Te
  - 100BASE-TX
  - 1000BASE-T
  - Power Down modes
  - Wake-on-LAN support
  - Integrated termination resistors
  - Supports transformerless Ethernet (TLE) for backplane applications
  - Low-EMI voltage mode line-driver
- Auto-negotiation with next-page support
- Auto-downspeed
- Auto-MDI/MDIX and Polarity selection
- Test Loops
- Cable diagnostics:
  - Cable open/short detection
  - Cable length estimation

3.5.2 Functional Description

3.5.2.1 Twisted-Pair Interface

The Twisted-Pair Interface (TPI) of the GPHY IP is fully compliant with IEEE 802.3. To facilitate low-power implementation and reduce PCB costs, the series resistors required to terminate the twisted-pair link to nominally 100 Ω are integrated into the device.

As a consequence, the TPI pins can be directly connected via the transformer to the RJ45 plug. Additional external circuitry is only required for proper common-mode termination and rejection. **Figure 18** shows a high-level schematic of the TPI circuitry, taking these components into account.

GPHY IP supports normal operation with transformers whose center-taps on the chip side are shorted and connected to capacitors.

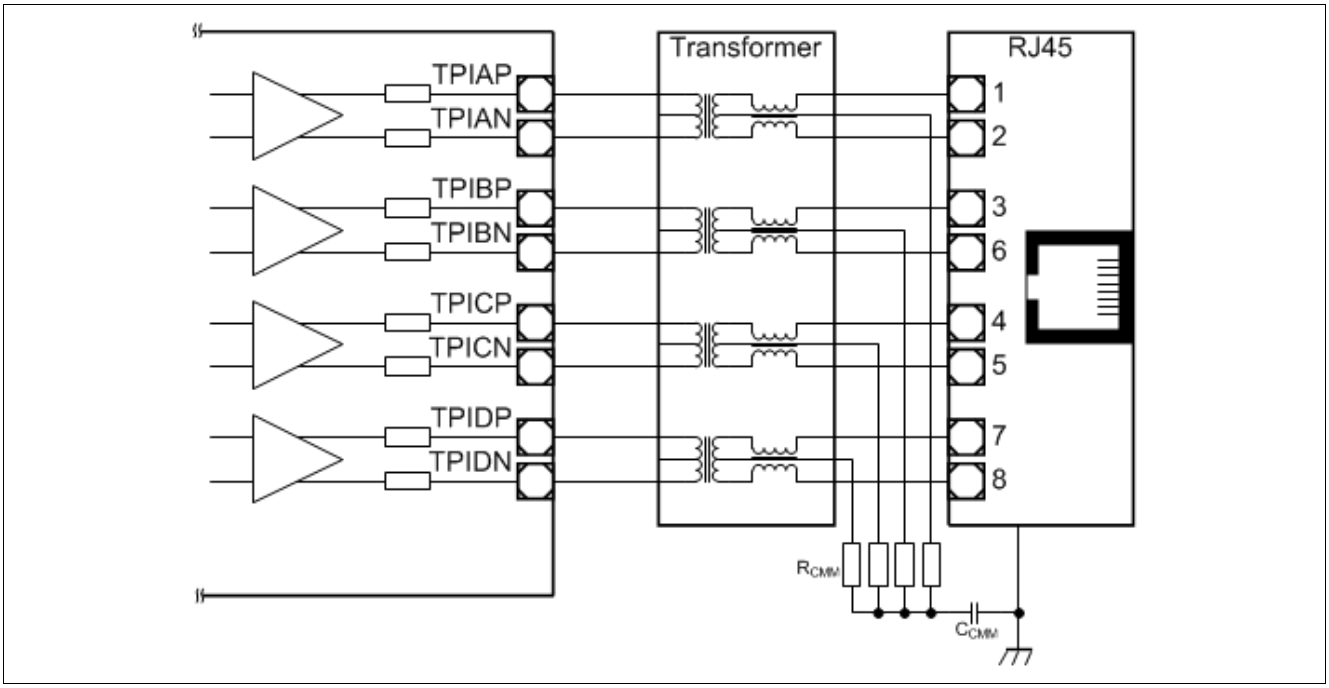


Figure 18 Twisted-Pair Interface of GPHY IP Including Transformer and RJ45 Plug

3.5.2.2 Auto-Negotiation (ANEG)

The GPHY IP supports Auto-Negotiation (ANEG) as a startup procedure to exchange capability information with the link partner.

Unless ANEG is manually disabled, the GPHY IP initiates each link-up using an ANEG procedure according to IEEE 802.3-2008 Clause 28 and essentially required for the 1000BASE-T mode in IEEE 802.3-2008 Clause 40.

Unless otherwise configured, the GPHY IP carries out an auto-crossover detect/enable procedure prior to the start of the ANEG process. This ensures optimal interoperability even in inadequate cable infrastructure environments. However, when ANEG is disabled, the auto-crossover procedure is still done during link-up.

The ANEG procedure implementation is compliant with standards given in IEEE 802.3-2008, clause 28. When the link partner does not support ANEG, the GPHY IP extracts the link-speed configuration using **parallel detection**.

The GPHY IP supports Next Page (NP) exchange, since it is mandatory for advertising 1000BASE-T capabilities. By default, NPs are exchanged autonomously and do not require interaction with any management device.

3.5.2.3 Auto-Downspeed

The Auto-Downspeed (ADS) feature ensures maximum interoperability even in harsh or inadequate cable infrastructure environments. In particular, ADS is applied during 1000BASE-T training. This is necessary because the information available about the cabling during ANEG is insufficient. It is possible to advertise 1000BASE-T during ANEG, even though it might happen that both link partners are connected via a CAT-3 cable, which does not support the 4-pair Gigabit Ethernet mode.

To avoid continuous link-up failures in such a situation, the GPHY IP operates a detection algorithm to identify this situation. As a consequence, Gigabit-capability indication is cleared from the ANEG registers. After the resulting link-down, the next ANEG process does not advertise 1000BASE-T anymore, so that even when the link partner does not implement this kind of ADS algorithm, the next link-up is done at the next advertised speed below 1000 Mbps.

It can also happen that the existing cable infrastructure is adequate, but that the integrity of received signals is not suitable for a 1000BASE-T link-up, for example due to increased alien noise, or over-length cables. When such a condition is detected, the GPHY IP also does an ADS procedure.

Finally, it can also happen that, even though the GPHY IP is able to link up properly, for example in slave mode, the link partner is not able to. In this situation, ADS criterion described previously does not become active, but the link also never comes up. To address this corner situation, the GPHY IP counts the number of attempts to link up to 1000BASE-T. When this number is greater than 3, the ADS procedure is carried out. This number is reset internally after each successful 1000BASE-T link-up.

In all flow and mode settings that support only speeds of 1000 Mbps, the ADS feature is automatically disabled.

The number of times GPHY IP decide to downspeed the link is counted and available as statistics via the MDIO.PHY.ERRCNT register.

3.5.2.4 Auto-Crossover and Polarity-Reversal Correction

To maximize interoperability even in inadequate wiring environments, the GPHY IP supports auto-crossover and polarity-reversal detection and correction. Both features are enabled by default.

Auto-crossover detection and correction operates at all supported twisted-pair speeds.

In 10BASE-T and 100BASE-TX, pairs C and D are not used. Consequently, modes 2 and 3 as well as 1 and 4 are identical.

In 1000BASE-T all modes are applicable.

The auto-crossover functionality is fully compliant with IEEE 802.3, clause 40.4.4, in 1000BASE-T mode. In the 10BASE-T and 100BASE-TX modes, this functionality depends on the detection of valid link pulses.

Polarity-reversal errors caused by improper wiring are automatically corrected by the GPHY IP. This correction is done on all pairs in the receive direction for all supported twisted-pair media modes. In 10BASE-T mode, the polarity correction is based on the detection of valid link pulses. In 100BASE-TX, the polarity of the receive signal is inherently corrected by the negation invariance of line code. In the 1000BASE-T mode, polarity detection is part of the training sequence. In all the modes, the detected polarity is frozen once the link has been established, and remains unchanged until the link is dropped.

3.5.2.5 Transformerless Ethernet (TLE)

Transformerless Ethernet (TLE) is required for back-plane or PICMG applications, where the use of a transformer (magnetics) is not necessarily required to fulfill the galvanic-decoupling requirements of the isolation specifications. In such applications, removing the transformer reduces both the external bill of materials and the space requirements on the PCB.

As the GPHY IP incorporates a novel type of voltage-mode line-driver, the only stringent requirement is to use AC coupling. AC coupling is achieved using simple SMD-type series capacitors, the value of which is selected so that the high-pass characteristics correspond to an equivalent transformer-based standard application (recommended $C_{coupling}$ = 100 nF). **Figure 19** shows the TLE external circuitry. The RJ45 connector is shown only for illustration purposes. The back-plane applications use different connectors.

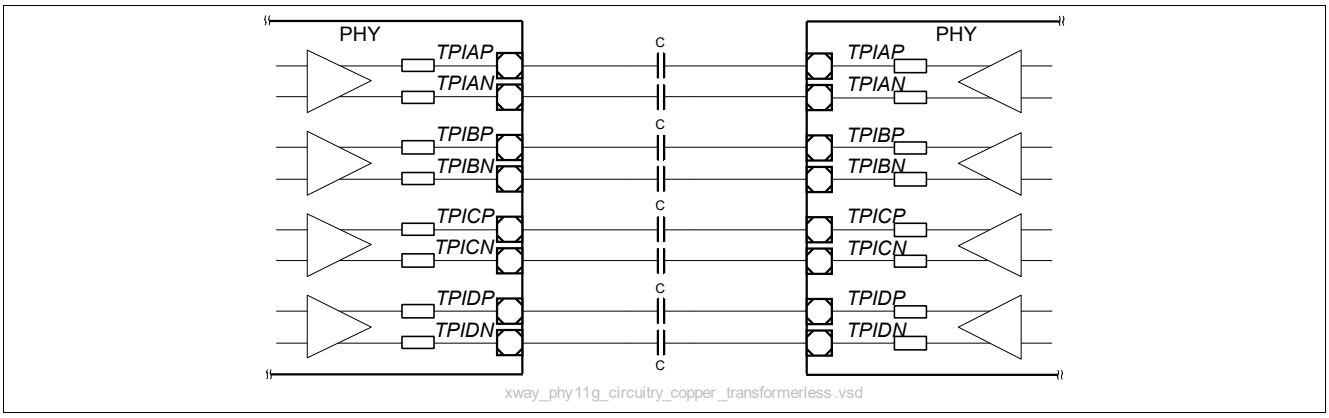


Figure 19 External Circuitry for the Transformerless Ethernet Application

3.5.2.6 Configuration and Control via MDIO

When a higher-level management entity exists in the system, this can configure and control the GPHY IP completely by means of the MDIO interface, according to IEEE 802.3-2008.

3.5.2.7 Power Management

This section introduces the power management functions of the GPHY IP.

3.5.2.7.1 Power Down Modes

This section introduces the power-down modes supported by the GPHY IP. **Figure 20** depicts how these modes are associated to states. The functionality of each mode and the state transitions are discussed in detail in the subsequent sections.

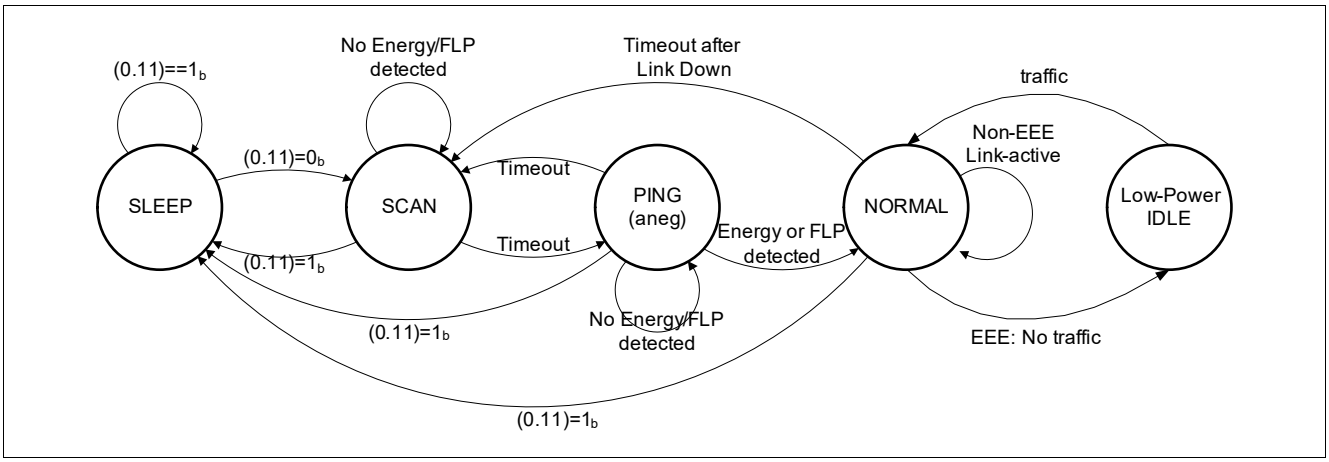


Figure 20 State Diagram for Power-Down Mode Management

3.5.2.7.2 Sleep Mode

The SLEEP mode is entered by setting register (0.11) to logic one, regardless of the current state of the device. Active links are dropped when the PHY is leaving the NORMAL mode. The sleep mode corresponds to power down as specified in IEEE802.3, clause 22.2.4.1.5. The device still reacts to MDIO management transactions. The interface clocks to the MAC are switched off. No signal is transmitted on the MDI.

Since this mode is entered manually, the device neither wakes itself nor any link partner. This functionality can be enabled by setting register (0.11) to logic zero and thus entering the SCAN mode.

3.5.2.7.3 Scan Mode

The SCAN mode differs from the SLEEP mode in that the receiver periodically scans for signal energy or FLP bursts on the media. In this mode, there is no transmission. This must correspond to the state of “NO-LINK”.

After a certain time-out has expired, the PHY moves into the PING mode. The time-out is randomized between configurable limits to prevent deadlock conditions.

3.5.2.7.4 Ping Mode

The PING mode is similar to the SCAN mode except that the transceiver transmits an FLP burst onto the TPI for a programmable amount of time. This is used to wake potential link partners from the power-down state. This must correspond to the state of ANEG.

After a certain time-out has expired, the PHY moves back into SCAN mode. The time-out is randomized between configurable limits to prevent deadlock conditions.

3.5.2.7.5 Normal Mode

The NORMAL mode is used to establish and maintain a link connection. Once this connection is dropped, the PHY moves back into SCAN mode after a configurable time-out has expired.

3.5.2.7.6 Low-Power Idle Mode: Energy-Efficient Ethernet

The IEEE 802.3az supports Energy-Efficient Ethernet (EEE) operation. The standard is also supported by the GPHY IP. Since the method used for saving energy depends on the PHY speed, this section is divided into 3 subsections corresponding to the various speeds of 10BASE-Te, 100BASE-TX and 1000BASE-T. Except for 10BASE-Te, the general idea of EEE is to save power during periods of low link utilization. Instead of sending an active idle, the transmitters are switched off for a short period of time (20 ms). The link is kept active by means of a frequent refresh cycle initiated by the PHY itself during low power mode. This sequence is repeated until a wake request is generated by one of the link-partners MACs. An EEE-compliant MAC must grant the PHY a time budget of wake time before the first packet is transmitted. The basic principle is shown in **Figure 21**.

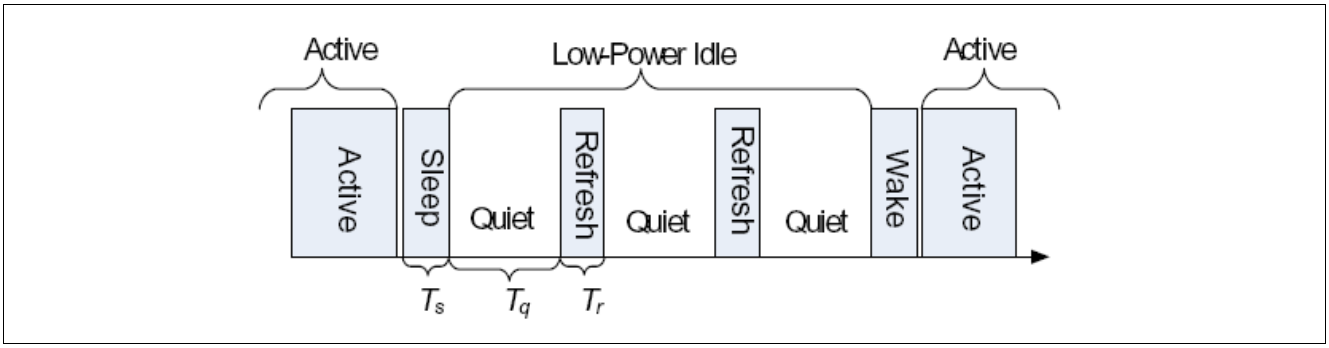


Figure 21 EEE Low-Power Idle Sequence

Auto-Negotiation for EEE Modes

It is imperative that the EEE capability is advertised, since, except for 10BASE-Te, a compliant link partner is required. Similarly to 1000BASE-T auto-negotiation, the GPHY IP automatically advertises EEE capability when this is enabled using next pages. EEE capability is stored in the `MMD.ANEG.EEE_AN_ADV` registers. Setting this register to zero disables EEE. After a successful negotiation the link partners' capabilities are stored in the `MMD.ANEG.EEE_AN_LPADV` register. After a successful auto-negotiation, the GPHY IP performs an auto-resolution on the exchanged capabilities. The result is combined with the speed resolution. Whether or not a link is able to operate EEE is reported in the `MDIO.PHY.MIISTAT.EEE` register.

3.6 SGMII Interface Function Description

3.6.1 Features

- One SGMII SerDes
  - Cisco* Serial-GMII Specification Rev 1.8 standard compliant operation at 1.25 Gbaud/s; extensions to achieve 3.125 GBaud/s by overclocking the SerDes
  - 2.5 Gbps (one lane of XAUI conforming per 802.3, part 4, clause 47: 10 Gigabit Attachment Unit Interface (XAUI)) full duplex)
  - SerDes interface includes Clock and Data Recovery (CDR)
  - Supports multiple power-down modes
  - Supports programmable TX attenuation and amplification
  - Supports programmable flat-band RX equalization
  - Supports auto-calibration of RX and TX impedances
  - Supports test loop feature for debugging
  - Requires an external resistor to calibrate the termination impedance of the high speed RX and TX signals
- One SGMII PCS
  - Integrates IEEE 802.3 clause 36 and 37 compliant PCS component
  - Cisco* Serial-GMII Specification Rev 1.8 standard compliant operation at 1.25 Gbaud/s; extensions to achieve 3.125 GBaud/s by overclocking the SGMII PCS
  - 2.5 Gbps (one lane of XAUI conforming per 802.3, part 4, clause 47: 10 Gigabit Attachment Unit Interface (XAUI)) full duplex
  - 2.5 Gbps full duplex, 1 Gbps full duplex, 100 Mbps full/half duplex, and 10 Mbps full/half duplex are supported
  - Support connecting to an external MAC at 1 Gbps full duplex or 2.5 Gbps full duplex
  - Support connecting to an external 1000BASE-T Ethernet PHY
  - Support connecting to an external 1000BASE-X (Fiber or Copper) Ethernet PHY
  - Support operation mode with auto-negotiation and without auto-negotiation
  - EEE LPI Encoding is not supported

3.6.2 Functional Description

3.6.2.1 Typical Applications

This section introduces and suggests typical applications of the GSW140 with SGMII interface.

3.6.2.1.1 Interface to an External MAC

It is GMII-replacement mode. It serves to primarily reduce the pin count of the interfaces between two MACs by replacing the signals with a 4-wire (2 pairs) differential connection. In this mode, auto-negotiation is disabled. The baud rate (1.25 Gbaud/s or 3.125 Gbaud/s), the bit rate (1 Gbps or 2.5 Gbps), pause support capability are preconfigured and must be known and same to both sides of the SGMII interface in advance. The link status is always on and in full duplex mode.

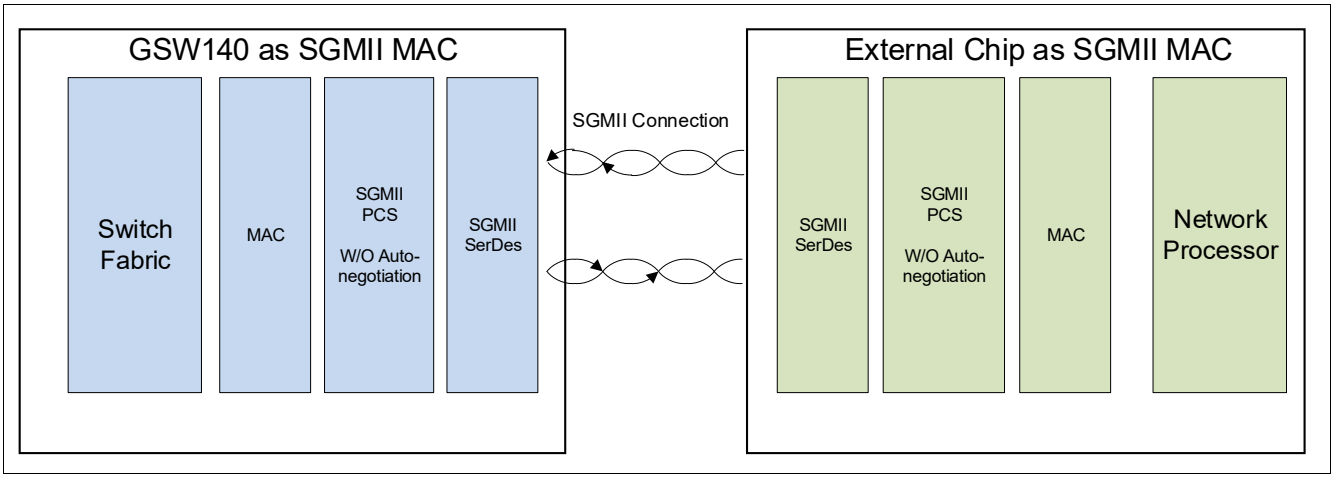


Figure 22 Interface to an External MAC

3.6.2.1.2 Interface to an External 1000BASE-T Ethernet PHY

Known as the SGMII mode, this mode follows the Cisco* Serial-GMII Specification 1.8. It serves to primarily reduce the pin count of the interface between a switch and PHY by replacing the signals with a 4-wire (2 pair) differential connection. Instead of transmitting the capability advertisement information as defined in IEEE 802.3 Clause 37, in this mode, the PHY sends over the control register value, and the MAC side macro acknowledges this. With this done, normal data transmission can commence. It is to be noted that the baud rate of the line in not negotiated (always 1.25 Gbaud/s), this is pre-fixed and known to both sides in advance. But the bit rate (10/100/1000 Mbps), duplex mode, link status and pause capability can be changed via auto-negotiation.

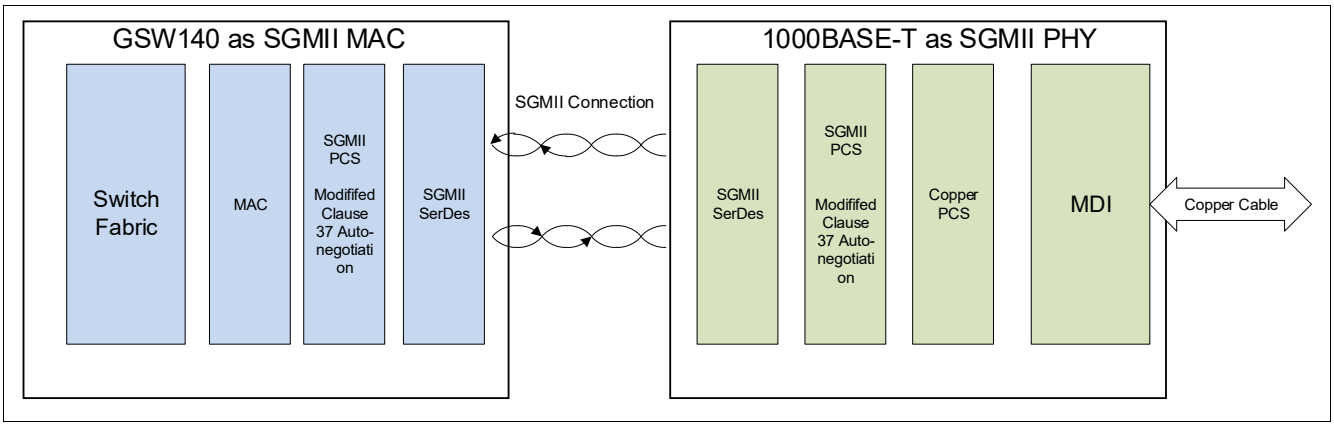


Figure 23 Interface to an External 1000BASE-T Copper Gigabit Ethernet PHY

3.6.2.1.3 Interface to an External 1000BASE-X Ethernet PHY

In this scenario, the MAC-connected SGMII IP is connected to an optical SFP transceiver over a 1000BASE-X link. The optical PHY is assumed to be merely translating the electrical signals to optical and transmitting them over an optical fibre. In this application, the SGMII PCS in GSW140 works according to the clauses 36 and 37 in the IEEE 802.3 standard, conducting full-blown auto-negotiation for the link. It acts as a PCS for the optical PHY, with all capabilities as required by the standard. External 1000BASE-T Copper Ethernet PHY with an 1000BASE-X interface can also be connected to GSW140 in this manner.

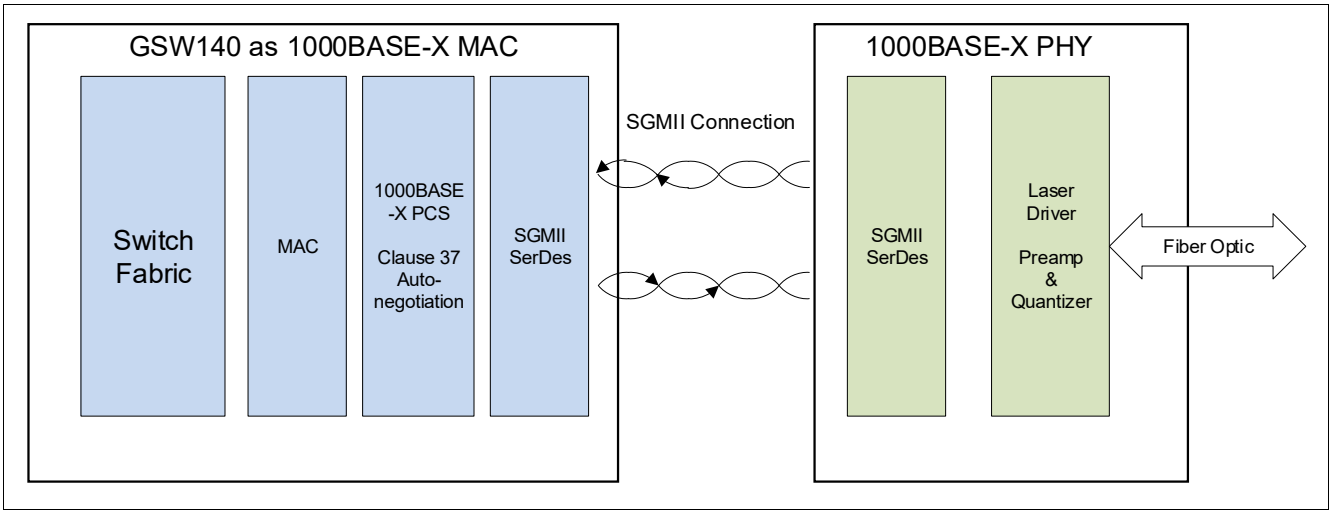


Figure 24 Interface to an External 1000BASE-X Ethernet PHY

3.6.2.2 Modes of Operation

The two basic operating modes are the SGMII mode and 1000BASE-X mode. In the former, it acts as GMII replacement, and does a minimum of link configuration operations before data transfer can commence. In the 1000BASE-X mode, full-fledged auto-negotiation including next page operation is supported.

In addition, **Table 25** lists the macro that can be operated in various different bit rates.

Table 25 Bit Rates

Application	PCS Mode	Auto-Negotiation Mode	Baud Rate at Line	Bit Rate Duplex	Data Repeat	Link Info
Interface to an External MAC	Don't Care	Disable	1.25 Gbaud/s	1 Gbps Full Duplex	1	Link info (bit rate and pause capability, link status) are known and preconfigured at both side.
			3.125 Gbaud/s	2.5 Gbps Full Duplex	1	
Interface to an External 1000BASE-T Ethernet PHY	SGMII	Enable	1.25 Gbaud/s	10 Mbps Full/half Duplex	100	Link info (bit rate, duplex mode, pause capability and link status) are auto-negotiated.
				100 Mbps Full/half Duplex	10	
				1 Gbps Full Duplex	1	
Interface to an External 1000BASE-X Ethernet PHY	1000BASE-X	Enable	1.25 Gbaud/s	1 Gbps Full Duplex	1	Link info (pause capability and link status) are auto-negotiated.

For SGMII mode, for bit rates of 1 Gbps or less, each data symbol is repeated 10 or 100 times as required by the SGMII specification, to arrive at the baud rate of 1.25 Gbps. The 8b10b coding scheme ensures that there are enough transitions for the clock recovery mechanism in the PMD to operate smoothly. To achieve this the bit rate is increased the bit rate by 25%.

3.6.2.3 Test Features, Status and Enabling

The GSW140 has several loops to aid system debugging, as shown in **Figure 25**.

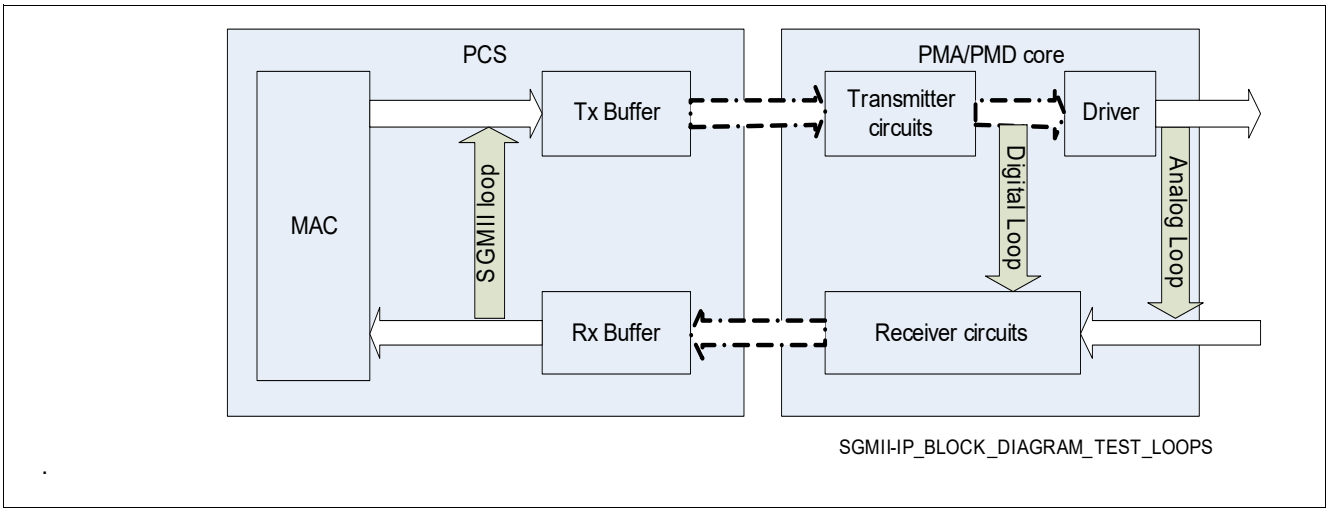


Figure 25 Test Loops in the GSW140

3.6.2.3.1 PMA/PMD Loops

The PMA/PMD core provides two loops internal to itself, both of which loops the data from the transmit path to receive path, as shown in **Figure 25**,

1. Digital Loop: Digital serial data loopback from transmit to receive. It takes data from the transmit path just before the analog drivers, and inserts into the receive path just after the first stage.
2. Analog Loop: Analog signals are looped back from transmit to receive path. Here the entire circuits of both the transmit and receive paths are activated. However, this test cannot be done on packaged devices due to loading effect of parasitic capacitances. This is meant for wafer level testing only.

The above loops are activated by register bits.

3.6.2.3.2 PCS Loops

In addition to above test mode, the logic external to the PMA/PMD core provides a loop as shown in **Figure 25** called SGMII Loop. This loops data from receive buffer output to transmit buffer input. This is activated by LPB bit in the SGMII_PCS_CFG register. This loop enables returning of data coming in from the analog interface back to itself.

3.7 Switch Fabric Functional Description

3.7.1 Overview

The Gigabit Ethernet Switch Macro is responsible for classifying, storing and forwarding multiple data flows. The macro consists of storage buffer, packet queueing and packet classification units. Ingress data can be received on one of the port interfaces, classified and placed in the appropriate QoS queue in the Shared Buffer. Ingress policing and access control rules are applied to the received traffic and packets not compliant to the rules are discarded. Prior to packet being fetched from the shared memory and transmitted on one of the egress ports, it is subject to egress scheduling and rate shaping.

Figure 26 describes a typical packet data flow through various stages of switch.

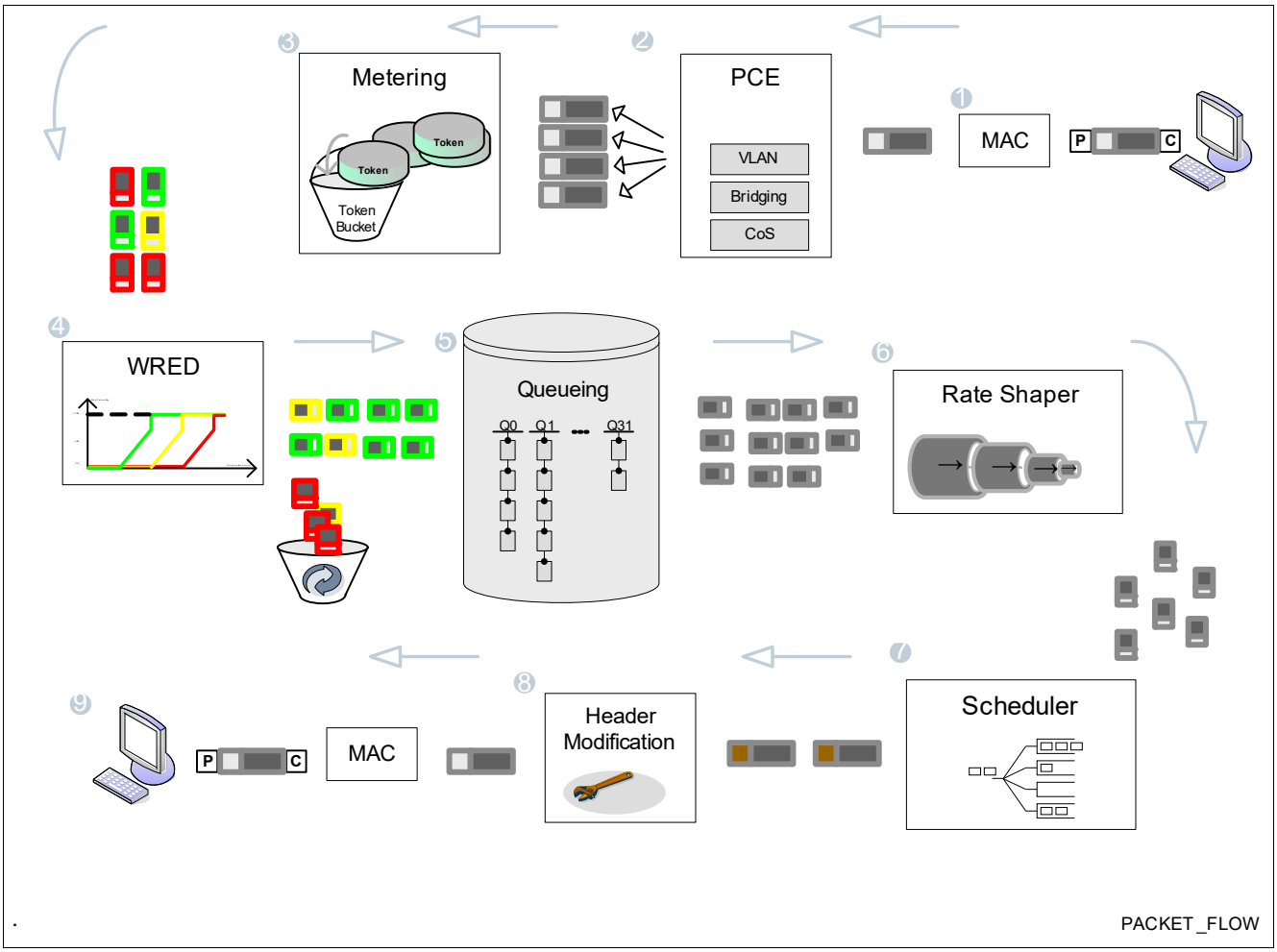


Figure 26 Packet Flow Diagram

Packet received on the ingress port is stripped from the Ethernet Preamble and checked for correct FCS. In case of any reception errors the packet might be discarded. Received packet is classified in the Packet Classification Engine and assigned to an appropriate QoS queue. Prior to accepting the packet to certain queue it is subject to metering and WRED functions. Packets marked as non-conforming by the Metering Engine might be discarded by the WRED algorithm based on the configurable drop precedence. Prior to transmission on the egress side, the packet is subject to Rate Shaping. When transmission of the packet is not delayed by the Rate Shaper it is subject to the Scheduling algorithm (WFQ or SP). Packets scheduled for transmission are subject to Header Modification, such as, VLAN Tag modification or DSCP remarking.

3.7.2 Ethernet Bridging

Ethernet bridging (or Switching) is the primary task of the Gigabit Ethernet Switch Macro. The frames received on one of the ingress ports must be forwarded to the appropriate destination port. The destination port is determined by a lookup in the MAC bridging table. The MAC bridging table can be populated by software (static entries) or entries can automatically be learned by the hardware learning function. The entries learned by the hardware can age out after a configurable time and are deleted from the MAC bridging table.

3.7.2.1 Parsing

The Gigabit Ethernet Switch Macro features a Parser realized as a microcoded engine. This allows a flexible adaptation to any future protocol changes. The parser microcode evaluates the frame header and is capable of extracting all relevant information up to the layer 4 protocol from the frame. The microcode must be loaded otherwise only the MAC destination and MAC source address is extracted from the frame. The parsed fields are:

- MAC source and destination address (also available without loading the parser microcode)
- Special tag
- Ethernet type field
- Service VLAN tag (VLAN ID, DEI/CFI and PCP)
- Customer VLAN Tag (VLAN ID, CFI and PCP)
- PPPoE Session ID (for PPPoE frames)
- DSCP/TOS/Traffic Class (for IPv4/IPv6 packets)
- IP Protocol/Next Header (for IPv4/IPv6 packets)
- IPv4/IPv6 source and destination address (for IPv4/IPv6 packets)
- Application, typically L4 source and destination port (for UDP and TCP)
- Flags (IP version, WOL Packet Flag, Parser Error Flag, Length Encapsulated Packet Flag, IP Short Option Flag, IP Long Option Flag)

A packet is also parsed when it was received encapsulated in a PPPoE frame. The parsing considers Zero or One Service tag, any number of customer VLAN tags and any number of extension headers, the parsing continues as long as the parsing depth (256 bytes) is not exceeded. When the Ethernet type field is not IPv4, IPv6 or PPPoE and IP protocol/next header is not UDP or TCP, the parsing is finished and the next four bytes are stored as application field. This allows to set up rules for unknown protocols.

Note: The outer customer VLAN tag is extracted by locking the register after the first customer VLAN tag is detected, the following customer VLAN tags cannot overwrite the value.
Parsing is not continued for length encapsulated frames.

3.7.2.2 MAC Bridging Table

The MAC bridging table is realized as a hash table with four collision buckets and holds the lookup key (MAC address, FID), control information (static indication, aging timer, changed indication) and the result (port or port map, MAC VLAN ID). A port map is a bitmap where each bit represents a single port. The port map allows to send the frame to multiple destination ports and is available for static entries only.

The Gigabit Ethernet Switch Macro supports shared and independent VLAN learning (SVL or IVL). It is achieved by mapping the default customer VLAN ID or a flow to a forwarding identifier (FID) used as part of the lookup key, together with the MAC address, for the MAC bridging table lookup. By default, FID is zero and all entries belong to shared VLAN learning. See **Shared/Independent VLAN Learning** for details on VLAN learning modes.

The Gigabit Ethernet Switch Macro supports MAC based VLAN. For example, it offers the possibility to extend the number of interfaces behind the same physical Ethernet port. The MAC VLAN ID represents a single sub-interface or a group of sub-interfaces behind a port. This is achieved by learning the MAC VLAN ID (shortened as MVID in this document) together with port ID. The MAC VLAN ID is carried via the Service VLAN Tag.
Entries are entered automatically by hardware (dynamic MAC address learning, described in **Dynamic Source MAC Address Learning and Aging**) or entered by software via manual learning. The software writes static entries into the MAC bridge table but it is also possible to write dynamic entries which are subject to aging.

The MAC bridge table is able to hold unicast, multicast or broadcast addresses. The table entries containing multiple egress ports as a destination, are entered only as static entries, by appropriate management action.

The MAC table is accessed by software to read out static or dynamically learned entries and optionally modify them. The following access modes are supported. For each access, a 12-bit MAC table pointer is returned.

- By KEY: MAC address and FID.
- By a 12-bit MAC table pointer
- By reading next valid entry
- By reading next changed entry. The changed entry is the entry added, updated or removed (invalidated) after the last read.

Note: Due to the table 4-bucket hash architecture, some MAC addresses may be rejected while others may still be added.

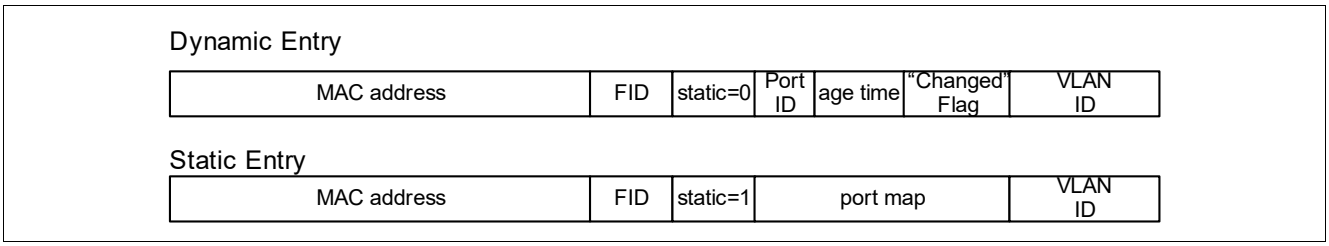


Figure 27 MAC Bridge Table Entry Formats

Bridging Table Flushing

When all learned entries must be removed, the complete MAC bridging table can be cleared by hardware automatically, with the help of an automated flushing function. This function removes all entries, static as well as dynamic ones. The flush function is triggered by writing 1_B to MTFL bit in PCE_PCTRL_0.

3.7.2.3 MAC Based Forwarding

For each frame the MAC destination address and the FID form, a lookup key is used to determine the destination port (or port map) and MAC VLAN ID. The lookup key is hashed and the hash index is used to address the MAC bridging table and read out the contents of the four buckets. The result of the lookup is an egress port (or multiple ports in case of a multicast entry) and MAC VLAN ID. In case the egress port or port map is programmed to all-zero, the frame is discarded.

Default Forwarding

When no match for the destination MAC address + FID pair is found in the Bridging table, the default port map is used. A default port map is configured for L2 unicast (via PCE_PMAP_3) and L2 multicast/broadcast (via PCE_PMAP_2) addresses separately. After reset, unknown destinations are flooded to all egress ports. MAC VLAN ID is “NULL” (all 0) for unknown unicast, unknown multicast and broadcast.

3.7.2.4 Dynamic Source MAC Address Learning and Aging

The MAC bridging table is populated automatically when learning is enabled on the ingress port. The lookup key (concatenation of the source MAC address and the FID) is hashed and the index is used to address the MAC bridging table.

Dynamic learning operates in the following way:

- **Match Found:** When the entry is found and the PortID+MVID association with SA+FID is unchanged, the entry aging timer is refreshed. When the entry contains a different port number or different MVID, the old PortID + MVID in the entry is replaced by the new PortID+MVID.
  Note: Static entries are not modified by dynamic learning function. When the matched entry is static, the association is not changed.

- **No Match - Table not full:** When the SA+FID pair is not found in any of the collision buckets and an empty bucket exists for this hash index, the lookup key is stored together with the PortID+MVID pair and the aging timer is refreshed.
- **No Match - Table full:** When the SA+FID pair is not found and there are no available entries (i.e. all collision buckets are full) and LRU mode (Least Recently Used) of the switch is enabled, the oldest entry (lowest age time) is replaced by the new lookup key and new PortID+MVID pair. When the LRU mode is disabled, no entry is overwritten and the source MAC address is not learned.
- **No Match - All static:** When the SA+FID pair is not found and all the collision buckets for this hash index are occupied by static entries, no entry is overwritten and the source MAC address is not learned.

The dynamic learning of SA+FID pair is performed only when all of the following conditions are fulfilled.

- The source MAC address is a unicast address.
- Learning is enabled on the ingress port.
- The frame discarded by the filtering function is not due to ingress reasons (e.g., VLAN filtering, Flow Classification filtering).
  – See **Flow Classification Function** for details.
- The bridging table is not full or table is full but overwriting existing entry is allowed.
- The number of entries for the port does not exceed the learning limit when MAC learning limitation is enabled. See **MAC Learning Limitation** for more details.
- The ingress PortID+MVID is identical to the stored PortID+MVID pair in the MAC bridge table when stored port MAC port locking is not enabled and the receiving port MAC spoofing is not disabled. See **MAC Port Locking and MAC Port Spoofing Detection** for more details.

When a packet SA+FID pair is new or its association with the PortID+MVID pair is changed, the packet can be mirrored to the monitoring port. This feature is switched on or off (default) via configuration (VIO_9 bit in PCE_PCTRL_3) per ingress port.

MAC Address Aging

To avoid table overflow over time, the entries learned must be removed once they have not been used for a certain amount of time. This functionality is covered by the aging process, which removes bridging table entries after a configurable time of inactivity (age time). The range of the age time reaches from 1 s up to more than 24 hours. A typical value of 300 s is used by default. Static entries do not age out, they must be deleted by software. The aging is enabled or disabled per ingress port. When disabled, addresses learned from this port are not aged out.

Shared/Independent VLAN Learning

When the VLAN function is used, each VLAN group is mapped to the Filtering Identifier (FID). Single or multiple VLAN groups are assigned to the same or to different FIDs. VLANs assigned to the same FID perform SVL. VLANs assigned to different FIDs perform IVL. The source MAC address of the received frame is learned using either the IVL or SVL method. Shared and independent VLAN learning is defined as follows:

- **Independent VLAN Learning**
  Each VLAN uses its own filtering database. The source MAC address learning is performed as a result of incoming VLAN traffic and is not made available to any other VLAN for forwarding purposes. One FID is assigned per VLAN group.
- **Shared VLAN Learning**
  Two or more VLANs are grouped to share common source MAC address information. This setting is useful for configuring complex VLAN traffic patterns without forcing the switch to flood the unicast traffic in each direction. Addressing information is shared among VLANs. One FID is used by two or more VLAN groups.

By default, all VLAN groups are assigned to the same FID (FID=0) and Shared VLAN Learning is performed for the source MAC addresses.

3.7.2.5 Layer 2 Security

This section summarizes the L2 security features of the GSWIP. The L2 security features comprise:

- IEEE 802.1X
- MAC Learning Limitation, allows only a limited number of MAC addresses to be learned on a port.
- MAC Port Locking and MAC Spoofing Detection, allows only frames with a previously learned MAC and PortID association.
- MAC Table Freeze, allows only frames with previously learned MAC addresses.
- Source MAC Address Filtering and Destination MAC Address Filtering, filters user defined MAC addresses.

IEEE 802.1X (Port-based Authorization) Support

Gigabit Ethernet Switch Macro supports the port states required for the 802.1X - Port Based Authorization and Network Access Control Protocol functionality. The following states are supported per port:

- Not Authorized. In this state, all frames received on the port are dropped, the source MAC address is not learned. Not authorized port is not taken as a destination for any frame received on another port.
  – EAPOL frames can ignore the port state and be received and forwarded to the original destination.
- Authorized for Ingress Traffic only. In this state, all regular traffic received on the port is accepted. However, the port is not allowed to transmit any traffic. This port is not taken as a destination for any frame received on another port.
  – EAPOL frames can ignore the port state and be received and forwarded to the original destination.
- Authorized for Egress Traffic only. In this state, all regular traffic received on the port is discarded. The port is allowed only to transmit traffic. This port can be taken as a destination for any frame received on another port.
  – EAPOL frames can ignore the port state and be received and forwarded to the original destination.
- Authorized. Normal operation, ingress and egress traffic on this port is enabled for all frames.

When both protocols, STP and IEEE 802.1X, are enabled - port states for the 802.1X are effective only when STP port state is set to Forwarding.

EAPOL frames forwarding

The Gigabit Ethernet Switch Macro supports special forwarding rules for the Extensible Authentication Protocol over LAN (EAPOL) frames used by the 802.1X protocol to exchange authentication information. EAPOL frames are identified by the unique group destination MAC address $01:80:C2:00:00:03_H$, and the Ethernet Type $88\ 8E_H$.

When the 802.1X functionality is enabled, the EAPOL frame forwarding is added as a dedicated rule to the Traffic Flow Table with a special action to ignore (cross) any states configured for the ingress or egress ports. The EAPOL frames must be forwarded to the defined CPU port or any other port where managing entity is connected for further 802.1X processing.

MAC Learning Disable

The MAC learning is disabled (via LNDIS bit in PCE_PCTRL_3) per ingress port. When MAC learning is disabled, the source MAC address is not learned and MAC learning limitation is not checked.

MAC Learning Limitation

The number of MAC addresses allowed to be learned are limited per port. This feature provides protection from DoS attacks and avoids bridging table overflow by single ports sending too many frames with different source MAC addresses.
By default, the number of MAC addresses learned by the switch is only limited by the size of the internal MAC bridging table. When MAC learning limitation is enabled on the ingress port and the programmed limit is reached, no more addresses are learned for this specific port. Dynamic learning is still enabled on other ports. The learning limitation violation is indicated to the software and the violating frame is configured to be discarded or forwarded as a normal frame. Regardless of the forwarding action, the source MAC address of the violating frame is not learned. Refreshing of already stored addresses is allowed and not considered a violation.

The learning limitation configuration may be changed (increased or decreased) during run-time. When number of addresses that can be learned on the port increased from the previous limit, more addresses from that port may now be added to the table. When the number of addresses that can be learned on the port decreased, no new addresses are learned and no active flushing is performed to reach the learning limitation. Addresses are expected to be aged out.

Note: The setting learning limitation to zero disables the dynamic learning on that port, the source MAC address is looked up and violating frame can be configured to be discarded or forwarded.

Table 26 describes the MAC learning disable, MAC learning limitation and corresponding behavior.

Table 26 MAC Learning Disable and MAC Learning Limitation Description

LNDIS in PCE_PCTRL_3 (per ingress port)	LRNLIM in PCE_PCTRL_1 (per ingress port)	PLIMMOD in PCE_GCTRL_0 (global)	Description
1_B	Don't care	Don't care	Source MAC address is not learned, the packets are not dropped
0_B	!= 255	0_B	Source MAC address is not learned and packets are dropped when learning limitation is exceeded. Source MAC address is learned and packets are not dropped when learning limitation is not exceeded.
0_B	!= 255	1_B	Source MAC address is not learned and packets are not dropped when learning limitation is exceeded. Source MAC address is learned and packets are not dropped when learning limitation is not exceeded.
0_B	255	Don't care	Source MAC address is learned and packets are not dropped.

MAC Port Locking and MAC Port Spoofing Detection

The port locking and spoofing detection function are intended to prohibit MAC spoofing attacks.

Ingress traffic from a port carrying a source MAC address that has previously been learned on a different port (port locking enabled on the stored port) is considered a violation. When a port locking violation is detected, this can be indicated to the software and the violating frame can be configured to be discarded. Regardless of the forwarding action, source MAC address of the violating frame is not learned.

Ingress traffic from the port on which port spoofing detection is enabled (via SPFDIS bit in PCE_PCTRL_0) carrying a source MAC address that has previously been learned on a different port (regardless of its port locking setting) is considered a violation. When port spoofing is detected, this can be indicated to the software and the violating frame can be configured to be discarded (via SPFMOD bit in PCE_GCTRL_1). Regardless of the forwarding action, source MAC address of the violating frame is not learned. MAC Port Spoofing detection function allows moving a MAC addresses to the port on which spoofing detection is disabled.

This feature ensures that a malicious user cannot spoof another user MAC address and gain illegitimate access to data traffic that he does not own.

When a user must change from one port to another, a wait time up to the configured aging time is required to be able to re-connect. When the locked MAC address is a static entry or when the aging time is too long, moving users between ports on which spoofing detection are enabled or port locking are enabled requires management interaction.

MAC Table Freeze

MAC Table Freeze can be enabled globally to freeze the MAC address table. When enabled no new entries can be entered into the MAC address table even when learning is enabled on the port. Refreshing of existing entries is performed, also when learning is disabled (by setting learning limitation to zero). This features allows to learn the MAC addresses from the connected stations for a given time and then freeze the MAC address table. Afterwards no new MAC addresses are learned. When learning is enabled and port locking is disabled, known stations are allowed to move. When port locking is enabled or learning is disabled, station moves are not allowed.

When a freeze violation is detected it can be configured to either discard the frame or to forward the frame. When the frame is to be discarded it can be configured to send it to the monitoring port. The freeze violation can be indicated to the software via a maskable interrupt.

Source MAC Address Filtering

A static MAC Table entry for specific source MAC address + FID pair can be programmed with a NULL (all-zero) value for the associated port map. When the source MAC address + FID pair of the received frame matches the configured entry, the frame is discarded. This function can be enabled or disabled per port.

Dedicated violation indication is asserted for any frame that has been discarded.

3.7.2.6 Spanning Tree Protocol Support

Gigabit Ethernet Switch Macro supports the port states required for the Spanning Tree Protocol (STP) functionality. 16 spanning tree instances per port are supported. Each Spanning Tree instance is associated with least significant 4 bits of the Filtering Identifier (FID) and a port. The port state programmed for one FID does not have effect on the behavior of another FID of the same port.The following states are supported per STP instance:

- **Disabled:** When disabled, all ingress frames are dropped, the source MAC address is not learned. All egress frames are discarded.
- **Blocking/Listening:** In this state, all ingress and egress regular traffic is discarded. BPDU frames can ignore the port state and be forwarded to the STP managing entity. Source MAC address is not learned in this state. *Note: To be recognized by the switch, BPDU frames must be defined in the appropriate rule in Traffic Flow table.*
- **Learning:** In this state, all ingress and egress regular traffic is discarded. Source MAC address is learned in this state. BPDU frames can ignore the port state and be forwarded to the STP managing entity. *Note: To be recognized by the switch, BPDU frames must be defined in the appropriate rule in Traffic Flow table.*
- **Forwarding:** Normal operation, ingress and egress traffic is enabled for all frames.

BPDU frames forwarding

Gigabit Ethernet Switch Macro supports special forwarding rules for the Bridge Protocol Data Unit (BPDU) frames used by the STP protocol to exchange information about bridge IDs and root path costs. BPDU frames identified by the unique group destination MAC address $01:80:C2:00:00:00_H$.

When STP functionality is enabled, BPDU frame forwarding is added as a dedicated rule to the Traffic Flow Table with a special action to ignore (cross) any states configured for the ingress or egress ports. BPDU frames must be forwarded to the defined CPU port or any other port where managing entity is connected for further STP processing.

3.7.2.7 Reserved MAC Addresses

The IEEE standard defines group destination MAC addresses in the range from $01:80:C2:00:00:00_H$ to $01:80:C2:00:00:FF_H$ as reserved. The Gigabit Ethernet Switch Macro can be configured to disable the forwarding of the frames containing reserved addresses. In this case a dedicated rule is added to the Traffic Flow Table with an action to discard any frame within the reserved address range.

3.7.2.8 Flow Control Function

To prevent buffer congestion and packet drop the Gigabit Ethernet Switch Macro supports a flow control mechanism. In full duplex operation the sender is notified to start or stop the transmission via a PAUSE frame based on the IEEE 802.3x standard. The Gigabit Ethernet Switch Macro is able to transmit/receive and react accordingly to 802.3x flow control frames. In half duplex operation, the Gigabit Ethernet Switch Macro supports a back pressure mechanism, specifically, a jam pattern is transmitted on the port forcing a collision. Flow control can be enabled or disabled per port. When enabled, it depends on the auto-negotiation result of the attached PHY.

Flow control is applied in the following ways.

When flow control on a port is activated by any one of the following triggerings, flow control is activated on that port.

When flow control on a port is deactivated by all the following triggerings, flow control is deactivated on that port.

- **Global flow control:** Flow control is activated when the global buffer congestion level exceeds a programmable global threshold and is deactivated when the global buffer congestion level is below a programmable global threshold. The flow control applies to all enabled ports.
- **Ingress port congestion based flow control:** Flow control is activated when the ingress port local buffer congestion level exceeds a programmable local threshold (via SDMA_PFCTHR9) and deactivated when the local buffer congestion level drops below a programmable local threshold (via SDMA_PFCTHR8). The flow control applies to each port individually.
- **Ingress port metering based flow control:** When the global buffer filling level exceeds a programmable global threshold (via SDMA_FCTHR2), flow control is activated on the port that exceed the configured ingress rate. When the global buffer filling level drops blow a programmable threshold (via SDMA_FCTHR1) or the traffic rate is reduced below the configured rate, flow control is deactivated on the port. See **Rate Metering** for details regarding the metering based flow control and metering assignment.

3.7.2.9 Port Trunking Functions

Switch supports link aggregation according to IEEE 802.3ad. Link aggregation, also called port trunking, allows to combine multiple ports to a trunk for high bandwidth inter-switch links. A maximum of two ports form a trunk, there is no restriction on the port sequence used for the trunk (port 0 and port 1 may form a trunk but also port 0 and port 5 may form a trunk). The ports must have the same speed and must work in full duplex mode only, otherwise a proper trunking functionality cannot be achieved. Fault tolerance is not supported. When one link is broken or disabled for any reason (link on/off), packets are lost.

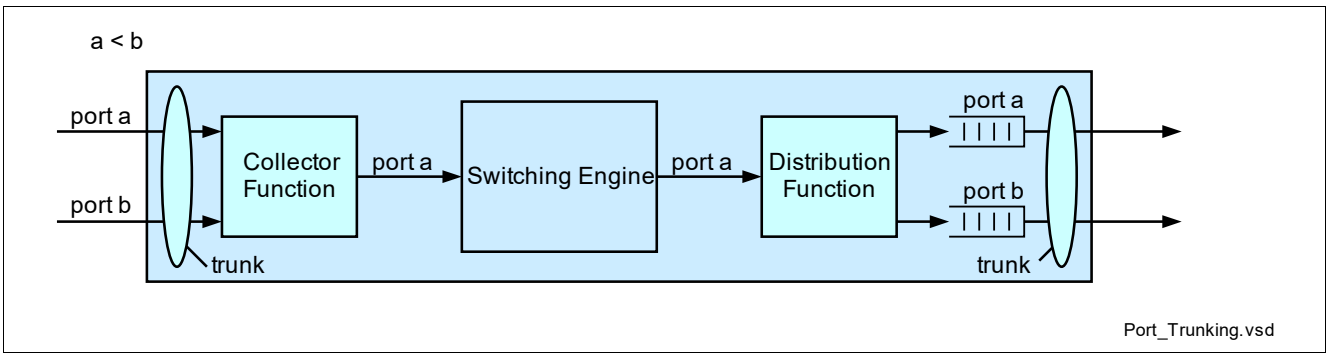


Figure 28 Port Trunking Function

When a frame was received on a trunk, the lowest port number of the trunk is used as ingress port by the collector function. This ingress port alone is used for the further processing, including learning and port security. The other port number (=higher port number of the trunk) is not used, all port parameters are taken from the lowest port number.

When a frame is to be transmitted on a trunk, the lowest port number of the trunk is the default port. Since the trunk consists of two ports it must be determined which of the ports is used for the transmission. This is done by a distribution function which evenly distributes the frames on the two ports of the trunk.

The distribution is according to either a hash function of 32-bit key (XOR of all bits) or a Flow classification action.

The hash key consists of the following fields.

- MAC Destination Address (MAC_DA): 8 bit only (MAC_DA[7:0]), can be masked via DA bit in PCE_TRUNK_CONF
- MAC Source Address (MAC_SA): 8 bit only (MAC_SA[7:0]), can be masked via SA bit in PCE_TRUNK_CONF
- IP Destination Address (IP_DA): 8 bit only, (IP_DA[7:0]), can be masked via DIP bit in PCE_TRUNK_CONF
- IP Source Address (IP_DA): 8 bit only, (IP_SA[7:0]), can be masked via SIP bit in PCE_TRUNK_CONF

When a field is masked, all zero value is assumed for that field for hash calculation. When a packet is not an IP packet, all zero value is assumed for IP address.

The higher port number of a trunk must not be configured as destination port or in a destination port map.

When a link in a trunk goes down, the link is no longer used in the distribution function and the partner link gets all the frames. The egress queue of the disabled port is flushed.

When a link changes the speed we treat the port which has the lower speed same as link down.

The RMON counters must be triggered for each ingress and egress port separately.

Flow control is also separately triggered for each ingress port. Each egress port can be shaped individually. The combined rate shaping of the trunk is also supported.

3.7.2.10 Gigabit Media Access Control (GMAC) Functions

GMAC modules are part of the Gigabit Ethernet Switch Macro and provide the following functions:

- Duplex Modes
  - Each MAC module interface can work in full- or half-duplex mode at any of the provided speeds. The duplex mode can be configured via auto-negotiation (autopolling) or forced by register settings
- Preamble Generation
  - For each Ethernet frame, the MAC generates a preamble and at the Start of Frame Delimiter (SFD). During the generation of preamble and SFD, the pending data is delayed. In receive direction, the preamble and SFD are removed
- FCS Generation and Checking
  - The Frame Checksum (FCS) is a 32-bit CRC checksum that covers the destination address, source address, type field, and the payload data. The FCS of each frame is checked in receive direction and is regenerated in transmit direction. The generation of the FCS for an outgoing frame and the check of the FCS for an incoming frame can be disabled per port.
- Full Duplex Flow Control
  - In case the pause frame based flow control is enabled, the MAC generates a pause frame when a congestion situation is signaled. When this situation occurs while the MAC sends a normal frame, the MAC finishes the current transmission and then sends a pause packet. When the congestion situation ends, the MAC finishes the pending transmission and then sends a pause termination packet. The source address of the pause frames is configurable per switch port. A pause frame is identified by a type/length field of 88 08_H. The following two bytes provide the opcode field. For pause operation the opcode is 0001_H. The next two bytes specify the pause length. The pause length is always set to the maximum value of $FFFF_H$, which instructs the link partner to seize transmission for 65535_D slot times. To terminate the pause state, a pause frame with a pause time of 0000_H is sent, allowing the link partner to resume data transmission. Each time the pause state exceeds the length of $65535_D/4 = 16384_D$ slot times, another pause frame is sent automatically to maintain the pause state.
  - Destination MAC address of the pause frame is 01 80 C2 00 00 01_H.
  - The default source MAC address of the pause frame is AC 9A 96 00 00 00_H. This can be changed by configuration.
- Half Duplex Flow Control
  - The flow control in half-duplex mode uses the back-pressure collision mechanism to take control over the media. When a congestion situation is signaled, the received frame is collided and MAC tries to occupy the

line with a egress frame transmission or a special back pressure pattern (in case no data pending for this port). When the congestion situation ends, the MAC resumes normal operation.

- Frame Padding
  - The minimum frame size of an untagged Ethernet frame is 64 byte. The MAC fills all Ethernet egress frames with padding bytes until the minimum frame size requirement is fulfilled. The minimum size is 68 byte for tagged frames (containing a single VLAN tag) and 72 byte for stacked frames (containing two VLAN tags). Frame padding can optionally be disabled for untagged, single or stacked frames separately.
- Jumbo Frame Support
  - The maximum frame size is configurable to support jumbo frames of 9K bytes and below.
- Energy-Efficient Ethernet Functions
  - For power saving purposes, the Low Power Idle (LPI) mode is supported as defined by IEEE 802.3az.
  - Recording of accumulated LPI state time period is supported. A 32-bit counter (accessible va MAC_LPITMER0 and MAC_LPITMER1) which counts the period during which the LPI idle state is maintained per port. The unit of the counter is 1 us. It is configurable to count one of the LPI state: RX LPI idle state, TX LPI idle state or both TX and RX in idle state.
- IFG Handling
  - The interframe gap (IFG) can be configured in receive and transmit direction. This allows the acceptance of frames with a short IFG of min. 8-bit times. It is possible to transmit frames with an IFG of 8 to 120 bit times. Typically the IFG is 96 bit times
- The MAC performs several checks on the received frame and signals the following errors. Typically frames with a receive error are discarded but it is also possible to monitor such frames or even ignore the error and process the frame like an error free frame.
  - PHY Error (rx_error)
  - Alignment Error (align_err)
  - Length Error (len_error)
  - Oversized Frame (len_toolong_error)
  - Undersized Frame (len_tooshort_error)
  - FCS Error (crc_error)
  - Pause Frame (pause_frame)

3.7.3 VLAN Functions

This section describes VLAN Bridging functionality.

A VLAN is a Virtual Local Area Network, a grouping of network devices logically segmented by functions or applications without regard to the physical location of the devices. Ports in a VLAN share broadcast traffic and belong to the same broadcast domain. Any traffic in one VLAN is by definition not transmitted outside that VLAN. However, there are exceptions to this general rule which can be configured to cover certain system requirements.

The following sections provide more details regarding the VLAN functionality.

3.7.3.1 VLAN Association

The VLAN classification function associates each packet received on the ingress side with a specific VLAN group. VLAN association can be performed in one of two ways:

- **Implicit VLAN Association**
  The VLAN group is based on packet attributes. When the association is based on the ingress port it is called port-based VLAN. When the association is based on the MAC address, it is called MAC-based VLAN. When the association is based on selected packet header fields (such as Ethernet Type, IP Protocol, IP Address Subnet, MAC Address, etc.), it is called protocol-based VLAN.
- **Explicit VLAN Association**
  The VLAN group information is carried in a VLAN tag in the Ethernet header of the received packet. This association is called tag-based VLAN.

3.7.3.2 VLAN QinQ

IEEE 802.1QinQ is an Ethernet networking standard formally known as IEEE 802.1ad and is an amendment to IEEE standard IEEE 802.1Q-1998. It is for Ethernet frame formats. The technique is also known as provider bridging, stacked VLANs or simply QinQ or Q-in-Q. The idea is to provide, for example, the possibility for customers to run their own VLANs inside service provider's provided VLAN. This way the service provider can just configure one VLAN for the customer and customer can then treat that VLAN as if it was a trunk.

The original 802.1Q specification allows a single VLAN header to be inserted into an Ethernet frame. QinQ allows multiple VLAN headers to be inserted into a single frame.

In this context, a QinQ frame is a frame that has two VLAN 802.1Q headers (double-tagged). A tag stack creates a mechanism for Internet Service Providers to encapsulate customer tagged 802.1Q traffic with service provider tag, the final frame being a QinQ frame.

A STAG (Service VLAN Tag) frame is identified by assignable Protocol Type value (typically $88A8_H$, but programmable) and followed by two bytes of TCI field. TCI field consists of 3-bit Priority Code Point (PCP) field, 1-bit Drop Eligible Indicator (DEI) and 12-bit VLAN Identifier field (VID).

A CTAG (Customer VLAN Tag) frame is identified by an Protocol Type value (typically 8100_H, but programmable) and followed by two bytes of TCI field. TCI field consists of 3-bit Priority Code Point (PCP) field, 1-bit Canonical Format Indicator (CFI) and 12-bit VLAN Identifier field (VID).

3.7.3.3 Supported Frame Format

STAG can be configured to be enabled or disabled per port via STEN bit in PCE_PCTRL_2.

Figure 29 shows the supported frame formats when STAG is enabled on a port.

Figure 30 shows the supported frame formats when STAG is not enabled on a port.

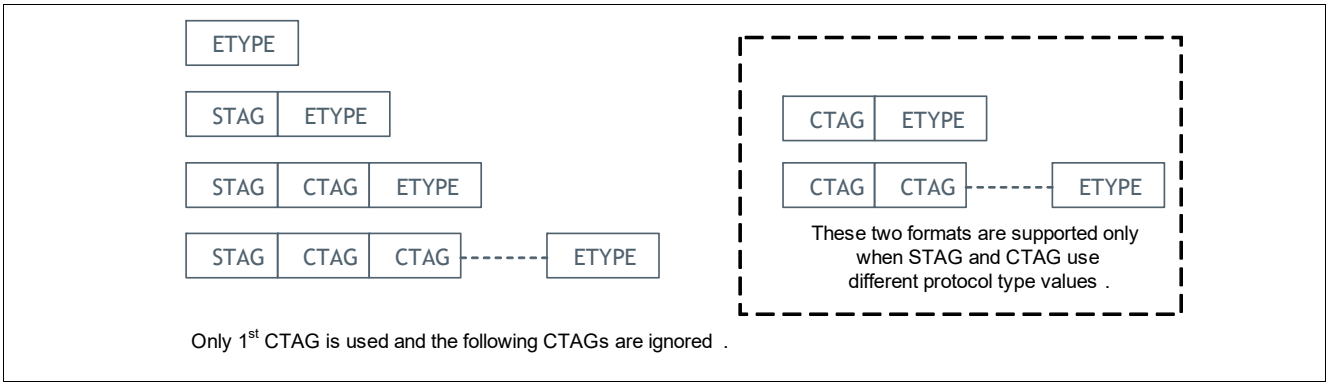


Figure 29 Supported Frame Formats when STAG is enabled

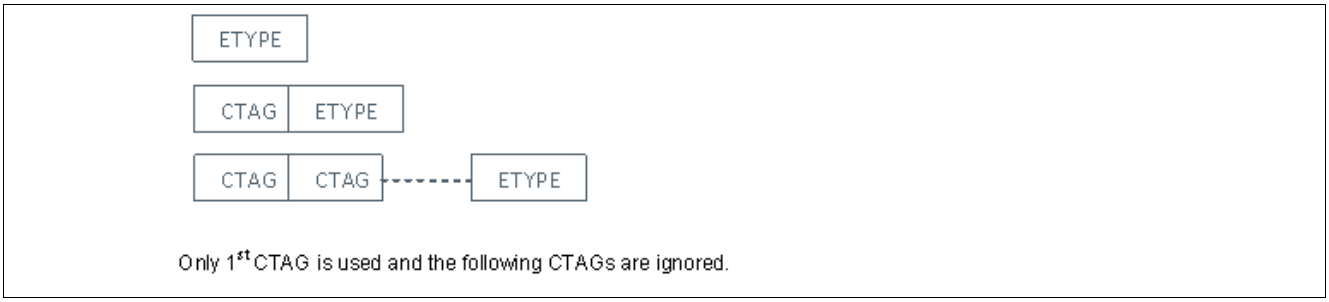


Figure 30 Supported Frame Formats when STAG is disabled

3.7.3.4 Double VLAN Tag Function

Double tag VLAN function is supported. Double VLAN mode is enabled via setting VLANMD bit in PCE_GCTRL_1 to 1_B.

For every packet, there are two VLAN groups: STAG VLAN group and CTAG VLAN group.

STAG VLAN group can determine when CTAG VLAN group is ignored or not.

- When CTAG VLAN group is ignored, then CTAG VLAN is treated as payload, CTAG filtering, CTAG insertion and CTAG removal are not performed.
- When CTAG VLAN group is not ignored, CTAG filtering, CTAG insertion and CTAG removal are performed together with STAG filtering, insertion and removal. Both CTAG filtering and STAG filtering apply on the packet.

3.7.3.5 Filtering Identifier Assignment

Single or multiple VLAN groups can be assigned to the same Filtering Identifier (FID) or to different FIDs. There are the following ways to map the traffic to FID.

- Default customer VLAN ID (either ingress port CTAG VID or ingress CTAG VID)
- Packet multiple fields via the traffic flow classification
  - A packet is associated to an alternative FID based on multiple fields of a packet, for example, ingress port, service VLAN Tag VID, customer VLAN Tag VID, Source MAC, Destination MAC, source IP, destination IP, etc. See **Section 3.7.6** for more details regarding traffic flow classification.

See **Shared/Independent VLAN Learning** for details on the shared/independent VLAN learning functionality.

3.7.3.6 VLAN Filtering

Received frame can be forwarded or discarded based on the VLAN group configuration and configured port attributes. The following sections describe the available filtering modes that can be applied.

CTAG and STAG Ingress Admit Mode

This mode is applied to ports to limit the ingress traffic to a certain profile, with respect to the embedded STAG and CTAG. The following filtering rules are relevant for both STAG and CTAG. There are separate mode configurations for STAG and CTAG. In case of contradiction, the discard rule has higher priority. For example, when according to CTAG filtering the frame is to be discarded and according to STAG filtering is to be admitted, the final rule is to discard the frame:

- Admit VLAN tagged frames only
  Only Ethernet frames that contain a VLAN tag in the Ethernet header are allowed on this port. When a received frame does not contain a VLAN tag, the frame is discarded.
  Note: Priority tag (VID=000_H) is not regarded as a VLAN tag, since it contains no explicit VLAN group. Priority tagged frames are discarded in this mode.
- Admit untagged frames only
  Only packets containing no VLAN tag or containing a priority tag only (VID=000_H) are allowed on this port. When a received frame contains a VLAN tag, the frame is discarded.
- Admit all
  Both tagged and untagged frames are allowed on the port.

The STAG ingress admit mode is configurable via SVINR field in PCE_VCTRL of each port. The CTAG ingress admit mode is configurable via VINR field in PCE_VCTRL of each port.

STAG VLAN Group and CTAG VLAN Group Port Members

The port members identify the group broadcast domain. The broadcast domain of the received packet is restricted according to the VLAN membership ports and is delivered only on ports belonging to the same broadcast domain.

The STAG VLAN group membership is configured via traffic flow classification action for the matched STAG VLAN group association. The CTAG VLAN group membership is configured via CTAG VLAN membership table.

By default, both STAG VLAN filtering and CTAG VLAN filtering apply. In case of contradiction, the discard rule has higher priority. For example, when according to CTAG filtering a port is not in the port member list, and according to STAG filtering the port is in the port member list, the final rule is that the port is not in the port member list. But the STAG VLAN group can determine whether the CTAG VLAN group is ignored or not. This is configured via traffic flow classification action for the matched STAG VLAN group association. When the CTAG VLAN group is ignored, then CTAG VLAN is treated as payload, CTAG filtering is not performed. See **Section 3.7.6** for details regarding traffic flow classification

CTAG and STAG Membership Filtering Mode

This mode enforces packet forwarding based on the port members in the associated VLAN group.

- Ingress Membership Filtering Mode
  The ingress port of the received frame is compared with the port members of the associated VLAN group. When this filtering mode is enabled, the packet is discarded when the ingress port is not contained in the port member list. The ingress membership filtering mode for STAG is configurable via SVIMR field in PCE_VCTRL of each port. The ingress membership filtering mode for CTAG is configurable via VIMR field in PCE_VCTRL of each port.
- Egress Membership Filtering Mode
  The egress membership filtering is the primary VLAN functionality. The egress port of the frame is compared with the port members of the associated VLAN group. When this filtering mode is enabled, the packet is discarded when the egress port is not contained in the port member list. When the frames are destined to multiple ports (multicast or broadcast packets), ports not included in the VLAN member list are excluded from

transmission and a copy of the frame is not delivered to these ports. The egress membership filtering mode for STAG is configurable via SVEMR field in PCE_VCTRL of each port. The ingress membership filtering mode for CTAG is configurable via VEMR field in PCE_VCTRL of each port.

- Ingress and Egress Membership Filtering Mode.
  This mode is a combination of the previous two modes. In this mode, both ingress and egress ports are compared with the port member list of the associated VLAN group.

Cross-VLAN Functionality

The Ethernet frames classified as cross-VLAN ignore any of the VLAN filtering modes for the ingress or egress ports and as such cross the VLAN boundaries.

The cross-VLAN classification is performed as part of the Traffic Flow classification function. See **Section 3.7.6** for details.

3.7.3.7 VLAN Tagging and Untagging

The tag members identify the group of egress ports on which the frame associated with the VLAN group must be transmitted as a VLAN-tagged frame. In this case, the associated VLAN is used for the VLAN ID of the transmitted frame.

STAG VLAN Tagging and Untagging

The ports with STAG VLAN enabled are the tag members of all STAG VLAN group. The STAG can be configured to be enabled or disabled per port via STEN bit in PCE_PCTRL_2.

CTAG VLAN Tagging and Untagging

The tag members is configured per CTAG VLAN group via VLAN membership table. But the STAG VLAN group can determine whether CTAG VLAN group is ignored or not. This is configured via traffic flow classification action for the matched STAG VLAN group association. When CTAG VLAN group is ignored, then CTAG VLAN is treated as payload, CTAG tagging and untagging is not performed and CTAG is not modified. See **Section 3.7.6** for more details regarding to traffic flow classification.

3.7.3.8 Transparent VLAN Mode

A port configured to Transparent VLAN Mode (TVM) ignores the explicit VLAN association and treats all received Ethernet frames as untagged frames, regardless of any existing VLAN tag in the Ethernet header. All tagged and untagged traffic on that port is associated with the port-based VLAN group. When the received packet contains a VLAN tag, this tag is treated as a part of the payload. There is separate transparent mode configuration for CTAG ad STAG.

When STAG transparent mode is enabled, CTAG must be configured to transparent mode too, otherwise the switch's behavior is undefined. STAG transparent mode is configurable via STVM field in PCE_VCTRL of each port. CTAG transparent mode is configurable via TVM field in PCE_PCTRL_0 of each port.

When transparent VLAN mode is enabled, ingress admit mode must be set to "Admit Untagged Frames Only" or "Admit All", since all frames are treated as if they were untagged frames.

VLAN Stacking

When TVM is enabled, the VLAN tag member attribute has a slightly different functionality for tagged frames. When the received frame contains a VLAN tag and the egress port is one of the VLAN tag members, the port-based VLAN is added to the frame as an additional outer tag. When the egress port is not one of the tag members, the packet is transmitted without modification, with the original VLAN tag (if any).

VLAN ID=0 Handling

It is configurable per ingress port when a frame with a VLAN ID=0 (priority tagged frame) must be handled like an untagged frame. When enabled, a priority tagged frame in transparent mode receives a single tag with VID=PVID. When disabled, a priority tagged frame in transparent mode receives a VLAN tag with VID=PVID on top of the priority tag (priority tag is tunneled in the PVID). The PCP of a priority tagged frame is still used even when the frame is handled like an untagged frame. Priority STAG VLAN handling mode is configurable via SVID0 field in PCE_VCTRL of each port. Priority CTAG VLAN handling mode is configurable via VID0 field in PCE_VCTRL of each port.

3.7.3.9 VLAN Security Mode

When the VLAN security mode is enabled on an ingress port, all tagged and untagged traffic on that port is associated with the port-based VLAN group. There are separate mode configuration for STAG and CTAG. The STAG VLAN security mode is configurable via SVSR field in PCE_VCTRL of each port. The CTAG VLAN security mode is configurable via VSR field in PCE_VCTRL of each port.

When the received frame contains a VLAN tag and the egress port is port and tag member of the port-based VLAN group, the port-based VLAN replaces the original VLAN tag in the Ethernet header. When the egress port is port member but not tag member of the port-based VLAN group, the original VLAN tag is stripped prior to transmission. When the frame has been received with more than one VLAN tag, the outer tag is removed.

These are the differences between the TVM and VLAN security mode for tagged packets.

- Egress port is port and tag member of the port-based VLAN
  - Transparent VLAN Mode: The port-based VLAN tag is added in addition to any existing VLAN tag. The number of VLAN tags in the frame is increased by one.
  - VLAN Security Mode: The port-based VLAN tag replaces the existing VLAN tag. The number of VLAN tags in the frame remains the same.
- Egress port is port member but not tag member of the port-based VLAN
  - Transparent VLAN Mode: The frame is transmitted without modification, containing the original VLAN tag. The number of VLAN tags in the frame remains the same.
  - VLAN Security Mode: The original VLAN tag is removed from the frame. The number of VLAN tags in the frame is reduced by one.

3.7.3.10 Reserved VLAN Groups

Any VLAN group in the active VLAN set can be assigned to a reserved VLAN group list by setting the reserved indication in VLAN membership table. The VLAN ID of a frame belonging to a reserved VLAN group can be replaced with the port-based VLAN group. When the frame contains a reserved VLAN tag and the egress port is port member and tag member of the port-based VLAN group, the port-based VLAN ID replaces the original VLAN ID in the Ethernet header.

The difference between VLAN Security and Reserved VLAN functions is that VLAN Security is applied on all traffic received on a certain port whereas Reserved VLAN is applied for a specific VLAN group on a certain port.

This feature applies only to CTAG.

3.7.3.11 VLAN Translation

Frames received with a certain VLAN ID can be modified on the egress and contain a different VLAN ID. The following sections describe the relevant functions related to the VLAN modification.

Note: When applying the VLAN modification, the VLAN membership filtering rules are based on the egress (translated) VLAN group.

STAG VLAN Translation

The egress STAG VLAN ID is one of the following:

- Ingress Port STAG VLAN ID in the following cases
  - Untagged packets
  - Ingress port is in STAG transparent mode
  - Ingress port is in STAG security mode
- Ingress STAG VLAN ID in the following cases
  - Tagged packets when the ingress port is not in transparent mode and not in security mode
- Alternative STAG VLAN ID
  - Alternative STAG VLAN ID is configured via traffic flow classification action for the matched STAG VLAN group association

CTAG VLAN Translation

The egress CTAG VLAN ID is one of the following:

- Ingress Port CTAG VLAN ID in the following cases
  - Untagged packets
  - Ingress port is in CTAG transparent mode
  - Ingress port is in CTAG security mode
  - The ingress CTAG VLAN ID is a reserved VLAN group ID
- Ingress CTAG VLAN ID in the following cases
  - Tagged packets when the ingress port is not in transparent mode, not in security mode and the not reserved VLAN group
- Alternative CTAG VLAN ID
  - Alternative CTAG VLAN ID is configured via traffic flow classification action for the matched CTAG VLAN group association

3.7.3.12 VLAN Priority Code Point

A dedicated Class of Service (CoS) is assigned based on either Service TAG VLAN Priority Code Point (PCP) and Drop Eligibility Indication (DEI) or Customer TAG VLAN Priority Code Point in the received VLAN-tagged frames.

CTAG PCP, STAG PCP and DEI can be regenerated for tagged frames or generated for untagged frames, based on the CoS assigned to that packet.

See **Chapter 3.7.5** for details regarding the CoS assignment and PCP&DEI generation and re-generation.

3.7.3.13 Port Based VLAN Examples

For a port-based VLAN group, the VLAN association is based on the ingress port number.

Every ingress port is configured with a port-based VLAN ID (PVID). The configured PVID must be part of the active VLAN set. Ingress ports configured with the same PVID belong to the same VLAN group. Any untagged packet received on a port is associated, by default, with the port-based VLAN group configured for that port.

Port-based VLAN Example

Figure 31 shows an example where four LAN stations are connected to a single 4-port switch device. Two VLAN groups are set up with two port members for each group. The active VLAN set contains two groups: port 0 and port 1 are members of VID = 10, port 2 and port 3 are members of VID = 11. Ethernet frames are exchanged between port 0 and port 1 as well as between port 2 and port 3, but not between port 0/1 and port 2/3.

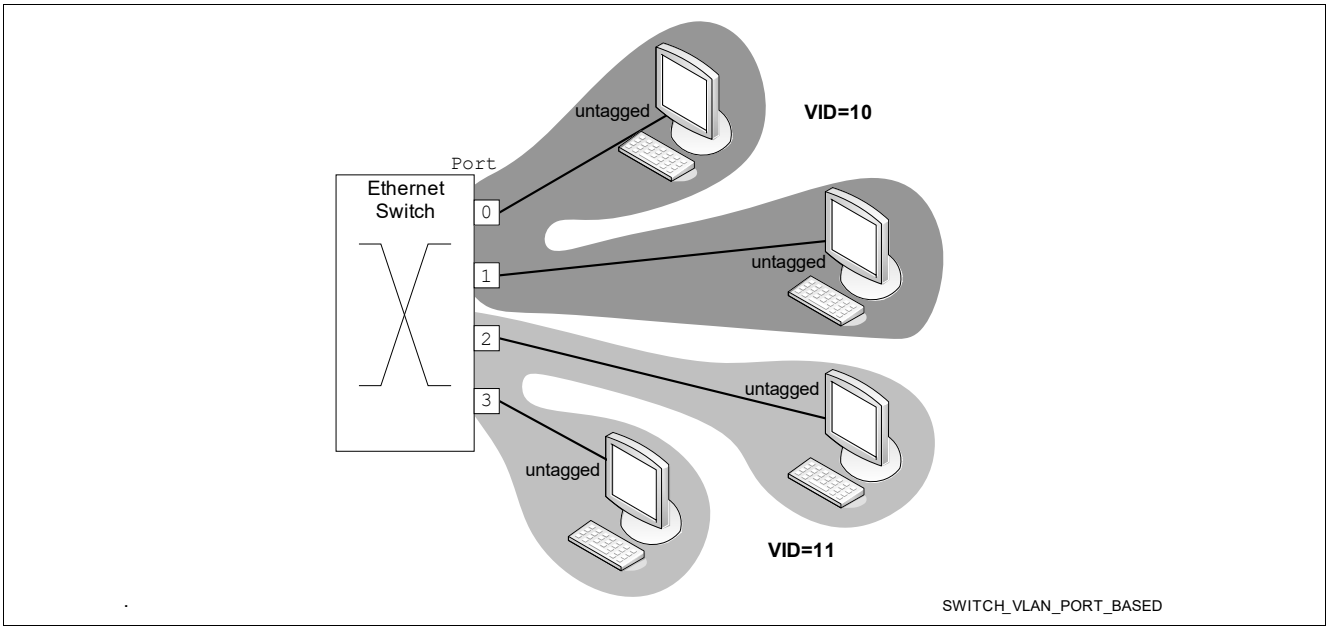


Figure 31 Port-based VLAN Example

3.7.3.14 Single Tag Based VLAN Examples

In a tag-based VLAN group, the VLAN association is based on the outer customer VLAN tag detected in the header of the received Ethernet frame.

Tag-based VLAN Example

Figure 32 shows an example where six LAN stations are connected to a single 6-port switch device. Three VLAN groups are added to the active VLAN set. Port 0 and port 1 are members of the port-based VLAN group with VID =10, port 2 and port 3 are members of the port-based VLAN group with VID = 11. Port 4 is member of the port-based VLAN group with VID = 12. Port 5 is connected to a server and may transmit and receive tagged VLAN packets of any of the defined groups.

Every configured VLAN group adds port 5 as a port and tag member. In this case, packets received from one of the untagged (VLAN unaware) LAN segments are transmitted as tagged Ethernet frames when they are targeted to port 5. The attached VLAN tag is the port-based VID of the ingress port.

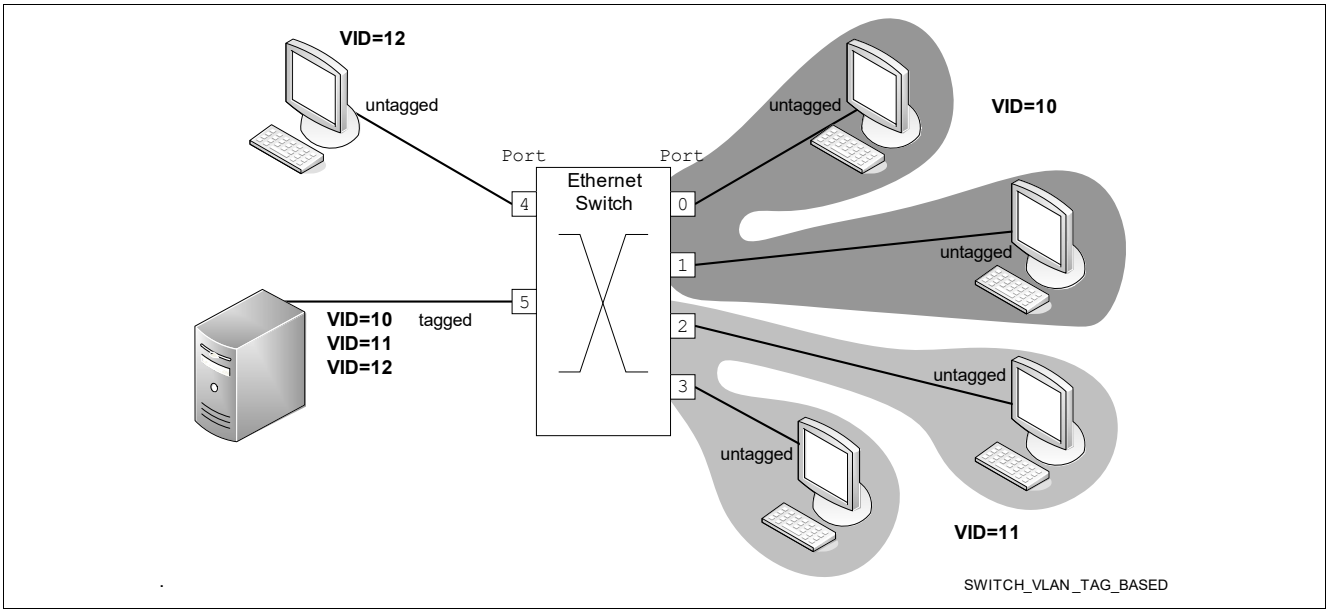


Figure 32 Tag-based VLAN Example

3.7.3.15 Double Tag Based VLAN Examples

In a double tag-based VLAN group, the VLAN association is based on STAG and CTAG detected in the header of the received Ethernet frame.

Figure 33 shows an example where six LAN stations are connected to a single 6-port switch device. Port 5 is connected to a server and may transmit and receive double tagged VLAN packets of any of the defined groups.

Table 27 Port Settings

Port	Port STAG Enable	Port SVID	CTAG Transparent Mode	Port CVID
0,1	Disable	301	No	Don't Care
2,3	Disable	302	Yes	11
4	Disable	301	Yes	12
5	Enable	Don't Care	No	Don't Care

Table 28 CTAG VLAN Membership Table

CTAG VLAN ID	CTAG Port Members	CTAG Tag Members
10	0, 1, 5	0,1,5
12	4, 5	5
11	2,3,5	Null

Table 29 Traffic Flow Table

STAG VID Pattern	Port Bitmap Action	Port Bitmap Multiplexing Control	Port Bitmap[1)]	VLAN Action	CTAG Ignore Control
301	1_B	1_B[1)]	0,1,4,5	0_B	Don't care
302	1_B	1_B[1)]	2,3,5	1_B	1_B[2)]

1) When Port Bitmap Multiplexing Control is 1_B, Port BitMap is used as STAG Port Members.

2) When CTAG Ignore Control is 1_B, CTAG VLAN group is ignored and CTAG is treated as transparent.

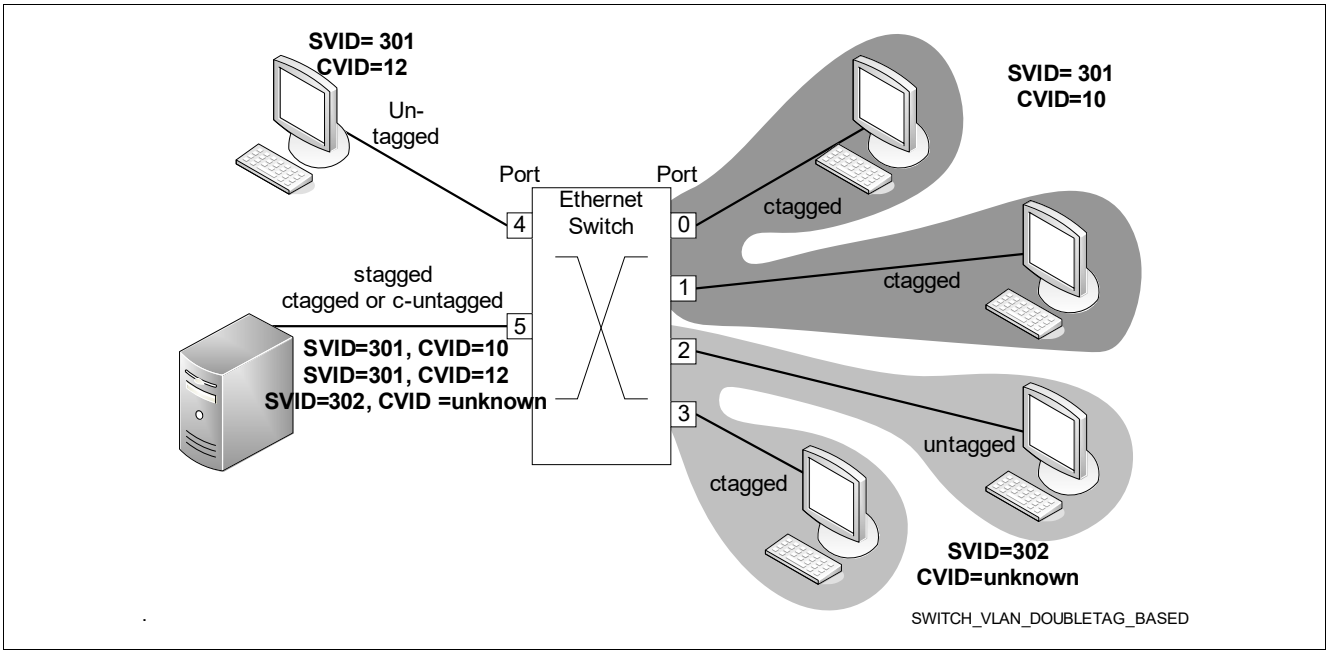


Figure 33 Double Tag and Port based VLAN Example

3.7.4 Multicast Forwarding Functions

Multicast forwarding is a method of forwarding Ethernet frames or IP datagrams to a group of receivers. A basic Ethernet switch floods all received multicast frames to all output ports even when no host on a port is interested in that particular multicast stream. This waste of bandwidth is avoided by the sophisticated multicast handling of the Gigabit Ethernet Switch Macro which allows to forward multicast frames based on L2 or L3 addresses to dedicated ports. In addition the Gigabit Ethernet Switch Macro is able to learn L3 multicast group addresses via IGMPv1/2 snooping in hardware.

The Gigabit Ethernet Switch Macro can be configured to ignore L3 information and forward multicast frames based on MAC destination address only. In this case, L2 multicast addresses must be added to the bridging table with the appropriate port members and is populated by software.

When L3 multicast handling is enabled and the packet contains an IP multicast address, a lookup in the dedicated L3 multicast table is performed. The frame is forwarded to the destination port (or multiple destinations) based on the match result. When the frame contains no IP multicast address or when there was no match in the L3 multicast table, a lookup based on the MAC address is done in the bridging table. A lookup match results in a port map which indicates relevant destination ports. **Table 30** describes frame forwarding decision. When there was no match in the bridging table, the non-IP multicast frame is forwarded according to the default multicast port map (via PCE_PMAP_2). When there is no match in bridging table and no match in L3 multicast table, the IP multicast data frame (IP protocol is not IGMP and MLD) is discarded or forwarded to default multicast port map. IGMP or MLD message frames are forwarded according to IGMP/MLD types.

Note: The lookup in the L2 bridging tables is done with the MAC address regardless whether the address is a unicast, multicast or broadcast address. This means that a mix of unicast, multicast and broad cast entries can be entered into the tables and that unicast addresses can also be forwarded to multiple ports. The lookup in the IP multicast table is done with the IP address only when the address is IP multicast.

Table 30 Multicast Forwarding Decision

Forwarding Mode	Packet Type	L3 Multicast Table	Bridging Table	Destination Result
L2 only	Don't Care	Don't Care	No Match	Default multicast port map (configured via PCE_PMAP_2).
L2 only	Don't Care	Don't Care	Match	Bridging Table, matched entry port members.
L2 / L3	IGMP/MLD Control	See **Table 33**.		
L2 / L3	IP Multicast (Excluding IGMP/MLD Control Packets)	Match	Don't Care	L3 Table, matched entry port members.
L2 / L3	Any Multicast (Excluding IGMP/MLD Control Packets)	No Match	Match	Bridging Table, matched entry port members.
L2 / L3	IP Multicast (excluding IGMP/MLD Control Packets)	No Match	No Match	Two Options (configured via UKIPMC bit in PCE_GCTRL_1): 0: Default multicast port map (default mode) 1: Discard
L2 / L3	Non-IP Multicast	No Match	No Match	Default multicast port map.

The <Informative> IPv4 multicast addresses are in the group historically called Class D, based on the leading bits of these addresses. The group includes the addresses from 224.0.0.0 to 239.255.255.255, or, equivalently, 224.0.0.0/4. The multicast addresses in IPv6 have the prefix ff00::/8_H. On Layer-2, IPv4 multicast packets are delivered by using the Ethernet MAC address range 01:00:5e:00:00:00_H - 01:00:5e:7f:ff:ff_H. This is 23 bits of available address space. The first octet includes the broadcast/multicast bit. The lower 23 bits of the 28-bit

multicast IP address are mapped into the 23 bits of available Ethernet address space. This means that there is ambiguity in delivering packets. When two hosts on the same subnet each subscribe to a different multicast group whose address differs only in the first 5 bits, Ethernet addresses for both multicast groups are the same. For IPv6 The multicast addresses, the Ethernet MAC address is derived by the four low order octets OR'ed with the MAC address $33:33:00:00:00:00_H$.

3.7.4.1 Layer-2 Multicast Forwarding

The layer-2 multicast forwarding function deals with multicast frame forwarding based on the Ethernet MAC address. The destination port map is looked up in the Bridging table. The multicast addresses are not added to the Bridging table by automatic learning function and must be configured manually, by appropriate management action. The associated port map contains all the relevant port members. When the destination MAC address of the received frame matches the entry in the Bridging table and the Forwarding Mode is Layer-2 only or there was no match in the Layer-3 multicast table or the packet is Non-IP multicast, the frame is delivered to all the destinations specified in the associated port map.

The <Informative> MAC Address is defined as multicast when the least significant bit of the most significant byte is set to "1_B". The broadcast Address (MAC address =$FF:FF:FF:FF:FF:FF_H$) is a special case and treated in this description as Multicast.

3.7.4.2 Layer-3 Multicast Forwarding

Layer-3 Multicast function deals with multicast frame forwarding based on the IPv4 or IPv6 Network Address. The destination port map is looked up in the L3 multicast table.

The lookup in the multicast table is performed using the destination IPv4/IPv6 address and optionally the source IPv4/IPv6 address. The addresses in the table are added automatically by hardware based IGMP snooping or by appropriate management action. See **IGMP and MLD Snooping** for details. In any source multicast (ASM) as in IGMPv1/IGMPv2/MLDv1, the source IP information is not required, in source specific multicast (SSM) as in IGMPv3/MLDv2 the source IP information is used for the lookup. For SSM, the include and exclude mode is supported. In include mode, the packets are forwarded to the multicast group address when they come from a specified IP source address (or multiple addresses). In exclude mode, the packets are forwarded to the multicast group address when they do not come from a specified IP source addresses.

3.7.4.3 IGMP and MLD Snooping

The Gigabit Ethernet Switch Macro supports IGMP (Internet Group Management Protocol) and MLD (Multicast Listener Discovery) snooping. IGMP/MLD snooping is designed to prevent hosts on a local network from receiving traffic for a multicast group they have not explicitly joined. It provides a mechanism to prune multicast traffic from links that do not contain a multicast listener (IGMP/MLD group member). IGMP/MLD snooping requires the Gigabit Ethernet Switch Macro to examine, or snoop, some Layer-3 information in the IGMP/MLD packets sent between the hosts and the router. In addition, adjacent routers also use these protocols to communicate and share routing information. This information exchange can be snooped as well to identify the multicast router port.

The Gigabit Ethernet Switch Macro supports HW-based IGMP snooping mode for the IGMPv1/IGMPv2 protocols. In this mode, the L3 multicast addresses are added to the multicast table or removed from it automatically, based on the relevant IGMP reports. No software intervention is required in this mode. See **HW Based IGMP Snooping** for details.

The Gigabit Ethernet Switch Macro supports SW-based IGMP/MLD snooping mode for the IGMPv1/2/3 or MLDv1/2 protocols. In this mode, specific IGMP/MLD reports can be intercepted by the switch and delivered to the CPU/Network Processor port. The reports are analyzed by the CPU and the L3 multicast table is populated by the SW with appropriate source/destination addresses. See **SW Based IGMP/MLD Snooping** for details.

HW Based IGMP Snooping

When HW-based IGMP snooping is enabled, the Gigabit Ethernet Switch Macro analyzes all IGMPv1/IGMPv2 packets between hosts connected to the switch and multicast routers in the network. **Table 31** and **Table 32** describe the packet structure of IGMP messages intercepted by the switch, these patterns are added as a dedicated rule to the Traffic Flow Table. **Table 31** describes the messages sent by the multicast host and **Table 32** describes the messages sent by the multicast router.

Table 31 Multicast Host Messages

Field	IGMPv1 Report	IGMPv2 Report	Leave
MAC_DA	01 00 $5E_H$--IP_DA	01 00 $5E_H$--IP_DA	01 00 5E 00 00 02_H
Ethertype	0800_H	0800_H	0800_H
IP Protocol (=IGMP)	02_H	02_H	02_H
IP_SA	Host_IP Address	Host_IP Address	Host_IP Address
IP_DA	Group_IP_Address	Group_IP_Address	224.0.0.2 or Group_IP_Address
Type	12_H	16_H	17_H
Max. Response Time	0	0	0
Group Address	Group_IP_Address	Group_IP_Address	Group_IP_Address

Table 32 Multicast Router Messages

Field	Solicitation	Advertisement	General Query	Group Specific Query
MAC_DA	01 00 5E 00 00 02_H	01 00 5E 00 00 $6A_H$	01 00 5E 00 00 01_H	01 00 $5E_H$--IP_DA
Ethertype	0800_H	0800_H	0800_H	0800_H
IP Protocol (=IGMP)	02_H	02_H	02_H	02_H
IP_SA	Router_IP Address	Router_IP Address	Router_IP Address	Router_IP Address
IP_DA	224.0.0.2	224.0.0.106	224.0.0.1	Group_IP_Address
Type	31_H	30_H	11_H [1)]	11_H

1) For IGMPv1 the type = 1 but together with the version = 1 a IGMPv2 host sees 11_H

When the switch detects an IGMP report or join group message sent from a host for a given multicast group, the switch adds the host's port number to the multicast table entry for that group. When a IGMP leave group message is received from a host, the host's port number is removed from the appropriate table entry when fast leave (also called immediate leave) mode is enabled. See the following sections for details.

Joining Multicast Group:

When the Gigabit Ethernet Switch Macro receives a host membership report on one of the ingress ports and HW-based IGMP snooping is enabled, this port is added to the specified multicast group in the L3 multicast table. When there was no such group entry in the table, a new entry is created with the appropriate group IP address. Received membership report is forwarded to the multicast router port (or multiple router ports).

Report Suppression:

The Gigabit Ethernet Switch Macro supports suppression of membership reports or join messages to reduce processing load of the multicast router. When report suppression is enabled, only the first report for specific group is forwarded to the router port. The rest of the reports from the other hosts are discarded. The suppression can be configured per port and can be selected separately for join or report messages.

Join message is an IGMP membership report from a host that previously did not participate in a group.

Leaving Multicast Group:

When a host wants to leave a multicast group it can send a Leave message (IGMPv2) or should not send a Report message after a Query (IGMPv1). A Leave message is sent to the all-routers multicast group (224.0.0.2) or to the group a host wants to leave.

Each port in the joined group maintains an aging timer. Repeated Reports refresh the timer. When no Reports are received for a particular group before this timer expires, the router assumes the group has no local members and does not require forward multicast frames for that group. Robustness variable is supported and determines how often the response timer is allowed to expire before the port is actually deleted. When the port map becomes zero the whole entry is deleted from the L3 multicast HW table. The response timer is reset each time a new query was received.

The age time for the entries is derived from the response time received in the IGMP Query messages. For a group specific query the response time is used only for the corresponding group, for a general query the response time is used for all the groups. It can be programmed that the default response time is used instead of the response time from the query message.

The Gigabit Ethernet Switch Macro supports a fast leave (also called immediate leave) feature. When fast leave is enabled and an IGMP Leave is received, the port from which the IGMP packet was received is cleared immediately from the port map of the corresponding group IP address. When the port map is empty, the group IP address and port map are deleted from the L3 multicast HW table. When fast leave is not enabled, the ports and group IP addresses age out when no reports have been detected for a given time.

Note: Enable fast leave mode where only one host is connected to each interface. When fast-leave is enabled where more than one host is connected to an interface, some hosts might be dropped inadvertently.

Router Port Detection:

The Gigabit Ethernet Switch Macro supports automatic detection of the multicast router port, based on the typical multicast router messages described in **Table 32**. When router port detection (auto-learning) is enabled, the learned router port is added as a destination to the snooped IGMP reports received from hosts and as a destination to any multicast frame destined to the hosts.

The default Router Port can also be configured by appropriate management action.

Each learned router port (or multiple ports) maintains an aging timer and can age out when the router message exchange is stopped on a port. The timer is automatically reset each time a new router message is received. When a port does not receive any router messages within the specified time period, the port is deleted from the learned router port map.

Multicast Steam Forwarding:

Table 33 describes typical forwarding destination for the multicast frames. Multicast data frames are typically received from the router port and forwarded based on the match in the L3 multicast table and to the router ports. When there was no match in the L3 multicast table the frames are forwarded based on the L2 addresses or to the default IP/IGMP multicast port map.

Table 33 Typical IGMP/MLD Control Packets Forwarding Destination

IGMP Message Name	Port Map
Report	Multicast router port map
Leave	Multicast router port map
General Query or Group Specific Query	Forwarding port map (based on L3 or L2 multicast table) + Multicast router port map
Unknown General Query or Group Specific Query	Default multicast port map+ Multicast router port map

SW Based IGMP/MLD Snooping

When SW-based IGMP snooping is enabled, IGMP/MLD control frames from Non-CPU ports are forwarded to the CPU port (IGMP/MLD control frame patterns are added as dedicated rules to the Traffic Flow Table as shown in Table 34) and the L3 multicast table is populated by software. IPv4 / IPv6 source and destination addresses can be added to the table and specify the direction of the multicast streams. A source address can be added using one of the following modes:

- Include Mode. In this mode, the forwarding of the multicast frame is based on the source and destination address pair. Specifically: the frame is forwarded to the specified port map only when both addresses (the source and destination) match in the L3 multicast table.
- Exclude Mode. In this mode, the forwarding of the multicast frame is based on destination and source address pair. Specifically: the frame is forwarded to the specified port map only when the source address does not match the address in the table and the destination address matches. When a frame contains specified source and destination address, this frame is discarded. When a frame contains any other source address and a matched destination, this frame is forwarded.
  Note: Adding an entry in exclude mode, creates up to two entries in the L3 multicast table. An exclude entry is implemented using two entries in the include mode: one contains an include entry with the wild-card source address and another an include entry with the respective host port cleared in the port map.
- Don't Care Mode. In this mode, the source IP address field of the packet is ignored and the multicast frame forwarding is based on the destination IP address alone.

Table 34 IGMP/MLD Messages

Field	IGMPv1/v2/v3 Host Messages	IGMPv1/v2/v3 Router Messages	MLDv1/v2 Host Messages	MLDv1/v2 Router Messages
IP Type	IPv4	IPv4	IPv6	IPv6
IP Protocol	2	2	58	58
Type	18, 24, 25, 34	17, 48, 49	131 - 132	130, 151 - 153

Table 35 Typical IGMP/MLD Messages Forwarding Destination

Source Port	IGMP/MLD Message Name	Port Map
Non-CPU	All messages	CPU Port
CPU	Host Messages	Router port map
CPU	Router Messages	Forwarding port map (based on L3 or L2 multicast table or default multicast port map)

3.7.5 Quality of Service Functions

The Gigabit Ethernet Switch Macro provides extensive support for Quality of Service functionality. Particularly, traffic class assignment based on multiple flow parameters, ingress traffic policing, multiple egress queues per port with strict or WFQ scheduling, traffic shaping and weighted random early discard (WRED) functions are supported.

The following sections describe in more details the QoS functions supported by the switch.

3.7.5.1 Class of Service Assignment

The Gigabit Ethernet Switch Macro supports classification of the incoming traffic into traffic classes or classes of service (CoS). Each traffic class can be managed (e.g., remarked, policed, shaped) differently, ensuring preferential treatment for higher-priority traffic on the network. The Gigabit Ethernet Switch Macro is able to assign the traffic class of the received packet, based on the following parameters:

- **Ingress Port:** CoS is based on the ingress port number of the received packet. This mode is used by default when no other criteria can be matched.
- **STAG PCP&DEI and CTAG PCP (VLAN Priority Code Point):** CoS is based on the VLAN priority code point placed in the VLAN tag of the incoming packet. The Gigabit Ethernet Switch Macro provides a global STAG PCP&DEI to Traffic Class assignment table and a global CTAG PCP to traffic class assignment table. In the tables, any STAG VLAN PCP/DEI or CTAG VLAN PCP combination is mapped to an appropriate class of service. Traffic class mapping from STAG VLAN PCP/DEI can be enabled per ingress port (via SPCP bit in PCE_PCTRL_2). Traffic class mapping from CTAG PCP can be enabled per ingress port (via PCP bit in PCE_PCTRL_2).
  - When the packet contains no STAG it can be configured to choose other methods for the traffic class classification (e.g., DSCP, CTAG PCP or ingress port).
  - When the packet contains no CTAG it can be configured to choose other methods for the traffic class classification (e.g., DSCP, STAG PCP&DEI or ingress port).
- **DSCP (Differentiated Services Code Point):** CoS is based on the Differentiated code point placed in the IP header of the incoming packet. The Gigabit Ethernet Switch Macro provides a global DSCP to traffic class assignment table. In this table any IP DSCP 6 bits combination is mapped to an appropriate class of service. *Note: When the packet contains no IP header it can be configured to choose other methods for the traffic class classification (e.g.CTAG PCP, STAG PCP/DEI or default traffic class).*
  - When more than one classification methods are enabled, the highest traffic class mapped from different fields is selected.
- **Traffic Flow:** Any combination of the following traffic flow parameters entered to the Traffic Flow table can be used to assign the class of service. When a flow with an appropriate traffic class assignment action matches for a given ingress frame, this assignment has higher priority over the default CoS assignments. In this case, the traffic class is assigned based on the traffic flow rule.
  - Destination MAC address (with nibble-mask support)
  - Source MAC address (with nibble-mask support)
  - STAG VLAN ID (with nibble mask or range support)
  - CTAG VLAN ID (with nibble mask or range support)
  - Ethertype
  - IP protocol and parser flags
  - IP packet length or length range
  - STAG PCP & DEI
  - CTAG PCP
  - IP DSCP
  - Source IP address (with nibble-mask support)
  - Destination IP address (with nibble-mask support)
  - Application field 1, for example, Source TCP/UDP port (with range support)
  - Application field 2, for example, Destination TCP/UDP (with range support)

Up to 16 different traffic classes can be supported and mapped individually to appropriate QoS queue. See **Queue Mapping** for more details regarding queue mapping. **Figure 34** describes the traffic class assignment selection order vs configuration.

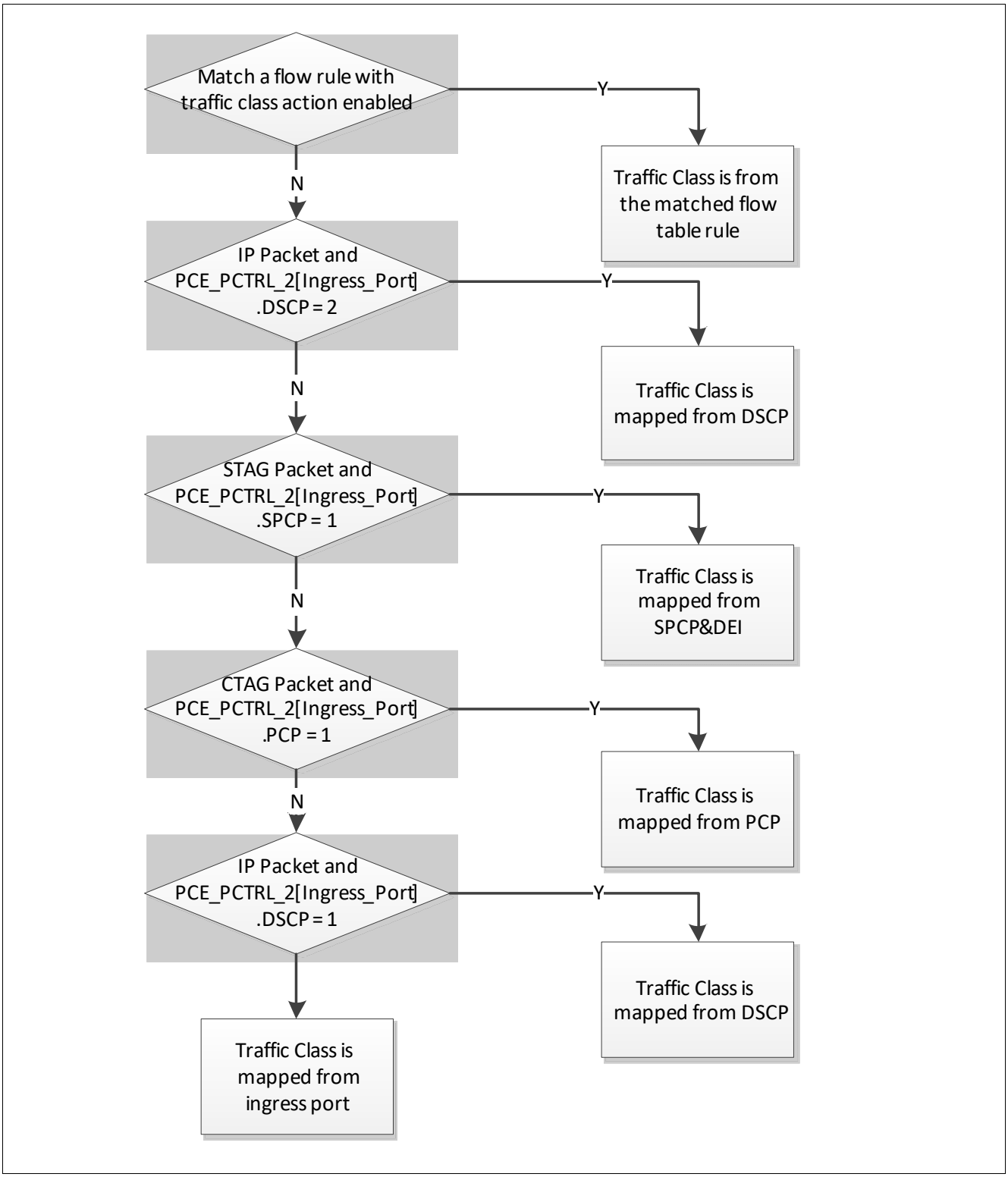


Figure 34 Traffic Class Assignment

3.7.5.2 Remarking Function

The Gigabit Ethernet Switch Macro supports the remarking of the DSCP, (re)generation of STAG PCP&DEI, and (re)generation of CTAG PCP in the egress frame. The modification of the code points in the outgoing packets is based on both traffic class and egress port. The Gigabit Ethernet Switch Macro provides a dedicated mapping table to assign the new DSCP, CTAG PCP and STAG PCP&DEI according to according to traffic class as well as egress port. **Figure 35** shows how DSCP (including drop precedence), CTAG PCP, STAG PCP and STAG DEI can be remarked based on any of the class of service assignment parameter.

Remarking can be enabled per ingress port. Remarking can also be disabled per egress port and per code point. In addition, the Traffic Flow table allows to disable remarking explicitly for certain flows.

Figure 36 shows the remarking DSCP flow diagram. **Figure 37** shows the remarking Drop Precedence flow diagram. **Figure 38** shows the STAP PCP remarking flow diagram. **Figure 39** shows the STAP DEI remarking flow diagram. **Figure 40** shows the CTAG PCP remarking flow diagram.

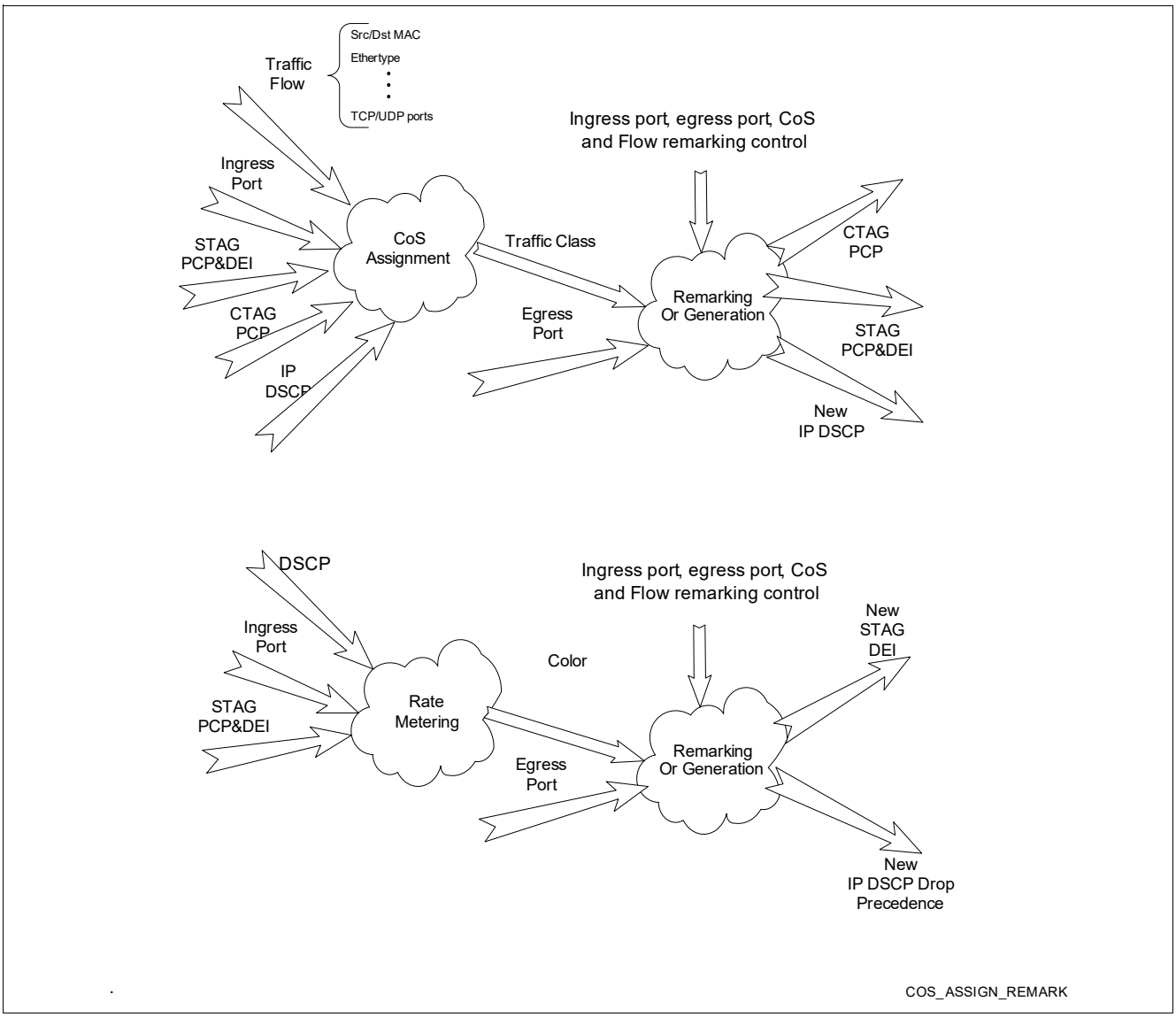


Figure 35 PCP/DSCP /DEI Remarking

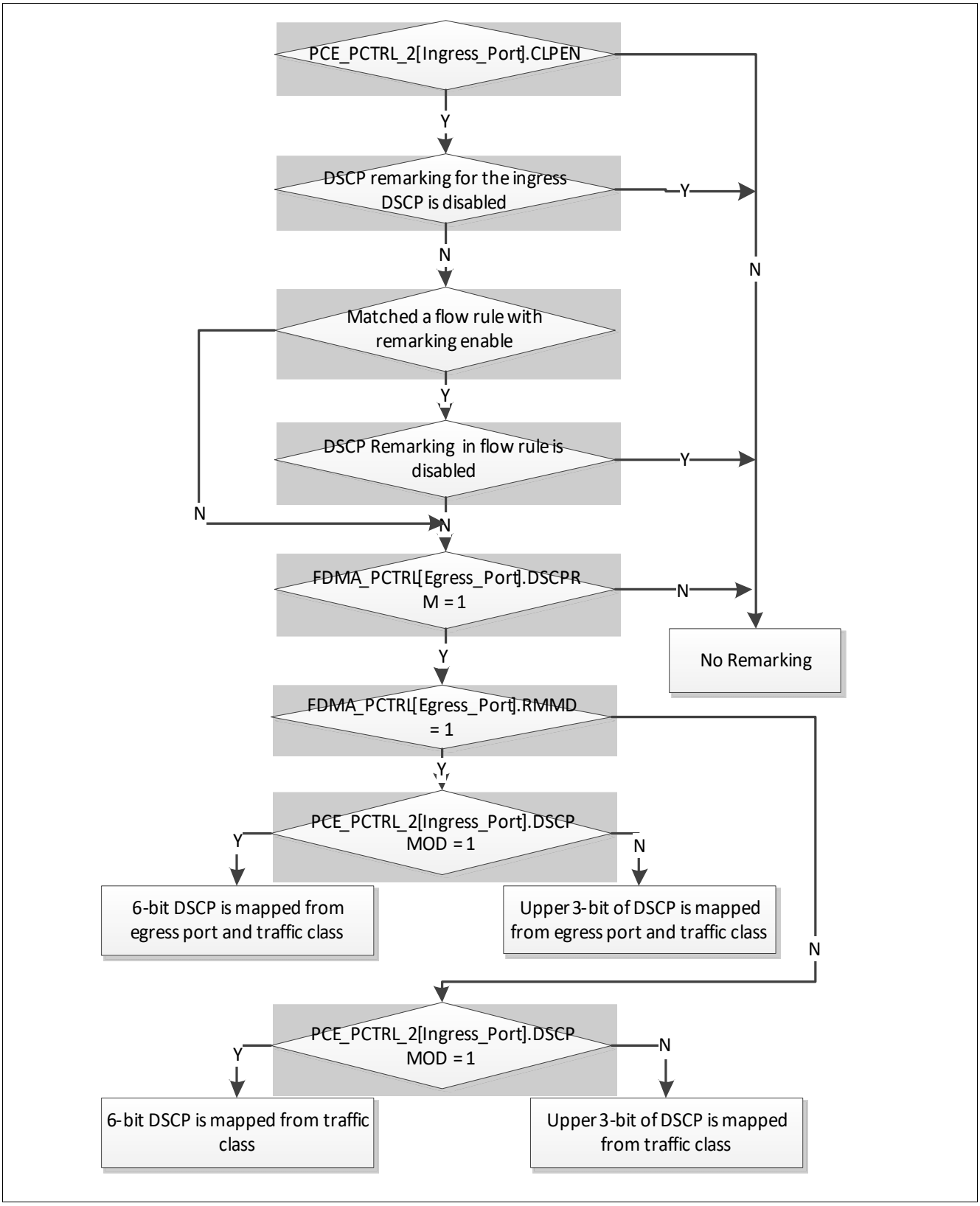


Figure 36 DSCP Remarking Flow Diagram

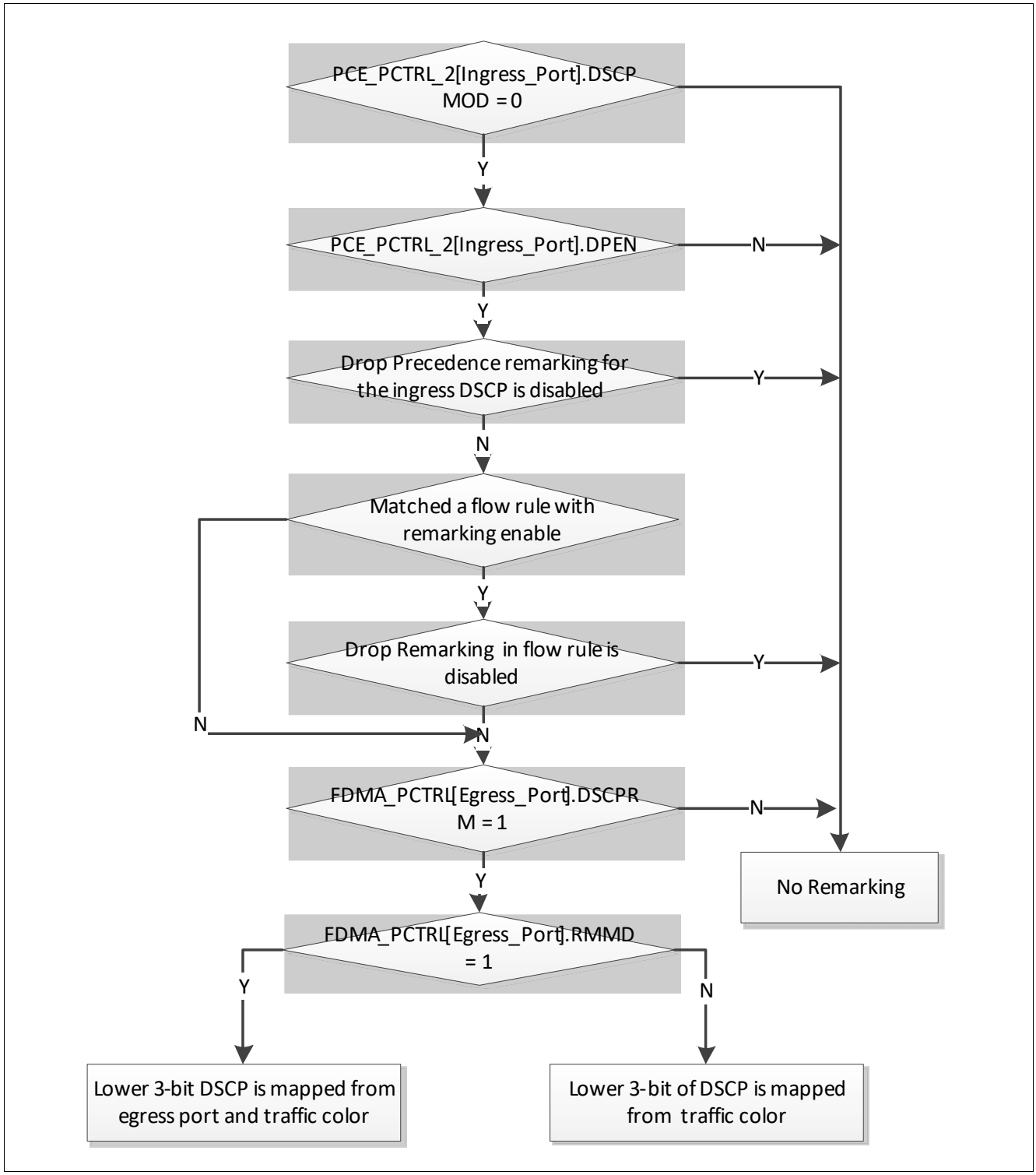


Figure 37 Drop Precedence Remarking Flow Diagram

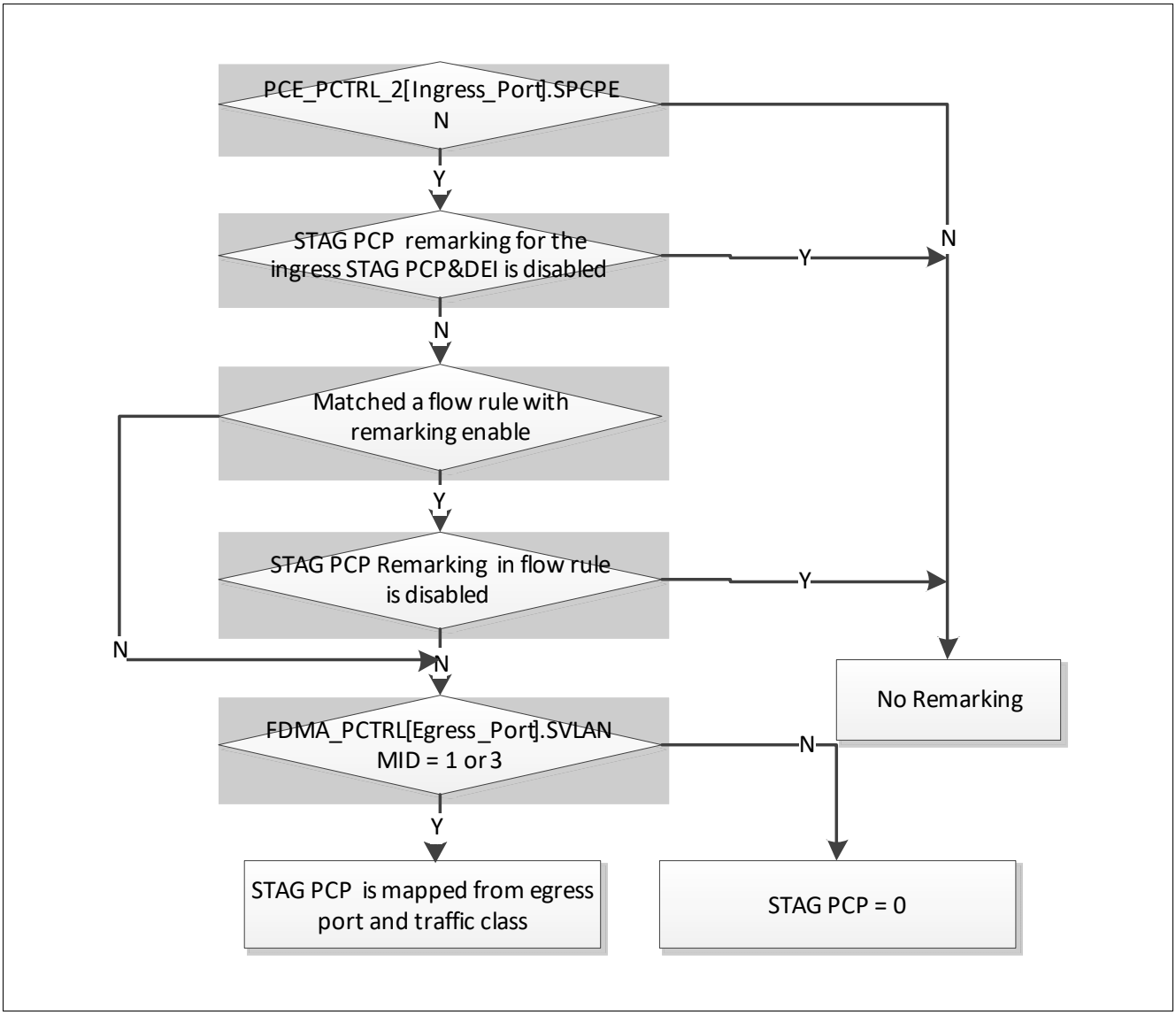


Figure 38 STAG PCP Remarking Flow Diagram

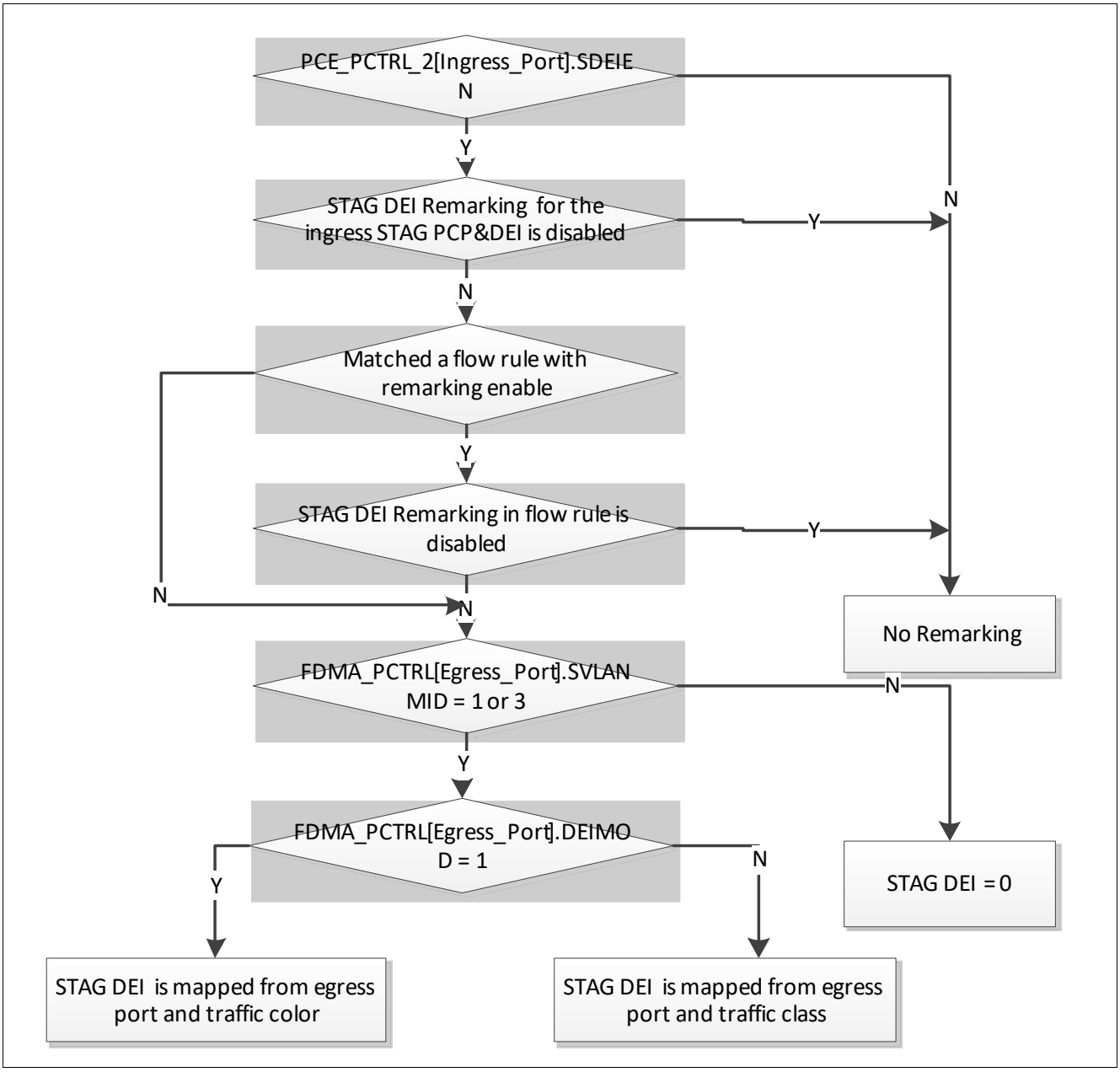


Figure 39 STAG DEI Remarking Flow Diagram

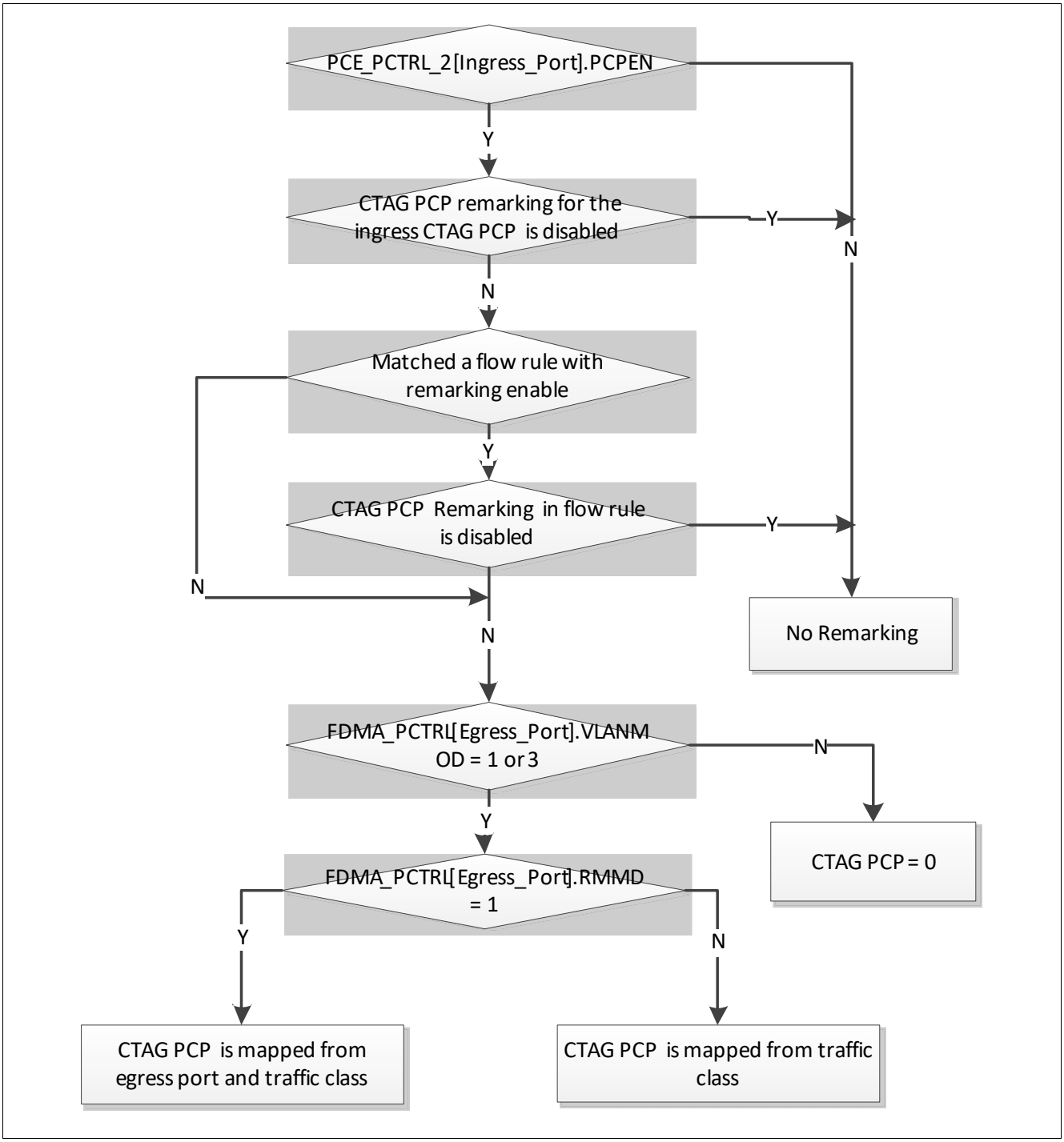


Figure 40 CTAG PCP Remarking Flow Diagram

3.7.5.3 Queue Mapping

The Gigabit Ethernet Switch Macro supports 32 egress QoS queues that can be flexibly assigned to egress ports and traffic classes. The following sections provide more details on the queue mapping functionality.

Queue to Port Mapping

Per default egress port 0 to 7 has 4 Quality of Service queues. For certain applications it might be desired to have a different number of QoS queues on specific ports. The Gigabit Ethernet Switch Macro supports flexible queue to port mapping. Each queue from the 32 queue pool can be assigned to any port. This way the default configuration can be changed so that one port, for example, contains 8 queues.

Note: In certain configurations there might be unassigned (unused) queues. However, the overall number of 32 queues for all ports cannot be exceeded.

In addition, an active port must have at least one queue and can have maximum 16 queues assigned to it.

Traffic Class to Queue Mapping

Incoming frames are being stored in the appropriate queues based on the traffic class assignment. The mapping of the traffic class to queue is specified in a dedicated queue mapping table per egress port. The mapping of the traffic classes to queues is related to the number of the queues available on certain port. For example, on one port 4 traffic classes could be mapped to 4 different queues, on another port all 4 traffic classes could be mapped to one single queue of this port.

3.7.5.4 Rate Metering

The Gigabit Ethernet Switch Macro supports 16 instances of a single rate Three Color Meter (srTCM). Each meter can measure the rate of a packet stream and mark the packets either green, yellow, or red. When there is no metering instance assigned to a traffic stream, this stream is considered to be green in the color-blind mode. In color-aware mode the stream is colored based on the drop-precedence encoded in the frame. See the following sections for details.

The color markings can be used later for policing in the active congestion management function, See **Congestion Management** for details. In addition the markings can be used to remark the drop precedence of the outgoing packet in the DSCP and STAG DEI.

Marking is based on a Committed Information Rate (CIR) and two associated burst sizes, a Committed Burst Size (CBS) and an Excess Burst Size (EBS). A packet is marked green when it does not exceed the CBS, yellow when it does exceed the CBS, but not the EBS, and red otherwise.

*Note: In color-aware mode as described in **Color-aware/ Color-blind modes**, the packet may already contain a color. In this case, for a yellow colored frame only the EBS is checked and when exceeded, the packet becomes red. For packets received with a red color - the CBS/EBS plays no role, the packet remains red.*

Only single meter instance can be assigned to measure the rate of a traffic flow.

The Gigabit Ethernet Switch Macro supports the following meter assignments:

- **Port:** A Meter can be assigned to the ingress or egress port or port pair, particularly:
  - Ingress port. The meter assigned to a specific ingress port. All packets received on that port are metered with the same meter instance.
  - Egress port. The meter assigned to a specific egress port. Any packets destined to that port are metered with the same meter instance.
    Note: The multicast packets get metered when a meter is assigned to one of the destination ports.
  - Ingress-Egress port pair. The meter assigned to a specific packet route, from specific ingress port to a specific egress port.
- **Traffic Flow:** Any combination of the following traffic flow parameters entered to the Traffic Flow table can be used to assign the metering instances.

- Destination MAC address (with nibble-mask support)
- Source MAC address (with nibble-mask support)
- STAG VLAN ID (with nibble mask or range support)
- CTAG VLAN ID (with nibble mask or range support)
- Ethertype
- IP protocol and parser flags
- IP packet length or length range
- STAG PCP & DEI
- CTAG PCP
- IP DSCP
- Source IP address (with nibble-mask support)
- Destination IP address (with nibble-mask support)
- Application field 1, for example, Source TCP/UDP port (with range support)
- Application field 2, for example, Destination TCP/UDP (with range support)

• **Storm Control:** (refer also to **Storm Control**) When storm control is enabled a meter can be assigned to
  - unknown unicast traffic
  - unknown multicast traffic
  - broadcast traffic

Figure 41 describes a metering algorithm of a single metering instance.

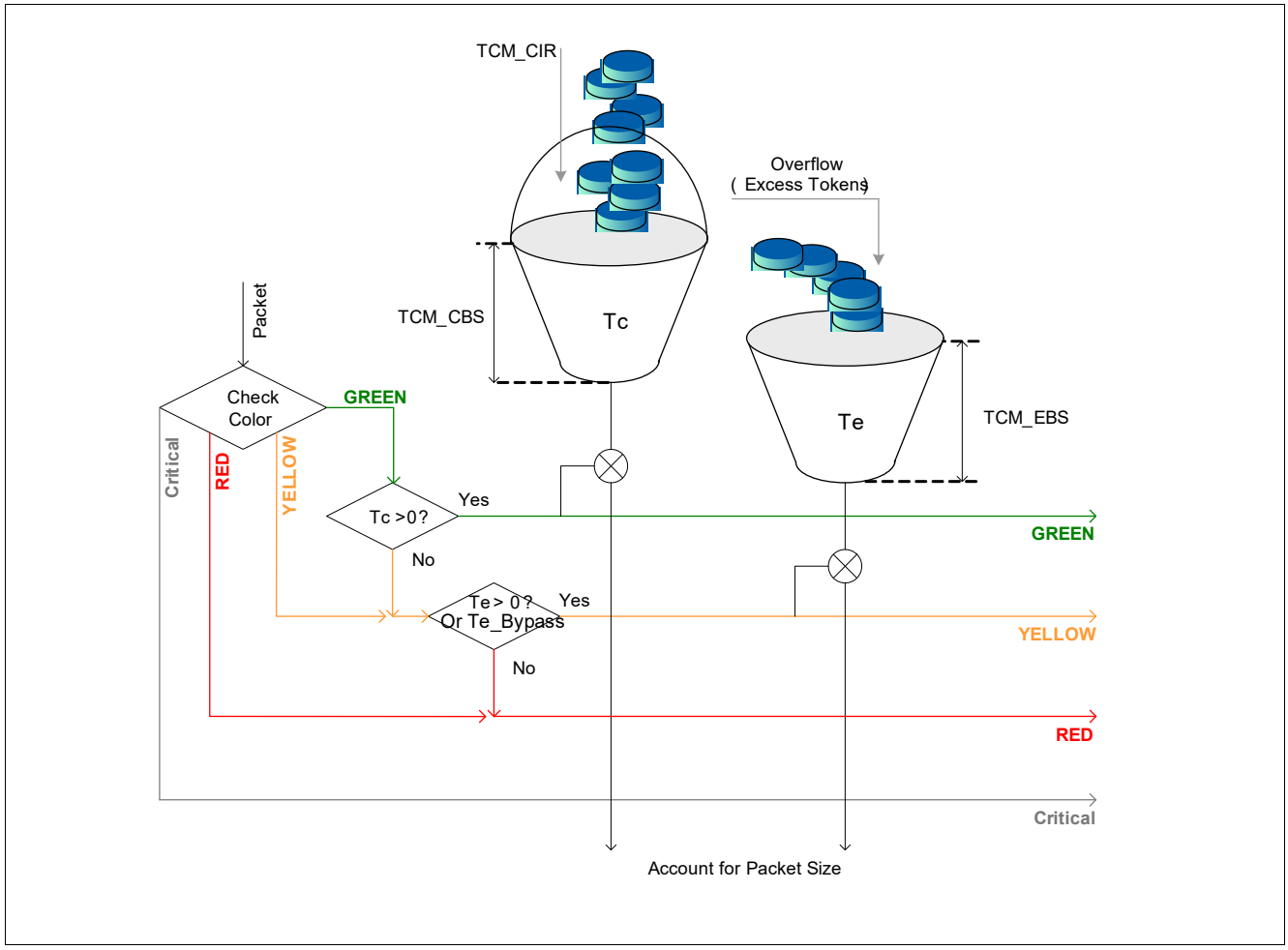


Figure 41 Metering Algorithm

Critical Frames

Frame can be classified as critical based on specific DSCP encoding in the appropriate DSCP mapping table or based on a rule configured in the Traffic Flow table. Critical frames bypass the metering instance and do not trigger the active congestion management function.

Color-aware/ Color-blind modes

The Gigabit Ethernet Switch Macro supports color-awareness modes to be configured per ingress port. In the color-aware mode, the meter assumes that some preceding entity has pre-colored the incoming packet stream so that each packet is either green, yellow, or red. The ingress color of the incoming frame is based on either DSCP value or STAG PCP&DEI value. It is retrieved from the appropriate DSCP mapping table or STAG PCP&DEI mapping table. Non-IP and Non-STAG packets are treated as pre-colored to green.

In color-blind mode, all packets are treated as green.

DSCP Drop Precedence Remarking

It can be enabled by both ingress port and egress port configuration to reflect the metering results by replacing the lower 3 bits of the received DSCP field with the value of appropriate color decided by the metering instance for the received packet. The mapping of the color to the lower 3 bits of the DSCP can be configured per egress port. See **Remarking Function** for details.

DEI (Re)generation

It is enabled by both ingress port and egress port configuration to reflect the metering result by setting the STAG DEI field of the packet with the value of appropriate color decided by the metering instance for the received packet. The mapping of the color to the DEI is configured per egress port. See **Remarking Function** for details.

Metering based Flow Control

When a metering instance is assigned to an ingress port, the conformance rate of this port can be used for triggering flow control. In other words, once the tokens in Tc bucket is below 8000_H, the start flow control can be generated on that port. When the tokens in Tc bucket is more than TCM_EBS*64, the stop flow control can be generated on that port.

Note: To achieve that functionality the assigned meter instance number must correspond to the respective ingress port. All ingress packets from the rate flow control enabled port must be green color.

Conforming status for each port are readable via MTEBP bit in PCE_TCM_STAT register. Any change of conforming status can trigger the interrupt.

3.7.5.5 Rate Shaping

The Gigabit Ethernet Switch Macro supports 32 instances of rate shaper. Each rate shaper can be configured to Token Bucket mode or Credit Rate shaper mode. Each shaper mode can be configured via RSMOD bit in RS_CTRL. Each shaper can measure the rate of an egress queue and prevent the queues which exceeded the configured rate from being scheduled for the next packet transmission. Shaping is based on a Committed Information Rate (CIR) and an associated Committed Burst Size (CBS). A queue can be selected for transmission only when it does not exceed the CBS for a given CIR.

Up to two shaping instances can be assigned to measure the egress rate of a specific queue or number of queues. Two shapers are typically being assigned to measure the peak and committed rate and typically have different CIR settings. Any number of queues can share the same shaping instance, in this case the committed rate and the burst size are shared among the assigned queues.

When there is no shaper assigned to a queue, the queue rate is not monitored. It is recommended to assign a shaper for queues with high scheduling weights or strict priority queues. See **Queue Scheduling** for details regarding queue scheduling.

3.7.5.6 Queue Scheduling

The scheduling function determines which queue is allowed to emit a packet. Queue scheduling is done after the rate shaping. The Gigabit Ethernet Switch Macro supports the following scheduling types for each one of the 32 egress QoS queues:

- **Weighted Fair Queueing (WFQ):** For a given port, packets in the WFQ queues are scheduled for transmission in accordance with their configured weight. The weight represents a ratio for transmission. The higher the weight of one queue compared to an other, the more often this queue is scheduled for transmission.
  – For example, a queue with weight 4000 is served twice more often than the queue with weight 2000.
- **Strict High Priority:** For a given port, packets in the strict high priority queue are scheduled for transmission before any packet in the WFQ queue. When there are multiple strict high priority queues configured for a port, the queues with a higher physical number are scheduled first.
- **Strict Low Priority:** For a given port, packets in the strict low priority queue are scheduled for transmission after any packet in the WFQ queue. When there are multiple strict low priority queues configured for a port, the queues with a higher physical number are scheduled first.

3.7.5.7 Congestion Management

The Gigabit Ethernet Switch Macro provides protection for the internal buffer from congestion and overflow.

When the shared buffer is fully occupied and does not have enough resources to receive any new frame, the incoming frames on all ports are discarded, until the congestion condition is relieved.

In addition, the Gigabit Ethernet Switch Macro provides two segment thresholds per color globally, per color per each egress port and per color per each egress queue. Based on the configured thresholds and the global, port or queue segment filling level a decision is made for every incoming packet, whether the packet with a given color can be enqueued or not. This protection mechanism is called Active Congestion Management (ACM).

The color of the packets is decided based on the conformance rate in the metering instance. See **Rate Metering** for details. The thresholds are checked with accordance to the incoming packet color: e.g., red thresholds for red colored packets, yellow for yellow and green for green.
The Gigabit Ethernet Switch Macro is able to reserve buffer per egress queue. This allows the protection of queues against congestion caused by other queues and ports. It provides a minimum buffer guarantee for each queue. A green frame can bypass ACM and is always accepted by the queue when the reserved buffer threshold of the queue is not exceeded.
The critical frames bypass the ACM and are enqueued regardless of the filling level. The critical frames are not enqueued only in case of buffer full event.
The ACM function discards the frames early (before the buffer full event) with certain drop probability. ACM thresholds provide the following functionality:

- MIN Threshold. When the filling level of the queue is below this threshold (excluding the threshold value), the packet with the appropriate color is not discarded and is enqueued.
- MAX Threshold. When the filling level of the queue is above this threshold (excluding the threshold value), the packet with the appropriate color is discarded.
- ½(MAX-MIN) Threshold. when filling level of the queue is between the MIN and MAX thresholds, the packet is discarded with certain probability. The drop probability profile can be selected globally between 25%, 50% and 75%. When the filling level is below half the distance between MIN and MAX thresholds, the packet is discarded with lower probability (P_{min}), when the filling level is above half the distance between MIN and MAX thresholds, the packet is discarded with higher probability (P_{max}). Specifically, the following drop probability profiles can be selected globally:
  – P0: P_{min} = 25%, P_{max} = 75% (default).
  – P1: P_{min} = 25%, P_{max} = 50%.
  – P2: P_{min} = 50%, P_{max} = 50%.
  – P3: P_{min} = 50%, P_{max} = 75%.

Note: When MIN = MAX, the drop probability changes from 0% to 100% at once.

Figure 42 shows drop probability as a function of queue filling level and configured thresholds.

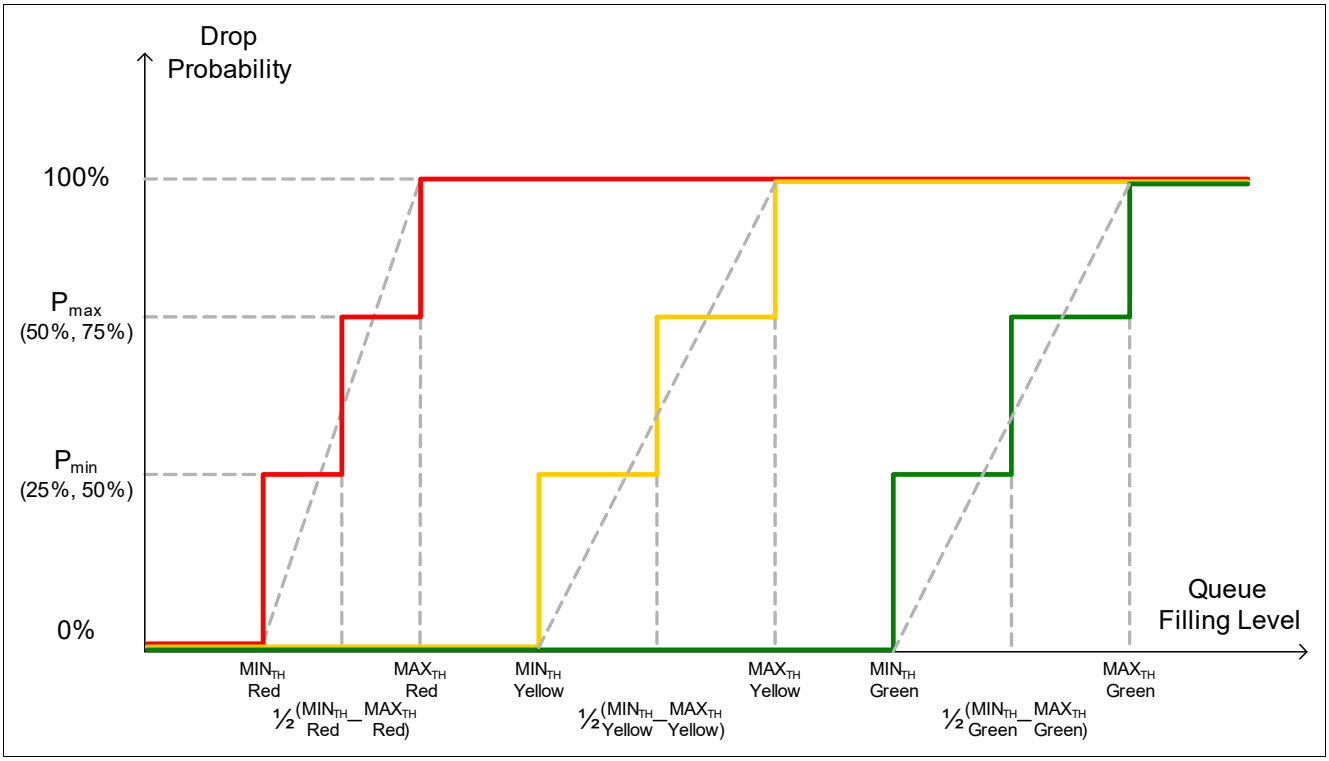


Figure 42 Drop Precedence Thresholds

Note: The thresholds for red frames shown in the figure are below the threshold for yellow frames and the thresholds for yellow are below the thresholds for green frames. This is how it would be usually configured in a real application scenarios. The thresholds can be configured MIN_{TH}=MAX_{TH}, in this case the frames are dropped as soon as they pass the drop threshold.

3.7.5.8 Ingress Port Congestion Based Flow Control

Flow control is activated when the ingress port local buffer congestion level exceeds a programmable local threshold (via SDMA_PFCTHR9 of each port) and deactivated when the local buffer congestion level drops below a programmable local threshold (via SDMA_PFCTHR8 of each port). The flow control applies to each port individually.

All ingress port congestion status are readable via SDMA_CGNBP register. Any change of congestion status can trigger the interrupt.

3.7.5.9 Overview of the Resource Protection Mechanism

The Gigabit Ethernet Switch Macro provides several mechanism to protects its limited resources. The limited resources are:

- number of segments (total 512 segments)
- number of packet pointers (total 1024 pointers)

The limitation can be on different levels:

- Global Packet Pointers Usage
- Global Shared Segment Buffer Usage
- Ingress Port Shared Segment Buffer Usage
- Egress Port Shared Segment Buffer Usage
- Egress Queue Shared Segment Buffer Usage

The limiting mechanisms are:

- Flow Control
- Buffer Reservation
- Tail Drop
- WRED

Resource Protection

One method to protect the GSWIP from running out of resources is by issuing Flow Control. Several thresholds are provided.

There are three level flow control thresholds. When any one of the start flow control conditions below is met, start flow control is triggered on a port. When all the stop flow control conditions below are met, stop flow control is triggered on a port.

- Flow control based on global buffer filling level
- Flow control based on ingress port buffer filling level
- Flow control based on ingress port metering result.

Flow Control can be used together with the WRED thresholds. In this case, the Flow Control thresholds and the WRED thresholds must be coordinated. With WRED it is possible to configure a global color threshold, per port per color threshold or per queue per color threshold for red/yellow/green packets. When the max threshold is exceeded the frame is dropped. Filling levels between the min threshold and max threshold are dropped with a global configurable drop probability. Filling levels below the min threshold do not result in a drop. WRED can be used to avoid a situation where one queue uses up all the resources and affect the traffic on other queues. Typically a system is configured with a certain oversubscription which gives each queue enough resources to operate in a bursty environment but the situation that ports affect each other cannot be avoided.

When frame drops must be avoided the only possibility is to use Flow Control. Flow control threshold must be lower than the WRED and tail drop threshold.

Critical frames are accepted by WRED even when the thresholds are exceeded.

Green frames are accepted by WRED when the egress queue buffer usage is below the reserve buffer threshold.

Table 36 Resource Protection Options

Level	Mechanism	Resource	Number of Thresholds	Granularity	Register (default values)
Global Packet Pointer Usage	Flow Control	Packet pointers	1 (THR7)	Global	SDMA_FCTHR7(MAX)
	Tail Drop	Packet pointers	3 (one per color)	Global per color	BM_DROP_GTH_0 (MAX) red BM_DROP_GTH_1 (MAX) yellow BM_DROP_GTH_2 (MAX) green
Global Shared Segment Buffer Usage	Flow Control	Segments	4 (THR1-4)	Global	SDMA_FCTHR1 (0x82) SDMA_FCTHR2 (0xAC) SDMA_FCTHR3 (0xAC) SDMA_FCTHR4 (0xAC)
	Tail Drop	Segments	2 (THR5-6)	Global	SDMA_FCTHR5 (MAX) SDMA_FCTHR6 (MAX)
	WRED[1) 2)]	Segments	6 (two per color)	Global per color	BM_WRED_RTH_0 (MAX) BM_WRED_RTH_1 (MAX) BM_WRED_YTH_0 (MAX) BM_WRED_YTH_1 (MAX) BM_WRED_GTH_0 (MAX) BM_WRED_GTH_0 (MAX)
Ingress Port Shared Segment Buffer Usage	Flow Control	Segments	Two per port	Per ingress port	SDMA_PFCTH8 (MAX) SDMA_PFCTH9 (MAX)
Egress Port Shared Segment Buffer Usage	WRED	Segments	Two per port per color	Per egress port and per color	BM_PWRED_RTH_0 (MAX) BM_PWRED_RTH_1 (MAX) BM_PWRED_YTH_0 (MAX) BM_PWRED_YTH_1 (MAX) BM_PWRED_GTH_0 (MAX) BM_PWRED_GTH_0 (MAX)
Queue	Buffer Reservation	Segments	One per queue	Per queue	PQM Context Table • reservation threshold (0)
	WRED	Segments	Two per queue per color	Per queue and per color	PQM Context Table • red max threshold (0x50) • red min threshold (0x50) • yellow max threshold (0x50) • yellow min threshold (0x50) • green max threshold (0x50) • green min threshold (0x50)

1) The drop probability can only be configured globally BM_QUEUE_GCTRL.DPROB (00 => Pmin = 25%, Pmax = 75%).
2) Tail Drop is realized by setting the min/max thresholds equal.

ACM and Flow Control

ACM and Flow control can be configured individually. Typically the two features are used exclusively.

- ACM is used to avoid that a single queue can use up all the resources. When a limit is exceeded additional frames to this queue are dropped. Frame switching between other ports is still possible.
- Flow Control is used to avoid frame drops. Before the global resource is used up the peers are informed to stop frame transmission.
- With buffer reservation and suitable ACM WRED threshold, non-congested queues are protected and do not stopped by congested queues.

3.7.5.10 Storm Control

The Gigabit Ethernet Switch Macro supports a broadcast storm control function. Broadcast storm is defined as an excessive amount of broadcast, multicast, or unknown unicast Ethernet frames received on a switch port. Due to the massive replication of data frames, broadcast storm can significantly degrade the system performance. Broadcast storm can also be a form of Denial-of-Service (DoS) attack.

The storm control function can effectively police specific traffic type and protect the resources from being flooded by the broadcast traffic.

The selected metering instance is configured to the required policed rate of the broadcast storm. The following traffic types can be selected for the storm control function:

- Broadcast frames
- Unknown multicast frames
- Unknown unicast frames

When the rate of the selected frame types exceeds the rate configured in the meter instance, the frames marked as yellow or red. When the active congestion management thresholds configured appropriately, the storm frames are discarded.

3.7.6 Flow Classification Function

The Gigabit Ethernet Switch Macro includes a powerful packet classification engine that performs multi-field classification based on up to 64 programmable rules.

Traffic Flow Table

Traffic Flow table contains up to 64 programmable rules. Rules can be configured per ingress port but can also be shared between ports. Each rule consists of a pattern and action sections, as depicted in **Figure 43**. A Pattern specifies certain combination of packet header fields. The Parser extracts the packet header fields from the received packet and provides them to the Traffic Flow table. When a pattern matches, the enabled actions apply. The pattern search continues until all actions are satisfied. This allows the definition of multiple pattern for different actions. Each action can be specifically enabled or disabled for a given pattern.

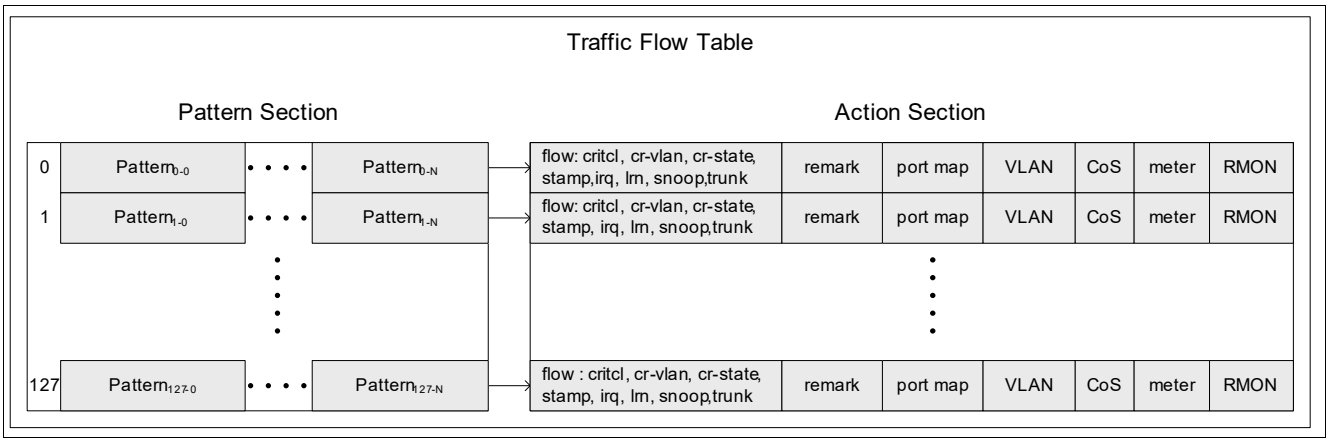


Figure 43 Traffic Flow Table

Rules location in the table defines their priority, rule entries with lower index number have higher priority. The Traffic Flow table is searched in a following way:

- **Pattern Match:** Pattern row is considered matched when all the fields in the pattern have been matched or configured to be ignored (not enabled). When a pattern row matches, the appropriate action row is checked for that pattern.
  Note: Multiple pattern rows in the table might match the search, however, only the first pattern in the table matched for certain action is applied.
- **Action Match:**
  Each action in the action row can be enabled or disabled for certain pattern row match. When the action is enabled and the pattern row matched, this action is applied for the classified packet. The search in the table terminates only when all the actions in the action section have been found. When not, the search continues for the next pattern match and the corresponding action match. An additional option is to enable the action and to select a default behavior for that action, i.e., the search for another enabled action is terminated.
  Note: For a given packet classification only one pattern may match one specific action, however, multiple patterns may match multiple different actions, i.e., the action section is searched independently for each action type.
  See the following examples for clarification:
  – First example: Consider two rules added to the table, one has a source MAC address in the pattern and a CoS assignment in the action section. Another rule (at different index) has an Ethertype in the pattern section and the action is a VLAN group association. When an incoming frame matches both patterns, both actions are applied for this frame.
  – Second example: Consider a similar scenario as in the first example, whereas the only the action is VLAN group association for both pattern rows. In this case, only the rule with the lowest index is applied, i.e., similar action is executed with priority of the rule depending on the location in the table.

Pattern Section

The pattern section contains the packet header fields and other parameters that can identify the incoming packet flow. Specifically, the following pattern fields are supported:

- Ingress port number. The parameter compared with the ingress port number of the incoming packet.
- Source MAC Address or part of the MAC Address specified by a programmable nibble mask[1)].
- Destination MAC Address or part of the MAC Address specified by a programmable nibble mask[1)].
- STAG VID or part of the STAG VID specified by a programmable nibble mask or a range.
- CTAG VID or part of the CTAG VID specified by a programmable nibble mask or a range.
- Ethernet type.
- IP Protocol and Parser Flags.
- PPPoE Session ID.
- IP Packet Length or length range.
- Source IP Address or part of the IP Address specified by a programmable nibble mask[1)].
- Destination IP Address or part of the IP Address specified by a programmable nibble mask[1)].
- CTAG PCP Code. This parameter is directly compared with the PCP code of the VLAN tag of the received frame. When the received frame contains no VLAN/Priority Tag, the parameter does not match.
- STAG PCP&DEI. This parameter is directly compared with the PCP&DEI of the VLAN tag of the received frame. When the received frame contains no VLAN/Priority Tag, the parameter does not match.
- DSCP Code. This parameter compared directly with the DSCP code in the IP header. When the received packet contains no IP header, the parameter does not match.
- The first 4 bytes of the packet content following the IP header or first 4 bytes of packet content following the Ethertype for non IP and non PPPoE packets or first 4 bytes of packet content following the PPPoE header for non IP and PPPoE packets. For TCP/UDP the 4 bytes following the IP header are the TCP/UDP source and destination ports. Any part of this content can be masked-out by a programmable nibble mask[1)].

Each field in the pattern section is enabled or disabled for the search. When the parameter is disabled, the corresponding pattern is not compared. The pattern is considered to be matched by default for any value of the corresponding packet field.

Note: When an IP packet is carried in a PPPoE frame, the Ethertype is 0x8864 but there is no explicit Parser Flag for IP_indication and no PPP_protocol field that shows that the PPPoE carried IP. A rule mat want to forward all IPoPPPoE to a specific port. When there would be a PPP_protocol field this rule could be defined by the a match on Ethertype=0x8864 AND PPP_protocol=0x0021. Since there is no PPP_protocol field such a rule can be defined by configuring an "always match" entry in the IP address table (an entry with all masks active). When there is an IP in the PPPoE frame, the "always match" entry matches, when there is no IP in the PPPoE frame, the IP address table is not searched and the result is a "no_match" indication. With this match indications and the Ethertype=0x8864, the IP_indication flag and PPP_protocol field are not required.

Actions Section

The action section contains the actions applicable to an incoming packet. Specifically, the following are supported:

- **Port Bitmap (used as Port Map/Port Member/Flow_ID):** The received packet (packet flow) can be redirected to a single or multiple egress ports based on a pattern match. Redirection includes the packet discard option when the packet is redirected to the NULL port (all zero port map). Based on the port bitmap multiplexing control in the action, this field is also used as STAG port member which identifies the broadcast domain. The broadcast domain of the received packet is restricted according to the this field on top of the other filtering function. When the Flow_ID action is configured, the field holds the Flow_ID instead of the port map or port member. The Flow_ID can be written into the egress special tag.
- **Traffic Class Assignment (CoS):** Traffic class of the received packet can be assigned or changed from a default assignment based on the pattern match.

1) Note: mask resolution is nibble, i.e., every 4 bits can be masked out.

- **VLAN Assignment:** VLAN classification of the received packet can be assigned or changed from a default assignment based on the pattern match. Both service VLAN tag and customer VLAN tag are supported.
- **Metering Assignment:** A Metering instance can be assigned or changed from a default assignment based on the pattern match.
- **RMON Assignment:** Dedicated packet counters can be assigned to a specific flow. The counters are incremented each time the pattern is matched.
- **Flow Actions:** The following additional flow actions can be assigned only in the flow table (by default these actions are disabled):
  - Cross VLAN packet indication. Certain packet can be identified as cross VLAN. VLAN filtering rules are ignored for these packets, e.g, cross VLAN packets may cross VLAN boundaries.
  - Cross state packet indication. Certain packet can be configured to ignore the port state of the ingress or egress port. These packets are forwarded even when all the “regular” frames are discarded.
  - Critical packet indication. Packets identified as critical bypass active congestion management function (ACM) and are enqueued to a certain queue regardless of the filling level of that queue.
  - Time stamping. Ingress/egress time stamp can be recorded for packets identified by matched pattern. The time stamps are sampled during packet reception/transmission and can be retrieved by the management action.
  - Interrupt request assertion. An external interrupt can be asserted based on a pattern match.
  - Learning action. Learning function can be forced to be enabled or disabled.
  - Snooping action. A specific IGMP snooping action can be selected for the IGMP messages. Note, relevant only for the IGMP hardware based snooping.
  - Flow_ID action. A Flow indication can be configured and written into the egress Special Tag. See **Special Tag Functionality** for more details.
  - Forwarding Multiplexing Control. These control signals select the appropriate Port-Map in Forwarding Classification.
  - Port Bitmap Multiplexing Control. This control signal select the port bitmap mode: used as STAG Port-Map or Port-Member in Forwarding Classification.
  - Trunking Link Selection. The destination trunking link can be assigned or changed from a default assignment based on the pattern match.

Each single action in the action section can be enabled or disabled for the search. When an action is disabled, the table search continues until another pattern matches for this action. When no other pattern matches, the corresponding action is not applied.

3.7.7 Operation, Administration, and Management Functions

This section summarizes the functions provided to control and monitor the data traffic through the switch.

3.7.7.1 Monitoring Counters

Multiple counters are provided per port to monitor incoming and outgoing data traffic as well as errors or special events. Each port provides the same set of counters. There are two main groups of counters, which are a set of standard Ethernet counters (also known as RMON counters) and a group of counters assigned to programmable traffic flows. See the following sections for details.

Standard (RMON) Counters

The Gigabit Ethernet Switch Macro supports 34 standard frame counters of 32-bit each and 3 byte counters of 64-bit each. The counters are not cleared on read, instead complete set of port counters can be cleared by the appropriate management action. It can be configured when the 8 byte special tag is excluded from the byte counters. **Table 37** lists the standard RMON counters.

Table 37 Standard RMON Counters

Short Name	Long Name	Description
Receive Counters		
nRxUnicastPkts	Received Unicast Ethernet frames	Counts the total number of valid[1)] Unicast Ethernet frames received on the ingress port.
nRxTotalPkts	Received Total Ethernet frames or Broadcast Ethernet frames	Counts the total number of valid[1)] Ethernet frames or total number of valid Broadcast Ethernet frames received on the ingress port. The mode is configurable via BCAST_CNT bit in BM_RMON_CTRL
nRxMulticastPkts	Received Multicast Ethernet frames	Counts the total number of valid[1)] Multicast Ethernet frames (not including Broadcast frames) received on the ingress port.
nRxFCSErrorPkts	Received CRC errors	Counts the total number of Ethernet frames that have been received with an FCS error.
nRxUnderSizeGoodPkts	Received good undersized Ethernet frames	Counts the total number of Ethernet frames received with Undersize Error but with correct FCS.
nRxUnderSizeErrorPkts	Received bad undersized Ethernet frames	Counts the total number of Ethernet frames received with Undersize Error and bad FCS.
nRxOversizeGoodPkts	Received good oversized Ethernet frames	Counts the total number of Ethernet frames received with Oversize Error but with correct FCS.
nRxOversizeErrorPkts	Received bad oversized Ethernet frames	Counts the total number of Ethernet frames received with Oversize Error and bad FCS.

Table 37 Standard RMON Counters (cont'd)

Short Name	Long Name	Description
nRxGoodPausePkts	Received good Pause Ethernet frames	Counts the total number of received valid[1)] Ethernet Pause frames.
nRxAlignErrorPkts	Received alignment errors	Counts the total number of packets received with a • alignment error or • length errors or • phy_rx errors or • all errors of above The error which must be counted can be configured globally. Error ignore flags are not considered (counting is done) only in the "all" case. An alignment error is specified as a non-integral number of octets.
nRx64BytePkts	Received frame size 64 byte	Counts the total number of valid[1)] Ethernet frames received with the minimum valid length of 64 byte.
nRx127BytePkts	Received frame size 65-127 byte	Counts the total number of valid[1)] Ethernet frames received with a length in the range of 65 to 127 byte.
nRx255BytePkts	Received frame size 128-255 byte	Counts the total number of valid[1)] Ethernet frames received with a length in the range of 128 to 255 byte.
nRx511BytePkts	Received frame size 256-511 byte	Counts the total number of valid[1)] Ethernet frames received with a length in the range of 256 to 511 byte.
nRx1023BytePkts	Received frame size 512-1023 byte	Counts the total number of valid[1)] Ethernet frames received with a length in the range of 512 to 1023 byte.
nRxMaxBytePkts	Received frame size larger than 1023 byte	Counts the total number of valid[1)] Ethernet frames received with a length of 1024 byte or more. *Note: When Jumbo frames are enabled on the related port, these frames are also included in this counter.*
nRxDroppedPkts	Receive dropped Ethernet frames	Counts the total number of frames discarded due to the lack of shared resources, i.e., in case of complete buffer congestion.
nRxFilteredPkts	Received filtered Ethernet frames	Counts the total number of Ethernet frames discarded due to a violation detected by the Classification Engine, i.e., frame filtering based on matched multi-field classification rule.
nRxGoodBytes	Received good bytes	Total number of bytes received in valid[1)] Ethernet frames. This is a 64-bit counter

Table 37 Standard RMON Counters (cont'd)

Short Name	Long Name	Description
nRxBadBytes	Received bad bytes	Total number of bytes received in invalid Ethernet frames. This is a 64-bit counter
Transmit Counters		
nTxACMDiscardPkts	Transmit Queue ACM Discard frames	Counts the total number of packets discarded by the ACM mechanism (Active Congestion Management) due to exceeded thresholds on the egress QoS queues.
nTxUnicastPkts	Transmitted Unicast Ethernet frames	Counts the total number of Unicast Ethernet frames transmitted on the egress port.
nTxTotalPkts	Transmitted Total Ethernet frames or Broadcast Ethernet frames	Counts the total number of total frames or Broadcast frames transmitted on the egress port. The mode is configurable via BCAST_CNT bit in BM_RMON_CTRL.
nTxMulticastPkts	Transmitted Multicast Ethernet frames	Counts the total number of Multicast Ethernet frames (not including Broadcast frames) transmitted on the egress port.
nTx64BytePkts	Transmitted frame size 64 byte	Counts the total number of Ethernet frames transmitted with the minimum valid length of 64 byte.
nTx127BytePkts	Transmitted frame size 65-127 byte	Counts the total number of Ethernet frames transmitted with a length in the range of 65 to 127 byte.
nTx255BytePkts	Transmitted frame size 128-255 byte	Counts the total number of Ethernet frames transmitted with a length in the range of 128 to 255 byte.
nTx511BytePkts	Transmitted frame size 256-511 byte	Counts the total number of Ethernet frames transmitted with a length in the range of 256 to 511 byte.
nTx1023BytePkts	Transmitted frame size 512-1023 byte	Counts the total number of Ethernet frames transmitted with a length in the range of 512 to 1023 byte.
nTxMaxBytePkts	Transmitted frame size larger than 1023 byte	Counts the total number of Ethernet frames transmitted with a length of 1024 byte or more. *Note: When Jumbo frames are enabled on the related port, these frames are also included in this counter.*
nTxCollCount	Transmitted total collision number	Counts the total number of Ethernet frames transmitted on the egress port after any "Collision" event.
nTxSingleCollCount	Transmitted single collisions	Counts the total number of Ethernet frames transmitted on the egress port after a "Single Collision" event.

Table 37 Standard RMON Counters (cont'd)

Short Name	Long Name	Description
nTxMultCollCount	Transmitted multiple collisions	Counts the total number of Ethernet frames transmitted on the egress port after a "Multiple Collision" event.
nTxLateCollCount	Transmitted late collisions	Counts the total number of Ethernet frames transmitted on the egress port after a "Late Collision" event.
nTxExcessCollCount	Transmitted excessive collisions	Counts the total number of Ethernet frames transmitted on the egress port after an "Excessive Collision" event.
nTxPauseCount	Transmitted Pause frames	Counts the total number of "Pause" frames transmitted on the egress port.
nTxDroppedPkts	Transmit dropped frames	Counts the total number of packets discarded due to port disable, excess collision or late collision.
nTxGoodBytes	Transmitted good bytes	Total number of bytes transmitted in Ethernet frames. This is a 64-bit counter.

1) Every packet received without any reception error is considered to be valid. This includes Unicast, Multicast and Broadcast packets.

Traffic Flow Counters

There is a set of 24 packet-based counters available per port, where each can be assigned to a dedicated traffic flow, as specified in the Traffic Flow table. Each traffic flow is defined by an entry in the traffic flow table, counters are connected with a traffic flow in a flexible way. The counter number is entered as one of the table actions. See **Flow Classification Function** for details.

3.7.7.2 Port Mirroring

The Gigabit Ethernet Switch Macro supports port monitoring to assist in system debugging or enable a software-controlled functionality. The data received on a selected port may be mirrored to another selected port (the monitoring port).

Mirroring Function

Mirroring means the received frame is processed and forwarded as normal, but a copy of that frame is in addition sent to the monitoring port. The options given by the port mirroring function are:

- Copy data received on a selected port to the monitoring port.
- Copy data received on a selected group of ports to the monitoring port.
- Copy data transmitted on a selected port to the monitoring port.
- Copy data transmitted on a selected group of ports to the monitoring port.
- Copy data received or transmitted on a selected port to the monitoring port.
- Copy data received or transmitted on a selected group of ports to the monitoring port.

Figure 44 and **Figure 45** provide illustrations on the ingress and egress monitoring.

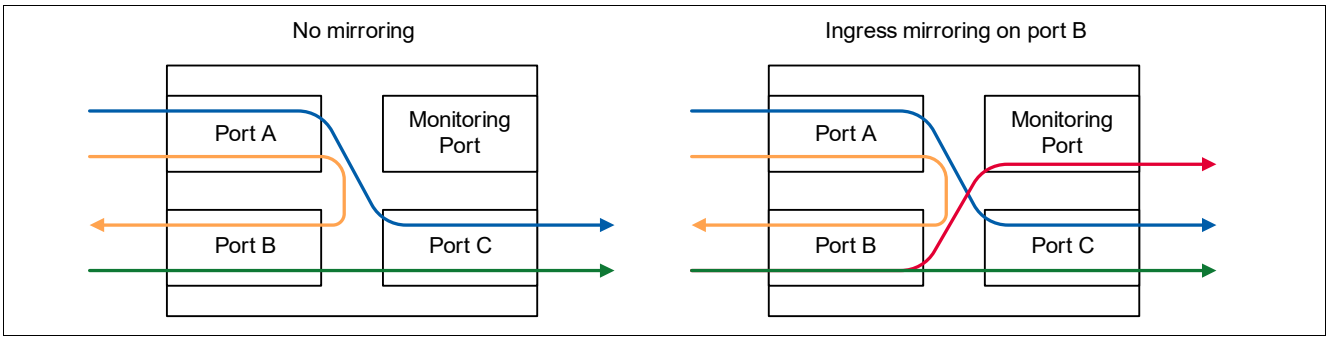


Figure 44 Port Mirroring Examples – Ingress Monitoring

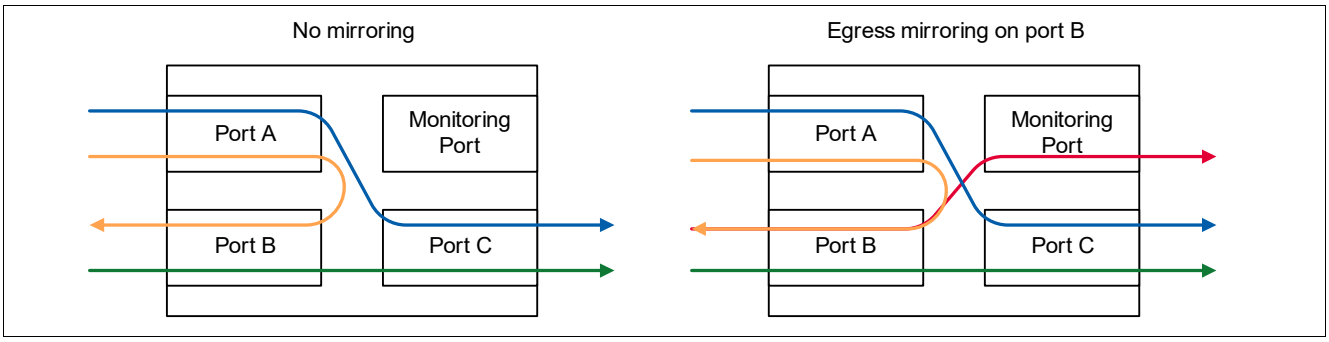


Figure 45 Port Mirroring Examples – Egress Monitoring

Mirroring can also be used to create diagnostic loopbacks, when the ingress port is identical to the monitoring port.

Error Monitoring

The mirroring function is used to monitor frames otherwise dropped due to reception errors, packet filtering, or violation of certain classification rules. In this case, the received frame is only delivered to the monitoring port and not to the target egress port defined in the egress port map.

Error monitoring can be explicitly enabled for the following type of violations:

- Frame dropped by the classification engine (the destination port map is all-zero)
- Frame contains L2 reception errors
- Frame contains an unknown VLAN ID (the frame carries a VLAN ID that has not been defined in the active VLAN table)

- VLAN Ingress rule violation (acceptable frame filter, i.e. “admit all tagged”)
- Ingress or egress VLAN membership violation (the frame carries a known VLAN ID, but the port is not member of the VLAN group)
- Port state violation
- MAC learning limit violation (the maximum number of MAC addresses to be learned for the port has been exceeded)
- MAC port lock or spoofing detection violation (the MAC source address has already been learned on another port)

3.7.7.3 Wake-on-LAN Functionality

Wake-on-LAN functionality (WoL) is used to wake up a network device by sending a dedicated Layer-2/Layer-3 data packet. The Gigabit Ethernet Switch Macro detects such packets on its Ethernet input ports and triggers an interrupt. This interrupt can be used to wake up an external device, such as a router connected to the switch. Particularly, the following functions are provided:

- Detects “magic packets”
  - Addressed to a dedicated unicast MAC destination address
  - Addressed to a known multicast destination address
  - Addressed to the broadcast MAC destination address
- Password protection can be enabled for magic packets
- Programmable target MAC address
- WoL Interrupt
- WoL packet receive port indication
- WoL enable/disable per port
- Magic packets are forwarded as any other packets (for example based on the MAC destination address) but may as well be dropped when the frame classification is set up accordingly.

In addition to these standard WoL functions, a wake-up can be triggered by making an entry in the Flow Engine and programing a corresponding action to generate an interrupt. This allows to wake up for any frame pattern. Typical patterns are:

- a specified MAC destination address
- a specified MAC source address
- ARP request packets
- directed IPv4/IPv6 packets

Figure 46 shows the typical Layer-2 magic packets structure. However the fixed pattern followed by the specific unicast address and an optional password can appear in any field location in a packet, including Layer-3 part.

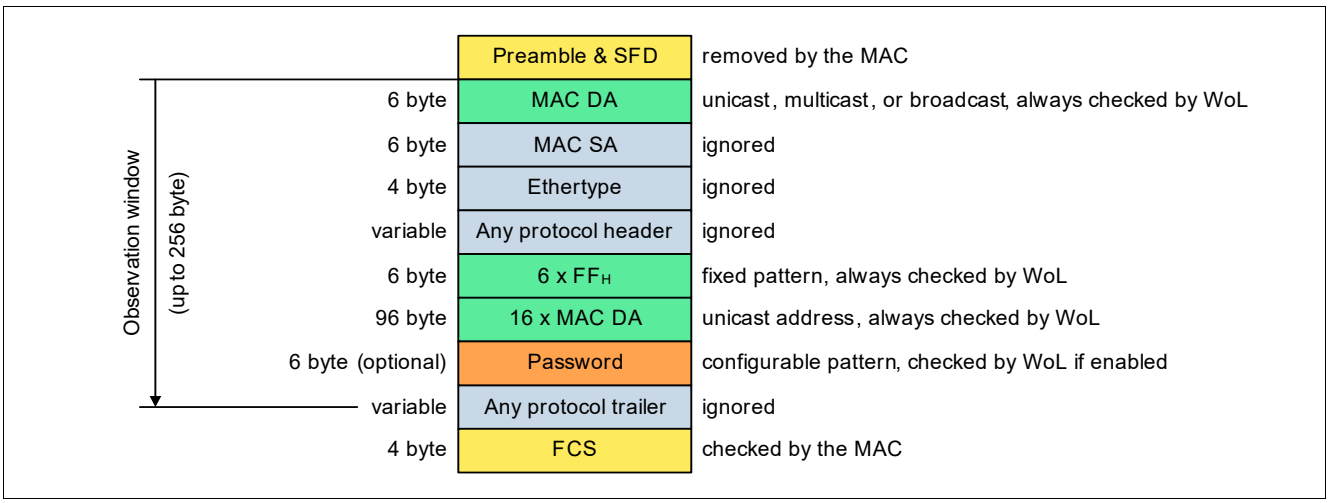


Figure 46 Typical Magic Packet Data Structure

The WoL sequence starts with a synchronization pattern of 6 × FF, followed by 16 repetitions of the target system's MAC address. This must be the unicast address, while the MAC destination address in the layer-2 header may be either the unicast address, the broadcast address, or a multicast address of a group that contains the target system's address. After the WoL pattern, any protocol-specific trailer may follow and the frame must be terminated by a valid frame checksum (FCS). The frame size must be less or equal to the maximum allowed frame size.

As an option, a password can be defined and checked for the received WoL frames. When the password does not match the configured value, the frame is ignored. The password has the same size as the MAC address (6 byte). **Figure 47** shows the frame structure of a typical Layer-2 password-protected WoL frames.

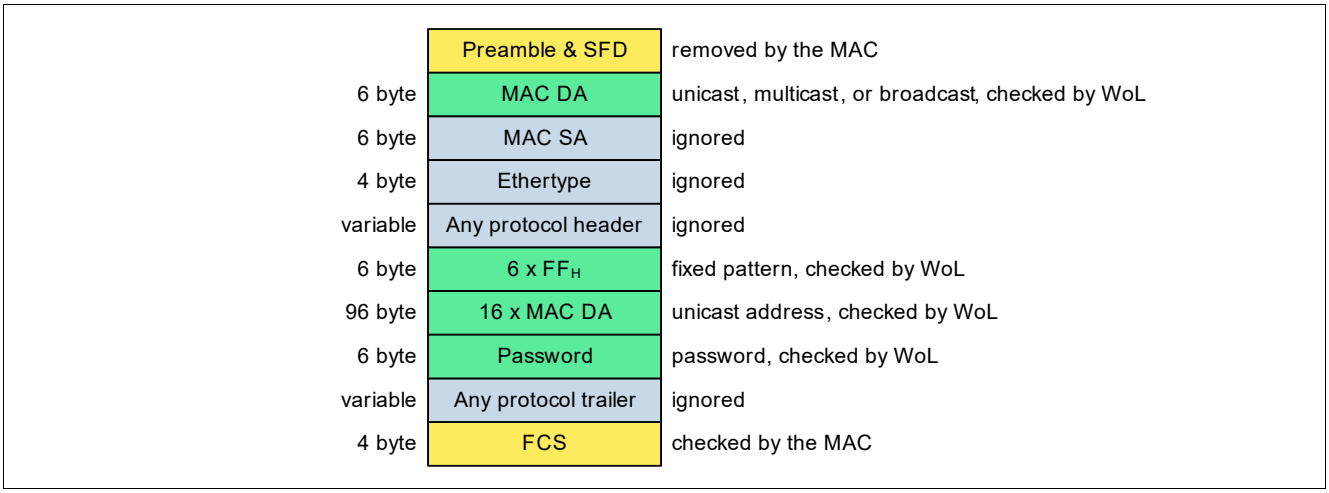


Figure 47 Magic Packet Data Structure – Password Protection

3.7.7.4 Time Stamp Functionality

A 94-bit global timer is implemented. It has three parts: a 32-bit second field, a 30-bit nano-second field and a 32-bit fractional-nano-second field. The global timer can be modified directly, adjusted with a positive/negative value or adjusted with a frequency offset via the following registers: TIMER_FS_LSB, TIMER_FS_MSB, TIMER_NS_LSB, TIMER_NS_MSB, TIMER_SEC_LSB, TIMER_SEC_MSB and TIMER_CTRL.

The Gigabit Ethernet Switch Macro can record a time stamp during frame reception and transmission to support IEEE 1588v2. The time stamp is recorded in hardware at the moment of reception (on ingress) or transmission (on egress) of the first byte of destination MAC address on the attached interface, as described in the **Figure 48**.

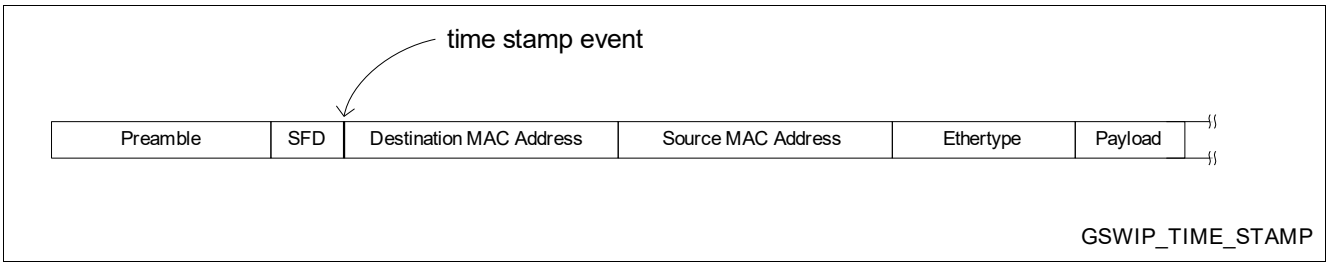


Figure 48 Time Stamp Event Location in the Frame

To have the time stamp recorded for a specific frame type, an appropriate rule must be added to the Traffic Flow table and a time stamp action selected for ingress time stamp, egress or both. In addition, an interrupt can be generated at the event of the time stamp record. The current timestamp value (2 least significant bit of second field and 30-bit nano-second field) is stored in a register, per port one register for the ingress arrival time (SDMA_TSTAMP0 and SDMA_TSTAMP1) and for the egress departure time (FDMA_TSTAMP0 and FDMA_TSTAMP1) is provided. The time stamp can be retrieved by an appropriate management action.

3.7.7.5 Special Tag Functionality

The special tag is used to override the forwarding and QoS functionality of the switch on the ingress side and to provide additional frame-status information on the egress side.

The special tag is identified by the special Ethertype located after the source MAC address in the frame. This allows the transmission of the frame via an Ethernet network to a remote receiver. The special tag content has a fixed length of 6 bytes. For internal communication or point-to-point communication it can be configured per egress port when the frame contains additional content in place of the Ethertype. This option is only available at egress direction, in ingress direction always an Ethertype is expected. See **Figure 49**.

The pause frames generated by the MAC do not contain a special tag. This may result in a mix of frames with and without special tag on one egress port. Frames with a special tag which do not use the special Ethertype can be distinguished from pause frames since the pause frames have an Ethertype of 0x8808 while the first nibble after the MAC addresses is 0 for frames with a special tag.

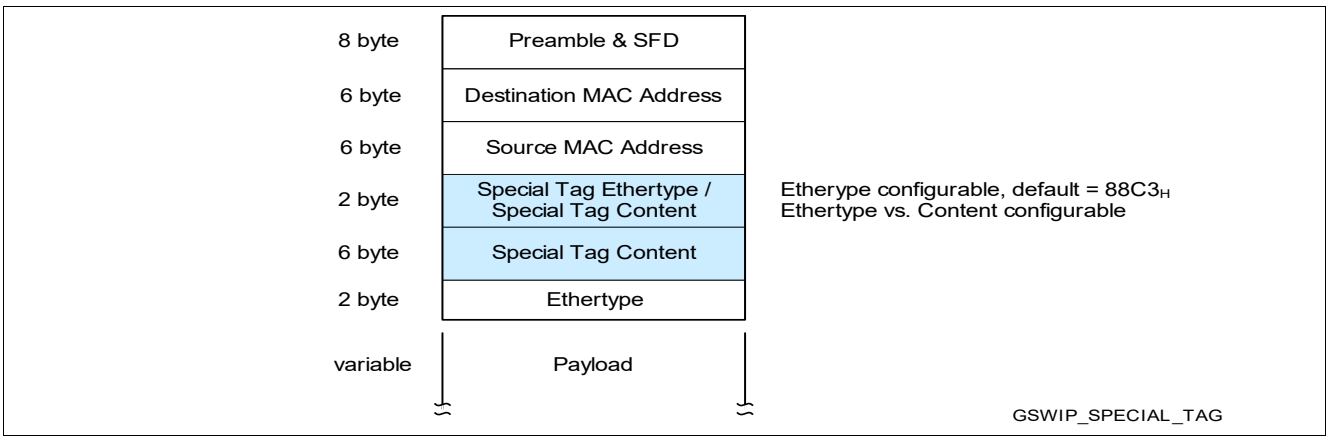


Figure 49 Special Tag Location in the Frame

Note: The special tag is used on the CPU port of the switch.

The content format of the special tag is different for the ingress and the egress, the egress special tag comes in two formats (internal and external format). The following sections describe the different formats of the tag.

Ingress Special Tag

The ingress special tag is used to override the classification function and the default frame forwarding of the switch. The special tag detection on ingress is enabled or disabled per port. When the detection is disabled, the frame containing a special tag is treated as regular frame and the content of the frame is ignored.

When the ingress special tag detection is enabled, the content of the tag is used for the frame forwarding decision. The ingress special tag must always have a special tag Ethertype. See **Table 38** for details.

Table 38 Special Tag Ingress Format

Byte	Bit	Description
0	[7:0]	**Ethertype byte** 1 (configurable, default: 88_H)
1	[7:0]	**Ethertype byte** 2 (configurable, default: $C3_H$)
2	7	**Port map enable** (1_B = use port map, 0_B = use port mask)
	6	**Traffic class enable** (1_B = use traffic class, 0_B = ignore)
	5	**Time stamp enable** (1_B = generate time stamps, 0_B = ignore)
	4	**Force no learning** (1_B = address is not learned, 0_B = ignore)
	[3:0]	**Target traffic class** (egress priority)

Table 38 Special Tag Ingress Format (cont'd)

Byte	Bit	Description
3	[7:0]	**Target egress port map** (low bits)
4	[7:0]	**Target egress port map** (Reserved)
5	[7:5]	**Reserved** (all zero)
	4	**Interrupt enable** (1_B = generate an interrupt, 0_B = ignore)
	[3:0]	**Source Port** (virtual port)
6	[7:0]	**Reserved** (all zero)
7	[7:0]	**Reserved** (all zero)

Note: Bytes are defined as MSB = bit 7 and LSB = bit 0.

Table 39 and Table 40 describes the encoding of the port map enable and traffic class enable fields of the special tag content.

Table 39 Port Map Coding

Port Map Enable	Resulting Port Map
0	The egress port map is based on the forwarding classification result. The port map in the special tag is used as a filter (AND mask) on the final egress port map in the forwarding function => when a bit in the special tag port map is not set for certain egress port this port is excluded from the final egress port map.
1	The port map determined by forwarding classification result in switch is overruled. The port map in the special tag is used as the egress port map.

Table 40 Traffic Class Map Coding

Traffic Class Enable	Resulting Traffic Class
0	The traffic class is based on the classification result in switch.
1	The traffic class is taken from the special tag (classified traffic class ignored).

Additional action flags in the ingress special tag:

- Time-stamp Action. This action flag triggers the latching of the time-stamps for the received packet.
- Interrupt Action. This action generates an interrupt upon the packet reception.
- Force No Learning. This action disables the learning of the source MAC address of the received frame in the MAC bridging table.

The special tag detected on the ingress side is not delivered to the egress side. The tag is removed prior to transmission.

Egress Special Tag

The egress special tag contains status and debug information of the switch. The special tag transmission on egress is enabled or disabled per egress port. When egress special tag is disabled, no special tag is inserted in the egress frame. When egress special tag function is enabled, each egress frame transmitted on that port contains the special tag.

The egress special tag is transmitted in one of the two formats:

- **External format.** This format contains Ethertype (2 bytes) and content (6 bytes).
- **Internal format.** This format contains no Ethertype and only content (8 bytes).

The external format can be used to transport the special tag via a network, the internal format is used for directly attached devices like a CPU which know how handle the special frame format. See **Table 41** and **Table 42** for details.

Note: Bytes are defined as MSB = bit 7 and LSB = bit 0.

Table 41 Special Tag Egress External Format (with Ethertype)

Byte	Bit	Description
0	[7:0]	**Ethertype** byte 1 (configurable, default: 88_H)
1	[7:0]	**Ethertype** byte 2 (configurable, default: $C3_H$)
2	[7:4]	**Traffic Class** The traffic class of the packet determined by the switch classification engine.
	[3:0]	**Ingress port number** (000_B = port 0, …, 110_B = port 6, ...)
3	7	**PPPoE Session Packet** 0_B The packet is not PPPoE session packet 1_B The packet is PPPoE session packet
	6	**IPv4 Packet** 0_B The packet is IPv6 packet when IP offset != 0 1_B The packet is IPv4 packet when IP offset != 0
	[5:0]	**IP Offset**[1]. It defines the byte offset of the first byte in IP field relative to the first byte of destination MAC address of the egress packet
4	[7:0]	**Destination Logical Port Map (low bits)**
5	[7:0]	**Destination Logical Port Map (Reserved)**
6	7	**Mirror indication**, signals when the frame has been mirrored. 0_B **NORM** normal frame 1_B **MIRR** mirrored frame
	6	**Known L2 unicast/multicast** 0_B The packet destination MAC does not match one entry in bridging table. 0_B The packet destination MAC matches one entry in bridging table.
	[5:0]	**Packet Length High Bits**[1] The total number of bytes in the egress packet.
7	[7:0]	**Packet Length Low Bits**[1] The total number of bytes in the egress packet.

1) When a packet is modified at the egress side (packet header modification) with new bytes inserted or removed, the Is Tagged Flag, IP Offset and Packet Length fields are updated accordingly and contain the adjusted value for the transmitted frame. The IP_Offset and the Packet_Length includes the length of the special tag.

Table 42 Special Tag Egress Internal Format (without Ethertype)

Byte	Bit	Description
0	[7:4]	**Reserved** (all zero). Serves also as code to distinguish pause frames generated by the MAC from frames with special tag without Ethertype since pause frames start with “8” and not 0.
	3	**Receive error** indication (MAC error) 0_B **OK** Frame is Ok 1_B **ERR** Frame contains a MAC error
	2	**Drop indication**, signals when a mirrored packet has been dropped (delivered only to the mirror port) or has been forwarded (delivered normally and to the mirror port) 0_B **FWD** frame has been forwarded 1_B **DROP** frame has been dropped
	[1:0]	**Drop precedence**, defines when the frame must be eligible for dropping. 00_B **CRT** Critical frame indication 01_B **GRN** drop precedence low 10_B **YEL** drop precedence medium 11_B **RED** drop precedence high
1	[7:0]	**Flow/Error Indication** • **Flow Indication** (when Receive error = OK and drop Indication = FWD) • **Error Indication** – errored frames (when Receive error = ERR) – dropped frames (when Receive error = OK and drop Indication = DROP) The error code for discarded or errored frames are described in **Table 43**
2	[7:4]	**Traffic Class** The traffic class of the packet determined by the switch classification engine.
	[3:0]	**Ingress port number** (000_B = port 0, …, 110_B = port 6, ...)
3	7	**PPPoE Session Packet** 0_B The packet is not PPPoE session packet 1_B The packet is PPPoE session packet
	6	**IPv4 Packet** 0_B The packet is IPv6 packet when IP offset != 0 1_B The packet is IPv4 packet when IP offset != 0
	[5:0]	**IP Offset**[1)]. It defines the byte offset of the first byte in IP field relative to the first byte of destination MAC address of the egress packet
4	[7:0]	**Destination Logical Port Map (low bits)**
5	[7:0]	**Destination Logical Port Map (Reserved)**

Table 42 Special Tag Egress Internal Format (without Ethertype) (cont'd)

Byte	Bit	Description
6	7	**Mirror indication**, signals when the frame has been mirrored. 0_B **NORM** normal frame 1_B **MIRR** mirrored frame
	6	**Known L2 unicast/multicast** 0_B The packet destination MAC does not match one entry in bridging table. 0_B The packet destination MAC matches one entry in bridging table.
	[5:0]	**Packet Length High Bits**[1)] The total number of bytes in the egress packet.
7	[7:0]	**Packet Length Low Bits**[1)] The total number of bytes in the egress packet.

1) When a packet is modified at the egress side (packet header modification) with new bytes inserted or removed, the Is Tagged Flag, IP Offset and Packet Length fields are updated accordingly and contain the adjusted value for the transmitted frame. The IP_Offset and the Packet_Length includes the length of the special tag.

Table 43 Error Codes

Bit Position	Error Type
Error Indication for Frames with MAC Error (byte 0, bit 3 = ERR, byte 0, bit 2 = don't care)	
7	Undefined, reserved for future use, set to 0_B
6	Receive Error
5	Is Pause Frame
4	FCS Error
3	Length Error
2	Alignment Error
1	Frame too Long
0	Frame too Short
Violation Indication for Dropped Frames (byte 0, bit 3 = OK, byte 0, bit 2 = DROP)	
0	Egress Port State Violation
1	Ingress Port-State Violation
2	Port-Lock Violation
3	MAC Learning Limitation Violation
4	VLAN Egress Membership Violation
5	VLAN Ingress Membership Violation
6	VLAN Ingress Tag Rule Violation
7	Unknown VLAN Violation
Flow Indication for Good Frames (byte 0.3 = OK, byte 0.2 = FWD)	
07:0	Flow Identification

4 Registers

This chapter describes the registers.

4.1 Top Level PDI Registers

Table 44 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Top Level PDI Registers, GPHY Shell Registers			
GPHY0_FCR	GPHY0 Firmware Address Offset Register	$F700_H$	132
GPHY0_CFG	GPHY0 General Configuration Register	$F701_H$	133
GPHY0_AFETX_CTRL	GPHY0 AFE TX Path Control Register	$F702_H$	134
GPHY0_FCR_SD	GPHY0 Firmware Address Offset Shadow Register	$F703_H$	135
GPHY0_GPS	GPHY0 General Pin-Strapping Register	$F708_H$	136
GPHY0_BFDEV	GPHY0 Base Frequency Deviation Configuration Register	$F709_H$	137
GPHY0_STATUS	GPHY0 General Status Register	$F70F_H$	138
GPHY1_FCR	GPHY1 Firmware Address Offset Register	$F710_H$	132
GPHY1_CFG	GPHY1 General Configuration Register	$F711_H$	133
GPHY1_AFETX_CTRL	GPHY1 AFE TX Path Control Register	$F712_H$	134
GPHY1_FCR_SD	GPHY1 Firmware Address Offset Shadow Register	$F713_H$	135
GPHY1_GPS	GPHY1 General Pin-Strapping Register	$F718_H$	136
GPHY1_BFDEV	GPHY1 Base Frequency Deviation Configuration Register	$F719_H$	137
GPHY1_STATUS	GPHY1 General Status Register	$F71F_H$	138
GPHY2_FCR	GPHY2 Firmware Address Offset Register	$F720_H$	132
GPHY2_CFG	GPHY2 General Configuration Register	$F721_H$	133
GPHY2_AFETX_CTRL	GPHY2 AFE TX Path Control Register	$F722_H$	134
GPHY2_FCR_SD	GPHY2 Firmware Address Offset Shadow Register	$F723_H$	135
GPHY2_GPS	GPHY2 General Pin-Strapping Register	$F728_H$	136
GPHY2_BFDEV	GPHY2 Base Frequency Deviation Configuration Register	$F729_H$	137
GPHY2_STATUS	GPHY2 General Status Register	$F72F_H$	138
GPHY3_FCR	GPHY3 Firmware Address Offset Register	$F730_H$	132
GPHY3_CFG	GPHY3 General Configuration Register	$F731_H$	133
GPHY3_AFETX_CTRL	GPHY3 AFE TX Path Control Register	$F732_H$	134
GPHY3_FCR_SD	GPHY3 Firmware Address Offset Shadow Register	$F733_H$	135
GPHY3_GPS	GPHY3 General Pin-Strapping Register	$F738_H$	136
GPHY3_BFDEV	GPHY3 Base Frequency Deviation Configuration Register	$F739_H$	137

Table 44 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY3_STATUS	GPHY3 General Status Register	$F73F_H$	138
Top Level PDI Registers, R(G)MII Registers			
MII_CFG_5	xMII Interface 5 Configuration Register	$F100_H$	139
PCDU_5	RGMII 5 Clock Delay Configuration Register	$F101_H$	141
RTXB_CTL_5	xMII5 Interface Receive Transmit Buffer Control Register	$F120_H$	142
MII_MUX_CFG	Pin and Port Multiplexing Configuration	$F130_H$	143
PKT_INS	Packet Insertion Register	$F140_H$	144
PKT_EXT_READ	Packet Extraction Read Register	$F141_H$	145
PKT_EXT_CMD	Packet Extraction Command Register	$F142_H$	146
PCDU5_TX_KVAL	PCDU5 TX K Value	$F160_H$	146
PCDU5_TX_MREQ	PCDU5 TX M Required	$F161_H$	147
PCDU5_TX_MBLK	PCDU5 TX M Blank	$F162_H$	147
PCDU5_TX_DELLEN	PCDU5 TX Delay Length	$F163_H$	148
PCDU5_RX_KVAL	PCDU5 RX K Value	$F168_H$	148
PCDU5_RX_MREQ	PCDU5 RX M Required	$F169_H$	149
PCDU5_RX_MBLK	PCDU5 RX M Blank	$F16A_H$	149
PCDU5_RX_DELLEN	PCDU5 RX Delay Length	$F16B_H$	150
Top Level PDI Registers, MDIO Master Registers			
GSWIP_CFG	GSWIP Configuration Register	$F400_H$	151
MMDIO_CTRL	MDIO Master Control Register	$F408_H$	153
MMDIO_READ	MDIO Master Read Data Register	$F409_H$	154
MMDIO_WRITE	MDIO Master Write Data Register	$F40A_H$	154
MMDC_CFG_0	MDC Master Clock Configuration Register 0	$F40B_H$	155
MMDC_CFG_1	MDC Master Clock Configuration Register 1	$F40C_H$	156
PHY_ADDR_5	PHY Address Register PORT 5	$F410_H$	169
PHY_ADDR_4	PHY Address Register PORT 4	$F411_H$	168
PHY_ADDR_3	PHY Address Register PORT 3	$F412_H$	166
PHY_ADDR_2	PHY Address Register PORT 2	$F413_H$	164
PHY_ADDR_1	PHY Address Register PORT 1	$F414_H$	162
PHY_ADDR_0	PHY Address Register PORT 0	$F415_H$	158
MMDIO_STAT_0	PHY MDIO Polling Status per PORT	$F416_H$	160
MMDIO_STAT_1	PHY MDIO Polling Status PORT 1	$F417_H$	161
MMDIO_STAT_2	PHY MDIO Polling Status PORT 2	$F418_H$	161
MMDIO_STAT_3	PHY MDIO Polling Status PORT 3	$F419_H$	161
MMDIO_STAT_5	PHY MDIO Polling Status PORT 5	$F41B_H$	161
ANEG_EEE_0	EEE Auto-Negotiation Overrides PORT 0	$F41D_H$	171
ANEG_EEE_1	EEE Auto-Negotiation Overrides PORT 1	$F41E_H$	171
ANEG_EEE_2	EEE Auto-Negotiation Overrides PORT 2	$F41F_H$	171

Table 44 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
ANEG_EEE_3	EEE Auto-Negotiation Overrides PORT 3	$F420_H$	171
ANEG_EEE_5	EEE Auto-Negotiation Overrides PORT 5	$F422_H$	171
Top Level PDI Registers, MDIO Slave Registers			
SMDIO_CFG	MDC Slave Configuration Register	$F480_H$	172
SMDIO_BADR	MDC Slave Target Base Address Register	$F481_H$	173
Top Level PDI Registers, SPI Master Registers			
MSPI_CFG	SPI Master Interface Configuration Register	$F510_H$	174
MSPI_OP	SPI Master Operating Mode Configuration Register	$F511_H$	175
MSPI_MANCTRL	SPI Master Manual Mode Control Register	$F512_H$	176
MSPI_ISR	SPI Master Interrupt Status Register	$F513_H$	177
MSPI_IER	SPI Master Interrupt Enable Register	$F514_H$	178
MSPI_DIN01	SPI Master Data In 0/1 Register	$F518_H$	178
MSPI_DIN23	SPI Master Data In 2/3 Register	$F519_H$	179
MSPI_DIN67	SPI Master Data In 6/7Register	$F51B_H$	180
MSPI_DOUT01	SPI Master Data Out 0/1 Register	$F51C_H$	180
MSPI_DOUT23	SPI Master Data Out 2/3 Register	$F51D_H$	181
MSPI_DOUT45	SPI Master Data Out 4/5 Register	$F51E_H$	181
MSPI_DOUT67	SPI Master Data Out 6/7 Register	$F51F_H$	182
MSPI_DIN45	SPI Master Data In 4/5 Register	$F51A_H$	179
Top Level PDI Registers, SPI Slave Registers			
SSPI_CFG	SPI Slave Configuration Register	$F580_H$	183
Top Level PDI Registers, UART Registers			
UART_CFG	UART Configuration Register	$F680_H$	184
UART_BD	UART Baud Rate Register	$F681_H$	185
UART_FDIV	UART Baud Rate Fractional Divider Register	$F682_H$	186
UART_PROMPT	UART PROPMP Register	$F683_H$	187
UART_ERRCNT	UART Error Counter Register	$F684_H$	188
Top Level PDI Registers, Clock Generation Unit Registers			
ROPLL_MISC	RO PLL Miscellaneous Control Register	$F990_H$	194
GPC0_CONF	GPC0 Configuration Register	$F948_H$	196
GPC1_CONF	GPC1 Configuration Register	$F94C_H$	197
SYSCLK_CONF	SYCCLK Configuration Register	$F950_H$	197
SGMII_CONF	SGMII Configuration Register	$F954_H$	198
NCO1_LSB	NCO1 LSB Configuration Register	$F958_H$	199
NCO1_MSB	NCO1 MSB Configuration Register	$F95C_H$	199
NCO2_LSB	NCO2 LSB Configuration Register	$F960_H$	200
NCO2_MSB	NCO2 MSB Configuration Register	$F964_H$	200
NCO_CTRL	NCO Control	$F968_H$	201

Table 44 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
ROPLL_CFG0	RO PLL Configuration 0 Register	$F980_H$	188
ROPLL_CFG1	RO PLL Configuration 1 Register	$F984_H$	189
ROPLL_CFG2	RO PLL Configuration Register 2	$F988_H$	190
ROPLL_CFG3	RO PLL Configuration Register 3	$F98C_H$	193
Top Level PDI Registers, Reset Control Unit Registers			
RESET_STATUS	Reset Status Register	$FA00_H$	202
RST_REQ	Reset Request Register	$FA01_H$	202
MANU_ID	MANU ID Register	$FA10_H$	204
PNUM_ID	PNUM ID Register	$FA11_H$	205
GPIO_DRIVE0_CFG	GPIO PAD Driver Strength 0 Control Register	$FA70_H$	206
GPIO_DRIVE1_CFG	GPIO PAD Driver Strength 1 Control Register	$FA71_H$	206
GPIO_SLEW_CFG	GPIO PAD Slew Control Register	$FA72_H$	207
GPIO2_DRIVE0_CFG	GPIO2 PAD Driver Strength 0 Control Register	$FA74_H$	207
GPIO2_DRIVE1_CFG	GPIO2 PAD Driver Strength 1 Control Register	$FA75_H$	208
GPIO2_SLEW_CFG	GPIO2 Slew Control Register	$FA76_H$	209
RGMII_SLEW_CFG	RGMII PAD Slew Control Register	$FA78_H$	209
PS0	Pin-Strapping Register	$FA80_H$	211
PS1	Pin-Strapping Register 1	$FA81_H$	211
Top Level PDI Registers, GPIO Registers			
GPIO_ALTSEL0	Port 0 Alternate Function Select Register 0	$F383_H$	213
GPIO_ALTSEL1	Port 0 Alternate Function Select Register 1	$F384_H$	214
GPIO_PUDSEL	GPIO Pull-Up/Pull-Down Select Register	$F386_H$	214
GPIO2_ALTSEL0	Port 2 Alternate Function Select Register 0	$F393_H$	217
GPIO2_ALTSEL1	Port 2 Alternate Function Select Register 1	$F394_H$	218
GPIO2_PUDSEL	GPIO2 Pull-Up/Pull-Down Select Register	$F396_H$	218
GPIO_OUT	GPIO Data Output Register	$F380_H$	212
GPIO_IN	GPIO Data Input Register	$F381_H$	212
GPIO_DIR	GPIO Direction Register	$F382_H$	213
GPIO_OD	GPIO Open Drain Control Register	$F385_H$	214
GPIO_PUDEN	GPIO Pull-Up/Pull-Down Enable Register	$F387_H$	215
GPIO2_OUT	GPIO2 Data Output Register	$F390_H$	216
GPIO2_IN	GPIO2 Data Input Register	$F391_H$	216
GPIO2_DIR	GPIO2 Direction Register	$F392_H$	217
GPIO2_OD	GPIO2 Open Drain Control Register	$F395_H$	218
GPIO2_PUDEN	GPIO2 Pull-Up/Pull-Down Enable Register	$F397_H$	219
Top Level PDI Registers, ICU Registers			
IM0_ISR	IM0 Interrupt Status Register	$F3C0_H$	220
IM0_EINT0_IER	IM0 EINT0 Interrupt Enable Register	$F3C2_H$	221

Table 44 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
IM0_EINT1_IER	IM0 EINT1 Interrupt Enable Register	$F3C3_H$	222
EIU_EXIN_CONF	EIU External Interrupt Controller Register	$F3C4_H$	223
Top Level PDI Registers, LED Registers			
LED_MD_CFG	LED Single Color LED Mode Register	$F3E0_H$	225
LED_BRT_CTRL	LED Brightness Control Register	$F3E1_H$	227
LED_LSENS_CTRL	LED Light Sensing Control Register	$F3E2_H$	227

The register is addressed wordwise.

Table 45 Register Access Types

Mode	Symbol
Interrupt status register, latching high, cleared by writing a ONE	lhsc
Hardware status, read-only	rh
Read/write register with input from and output to hardware	rwh
Standard read/write register with output to hardware	rw

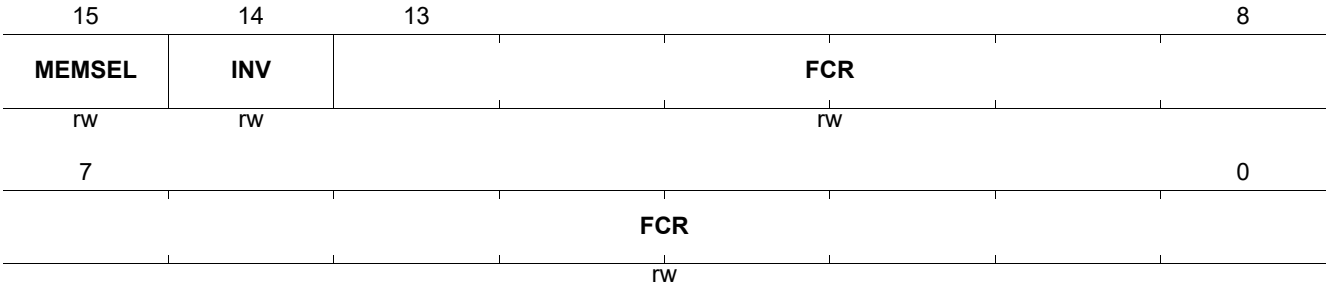
4.1.1 GPHY Shell Registers

This section provides the registers required for GPHY configuration.

GPHY0 Firmware Address Offset Configuration Register

This register is used to store GPHY0 firmware address offset.

GPHY0_FCR	Offset	Reset Value
GPHY0 Firmware Address Offset Register	$F700_H$	4000_H



Field	Bits	Type	Description
MEMSEL	15	rw	**GPHY Code Memory Mode** 0_B **INT** GPHY macro loads firmware memory from internal ROM or internal RAM. 1_B **EXTROM** GPHY macro loads firmware memory by external E2PROM.
INV	14	rw	**Firmware Address Inversion** 0_B **NOINV** Firmware address is not inverted. 1_B **INV** Firmware address is inverted when access internal ROM or internal RAM.
FCR	13:0	rw	**Firmware Address Offset MSB** It stores PHY0 firmware offset address bits 17 to 4. The lower 4 address bits are 0.

Similar Registers

The following registers are identical to the Register **GPHY0_FCR** defined above.

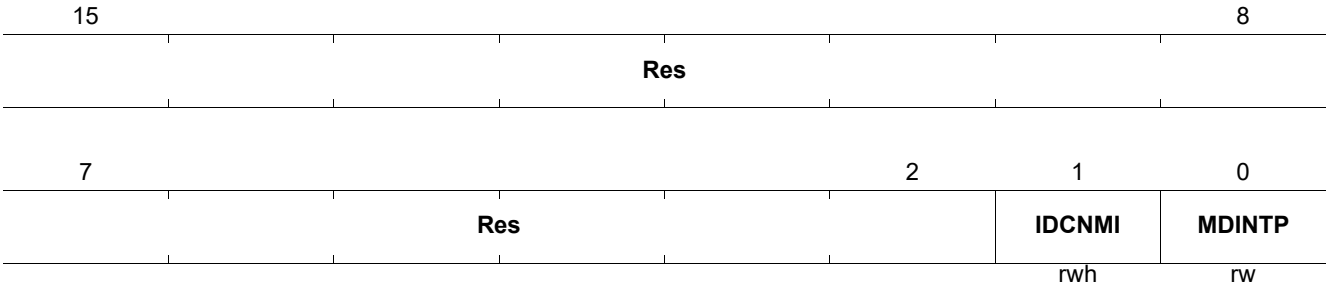
Table 46 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_FCR	GPHY1 Firmware Address Offset Register	$F710_H$	
GPHY2_FCR	GPHY2 Firmware Address Offset Register	$F720_H$	
GPHY3_FCR	GPHY3 Firmware Address Offset Register	$F730_H$	

GPHY0 General Configuration Register

This register is used to store GPHY0 general configuration register.

GPHY0_CFG	Offset	Reset Value
GPHY0 General Configuration Register	$F701_H$	0000_H



Field	Bits	Type	Description
IDCNMI	1	rwh	**IDC Non-maskable Interrupt** This is a non-maskable interrupt to the IDC. As such this is the highest priority interrupt possible. It can be used for emergency applications. This signal is cleared when interrupt is acknowledged. 0_B **NIL** NMI interrupt is not pending. 1_B **INT** NMI interrupt is pending.
MDINTP	0	rw	**MDIO Interrupt Polarity** This type of information is evaluated by the integrated controller to allow configuration of the MDIO interrupt polarity by the instantiating SOC. For automatic configuration of the MDIO Interrupt polarity this configuration bit could be connected to the input of the MDIO interrupt pad. This field must be configured to 0_B. 0_B **HIGH** MDIO Interrupt is active high. 1_B **LOW** MDIO Interrupt is active low.

Similar Registers

The following registers are identical to the Register **GPHY0_CFG** defined above.

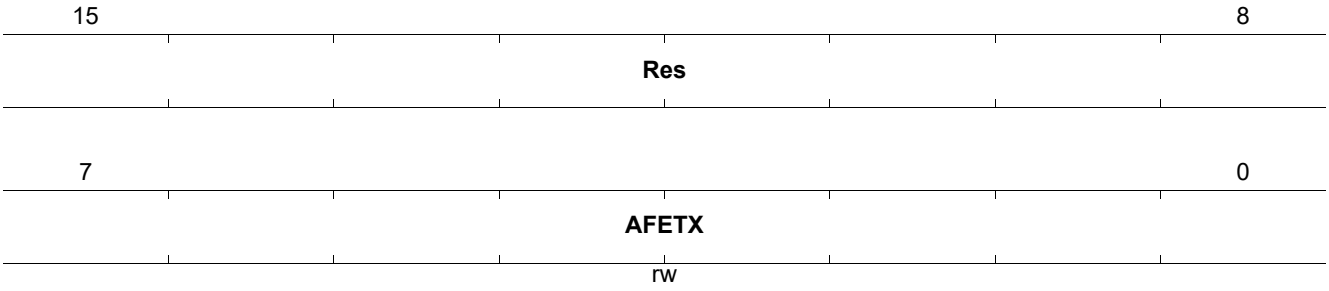
Table 47 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_CFG	GPHY1 General Configuration Register	$F711_H$	
GPHY2_CFG	GPHY2 General Configuration Register	$F721_H$	
GPHY3_CFG	GPHY3 General Configuration Register	$F731_H$	

GPHY0 AFE TX Path Control Register

This register is used to store the control information for GPHY0 AFE TX Path.

GPHY0_AFETX_CTRL	Offset	Reset Value
GPHY0 AFE TX Path Control Register	$F702_H$	0000_H



Field	Bits	Type	Description
AFETX	7:0	rw	**Control for AFE TX** Use this input to configure AFE TX path parameters.

Similar Registers

The following registers are identical to the Register **GPHY0_AFETX_CTRL** defined above.

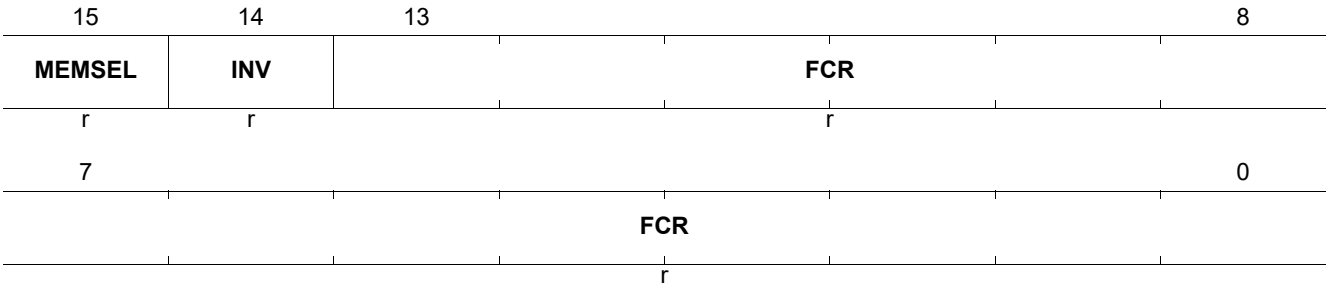
Table 48 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_AFETX_CTRL	GPHY1 AFE TX Path Control Register	$F712_H$	
GPHY2_AFETX_CTRL	GPHY2 AFE TX Path Control Register	$F722_H$	
GPHY3_AFETX_CTRL	GPHY3 AFE TX Path Control Register	$F732_H$	

GPHY0 Firmware Address Offset Configuration Shadow Register

This register is used to store GPHY0 firmware address offset shadow value.

GPHY0_FCR_SD	Offset	Reset Value
GPHY0 Firmware Address Offset Shadow Register	$F703_H$	4000_H



Field	Bits	Type	Description
MEMSEL	15	r	**GPHY Code Memory Mode** 0_B **INT** GPHY Macro loads firmware memory from internal ROM or internal RAM. 1_B **EXTROM** GPHY Macro loads firmware memory by external E2PROM.
INV	14	r	**Firmware Address Inversion** 0_B **NOINV** Firmware address is not inverted. 1_B **INV** Firmware address is inverted when access internal ROM or internal RAM.
FCR	13:0	r	**Firmware Address Offset MSB** It stores PHY0 firmware offset address bits 17 to 4. The lower 4 address bits are 0.

Similar Registers

The following registers are identical to the Register **GPHY0_FCR_SD** defined above.

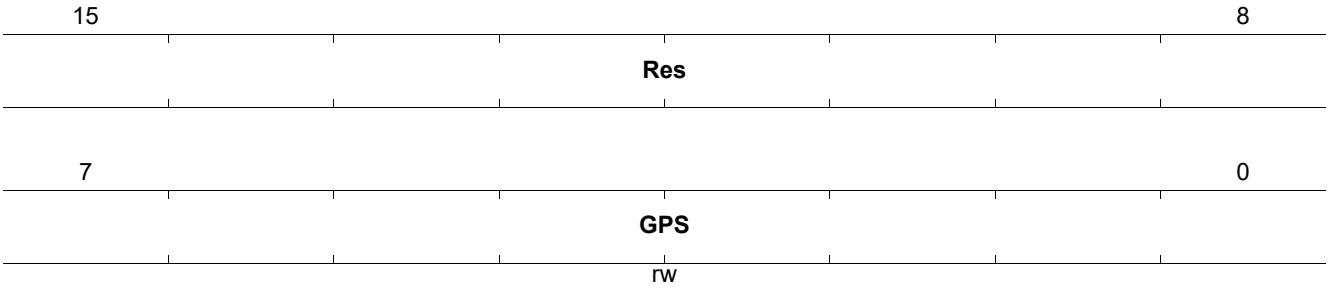
Table 49 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_FCR_SD	GPHY1 Firmware Address Offset Shadow Register	$F713_H$	
GPHY2_FCR_SD	GPHY2 Firmware Address Offset Shadow Register	$F723_H$	
GPHY3_FCR_SD	GPHY3 Firmware Address Offset Shadow Register	$F733_H$	

GPHY0 General Pin-Strapping Register

This register is used to store general pin-strapping configuration register.

GPHY0_GPS	Offset	Reset Value
GPHY0 General Pin-Strapping Register	$F708_H$	$00FF_H$



Field	Bits	Type	Description
GPS	7:0	rw	**General Pin-Strapping** This connects GPHY general pin-strapping bit 7 to 0.

Similar Registers

The following registers are identical to the Register **GPHY0_GPS** defined above.

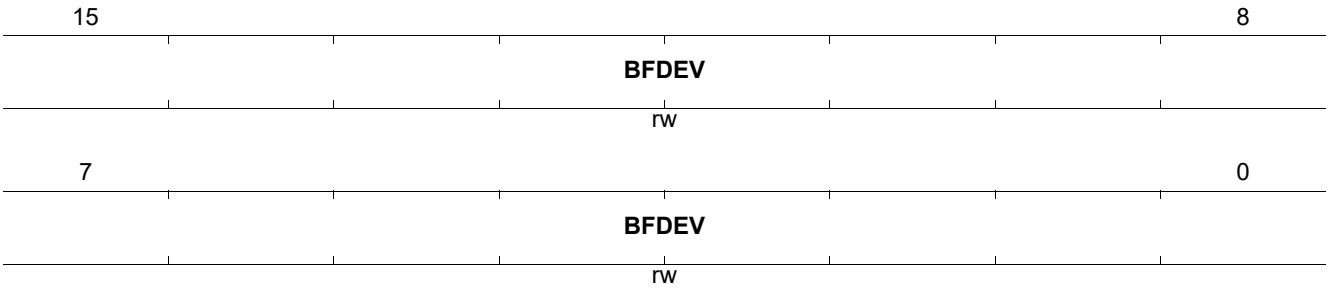
Table 50 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_GPS	GPHY1 General Pin-Strapping Register	$F718_H$	
GPHY2_GPS	GPHY2 General Pin-Strapping Register	$F728_H$	
GPHY3_GPS	GPHY3 General Pin-Strapping Register	$F738_H$	

GPHY0 Base Frequency Deviation Configuration Register

This register is used to store base frequency deviation configuration register.

GPHY0_BFDEV	Offset	Reset Value
GPHY0 Base Frequency Deviation Configuration Register	$F709_H$	3333_H



Field	Bits	Type	Description
BFDEV	15:0	rw	**Base Frequency Deviation** Use this input to specify base frequency deviation from nominal base.

Similar Registers

The following registers are identical to the Register **GPHY0_BFDEV** defined above.

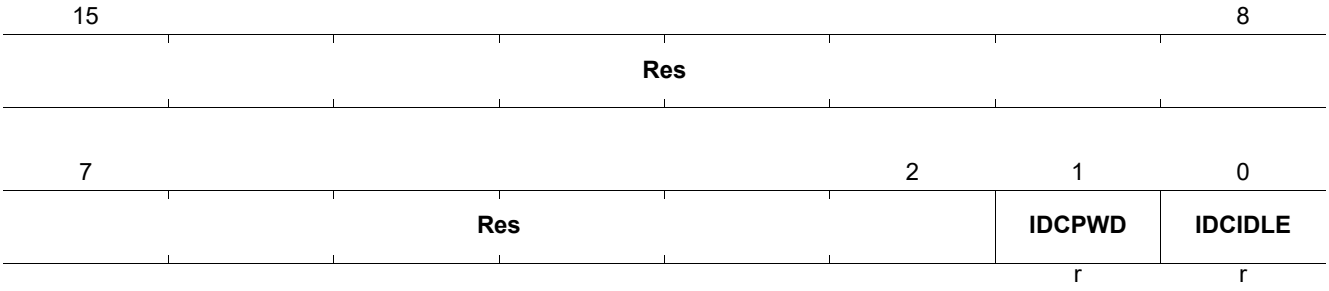
Table 51 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_BFDEV	GPHY1 Base Frequency Deviation Configuration Register	$F719_H$	
GPHY2_BFDEV	GPHY2 Base Frequency Deviation Configuration Register	$F729_H$	
GPHY3_BFDEV	GPHY3 Base Frequency Deviation Configuration Register	$F739_H$	

GPHY0 General Status Register

This register is used to store GPHY0 general status register.

GPHY0_STATUS	Offset	Reset Value
GPHY0 General Status Register	$F70F_H$	0000_H



Field	Bits	Type	Description
IDCPWD	1	r	**IDC Power Down** 0_B **PUP** IDC is powered up. 1_B **PDOWN** IDC is powered down.
IDCIDLE	0	r	**IDC Idle** 0_B **ACT** IDC is active. 1_B **IDLE** IDC is idle.

Similar Registers

The following registers are identical to the Register **GPHY0_STATUS** defined above.

Table 52 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPHY1_STATUS	GPHY1 General Status Register	$F71F_H$	
GPHY2_STATUS	GPHY2 General Status Register	$F72F_H$	
GPHY3_STATUS	GPHY3 General Status Register	$F73F_H$	

4.1.2 R(G)MII Registers

This section provides the control registers of the R(G)MII Interfaces.

xMII Interface 5 Configuration Register

This register controls the settings of the xMII Interface.

MII_CFG_5	Offset	Reset Value
xMII Interface 5 Configuration Register	$F100_H$	2044_H

15	14	13	12	11	10	9	8
RST	EN	ISOL	CLKDIS	Res	CRS		RGMII_IBS
rwh	rw	rw	rw		rw		rw

7	6	4	3	0
Res	MIIRATE		MIIMODE	
	rw		rw	

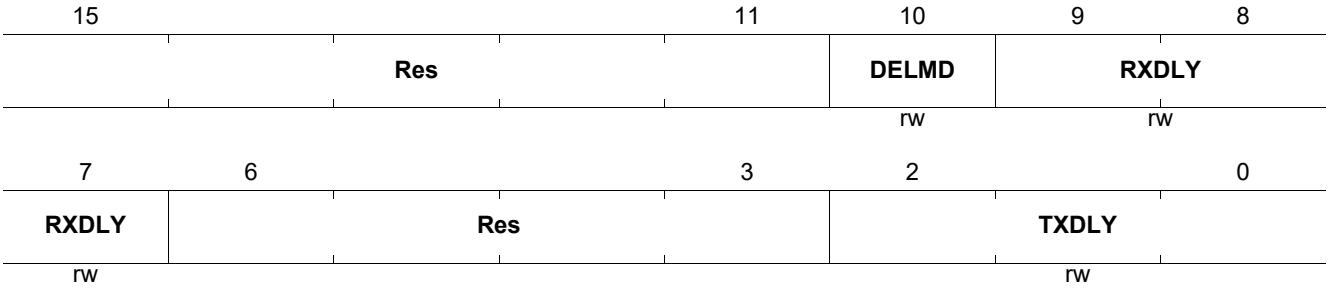
Field	Bits	Type	Description
RST	15	rwh	**Hardware Reset** Resets all related hardware modules except for the register settings. This reset acts similar to the hardware reset, but maintains any programming of the control registers. 0_B **OFF** reset is off 1_B **ON** reset is active
EN	14	rw	**xMII Interface Enable** The corresponding interface can only be enabled when the disable signal at macro boundary is inactive. Otherwise the interface is disabled. 0_B **DIS** disable the interface 1_B **EN** enable the interface
ISOL	13	rw	**ISOLATE xMII Interface** Set to 0 for normal operation. In ISOLATE all xMII Output Pins are set to be disabled 0_B **EN** Interface is active 1_B **ISO** Interface outputs are isolated
CLKDIS	12	rw	**Link Down Clock Disable** For power save in case of link down signaled by MDIO, the clocks in the xMII module and in the xMII Interface can be switched off automatically. The automatic switching off can be enabled by setting this parameter to “On”. 0_B **OFF** No automatic disable in case of link down 1_B **ON** Disable clocks in case of link down and switch interface off

Field	Bits	Type	Description
CRS	10:9	rw	**CRS Sensitivity Configuration** These Bits are only valid in PHY Mode. CRS can be configured depending on RX and TX activity and Half/Full Duplex Modes (HDX/FDX) 00_B **MD0** HDX:TX+RX, FDX:RX 01_B **MD1** HDX:TX+RX, FDX:0 10_B **MD2** HDX:RX, FDX:RX 11_B **MD3** HDX:RX, FDX:0
RGMII_IBS	8	rw	**RGMII In Band Status** When RGMII mode is selected, this bit controls whether the In Band Status Bits Link, Clock Speed duplex are transmitted during IPG Could be set to “On” in case of connected to an external MAC. RGMII in band status extraction is always on regardless of this setting. 0_B **OFF** RGMII In Band Status is off 1_B **ON** RGMII In Band Status is on
MIIRATE	6:4	rw	**xMII Interface Clock Rate** Selects the data and clock rate for the xMII interface. 000_B **M2P5** 2.5 MHz 001_B **M25** 25 MHz 010_B **M125** 125 MHz 100_B **Auto** Automatically clock rate based on speed
MIIMODE	3:0	rw	**xMII Interface Mode** This selects the xMII interface mode. 0100_B **RGMII** RGMII mode, connected to external PHY or MAC.

RGMII 5 Clock Delay Configuration Register

This register controls the settings of the receive and transmit clock delay.

PCDU_5	Offset	Reset Value
RGMII 5 Clock Delay Configuration Register	$F101_H$	0000_H

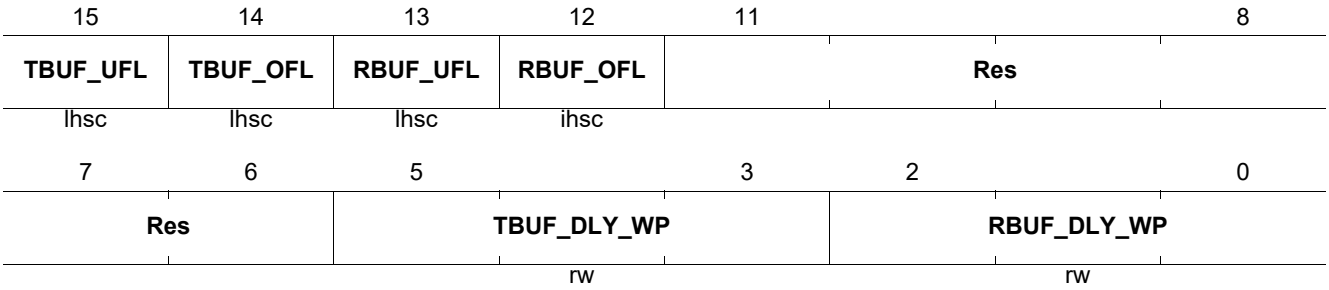


Field	Bits	Type	Description
DELMD	10	rw	**PCDU Delay Setting Mode** 0_B **DELAY** Setting clock delay directly 1_B **MK** Setting M, K values
RXDLY	9:7	rw	**Configure Receive Clock Delay** Configure the delay of RX_CLK_D versus RX_CLK in steps of 500 ps. The resulting delay is TD = unsigned(RXDLY) * 500 ps
TXDLY	2:0	rw	**Configure Transmit Clock Delay** Configure the delay of TX_CLK_D versus TX_CLK in steps of 500 ps. The total configured delay is TD=unsigned(TXDLY)*500 ps.

xMII5 Interface Receive Transmit Buffer Control Register

This register is used to configure the internal receive buffer and check under and overflow.

RTXB_CTL_5	Offset	Reset Value
xMII5 Interface Receive Transmit Buffer Control Register	$F120_H$	0009_H



Field	Bits	Type	Description
TBUF_UFL	15	lhsc	**Transmit Buffer Underflow Indicator** Indicates when one or more transmit buffer underflow events have been detected. 0_B **NONE** Underflow never detected 1_B **UFL** Underflow occurred at least once
TBUF_OFL	14	lhsc	**Transmit Buffer Overflow Indicator** Indicates when one or more transmit buffer overflow events have been detected. 0_B **NONE** Overflow never detected 1_B **OFL** Overflow occurred at least once
RBUF_UFL	13	lhsc	**Receive Buffer Underflow Indicator** Indicates when one or more receive buffer underflow events have been detected. 0_B **NONE** Underflow is never detected 1_B **UFL** Underflow occurred at least once
RBUF_OFL	12	lhsc	**Receive Buffer Overflow Indicator** Indicates when one or more receive buffer overflow events have been detected. 0_B **NONE** Overflow is never detected 1_B **OFL** Overflow occurred at least once
TBUF_DLY_WP	5:3	rw	**TX Buffer Delay Write Pointer** This register is used to configure the initial delay of the write pointer in the transmit buffer. This delay must be larger than zero to support negative frequency offsets. This delay must be smaller than max to support positive frequency offsets.
RBUF_DLY_WP	2:0	rw	**RX Buffer Delay Write Pointer** This register is used to configure the initial delay of the write pointer in the receive buffer. This delay must be larger than zero to support negative frequency offsets. This delay must be smaller than max to support positive frequency offsets.

Pin and Port Multiplexing Configuration

This register is used to configure Pin and Port Multiplexing.

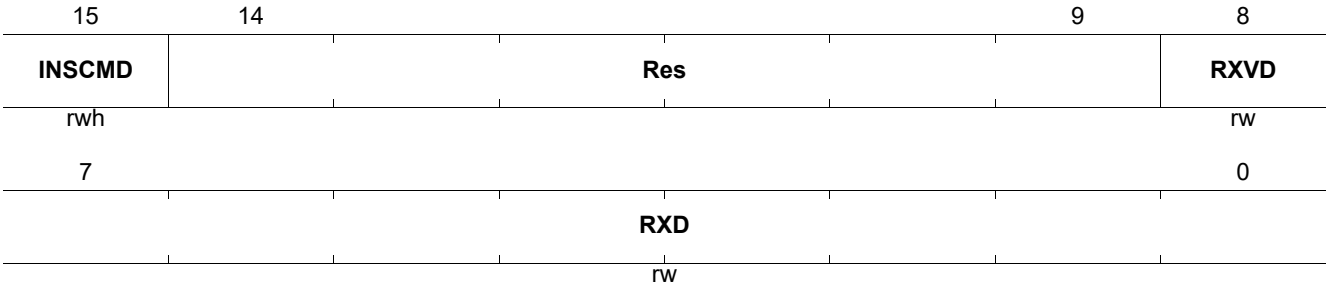
MII_MUX_CFG	Offset	Reset Value
Pin and Port Multiplexing Configuration	$F130_H$	0000_H

Field	Bits	Type	Description
PIE	9	rw	**Packet Insertion and Extraction Mode** This is to select packet insertion and extraction mode. 0_B **DIS** Packet insertion and extraction mode is disabled. 1_B **EN** Packet insertion and extraction mode is enabled. GSWIP port 6 is connected to packet insertion and extraction mode.
GPHY0_ISO	0	rw	**GPHY0 Isolation Mode** This is to enable or disable GPHY isolation mode. 0_B **DIS** Isolation mode is disabled, GPHY0 is connected to switch fabric. 1_B **EN** Isolation mode is enabled, GPHY0 is connected to RGMII5.

Packet Insertion Register

This register is used to insert packet to port 6.

PKT_INS	Offset	Reset Value
Packet Insertion Register	$F140_H$	0000_H

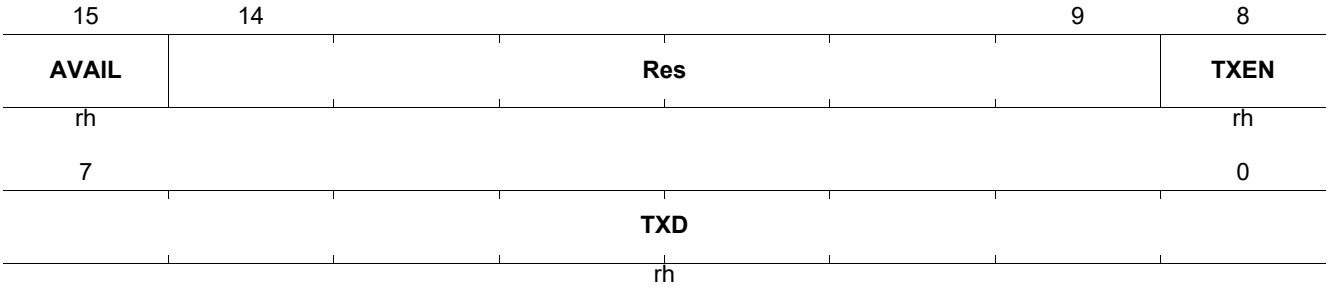


Field	Bits	Type	Description
INSCMD	15	rwh	**Packet Insertion Command** 0_B **NIL** Packet insertion is not triggered. 1_B **CMD** Start Packet insertion. CPU write ‘1’ to this bit to trigger the insertion. This is a single cycle pulse and the bit is self clearing.
RXVD	8	rw	**RX Valid** This is to indicate whether the data byte is valid or not. 0_B **GAP** The data byte is not valid. Writing IPG. 1_B **VLD** The data byte is valid. Wring Preamble, SFD and packet data.
RXD	7:0	rw	**RX Data** Data Byte to be inserted. Including IPG, Preamble, SFD and packet data.

Packet Extraction Read Register

This register is used to extract packet from port 6.

PKT_EXT_READ	Offset	Reset Value
Packet Extraction Read Register	$F141_H$	0000_H

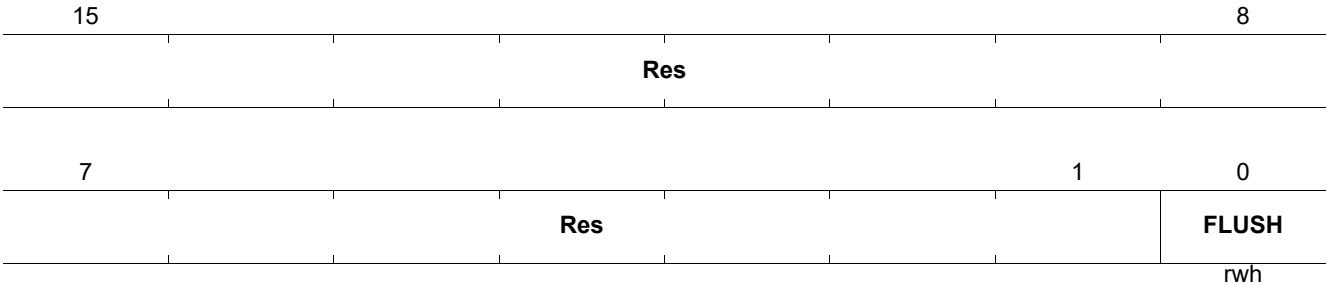


Field	Bits	Type	Description
AVAIL	15	rh	**Packet Available** This is to indicate a new packet is available to be extracted. When packet available, an interrupt is set. 0_B **NAVL** Packet is not available to be available. 1_B **AVL** Packet is available to be available.
TXEN	8	rh	**TX Data Valid** This is to indicate the extracted data byte is valid 0_B **NIL** The extracted byte is not valid 1_B **EN** The extracted byte is valid.
TXD	7:0	rh	**TX Data** Data byte extracted.

Packet Extraction Command Register

This register is used to extract packet from port 6.

PKT_EXT_CMD	Offset	Reset Value
Packet Extraction Command Register	$F142_H$	0000_H

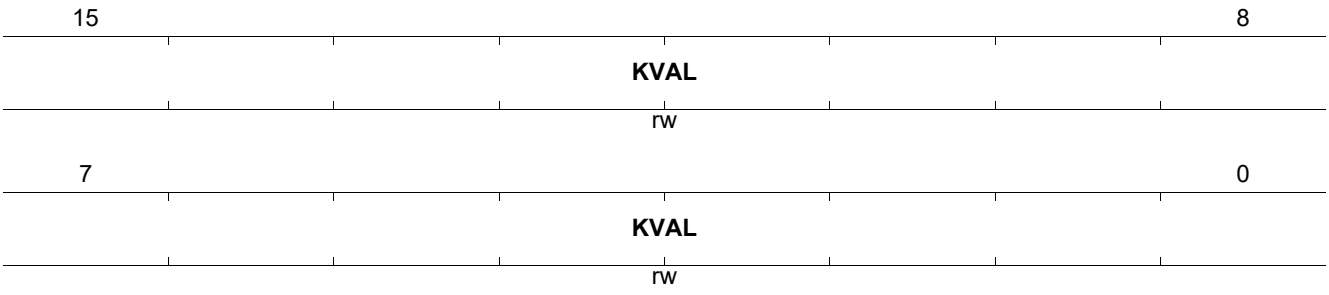


Field	Bits	Type	Description
FLUSH	0	rwh	**Packet Extraction Flush Command** This is to indicate to flush the rest of the current packet 0_B **NIL** The flush command is not triggered 1_B **CMD** The flush command is triggered. This bit is self-clearing and it is cleared until the flush of the current packet is done.

PCDU5 TX K Value Register

This register is used to configure TX K value.

PCDU5_TX_KVAL	Offset	Reset Value
PCDU5 TX K Value	$F160_H$	0040_H

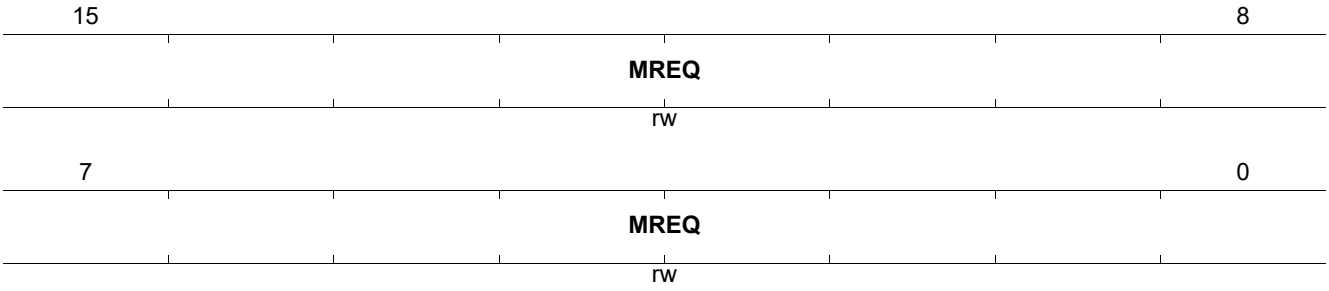


Field	Bits	Type	Description
KVAL	15:0	rw	**K Value for TX Delay Path**

PCDU5 TX M Required Register

This register is used to configure TX M Required.

PCDU5_TX_MREQ	Offset	Reset Value
PCDU5 TX M Required	$F161_H$	0000_H

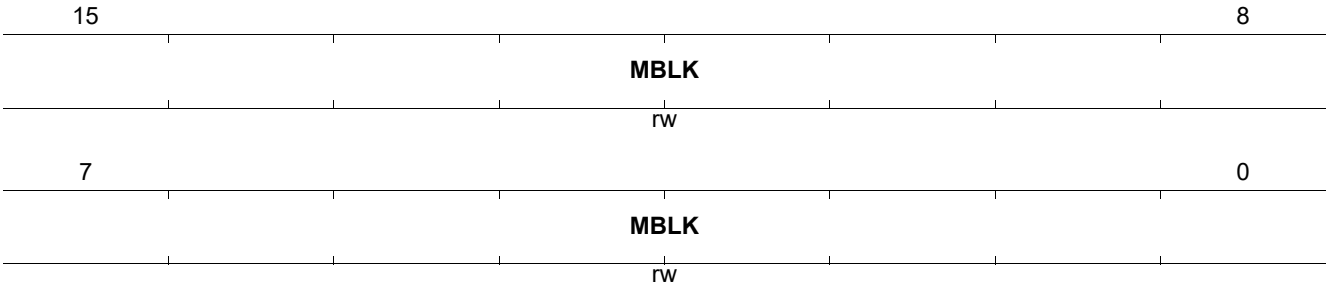


Field	Bits	Type	Description
MREQ	15:0	rw	**M Required for TX Delay Path**

PCDU5 TX M Blank Register

This register is used to configure TX M Blank.

PCDU5_TX_MBLK	Offset	Reset Value
PCDU5 TX M Blank	$F162_H$	0002_H

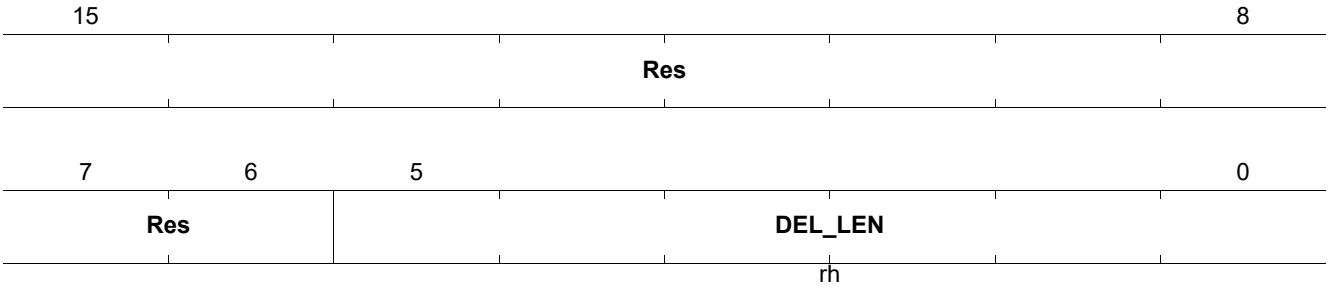


Field	Bits	Type	Description
MBLK	15:0	rw	**M Blank for TX Delay Path**

PCDU5 TX Delay Length Register

This register is used to configure TX Delay Length.

PCDU5_TX_DELLEN	Offset	Reset Value
PCDU5 TX Delay Length	$F163_H$	0000_H

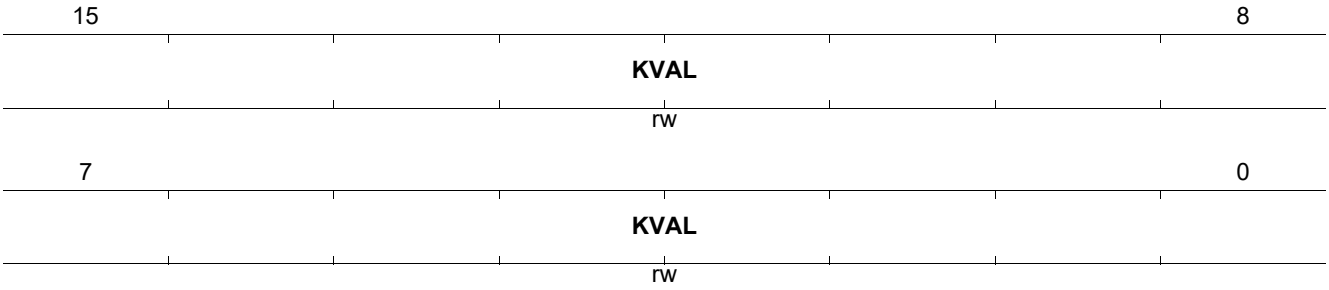


Field	Bits	Type	Description
DEL_LEN	5:0	rh	**Delay Length for TX Delay Path**

PCDU 5 RX K Value Register

This register is used to configure RX K value.

PCDU5_RX_KVAL	Offset	Reset Value
PCDU5 RX K Value	$F168_H$	0040_H

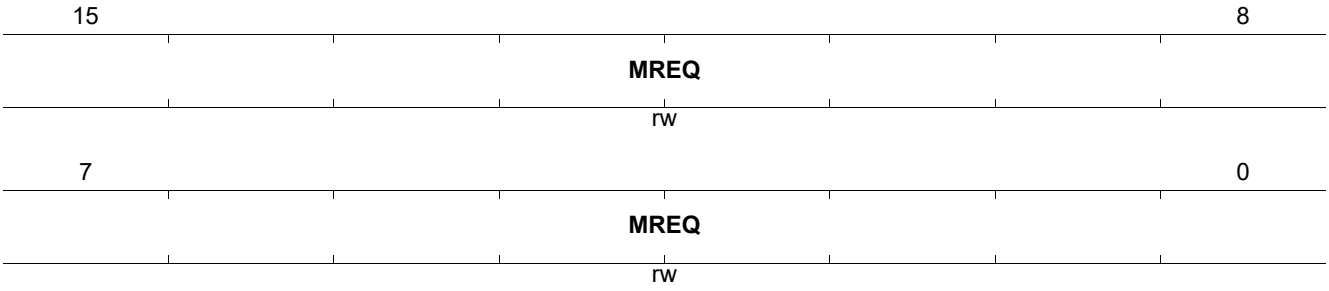


Field	Bits	Type	Description
KVAL	15:0	rw	**K Value for RX Delay Path**

PCDU5 RX M Required Register

This register is used to configure RX M Required.

PCDU5_RX_MREQ	Offset	Reset Value
PCDU5 RX M Required	$F169_H$	0000_H

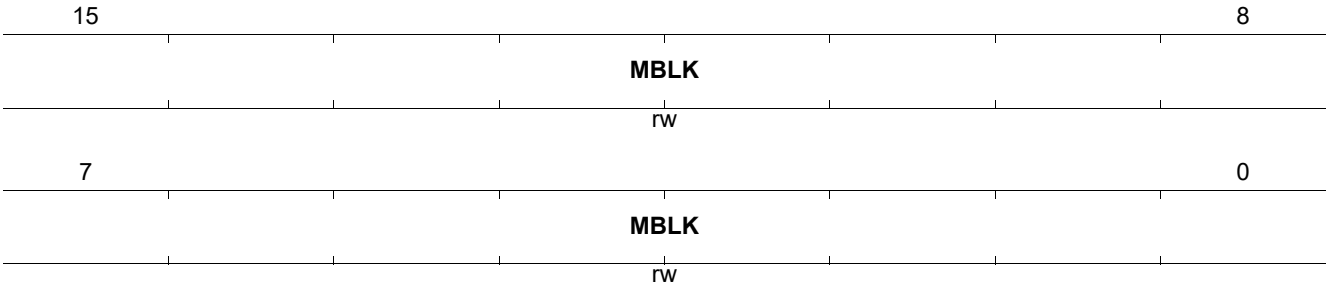


Field	Bits	Type	Description
MREQ	15:0	rw	**M Required for RX Delay Path**

PCDU5 RX M Blank Register

This register is used to configure RX M Blank.

PCDU5_RX_MBLK	Offset	Reset Value
PCDU5 RX M Blank	$F16A_H$	0002_H

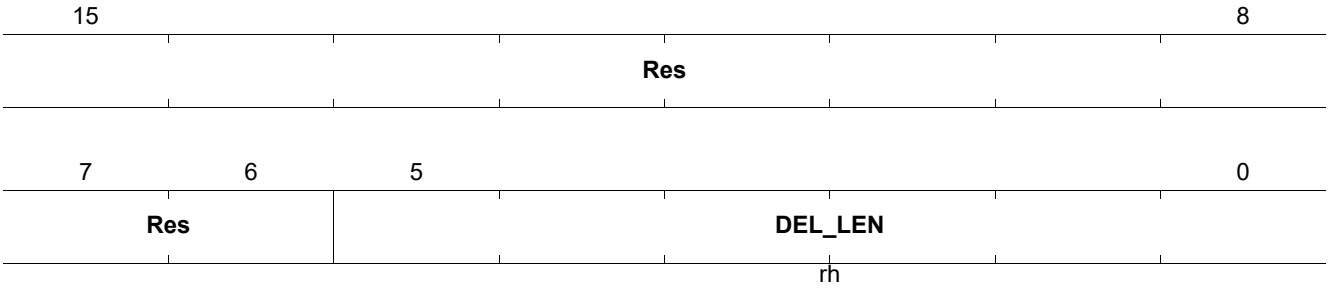


Field	Bits	Type	Description
MBLK	15:0	rw	**M Blank for RX Delay Path**

PCDU5 RX Delay Length Register

This register is used to configure RX Delay Length.

PCDU5_RX_DELLEN	Offset	Reset Value
PCDU5 RX Delay Length	$F16B_H$	0000_H



Field	Bits	Type	Description
DEL_LEN	5:0	rh	**Delay Length for RX Delay Path**

4.1.3 MDIO Master Registers

This section provides the registers required to control the MDIO Master Interface.

GSWIP Configuration Register

This register is used to configuration GSWIP port enable and disable.

GSWIP_CFG	Offset	Reset Value
GSWIP Configuration Register	$F400_H$	0000_H

15	14	13	12	11	10	9	8
SE	P6	P5	P4	P3	P2	P1	P0
rw	rw	rw	rw	rw	rw	rw	rw

7					2	1	0
Res						HWRES	SWRES
						rwh	rwh

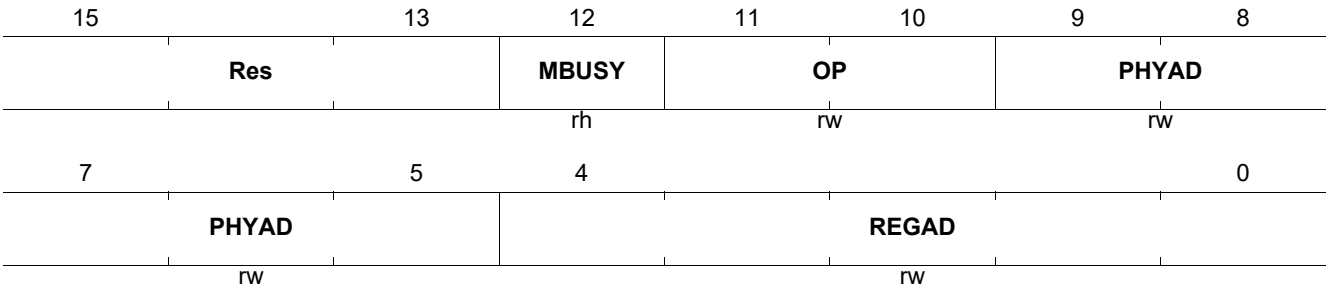
Field	Bits	Type	Description
SE	15	rw	**Global Switch Macro Enable** When set to OFF, the switch macro is inactive and frame forwarding is disabled. Register configuration and memory access is enabled in the OFF state. A register programming must activate the switch by setting this bit. This is used for setting all relevant registers before enabling the data traffic 0_B **Disable** Macro is disabled 1_B **Enable** Macro is enabled
P6	14	rw	**Port 6 Disable Configuration** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled
P5	13	rw	**Port 5 Disable Configuration** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled
P4	12	rw	**Port 4 Disable Configuration** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled
P3	11	rw	**Port 3 Disable Configuration** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled
P2	10	rw	**Port 2 Disable Configuration** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled
P1	9	rw	**Port 1 Disable Configuration** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled

Field	Bits	Type	Description
P0	8	rw	**Port 0 Disable Configuration** 0_B **Enable** Port is enabled 1_B **Disable** Port is disabled
HWRES	1	rwh	**Global Switch Macro Hardware Reset** Reset all hardware modules including the register settings. This reset acts similar to the hardware reset and is cleared by HW after Reset is executed. 0_B **OFF** Reset is off 1_B **ON** Reset is active
SWRES	0	rwh	**Global Switch Macro Software Reset** Reset all GSWIP hardware modules excluding the register settings.This reset acts similar to the hardware reset, but maintains any programming of the control registers and is cleared by HW after Reset is executed. 0_B **OFF** Reset is off 1_B **ON** Reset is active

MDIO Master Indirect Control Register

This register is used to access devices connected to the serial MDIO master interface, internally or externally. Each write access to this register starts a transmission, either read or write.

MMDIO_CTRL	Offset	Reset Value
MDIO Master Control Register	$F408_H$	0000_H

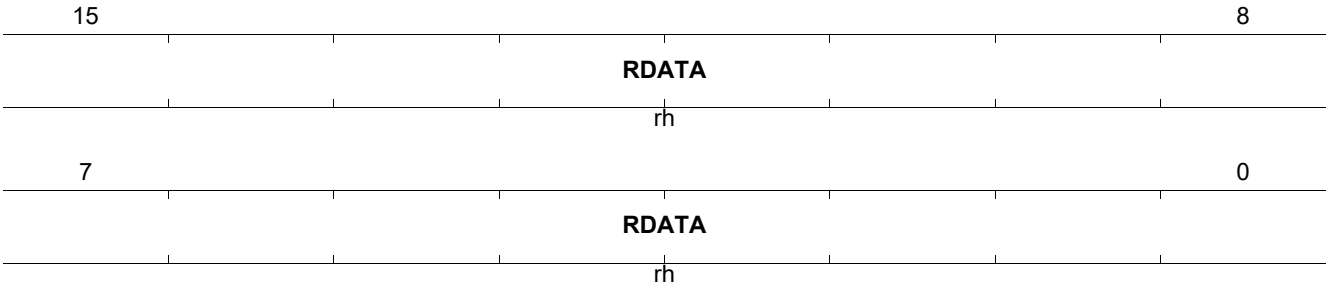


Field	Bits	Type	Description
MBUSY	12	rh	**MDIO Busy** This bit is set by hardware upon each write access to the register, which starts a transmission. As soon as a new command can be accepted, this bit is cleared by hardware. During write access, this bit is ignored and can be written to either value, 0 or 1. 0_B **IDLE** The bus is available 1_B **BUSY** The bus is busy
OP	11:10	rw	**Operation Code** Selects the operation command. The value is directly mapped into the serial access frame. 00_B **RES0** Reserved, do not use 01_B **WR** Write access 10_B **RD** Read access 11_B **RES3** Reserved, do not use
PHYAD	9:5	rw	**PHY Address** PHY address of the target device. The value is directly mapped into the serial access frame.
REGAD	4:0	rw	**Register Address** Register address in the target device. The value is directly mapped into the serial access frame.

MDIO Master Indirect Read Data Register

This register is used to read back data across the serial MDIO master interface, internally or externally.

MMDIO_READ	Offset	Reset Value
MDIO Master Read Data Register	$F409_H$	0000_H

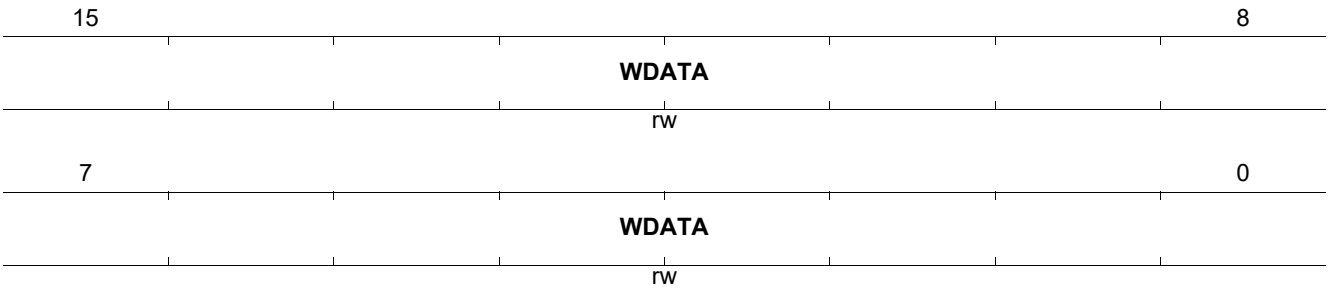


Field	Bits	Type	Description
RDATA	15:0	rh	**Read Data** A read access is triggered by writing to MDIO_CTRL (OP = RD, MBUSY = BUSY). After MBUSY = IDLE, data can be read.

MDIO Master Indirect Write Data Register

This register is used to write data across the serial MDIO master interface, internally or externally.

MMDIO_WRITE	Offset	Reset Value
MDIO Master Write Data Register	$F40A_H$	0000_H

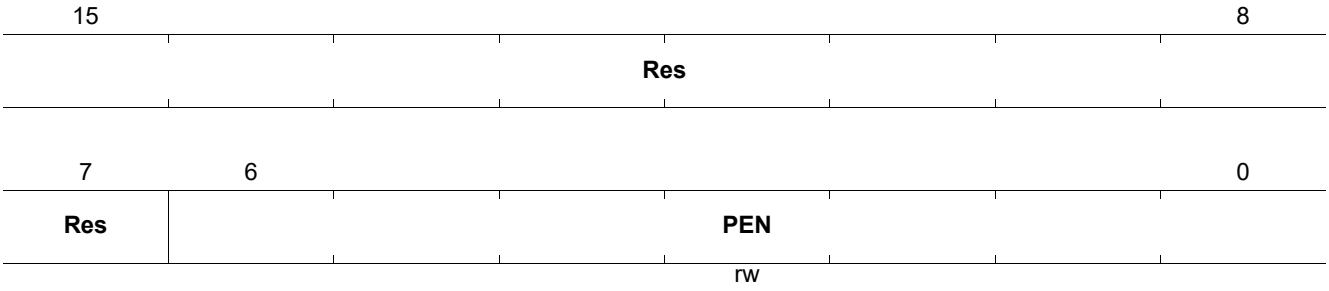


Field	Bits	Type	Description
WDATA	15:0	rw	**Write Data** A write access is triggered by writing to MDIO_CTRL (OP = WR, MBUSY = BUSY). This register must be written before the write command is given.

MDC Master Configuration Register 0

This register is used to control the MDC clock output and polling state machine.

MMDC_CFG_0	Offset	Reset Value
MDC Master Clock Configuration Register 0	$F40B_H$	$006F_H$

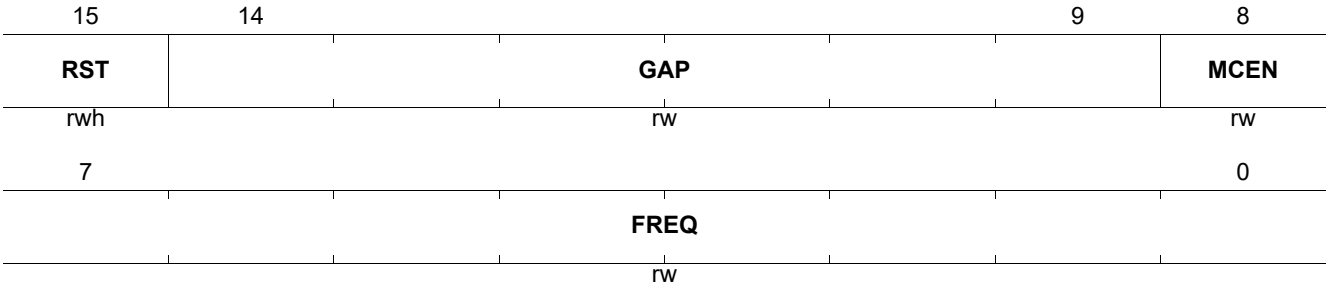


Field	Bits	Type	Description
PEN	6:0	rw	**Polling State Machine Enable** Enables the state machine to read PHY information automatically on this port. Unused ports must be disabled to reduce the polling latency. 0_B **DIS** Automatic PHY polling is disabled on this port 1_B **EN** Automatic PHY polling is enabled on this port (default)

MDC Master Clock Configuration Register 1

This register is used to configure clocking rate for the MDIO master interfaces.

MMDC_CFG_1	Offset	Reset Value
MDC Master Clock Configuration Register 1	$F40C_H$	0109_H



Field	Bits	Type	Description
RST	15	rwh	**MDIO Hardware Reset** Reset all hardware modules except for the register settings. This reset acts similar to the hardware reset, but maintains any programming of the control registers and is cleared by HW after Reset is executed. 0_B **OFF** Reset is off 1_B **ON** Reset is active
GAP	14:9	rw	**Autopolling Gap** This register configures the number of cycles between each auto-polling read access. The number of MDIO clock cycles is 256*GAP.
MCEN	8	rw	**Management Clock Enable** Enables the MDC clock driver. The driver can be disabled to save power when no external devices are connected to the MDIO master interface. When the MDC clock is disabled, the MDIO pad is switched to input mode and the MDIO drivers are also disabled. 0_B **DIS** Clock driver is disabled 1_B **EN** Clock driver is enabled (default)

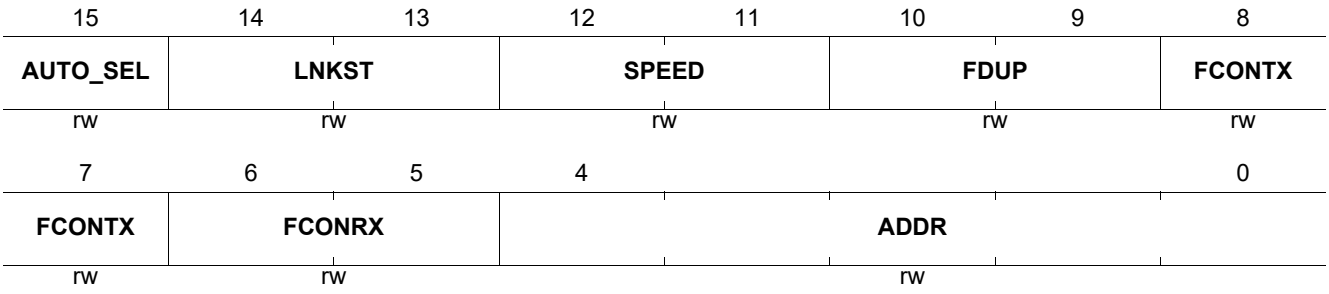
Field	Bits	Type	Description
FREQ	7:0	rw	**MDIO Interface Clock Rate** Selects the interface data and clock rate for the MDIO master interface. The MDC clock frequency calculates as: fMDC = Sys_clock_freq/5/((value + 1)*2). This frequency changes when system clock frequency changes. The following values are the frequencies when system clock is 340 MHz. 00000000_B**S0** 34.0 MHz 00000001_B**S1** 17.0 MHz 00000010_B**S2** 11.333 MHz 00000011_B**S3** 8.50 MHz 00000100_B**S4** 6.80 MHz 00000101_B**S5** 5.66 MHz 00000110_B**S6** 4.86 MHz 00000111_B**S7** 4.25 MHz 00001000_B**S8** 3.78 MHz 00001001_B**S9** 3.4 MHz 00001010_B**S10** 3.09 MHz 00001011_B**S11** 2.83 MHz 00001100_B**S12** 2.61 MHz 00001101_B**S13** 2.43 MHz 00001110_B**S14** 2.27 MHz 00001111_B**S15** 2.13 MHz 11111111_B**S255** 132.8 kHz

PHY Address Register PORT 0

This register is used to define the PHY address of the port.

When autopolling in MMDC_CFG_1 is disabled, the modes defined here are used instead of the polling values

PHY_ADDR_0	Offset	Reset Value
PHY Address Register PORT 0	$F415_H$	1800_H



Field	Bits	Type	Description
AUTO_SEL	15	rw	**Information Source for Automatic Mode** 0_B **POLLING** MDIO autopolling results are used for final link information 1_B **GPHY** GPHY link information outputs are used for final link information
LNKST	14:13	rw	**Link Status Control** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **UP** The link status is forced up 10_B **DOWN** The link status is forced down 11_B **RES** Reserved, do not use
SPEED	12:11	rw	**Speed Control** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps 11_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1)
FDUP	10:9	rw	**Full Duplex Control** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Full duplex mode 10_B **RES** Reserved 11_B **DIS** Half duplex mode

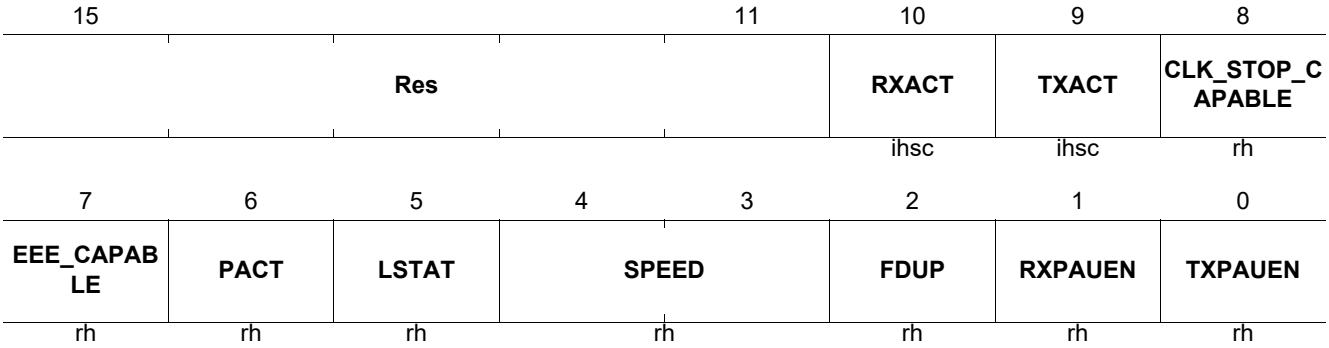
Field	Bits	Type	Description
FCONTX	8:7	rw	**Flow Control Mode TX** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Flow control in receive (ingress direction) only 10_B **RES** Reserved 11_B **DIS** Flow control in transmit (egress direction) only
FCONRX	6:5	rw	**Flow Control Mode RX** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Flow control in receive (ingress direction) only 10_B **RES** Reserved 11_B **DIS** Flow control in transmit (egress direction) only
ADDR	4:0	rw	**PHY Address** Default value is based on **Table 10**.

PHY MDIO Polling Status PORT 0

This register provides information about the current status of the attached Ethernet PHY retrieved by using the auto-polling process.

This status information is retrieved from the attached Ethernet PHY by polling the related MDIO register.

MMDIO_STAT_0	Offset	Reset Value
PHY MDIO Polling Status PORT 0	$F416_H$	0000_H



Field	Bits	Type	Description
RXACT	10	lhsc	**RX Traffic Active** When there is RX traffic (RXDV = ‘1’), this bit is set to 1 by hardware. uC can write ‘1’ to this bit to clear it. 0_B **NOT Active** Not active 1_B **ACT** TX traffic is active
TXACT	9	lhsc	**TX Traffic Active** When there is TX traffic (TXEN = ‘1’), this bit is set to 1 by hardware. uC can write ‘1’ to this bit to clear it. 0_B **NOT Active** Not active 1_B **ACT** TX traffic is active
CLK_STOP_CAPABLE	8	rh	**PHY Supports TX Clock Stop** 0_B **DIS** Clock stop is not supported 1_B **EN** Clock is supported
EEE_CAPABLE	7	rh	**PHY and Link Partner Support EEE for Current Speed** 0_B **DIS** EEE is not supported 1_B **EN** EEE is supported
PACT	6	rh	**PHY Active Status** Indicates when the external PHY is responding to MDIO accesses. This status information is retrieved from the attached Ethernet PHY by polling MDIO registers. 0_B **INACTIVE** The PHY is inactive or not present 1_B **ACTIVE** The PHY is active and responds to MDIO accesses
LSTAT	5	rh	**Link Status** This status information is retrieved from the attached Ethernet PHY by polling the related MDIO register. 0_B **DOWN** The link is down 1_B **UP** The link is up

Field	Bits	Type	Description
SPEED	4:3	rh	**Speed Control** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps or above 11_B **RES** Reserved
FDUP	2	rh	**Full Duplex Status** Indicates when the attached PHY runs in half- or full-duplex mode. This status information is retrieved from the attached Ethernet PHY by polling the related MDIO register. 0_B **HALF** Half-duplex mode 1_B **FULL** Full-duplex mode
RXPAUEN	1	rh	**Receive Pause Enable Status** This status information is retrieved from the attached Ethernet PHY by polling the related MDIO register. 0_B **DIS** The link partner does not send pause frames 1_B **EN** The link partner sends pause frames
TXPAUEN	0	rh	**Transmit Pause Enable Status** This status information is retrieved from the attached Ethernet PHY by polling the related MDIO register. 0_B **DIS** The link partner does not accept pause frames 1_B **EN** The link partner accepts pause frames

Similar Registers

The following registers are identical to the Register **MMDIO_STAT_0** defined above.

Table 53 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
MMDIO_STAT_1	PHY MDIO Polling Status PORT 1	$F417_H$	
MMDIO_STAT_2	PHY MDIO Polling Status PORT 2	$F418_H$	
MMDIO_STAT_3	PHY MDIO Polling Status PORT 3	$F419_H$	
MMDIO_STAT_5	PHY MDIO Polling Status PORT 5	$F41B_H$	

PHY Address Register PORT 1

This register is used to define the PHY address of the port.

When autopolling in MMDC_CFG_1 is disabled, the modes defined here are used instead of the polling values.

PHY_ADDR_1	Offset	Reset Value
PHY Address Register PORT 1	$F414_H$	1801_H

15	14	13	12	11	10	9	8
AUTO_SEL	LNKST		SPEED		FDUP		FCONTX
rw	rw		rw		rw		rw

7	6	5	4				0
FCONTX	FCONRX		ADDR				
rw	rw		rw				

Field	Bits	Type	Description
AUTO_SEL	15	rw	**Information Source for Automatic Mode** 0_B **POLLING** MDIO autopolling results are used for final link information 1_B **GPHY** GPHY link information outputs are used for final link information
LNKST	14:13	rw	**Link Status Control** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **UP** The link status is forced up 10_B **DOWN** The link status is forced down 11_B **RES** Reserved, do not use
SPEED	12:11	rw	**Speed Control** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps 11_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1)
FDUP	10:9	rw	**Full Duplex Control** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Full duplex mode 10_B **RES** Reserved 11_B **DIS** Half duplex mode

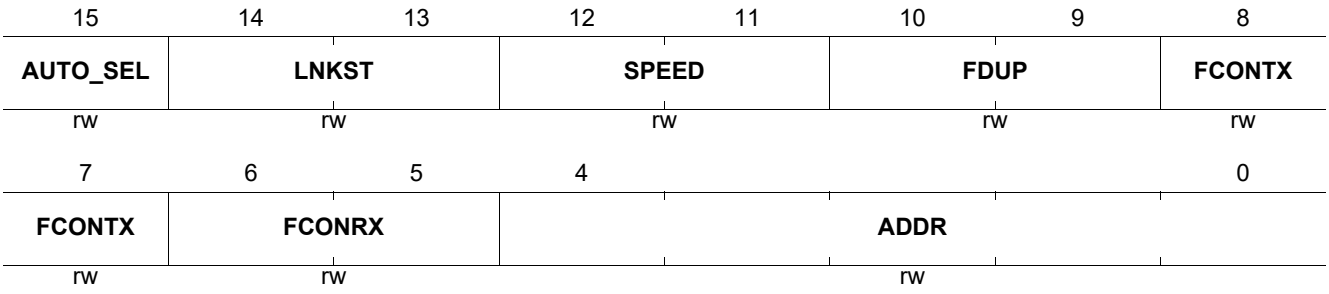
Field	Bits	Type	Description
FCONTX	8:7	rw	**Flow Control Mode TX** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Flow control in receive (ingress direction) only 10_B **RES** Reserved 11_B **DIS** Flow control in transmit (egress direction) only
FCONRX	6:5	rw	**Flow Control Mode RX** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Flow control in receive (ingress direction) only 10_B **RES** Reserved 11_B **DIS** Flow control in transmit (egress direction) only
ADDR	4:0	rw	**PHY Address** Default value is based on **Table 10**.

PHY Address Register PORT 2

This register is used to define the PHY address of the port.

When autopolling in MMDC_CFG_1 is disabled, the modes defined here are used instead of the polling values.

PHY_ADDR_2	Offset	Reset Value
PHY Address Register PORT 2	$F413_H$	1802_H



Field	Bits	Type	Description
AUTO_SEL	15	rw	**Information Source for Automatic Mode** 0_B **POLLING** MDIO autopolling results are used for final link information 1_B **GPHY** GPHY link information outputs are used for final link information
LNKST	14:13	rw	**Link Status Control** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **UP** The link status is forced up 10_B **DOWN** The link status is forced down 11_B **RES** Reserved, do not use
SPEED	12:11	rw	**Speed Control** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps 11_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1)
FDUP	10:9	rw	**Full Duplex Control** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Full duplex mode 10_B **RES** Reserved 11_B **DIS** Half duplex mode

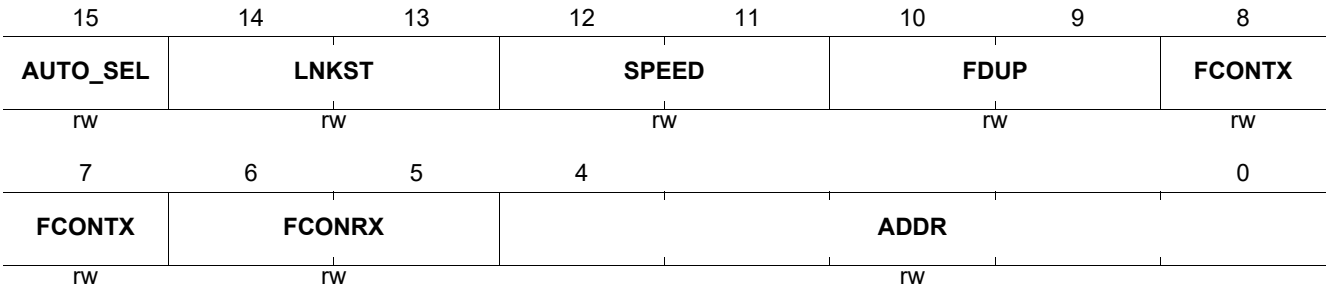
Field	Bits	Type	Description
FCONTX	8:7	rw	**Flow Control Mode TX** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Flow control in receive (ingress direction) only 10_B **RES** Reserved 11_B **DIS** Flow control in transmit (egress direction) only
FCONRX	6:5	rw	**Flow Control Mode RX** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Flow control in receive (ingress direction) only 10_B **RES** Reserved 11_B **DIS** Flow control in transmit (egress direction) only
ADDR	4:0	rw	**PHY Address** Default value is based on **Table 10**.

PHY Address Register PORT 3

This register is used to define the PHY address of the port.

When autopolling in MMDC_CFG_1 is disabled, the modes defined here are used instead of the polling values.

PHY_ADDR_3	Offset	Reset Value
PHY Address Register PORT 3	$F412_H$	1803_H



Field	Bits	Type	Description
AUTO_SEL	15	rw	**Information Source for Automatic Mode** 0_B **POLLING** MDIO autopolling results are used for final link information 1_B **GPHY** GPHY link information outputs are used for final link information
LNKST	14:13	rw	**Link Status Control** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **UP** The link status is forced up 10_B **DOWN** The link status is forced down 11_B **RES** Reserved, do not use
SPEED	12:11	rw	**Speed Control** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps 11_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1)
FDUP	10:9	rw	**Full Duplex Control** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Full duplex mode 10_B **RES** Reserved 11_B **DIS** Half duplex mode

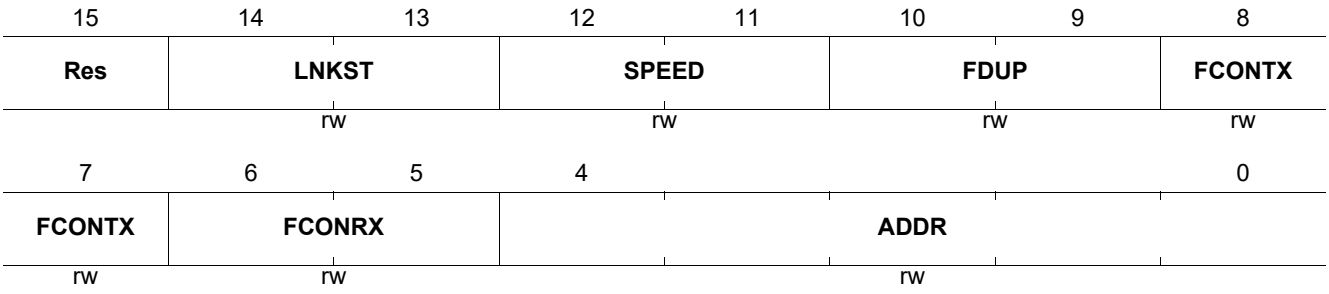
Field	Bits	Type	Description
FCONTX	8:7	rw	**Flow Control Mode TX** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Flow control in receive (ingress direction) only 10_B **RES** Reserved 11_B **DIS** Flow control in transmit (egress direction) only
FCONRX	6:5	rw	**Flow Control Mode RX** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Flow control in receive (ingress direction) only 10_B **RES** Reserved 11_B **DIS** Flow control in transmit (egress direction) only
ADDR	4:0	rw	**PHY Address** Default value is based on **Table 10**.

PHY Address Register PORT 4

This register is used to define the PHY address of the port.

When autopolling in MMDC_CFG_1 is disabled, the modes defined here are used instead of the polling values.

PHY_ADDR_4	Offset	Reset Value
PHY Address Register PORT 4	$F411_H$	1804_H



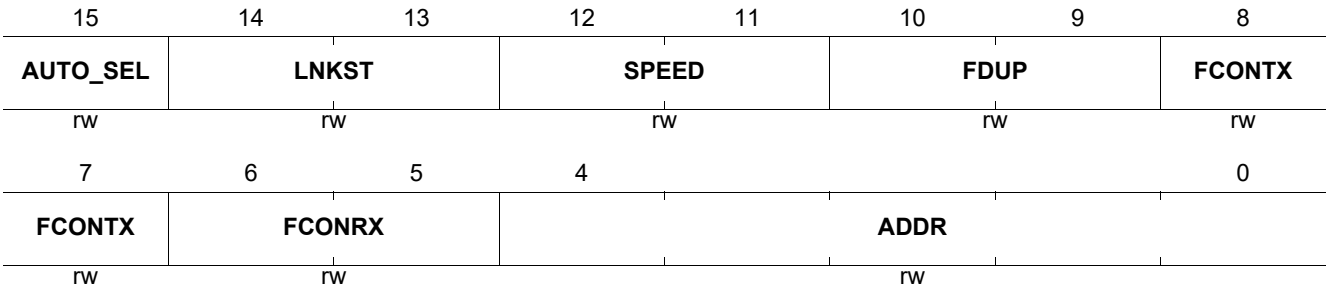
Field	Bits	Type	Description
LNKST	14:13	rw	**Link Status Control** 00_B **AUTO** Automatic mode detection by SGMII 01_B **UP** The link status is forced up 10_B **DOWN** The link status is forced down 11_B **RES** Reserved, do not use
SPEED	12:11	rw	**Speed Control** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps or above 11_B **AUTO** Automatic mode detection by SGMII
FDUP	10:9	rw	**Full Duplex Control** 00_B **AUTO** Automatic mode detection by SGMII 01_B **EN** Full duplex mode 10_B **RES** Reserved 11_B **DIS** Half duplex mode
FCONTX	8:7	rw	**Flow Control Mode TX** 00_B **AUTO** Automatic mode detection SGMII 01_B **EN** Flow control in receive (ingress direction) only 10_B **RES** Reserved 11_B **DIS** Flow control in transmit (egress direction) only
FCONRX	6:5	rw	**Flow Control Mode RX** 00_B **AUTO** Automatic mode detection by SGMII (default) 01_B **EN** Flow control in receive (ingress direction) only 10_B **RES** Reserved 11_B **DIS** Flow control in transmit (egress direction) only
ADDR	4:0	rw	**PHY Address** Default value is based on **Table 10**.

PHY Address Register PORT 5

This register is used to define the PHY address of the port.

When autopolling in MMDC_CFG_1 is disabled, the modes defined here are used instead of the polling values.

PHY_ADDR_5	Offset	Reset Value
PHY Address Register PORT 5	$F410_H$	1805_H



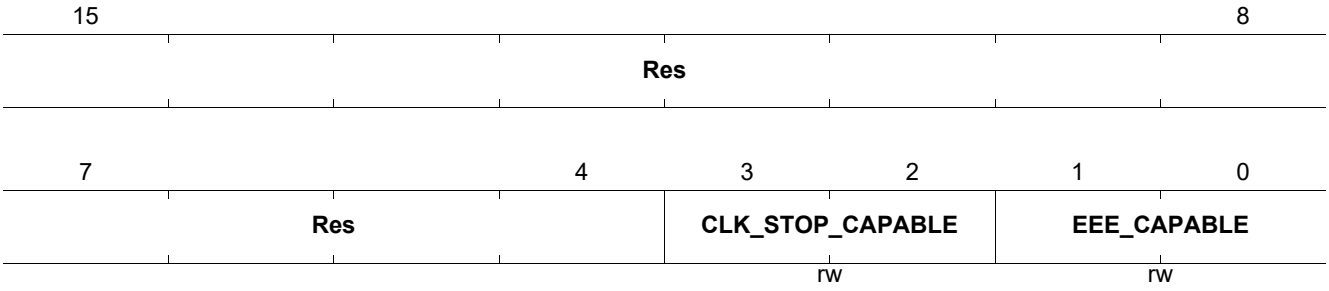
Field	Bits	Type	Description
AUTO_SEL	15	rw	**Information Source for Automatic Mode** 0_B **POLLING** MDIO autopolling results are used for final link information 1_B **GPHY** GPHY link information outputs are used for final link information
LNKST	14:13	rw	**Link Status Control** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **UP** The link status is forced up 10_B **DOWN** The link status is forced down 11_B **RES** Reserved, do not use
SPEED	12:11	rw	**Speed Control** 00_B **M10** Data Rate 10 Mbps 01_B **M100** Data Rate 100 Mbps 10_B **G1** Data Rate 1 Gbps 11_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1)
FDUP	10:9	rw	**Full Duplex Control** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Full duplex mode 10_B **RES** Reserved 11_B **DIS** Half duplex mode

Field	Bits	Type	Description
FCONTX	8:7	rw	**Flow Control Mode TX** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Flow control in receive (ingress direction) only 10_B **RES** Reserved 11_B **DIS** Flow control in transmit (egress direction) only
FCONRX	6:5	rw	**Flow Control Mode RX** 00_B **AUTO** Automatic mode detection by MDIO autopolling (AUTO_SEL = 0) or by GPHY link information outputs (AUTO_SEL = 1) 01_B **EN** Flow control in receive (ingress direction) only 10_B **RES** Reserved 11_B **DIS** Flow control in transmit (egress direction) only
ADDR	4:0	rw	**PHY Address** Default value is based on **Table 10**.

EEE Auto-Negotiation Overrides Port 0

Override what is conveyed to the MAC from the auto-negotiation with PHY.

ANEG_EEE_0	Offset	Reset Value
EEE Auto-Negotiation Overrides Port 0	$F41D_H$	0000_H



Field	Bits	Type	Description
CLK_STOP_CAPABLE	3:2	rw	**Clock Stop Capable** 00_B **AUTO** Automatic detection by autopolling 01_B **EN** Force capable on 10_B **RES** Reserved 11_B **DIS** Force capable off
EEE_CAPABLE	1:0	rw	**EEE Capable** 00_B **AUTO** Automatic detection by auto polling 01_B **EN** Force capable on 10_B **RES** Reserved 11_B **DIS** Force capable off

Similar Registers

The following registers are identical to the Register **ANEG_EEE_0** defined above.

Table 54 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
ANEG_EEE_1	EEE Auto-Negotiation Overrides Port 1	$F41E_H$	
ANEG_EEE_2	EEE Auto-Negotiation Overrides Port 2	$F41F_H$	
ANEG_EEE_3	EEE Auto-Negotiation Overrides Port 3	$F420_H$	
ANEG_EEE_5	EEE Auto-Negotiation Overrides Port 5	$F422_H$	

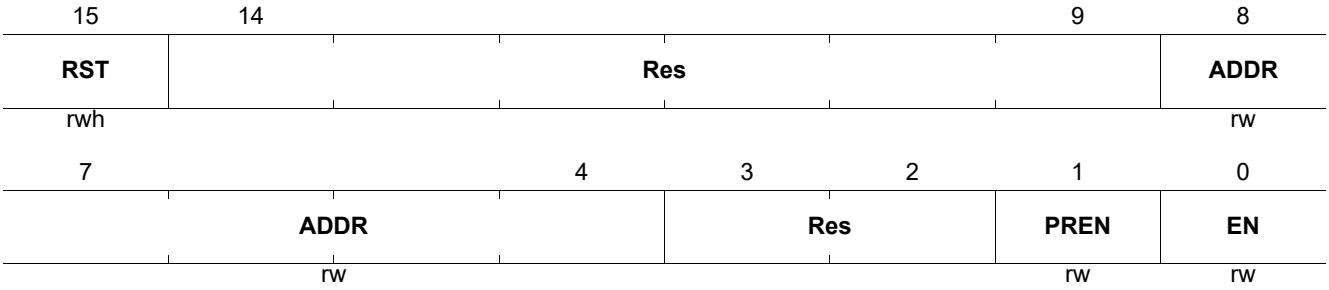
4.1.4 MDIO Slave Registers

This section provides the registers required to control the MDIO slave interface.

MDIO Slave Configuration

This register is used to configure MDIO slave interface.

SMDIO_CFG	Offset	Reset Value
MDC Slave Configuration Register	$F480_H$	$01F1_H$

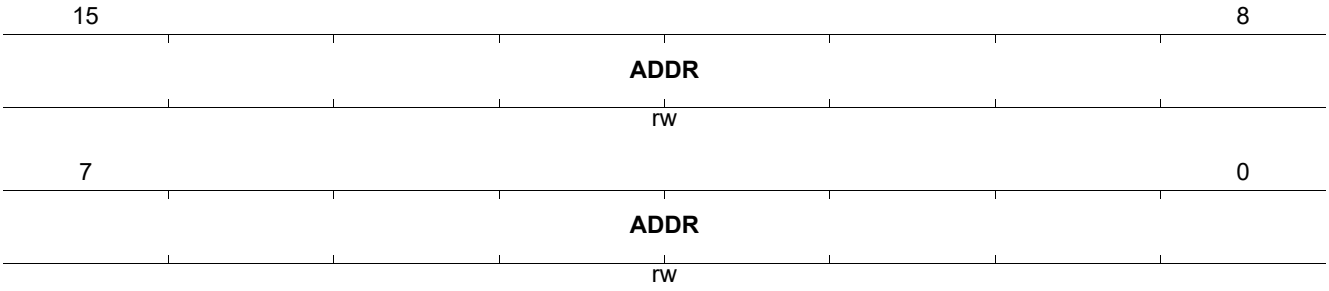


Field	Bits	Type	Description
RST	15	rwh	**MDIO Slave Hardware Reset** Reset all hardware modules except for the register settings. This reset acts similar to the hardware reset, but maintains any programming of the control registers and is cleared by HW after Reset is executed. 0_B **OFF** Reset is off 1_B **ON** Reset is active
ADDR	8:4	rw	**SMDIO Address** This field defined SMDIO address. SMDIO responds to the access of this address.
PREN	1	rw	**SMDIO 32-bit Preamble Enable** 0_B **DIS** Any preamble length can be accepted. 1_B **EN** Only 32-bit preamble length can be accepted.
EN	0	rw	**SMDIO Interface Enable** 0_B **DIS** SMDIO Slave interface is disabled. 1_B **EN** SMDIO Slave interface is enabled.

MDIO Slave Target Base Address

This register is used to configure MDIO slave target base address

SMDIO_BADR	Offset	Reset Value
MDC Slave Target Base Address Register	$F481_H$	00000_H



Field	Bits	Type	Description
ADDR	15:0	rw	**Target Base Address** It stores the target base address. For MDIO slave access, the address of target register is target base address + 5-bit offset address [in SMDIO REGADDR]. This register's SMDIO REGADDR is $1F_H$.

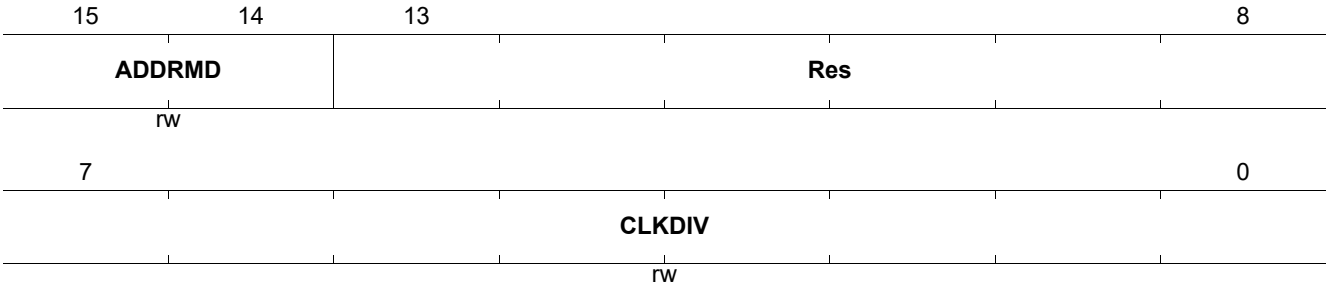
4.1.5 SPI Master Registers

This section provides the registers required for the SPI master interface.

SPI Master Interface Configuration

This register is used to configure SPI master interface mode.

MSPI_CFG	Offset	Reset Value
SPI Master Interface Configuration Register	$F510_H$	8019_H



Field	Bits	Type	Description
ADDRMD	15:14	rw	**SPI Master Addressing Mode** This bit specifies SPI master interface addressing mode. 00_B **9-bit** SPI master interface is in 9-bit address mode. 01_B **16-bit** SPI master interface is in 16/17-bit address mode. 10_B **24-bit** SPI master interface is in 24-bit address mode. 11_B **24H-bit** SPI master interface is in 24-bit high speed access mode.
CLKDIV	7:0	rw	**SPI Clock Divider** This bit specifies SPI master interface clock divider. SPI clock is system core clock divided by this configuration. Frequency of SPI Clock = Sys_clock_freq/8/(CLKDIV+1)

SPI Master Operating Mode Configuration

This register is used to configure SPI master interface operating mode.

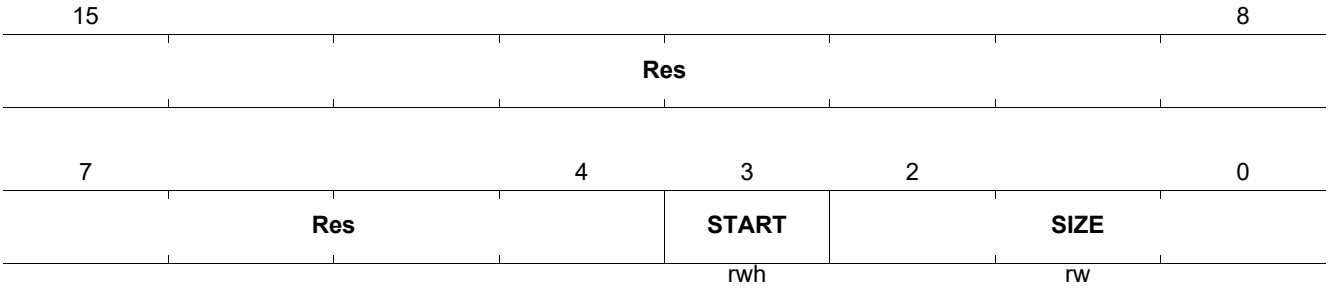
MSPI_OP	Offset	Reset Value
SPI Master Operating Mode Configuration Register	$F511_H$	0000_H

Field	Bits	Type	Description
BUSY	2	rh	**SPI Master Transaction Ongoing** This bit tells SPI master transaction status. 0_B **IDLE** There is no ongoing SPI master transaction. 1_B **PEND** Pending request of manual mode is acknowledged.
MDSTA	1	rh	**SPI Master Operation Mode Status** This bit indicates SPI master operation mode status. 0_B **AUTO** SPI master is in Auto operation mode. 1_B **MANU** SPI master is in manual operation mode.
MDSEL	0	rw	**SPI Master Operation Mode Selection** This bit specifies SPI manual or auto operation mode selection. The changing of this bit triggers the operation mode change request. Manual mode operation can be started when operation mode status is changed to manual mode. 0_B **AUTO** Auto operation mode is selected. 1_B **MANU** Manual operation mode is selected.

SPI Master Manual Mode Control

This register is used to control SPI master manual mode transaction.

MSPI_MANCTRL	Offset	Reset Value
SPI Master Manual Mode Control Register	$F512_H$	0000_H

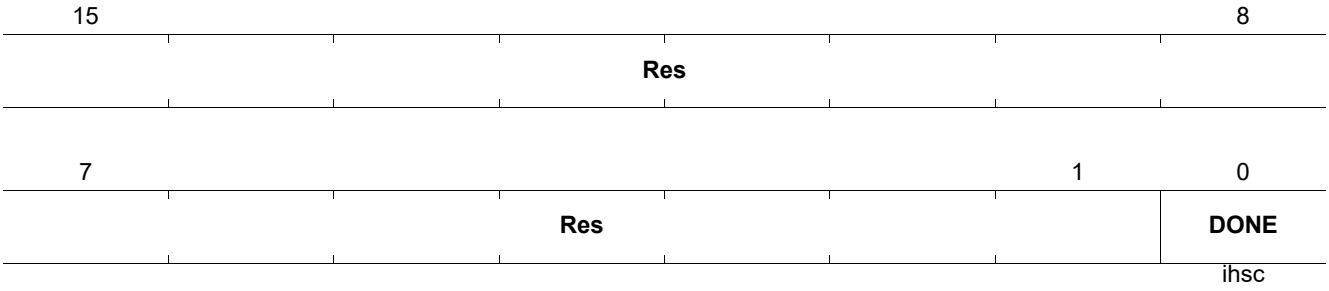


Field	Bits	Type	Description
START	3	rwh	**SPI Manual Mode Transaction Start Request** This bit triggers SPI manual mode transaction to start. Wring to '1' to triggers the manual mode transaction. When the transaction is done, this bit is clear by hardware automatically 0_B **NIL** There is no ongoing manual mode transaction. 1_B **START** Manual mode transaction is started and ongoing.
SIZE	2:0	rw	**SPI Manual Mode Transaction Size** Size of SPI transaction in Bytes (actual size = t_size +1), i.e. 0: size = 1 Byte, 7: size = 8 Byte

SPI Master Interrupt Status Register

This register is used to hold SPI interrupt status.

MSPI_ISR	Offset	Reset Value
SPI Master Interrupt Status Register	$F513_H$	0000_H

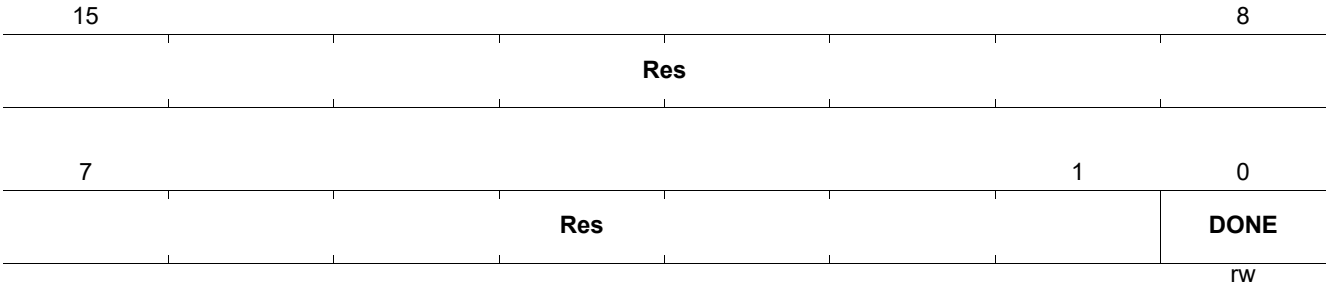


Field	Bits	Type	Description
DONE	0	lhsc	**SPI Manual Operation Transaction Done** This field holds SPI manual operation mode transaction done interrupt. 0_B **NONE** Done interrupt is not triggered. 1_B **DONE** Done interrupt is triggered.

SPI Master Interrupt Enable Register

This register is used to specify SPI interrupt enable.

MSPI_IER	Offset	Reset Value
SPI Master Interrupt Enable Register	$F514_H$	0000_H

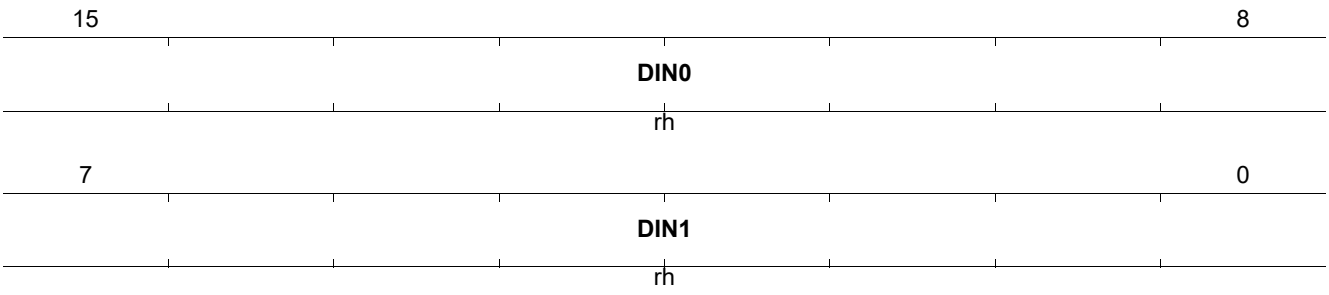


Field	Bits	Type	Description
DONE	0	rw	**SPI Access Done** This field specifies SPI access done interrupt enable 0_B **DIS** Access Done interrupt is disabled. 1_B **EN** Access Done interrupt is enabled.

SPI Master Data In 0/1 Register

This register is used to store SPI data in byte 0 and 1.

MSPI_DIN01	Offset	Reset Value
SPI Master Data In 0/1 Register	$F518_H$	0000_H

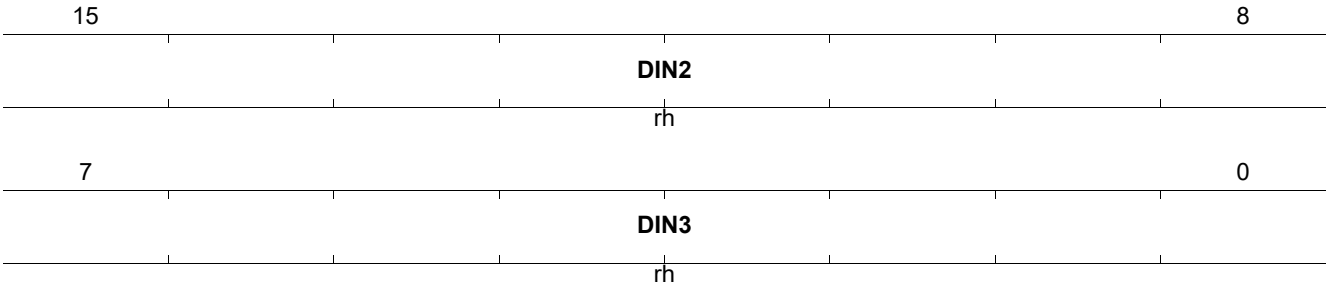


Field	Bits	Type	Description
DIN0	15:8	rh	**SPI Data In Byte 0** This field holds byte 0 (first byte) of the latest read transaction.
DIN1	7:0	rh	**SPI Data In Byte 1** This field holds byte 1 of the latest read transaction.

SPI Master Data In 2/3 Register

This register is used to store SPI data in byte 2 and 3.

MSPI_DIN23	Offset	Reset Value
SPI Master Data In 2/3 Register	$F519_H$	0000_H

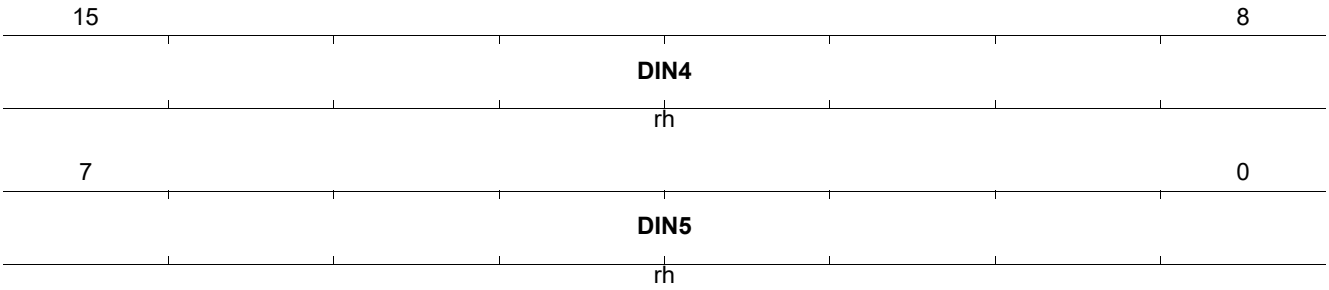


Field	Bits	Type	Description
DIN2	15:8	rh	**SPI Data In Byte 2** This field holds byte 2 of the latest read transaction.
DIN3	7:0	rh	**SPI Data In Byte 3** This field holds byte 3 of the latest read transaction.

SPI Master Data In 4/5 Register

This register is used to store SPI data in byte 4 and 5.

MSPI_DIN45	Offset	Reset Value
SPI Master Data In 4/5 Register	$F51A_H$	0000_H

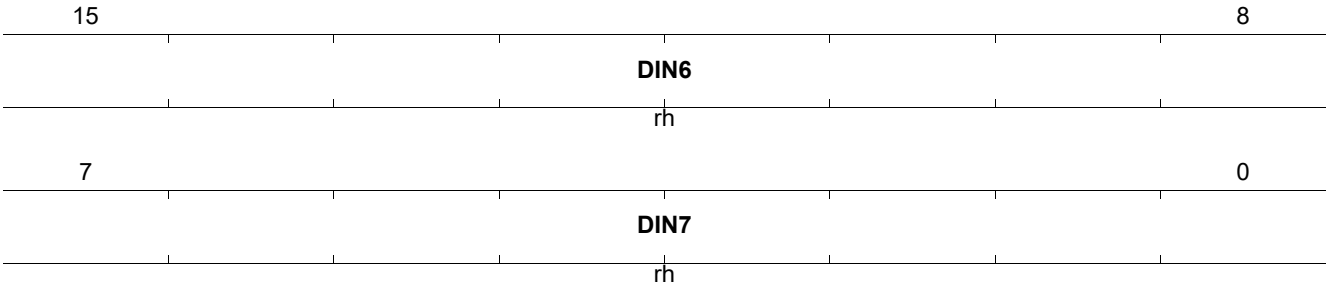


Field	Bits	Type	Description
DIN4	15:8	rh	**SPI Data In Byte 4** This field holds byte 4 of the latest read transaction.
DIN5	7:0	rh	**SPI Data In Byte 5** This field holds byte 5 of the latest read transaction.

SPI Master Data In 6/7 Register

This register is used to store SPI data in byte 6 and 7.

MSPI_DIN67	Offset	Reset Value
SPI Master Data In 6/7Register	$F51B_H$	0000_H

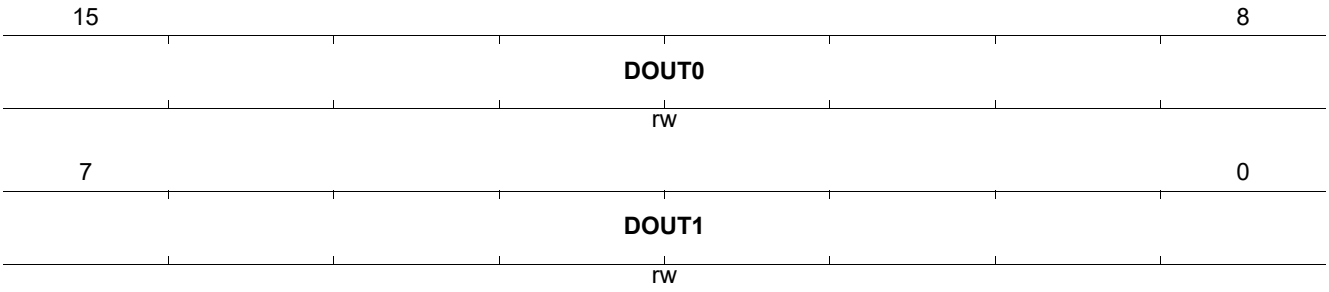


Field	Bits	Type	Description
DIN6	15:8	rh	**SPI Data In Byte 6** This field holds byte 6 of the latest read transaction.
DIN7	7:0	rh	**SPI Data In Byte 7** This field holds byte 7 of the latest read transaction.

SPI Master Data Out 0/1 Register

This register is used to store SPI data out byte 0 and 1.

MSPI_DOUT01	Offset	Reset Value
SPI Master Data Out 0/1 Register	$F51C_H$	0000_H

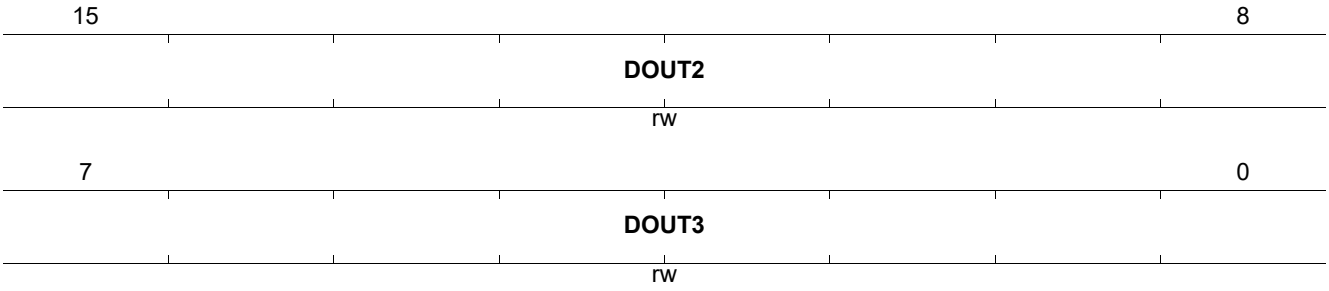


Field	Bits	Type	Description
DOUT0	15:8	rw	**SPI Data Out Byte 0** This field holds byte 0 (first byte) of the latest write transaction.
DOUT1	7:0	rw	**SPI Data Out Byte 1** This field holds byte 1 of the latest write transaction.

SPI Master Data Out 2/3 Register

This register is used to store SPI data out byte 2 and 3.

MSPI_DOUT23	Offset	Reset Value
SPI Master Data Out 2/3 Register	$F51D_H$	0000_H

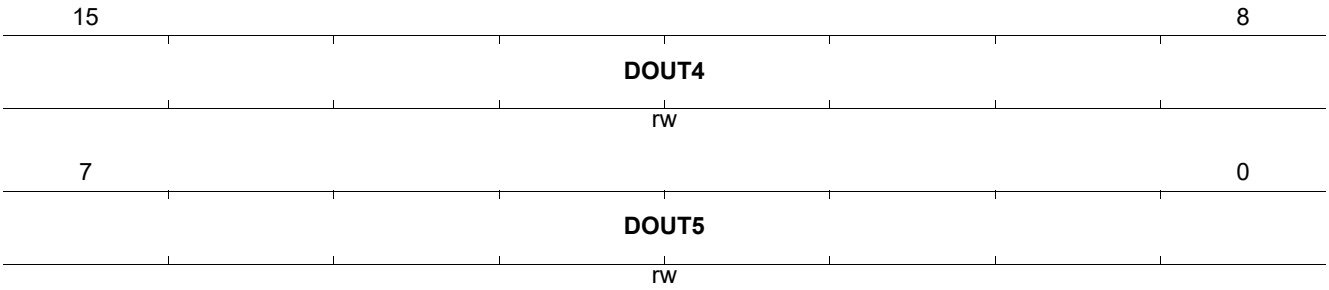


Field	Bits	Type	Description
DOUT2	15:8	rw	**SPI Data Out Byte 2** This field holds byte 2 of the latest write transaction.
DOUT3	7:0	rw	**SPI Data Out Byte 3** This field holds byte 3 of the latest write transaction.

SPI Master Data Out 4/5 Register

This register is used to store SPI data out byte 4 and 5.

MSPI_DOUT45	Offset	Reset Value
SPI Master Data Out 4/5 Register	$F51E_H$	0000_H

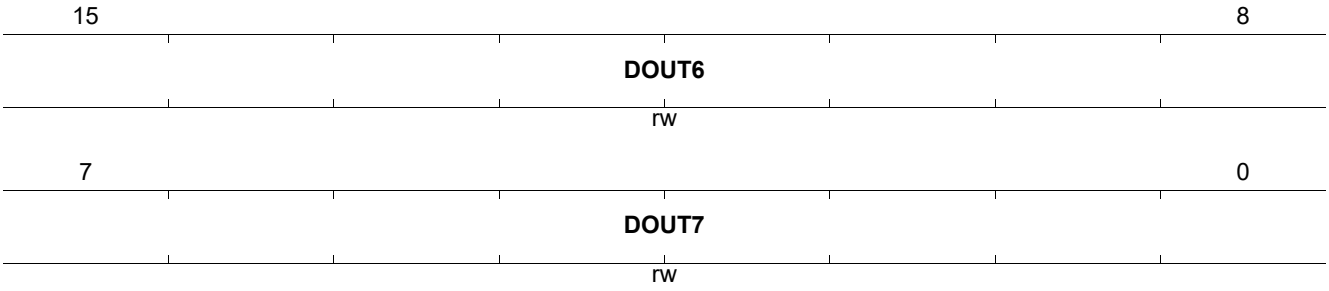


Field	Bits	Type	Description
DOUT4	15:8	rw	**SPI Data Out Byte 4** This field holds byte 4 of the latest write transaction.
DOUT5	7:0	rw	**SPI Data Out Byte 5** This field holds byte 5 of the latest write transaction.

SPI Master Data Out 6/7 Register

This register is used to store SPI data out byte 6 and 7.

MSPI_DOUT67	Offset	Reset Value
SPI Master Data Out 6/7 Register	$F51F_H$	0000_H



Field	Bits	Type	Description
DOUT6	15:8	rw	**SPI Data Out Byte 6** This field holds byte 6 of the latest write transaction.
DOUT7	7:0	rw	**SPI Data Out Byte 7** This field holds byte 7 of the latest write transaction.

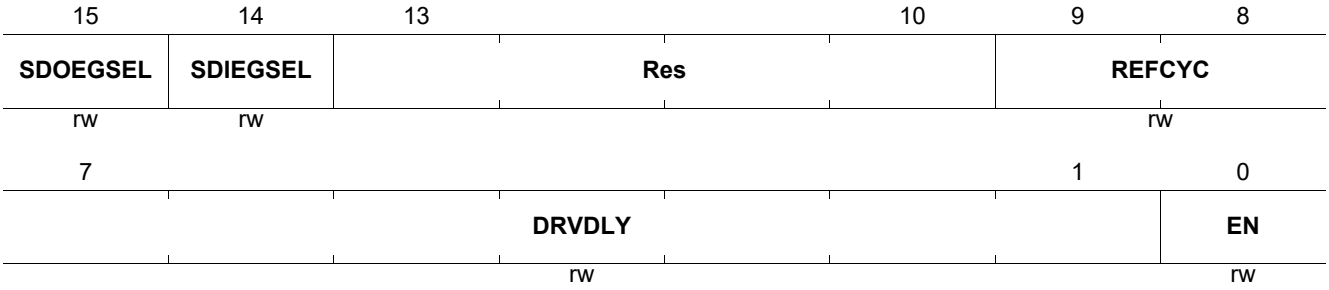
4.1.6 SPI Slave Registers

This section provides the registers required for the SPI slave interface.

SPI Slave Configuration Register

This register is used for SPI Slave Interface Configuration.

SSPI_CFG	Offset	Reset Value
SPI Slave Configuration Register	$F580_H$	0200_H



Field	Bits	Type	Description
SDOEGSEL	15	rw	**SDO Edge Select** This field selects the edge with which a SDO is driven out. For example, when the master expects a rising edge, the driving must be at the rising edge. 0_B **FALL** SDO is driven at falling edge. 1_B **RISE** SDO is driven at rising edge.
SDIEGSEL	14	rw	**SDI Edge Select** This field selects the edge with which a SDI is sampled reliably (e.g. when master drives with rising edge, sampling must be set to falling, VERY IMPORTANT). 0_B **FALL** SDI is sampled at falling edge. 1_B **RISE** SDI is sampled at rising edge.
REFCYC	9:8	rw	**SPI Slave Bus Reference Cycle** It specifies SDO output cycle adjustment, default value is 2, as to allow for adjustments up to 2 SCK clock cycles earlier.
DRVDLY	7:1	rw	**SPI Slave Bus Driver Delay** It specifies delay given in number of core clock cycles. *Note: Values 0 and 1 correspond to about delay of 4 core clock cycles as seen from PAD.*
EN	0	rw	**SPI Save Interface Enable** 0_B **DIS** SPI Slave interface is disabled. 1_B **EN** SPI Slave interface is enabled.

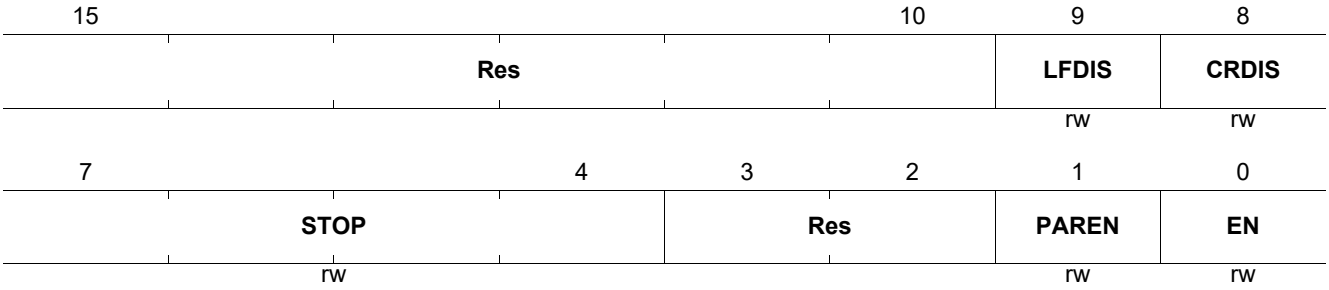
4.1.7 UART Registers

This section provides the registers required for the UART interface.

UART Configuration Register

This register is used for UART Configuration.

UART_CFG	Offset	Reset Value
UART Configuration Register	$F680_H$	0001_H

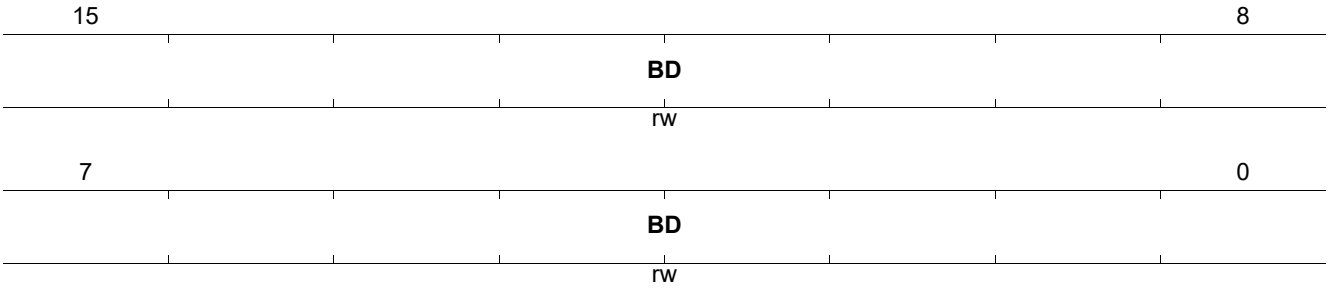


Field	Bits	Type	Description
LFDIS	9	rw	**LF As Enter Disable** 0_B **EN** LF as “echoed enter” is enabled. 1_B **DIS** LF as “echoed enter” is disabled.
CRDIS	8	rw	**CR As Enter Disable** 0_B **EN** CR as “echoed enter” is enabled. 1_B **DIS** CR as “echoed enter” is disabled.
STOP	7:4	rw	**Additional Stop Bits** The number of additional stop bits. The number of stop bits is 1 plus additional stop bits.
PAREN	1	rw	**UART Parity Enable** 0_B **DIS** Parity is disabled. 1_B **EN** Parity is enabled.
EN	0	rw	**UART Interface Enable** 0_B **DIS** UART interface is disabled. 1_B **EN** UART interface is enabled.

UART Baud Rate Register

This register is used for UART Baut Rate Configuration.

UART_BD	Offset	Reset Value
UART Baud Rate Register	$F681_H$	$0B71_H$

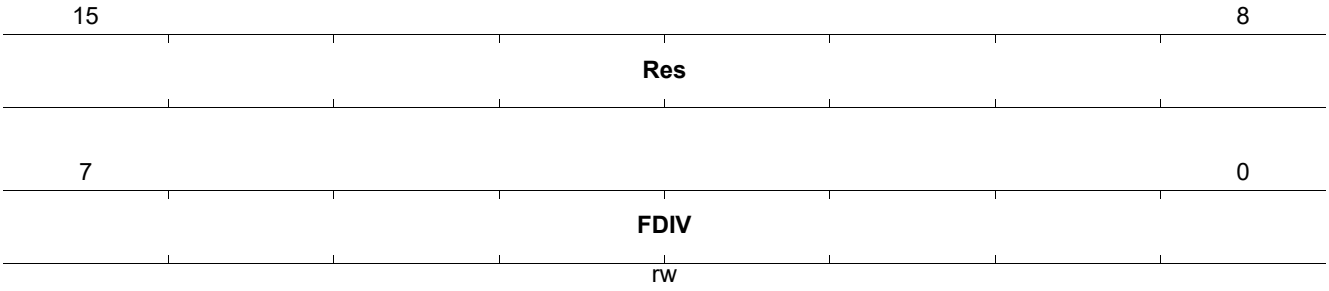


Field	Bits	Type	Description
BD	15:0	rw	**Baud Rate Divider** This field must be configured: round down 250M/baud rate to an integer.

UART Baud Rate Fractional Divider Register

This register is used for UART Baut Rate Fractional Divider Configuration.

UART_FDIV	Offset	Reset Value
UART Baud Rate Fractional Divider Register	$F682_H$	$00B0_H$

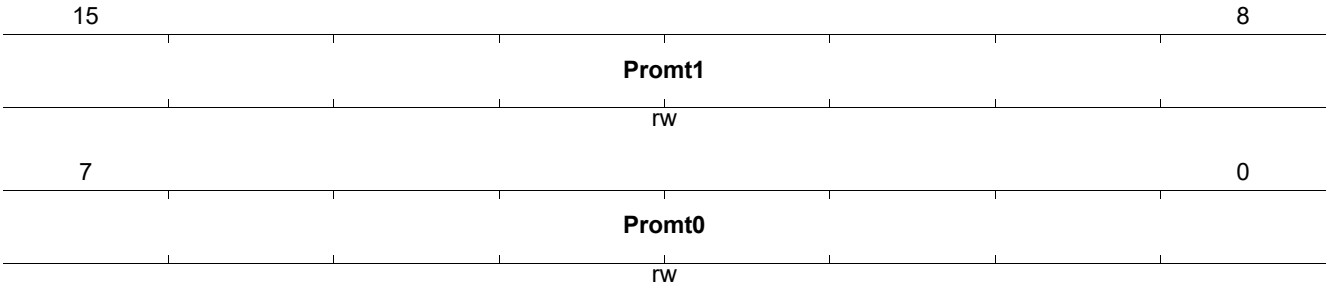


Field	Bits	Type	Description
FDIV	7:0	rw	**Baud Rate Fractional Divider** The baud rate fractional divider is configured to: round up 256*(250M/baud rate - BD) to an integer

UART PROMPT Register

This register is used for UART Prompt.

UART_PROMPT	Offset	Reset Value
UART PROMPT Register	$F683_H$	$003E_H$

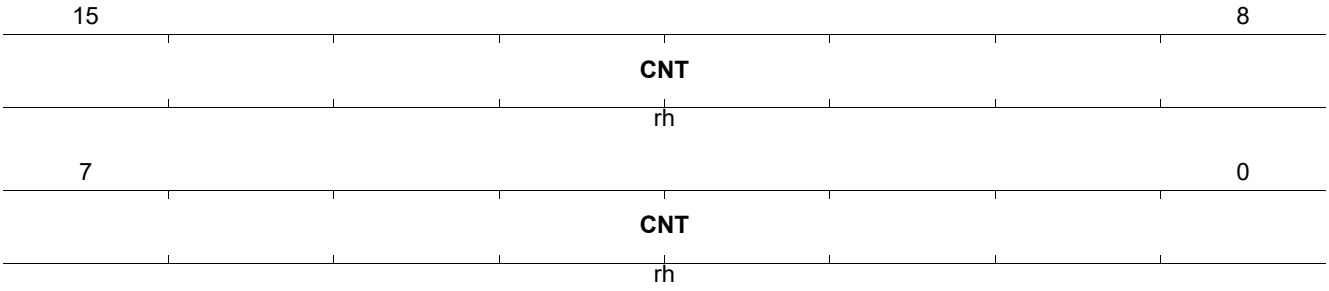


Field	Bits	Type	Description
Promt1	15:8	rw	**Second Prompt Character** When this field is 0, then second prompt character is disabled.
Promt0	7:0	rw	**First Prompt Character**

UART Error Counter Register

This register is used for UART Error Counter Register.

UART_ERRCNT	Offset	Reset Value
UART Error Counter Register	$F684_H$	0000_H



Field	Bits	Type	Description
CNT	15:0	rh	**Error Counter** Error Counter

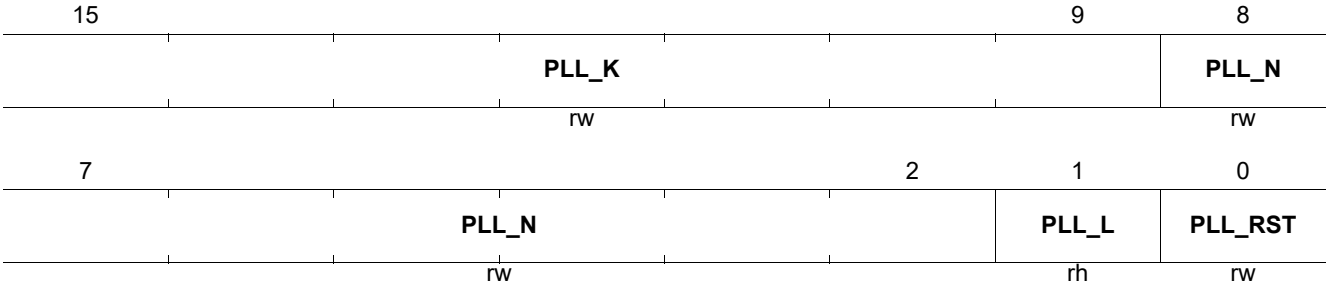
4.1.8 Clock Generation Unit Registers

This section describes all registers in CGU module.

Top Level RO PLL Configuration 0 Register

It configures the top level RO PLL. This register cannot be reset by global software reset and module software reset.

ROPLL_CFG0	Offset	Reset Value
RO PLL Configuration 0 Register	$F980_H$	0141_H



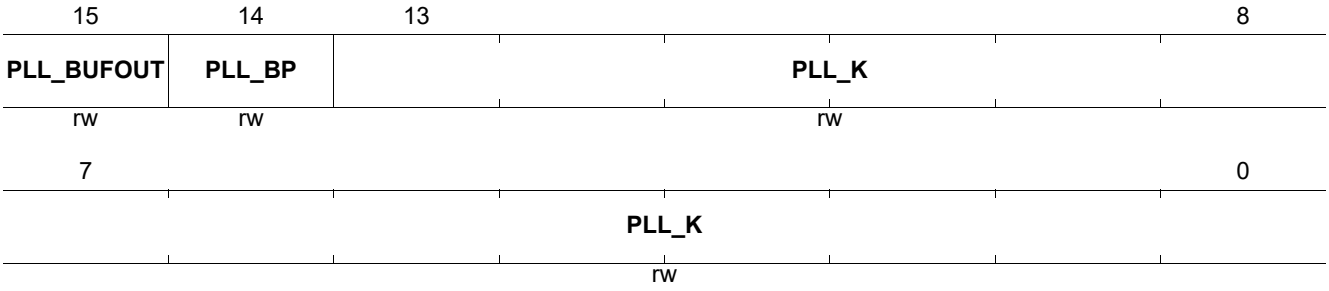
Field	Bits	Type	Description
PLL_K	15:9	rw	**PLL Fractional K Divider 6:0** PLL fractional K divider configuration.
PLL_N	8:2	rw	**PLL N Divider** PLL N divider configuration.

Field	Bits	Type	Description
PLL_L	1	rh	**PLL Lock Status** PLL lock/unlock status information. 0_B **DISABLE** Disable PLL is not locked (default after reset). 1_B **ENABLE** Enable PLL is locked.
PLL_RST	0	rw	**PLL Reset** PLL reset control. 0_B **RST** Reset PLL. 1_B **NORST** No reset PLL.

Top Level RO PLL Configuration 1 Register

It configures the RO PLL. This register cannot be reset by global software reset and module software reset.

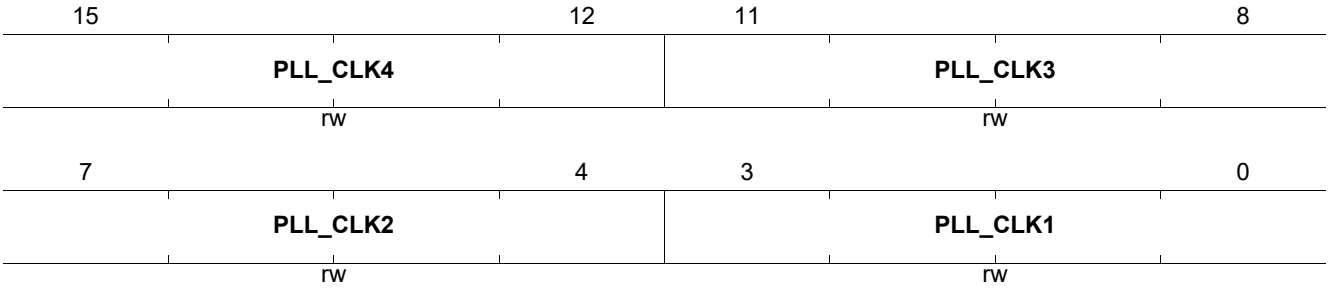
ROPLL_CFG1	Offset	Reset Value
RO PLL Configuration 1 Register	$F984_H$	0000_H



Field	Bits	Type	Description
PLL_BUFOUT	15	rw	**PLL CML input buffer** PLL CML input buffered output enable. Disabled by default, this enable the CML clock buffer for CLKREF and supports buffered clock cascade on chip 0_B **DSIABLE** Disable CML input buffered output disabled 1_B **ENABLE** Enable CML input buffered output enabled
PLL_BP	14	rw	**PLL Bypass** PLL bypass enable. 0_B **DISABLE** Disable PLL is enabled (default). 1_B **ENABLE** Enable PLL is bypassed.
PLL_K	13:0	rw	**PLL0 Fractional K Divider 20 to 7** PLL fractional K divider configuration.

Top Level RO PLL Configuration 2 Register

ROPLL_CFG2	Offset	Reset Value
RO PLL Configuration Register 2	$F988_H$	6666_H



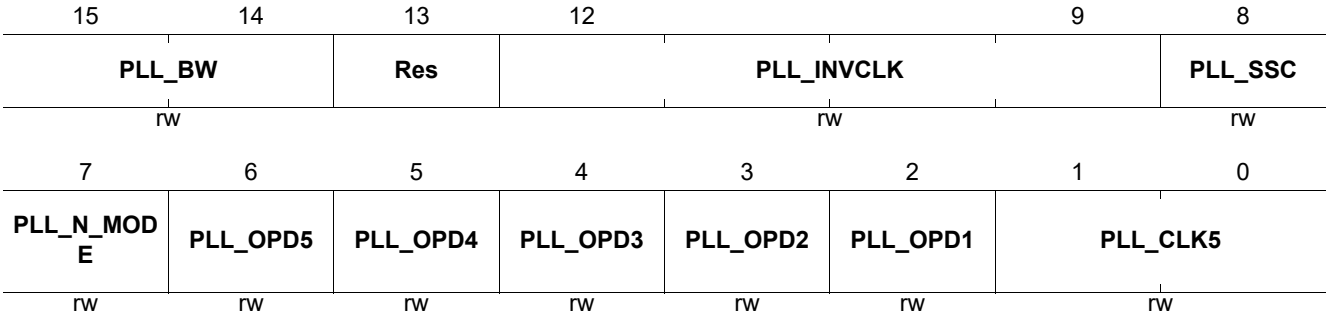
Field	Bits	Type	Description
PLL_CLK4	15:12	rw	**PLL Clock Output 4** PLL Clock output 4 configuration. 0000_B**GND** Ground output clock is disabled 0001_B**DIV2** Divide by 2 of VCO 2 GHz 0010_B**DIV3** Divide by 3 of VCO 2 GHz 0011_B**DIV4** Divide by 4 of VCO 2 GHz 0100_B**DIV5** Divide by 5 of VCO 2 GHz 0101_B**DIV6** Divide by 6 of VCO 2 GHz 0110_B**DIV8** Divide by 8 of VCO 2 GHz 0111_B**DIV10** Divide by 10 of VCO 2 GHz 1000_B**DIV12** Divide by 12 of VCO 2 GHz 1001_B**DIV16** Divide by 16 of VCO 2 GHz 1010_B**DIV20** Divide by 20 of VCO 2 GHz 1011_B**DIV24** Divide by 24 of VCO 2 GHz 1100_B**DIV32** Divide by 32 of VCO 2 GHz 1101_B**DIV40** Divide by 40 of VCO 2 GHz 1110_B**DIV48** Divide by 48 of VCO 2 GHz 1111_B**DIV64** Divide by 64 of VCO 2 GHz

Field	Bits	Type	Description (cont'd)
PLL_CLK3	11:8	rw	**PLL Clock Output 3** PLL Clock output 3 configuration. 0000_B**GND** Ground output clock is disabled 0001_B**DIV2** Divide by 2 of VCO 2 GHz 0010_B**DIV3** Divide by 3 of VCO 2 GHz 0011_B**DIV4** Divide by 4 of VCO 2 GHz 0100_B**DIV5** Divide by 5 of VCO 2 GHz 0101_B**DIV6** Divide by 6 of VCO 2 GHz 0110_B**DIV8** Divide by 8 of VCO 2 GHz 0111_B**DIV10** Divide by 10 of VCO 2 GHz 1000_B**DIV12** Divide by 12 of VCO 2 GHz 1001_B**DIV16** Divide by 16 of VCO 2 GHz 1010_B**DIV20** Divide by 20 of VCO 2 GHz 1011_B**DIV24** Divide by 24 of VCO 2 GHz 1100_B**DIV32** Divide by 32 of VCO 2 GHz 1101_B**DIV40** Divide by 40 of VCO 2 GHz 1110_B**DIV48** Divide by 48 of VCO 2 GHz 1111_B**DIV64** Divide by 64 of VCO 2 GHz
PLL_CLK2	7:4	rw	**PLL Clock Output 2** PLL Clock output 2 configuration. 0000_B**GND** Ground output clock is disabled 0001_B**DIV2** Divide by 2 of VCO 2 GHz 0010_B**DIV3** Divide by 3 of VCO 2 GHz 0011_B**DIV4** Divide by 4 of VCO 2 GHz 0100_B**DIV5** Divide by 5 of VCO 2 GHz 0101_B**DIV6** Divide by 6 of VCO 2 GHz 0110_B**DIV8** Divide by 8 of VCO 2 GHz 0111_B**DIV10** Divide by 10 of VCO 2 GHz 1000_B**DIV12** Divide by 12 of VCO 2 GHz 1001_B**DIV16** Divide by 16 of VCO 2 GHz 1010_B**DIV20** Divide by 20 of VCO 2 GHz 1011_B**DIV24** Divide by 24 of VCO 2 GHz 1100_B**DIV32** Divide by 32 of VCO 2 GHz 1101_B**DIV40** Divide by 40 of VCO 2 GHz 1110_B**DIV48** Divide by 48 of VCO 2 GHz 1111_B**DIV64** Divide by 64 of VCO 2 GHz

Field	Bits	Type	Description (cont'd)
PLL_CLK1	3:0	rw	**PLL Clock Output 1** PLL Clock output 1 configuration. 0000_B**GND** Ground output clock is disabled 0001_B**DIV2** Divide by 2 of VCO 2 GHz 1000 MHz 0010_B**DIV3** Divide by 3 of VCO 2 GHz 666.66 MHz 0011_B**DIV4** Divide by 4 of VCO 2 GHz 500 MHz 0100_B**DIV5** Divide by 5 of VCO 2 GHz 400 MHz 0101_B**DIV6** Divide by 6 of VCO 2 GHz 333.33 MHz 0110_B**DIV8** Divide by 8 of VCO 2 GHz 250 MHz 0111_B**DIV10** Divide by 10 of VCO 2 GHz 200 MHz 1000_B**DIV12** Divide by 12 of VCO 2 GHz 166.66 MHz 1001_B**DIV16** Divide by 16 of VCO 2 GHz 125 MHz 1010_B**DIV20** Divide by 20 of VCO 2 GHz 100 MHz 1011_B**DIV24** Divide by 24 of VCO 2 GHz 83.33 MHz 1100_B**DIV32** Divide by 32 of VCO 2 GHz 62.5 MHz 1101_B**DIV40** Divide by 40 of VCO 2 GHz 50 MHz 1110_B**DIV48** Divide by 48 of VCO 2 GHz 41.67 MHz 1111_B**DIV64** Divide by 64 of VCO 2 GHz 31.25 MHz

Top Level RO PLL Configuration 3 Register

ROPLL_CFG3	Offset	Reset Value
RO PLL Configuration Register 3	$F98C_H$	0178_H



Field	Bits	Type	Description
PLL_BW	15:14	rw	**PLL Bandwidth Select** PLL Bandwidth configuration.
PLL_INVCLK	12:9	rw	**PLL Invert Clock Enable** When '1' select the respective CLK1, CLK2, CLK3, CLK4 output buffer to be inverted as the output. 0_B **DIS** Inverter not enabled. 1_B **EN** Inverter enabled
PLL_SSC	8	rw	**PLL Spread Spectrum Mode** Configures the PLL N mode. 0_B **ENABLE** Enable Fractional input and SSC code is used. 1_B **DISABLE** Disable Ignores fractional and SS code
PLL_N_MODE	7	rw	**Integer N Mode Enable** Integer-N Mode. When high, it ignores the fractional code and SSC code. 0_B **FRAC** Fractional Mode with SSC 1_B **INT** Integer-N Mode only
PLL_OPD5	6	rw	**PLL CLK5 Output Buffer Power Down** Output Clock buffer power down for CLK5 0_B **NORMAL** Buffer is active 1_B **PD** Buffer is power down
PLL_OPD4	5	rw	**PLL CLK4 Output Buffer Power Down** Output Clock buffer power down for CLK4 0_B **NORMAL** Buffer is active 1_B **PD** Buffer is power down
PLL_OPD3	4	rw	**PLL CLK3 Output Buffer Power Down** Output Clock buffer power down for CLK3 0_B **NORMAL** Buffer is active 1_B **PD** Buffer is power down

Field	Bits	Type	Description (cont'd)
PLL_OPD2	3	rw	**PLL CLK2 Output Buffer Power Down** Output Clock buffer power down for CLK2 0_B **NORMAL** Buffer is active 1_B **PD** Buffer is power down
PLL_OPD1	2	rw	**PLL CLK1 Output Buffer Power Down** Output Clock buffer power down for CLK1 0_B **NORMAL** Buffer is active 1_B **PD** Buffer is power down
PLL_CLK5	1:0	rw	**PLL CML CLK5 Output Buffer Frequency Selection** PLL CLK5 CML output freq select 00_B **DIV4** VCO Clock divide by 4 01_B **DIV6** VCO Clock divide by 6 10_B **DIV8** VCO Clock divide by 8 11_B **DIV12** VCO Clock divide by 12

Top Level RO PLL Miscellaneous Control Register

Not specified.

ROPLL_MISC	Offset	Reset Value
RO PLL Miscellaneous Control Register	$F990_H$	0022_H

15	14	13	12	11	10	9	8
PSOVR	UNLCK	FORCE	VEXT	EXTREF	LCKOVR	IPOK	IOPFSEL
rw	ihsc	rwh	rw	rw	rw	rw	rw
7	6	5	4	3	2		0
INKSEL	FPUP	CLKSEL		MODE	MPROG		
rw	rw	rw		rw	rw		

Field	Bits	Type	Description
PSOVR	15	rw	**Pin-Strap Overwrite** When PSOVR='1' we can choose to overwrite the pin-strapped values (MODE, CLKSEL[1:0], INKSEL) with the content of this register.
UNLCK	14	ihsc	**Sticky Bit for Unlock Status** This is a sticky bit status to detect whether the PLL was ever unlock and then relock again. Write 1 to clear.
FORCE	13	rwh	**Force Latching of Shadow Registers** By default, all changes in the PDI registers must not take effect until the next SRSTN. For debug purpose, this bit = '1' enable the user to force the latching without using the SRSTN. The changes can take immediate effect. This bit has a self-clearing behaviour to be implemented behind the rwh register type

Field	Bits	Type	Description
VEXT	12	rw	**PLL Output Buffer Power Supply** PLL output buffer supply select signal - Selects between external 1.1 V supply, or internal Regulator supply to drive the output buffers. **Constants** 0_B **INT** Use Internally generated 1.1 V supply 1_B **EXT** Use Externally generated 1.1 V supply
EXTREF	11	rw	**Select External Reference Current** Select whether we use external Reference Current or the internally generated one. 0_B **INT** Use Internally generated REFERENCE BIASING current 1_B **EXT** Use Externally generated REFERENCE BIASING current
LCKOVR	10	rw	**PLL Lock Overwrite** When set to '1' force the ROPLL to assert lock state regardless of the lock detection status.
IPOK	9	rw	**Internal POK Override** Internal POK Override. This is for debug purpose and force the internal check of Power OK for 1V1 internal LDO power supply generation 0_B **ENABLE** Internal check for Power OK state of the LDO 1_B **OVR** Internal Power OK module disabled
IOPFSEL	8	rw	**PLL Internal Digital Allocates Default Output Frequencies** Selects if PLL internal digital allocates the default output frequencies. When high, the ropll_op_freq_sel_clk1-4 pins are ignored. **Constants** 0_B **EXT** PDI selected output frequencies are used for CLK1-CLK4 1_B **INT** Internal LUT used for the CLK1-CLK4 frequency selection
INKSEL	7	rw	**PLL Internal Mapped N,K or Based on PLL_CFG0/1 N,K** Selects the values of divider (int, frac) from the internal table lookup. When high, ignores the values of PLL_CFG1.K,PLL_CFG0.K, PLL_CFG1.N bits. Effective only when PSOVR=1. Otherwise according to pin-strap PS_XTAL.
FPUP	6	rw	**Force Power Up of All Divider Chains** Force Power up of all Divider chains. For debug purpose only 0_B **NORMAL** Power up the divider chains according to mode select LUT 1_B **FORCE** All divider chain output are forced to power up
CLKSEL	5:4	rw	**PLL Input Clock Select** PLL input clock select - 25/36/125/40 MHz. Effective only when PSOVR=1. Otherwise according to pin-strap PS_XTAL. 00_B **XTAL36** RefCLK is 36 MHz 01_B **XTAL40** RefCLK is 40 MHz 10_B **XTAL25** RefCLK is 25 MHz 11_B **XTAL125** RefCLK is 125 MHz
MODE	3	rw	**Selects CML/CMOS input Clock** PLL input mode select - CML/CMOS. Effective only when PSOVR=1. Otherwise always ‘0’. 0_B **CML** CML differential input clock selected 1_B **CMOS** CMOS differential input clock selected

Field	Bits	Type	Description
MPROG	2:0	rw	**PLL Mode Selection** PLL mode selection. 000_B **TM** Test Mode 001_B **PLL0A** GRX application, PLL0A mode 010_B **PLL0B** GRX application, PLL0B mode 011_B **PLL1** GRX application, PLL1 mode 100_B **GPHY** GPHY ROPLL mode 101_B **WLAN** WAVE application mode

GPC0 Configuration Register

It configures general purpose clock 0.

GPC0_CONF	Offset	Reset Value
GPC0 Configuration Register	$F948_H$	0007_H

Field	Bits	Type	Description
SEL	2:0	rw	**GPC0 Output Clock Selection** This is to select output clock source. 101_B **UCCLK** 1/4 of system clock. 110_B **XO** XO output. 111_B **CLK250** The divided clock of CLK250.

Similar Registers

The following registers are identical to the Register **GPC0_CONF** defined above.

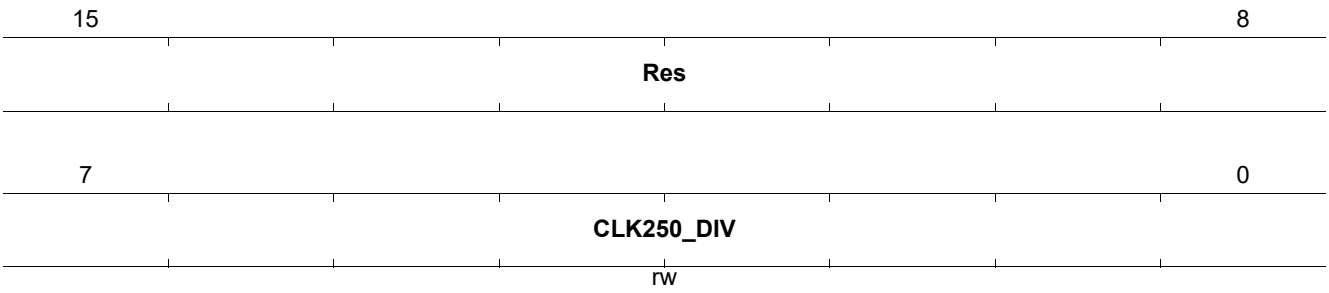
Table 55 Similar Registers

Register Short Name	Register Long Name	Offset Address	Page Number
GPC1_CONF	GPC1 Configuration Register	$F94C_H$	

SYSCLK Configuration Register

It configures sys clock divider.

SYSCLK_CONF	Offset	Reset Value
SYCCLK Configuration Register	$F950_H$	0004_H

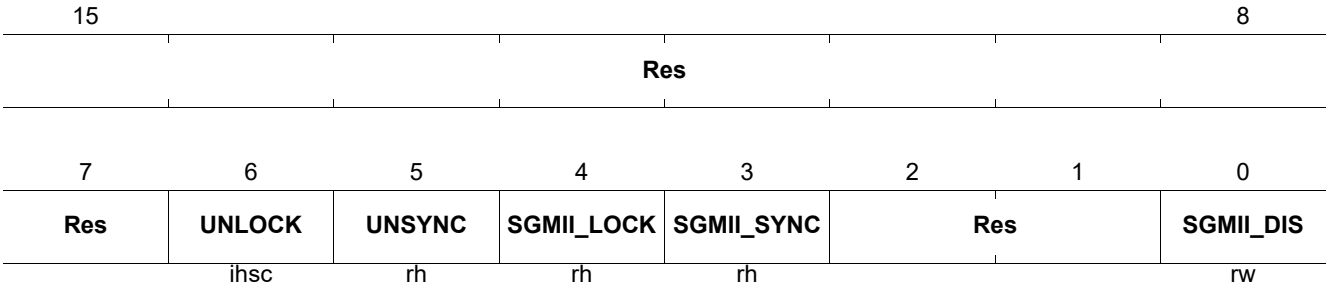


Field	Bits	Type	Description
CLK250_DIV	7:0	rw	**CLK250_LC Clock Divider Selection** When CLK250 is selected for GPC output, the CLK250 is divided before feeding to GPC. The divider is 2*(CLK250_DIV+1).

SGMII Configuration Register

It configures SGMII PLL and macro.

SGMII_CONF	Offset	Reset Value
SGMII Configuration Register	$F954_H$	0000_H

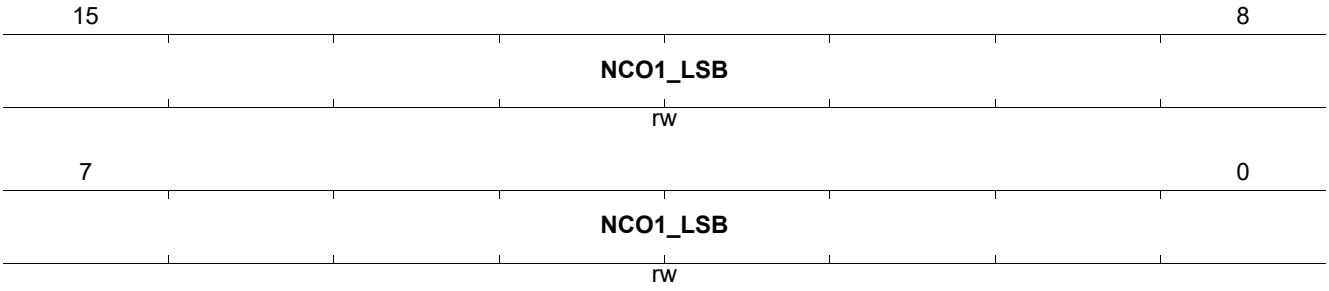


Field	Bits	Type	Description
UNLOCK	6	ihsc	**SGMII PLL Unlock Stick Bit** This is a sticky bit status to detect whether the PLL was ever unlock and then relock again. Write 1 to clear. 0_B **LOCKED** PLL is locked. 1_B **UNLOCKED** PLL is unlocked.
UNSYNC	5	rh	**SGMII PMD/PMA Ready** This is stick bit status to detect whether SGMII PMD/PMA is un-synced. Write 1 to clear. 0_B **SYNCED** PMD/PMA is synced. 1_B **UNSYNC** PMA/PMD is unsynced.
SGMII_LOCK	4	rh	**SGMII PLL Lock** Indicates whether the PMA/PMD receive PLL has achieved lock. This is independent of availability of valid data at RXP/RXM input. 0_B **UNLOCKED** PMA/PMD receive PLL is unlocked. 1_B **LOCKED** PMA/PMD receive PLL is locked.
SGMII_SYNC	3	rh	**SGMII PMD/PMA Ready** Indicates whether the PMA/PMD is able to successfully synch and extract binary data from the incoming differential signals in the RXP/RXM input (when present). Note: This ready status can also be extracted by reading RX_VALID bit in the SGMII_PHY_STAT internal status register. 0_B **NOT_RDY** PMA/PMD core is not able to extract data. 1_B **RDY** PMA/PMD core is able to extract data.
SGMII_DIS	0	rw	**SGMII Macro Disable** This is a high-active level sensitive signal. When activated, inhibits the all activity of the macro and the PMA/PMD core in particular. *Note: The macro is not activated by its non-assertion, it still must be brought up in the proper sequence either by hardware signals or by programming.* 0_B **EN** SGMII Macro is enabled. 1_B **DIS** SGMII Macro is disabled.

NCO1 LSB Configuration Register

It configures NCO1 bit 15 to 0 for generating strobe of 125 MHz average frequency with system clock.

NCO1_LSB	Offset	Reset Value
NCO1 LSB Configuration Register	$F958_H$	$D098_H$

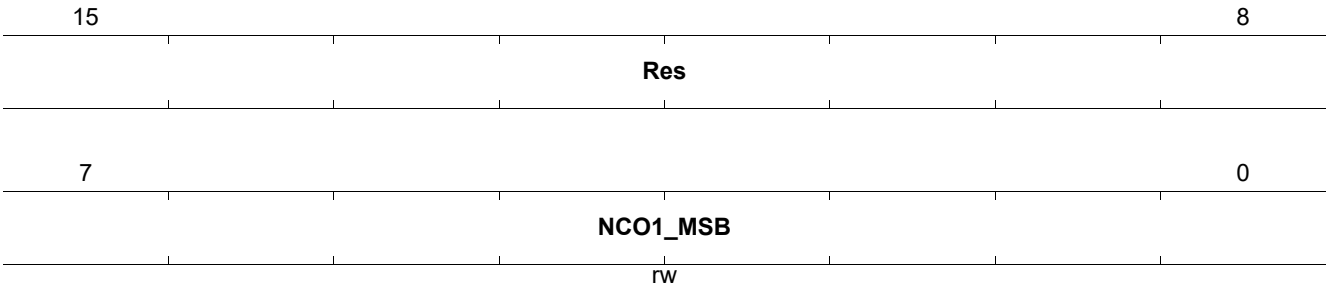


Field	Bits	Type	Description
NCO1_LSB	15:0	rw	**NCO1 LSB** NCO1 value must be 125 MHz/SYS_CLK_Freq* 2^24.

NCO1 MSB Configuration Register

It configures NCO1 bit 23 to 16 for generating strobe of 125 MHz average frequency with system clock.

NCO1_MSB	Offset	Reset Value
NCO1 MSB Configuration Register	$F95C_H$	$005E_H$

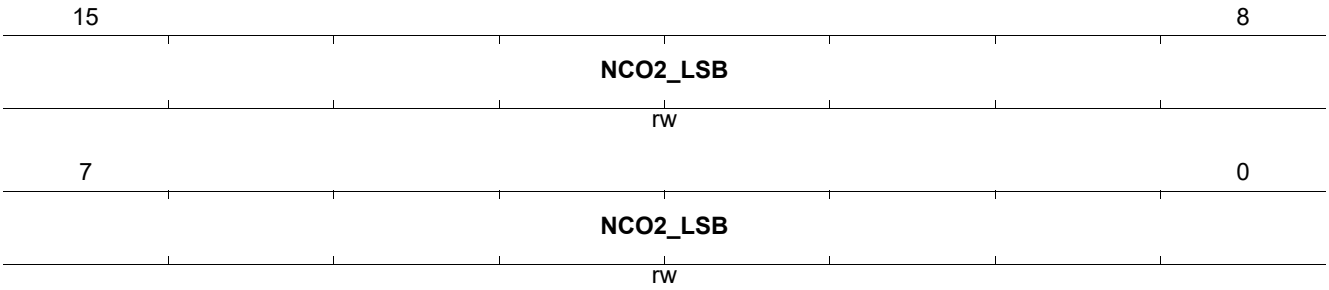


Field	Bits	Type	Description
NCO1_MSB	7:0	rw	**NCO1 MSB** NCO1 value must be 125 MHz/SYS_CLK_Freq* 2^24.

NCO2 LSB Configuration Register

It configures NCO1 bit 15 to 0 for generating strobe of 312.5 MHz or 250 MHz average frequency with system clock.

NCO2_LSB	Offset	Reset Value
NCO2 LSB Configuration Register	$F960_H$	$097C_H$

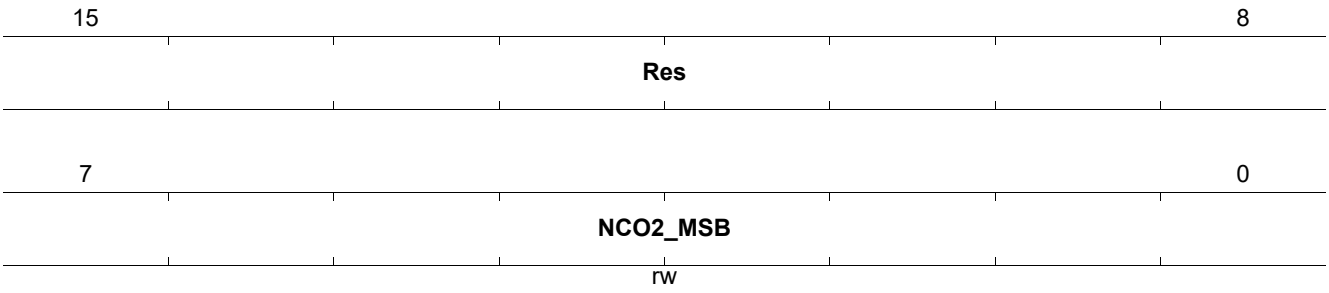


Field	Bits	Type	Description
NCO2_LSB	15:0	rw	**NCO2 LSB** NCO2 value must be 312.5 MHz/SYS_CLK_Freq* 2^24 or 250 MHz/SYS_CLK_Freq*2^24.

NCO2 MSB Configuration Register

It configures NCO2 bit 23 to 16 for generating strobe of 312.5 MHz or 250 MHz average frequency with system clock.

NCO2_MSB	Offset	Reset Value
NCO2 MSB Configuration Register	$F964_H$	$00ED_H$

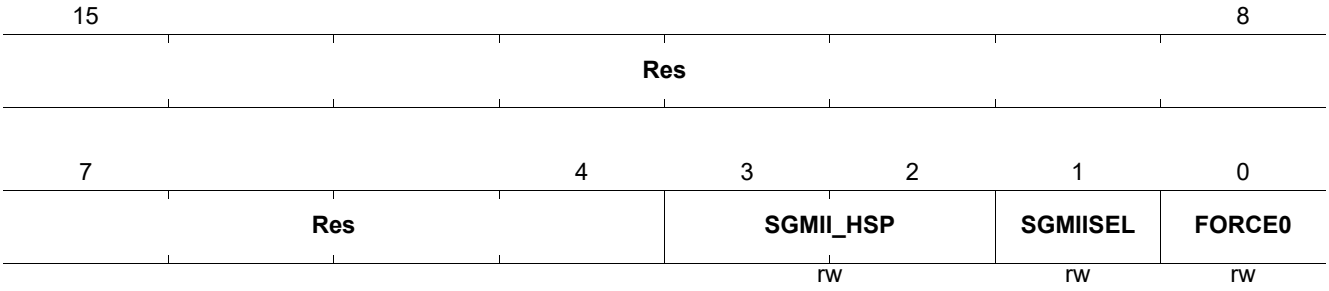


Field	Bits	Type	Description
NCO2_MSB	7:0	rw	**NCO2 MSB** NCO2 value must be 312.5 MHz/SYS_CLK_Freq* 2^24 or 250 MHz/SYS_CLK_Freq*2^24.

NCO Control

This controls NCO1 and NCO2 operation

NCO_CTRL	Offset	Reset Value
NCO Control	$F968_H$	0000_H



Field	Bits	Type	Description
SGMII_HSP	3:2	rw	**SGMII High Speed Selection** When data rate is 1Gbps, NCO1 must be selected for SGMII clock. Otherwise, NCO2 is selected for SGMII clock. 00_B **1Gbps** 1Gbps data rate or below 10_B **2Gbps** 2Gbps data rate. 11_B **2_5Gbps** 2.5Gbps data rate.
SGMIISEL	1	rw	**SGMII Clock NCO Selection** 0_B **NCO1** NCO1 output strobe is used for GMII* interface clock for the port connecting to SGMII. 1_B **NCO2** NCO2 output strobe is used for GMII* interface clock for the port connecting to SGMII.
FORCE0	0	rw	**Reset NCO1 and NCO2 counter to 0** 0_B **NIL** NCO1 and NCO2 counters run. 1_B **ZERO** NCO1 and NCO2 counter stay at 0.

4.1.9 Reset Control Unit Registers

This section describes all registers in RCU module.

Reset Status Register

After a reset, the read-only reset status register RST_STAT indicates the type of reset that occurred and indicates which parts of the chip were affected by the reset.

RESET_STATUS	Offset	Reset Value
Reset Status Register	$FA00_H$	8000_H

15	14						8
HRST	RECORD						
rh	rw						

7						1	0
RECORD							INIT
rw							rw

Field	Bits	Type	Description
HRST	15	rh	**Hardware Reset Cause Flag** 0_B **SRST** The last reset is software reset. 1_B **HRST** The last reset is hardware reset.
RECORD	14:1	rw	**Last Reset Record** The value is not cleared by software reset.
INIT	0	rw	**Initialization Done Flag** The value is not cleared by software reset. 0_B **NO** Initialization is not done. 1_B **DONE** Initialization is done.

Reset Request Register

The Reset Request Register RST_REQ is used to generate a software reset. Unlike the other reset types, the software reset can exclude functions from reset. A software reset is invoked by writing ‘1’ to register RST_REQ.

RST_REQ	Offset	Reset Value
Reset Request Register	$FA01_H$	$002F_H$

15	14	13	12	11	10	9	8
SRST	RD14	Res	G0RST	Res	RD10	RD9	Res
rwh	rw		rwh		rw	rw	

7	6	5	4	3	2	1	0
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
rw	rw	rw	rw	rw	rw	rw	rw

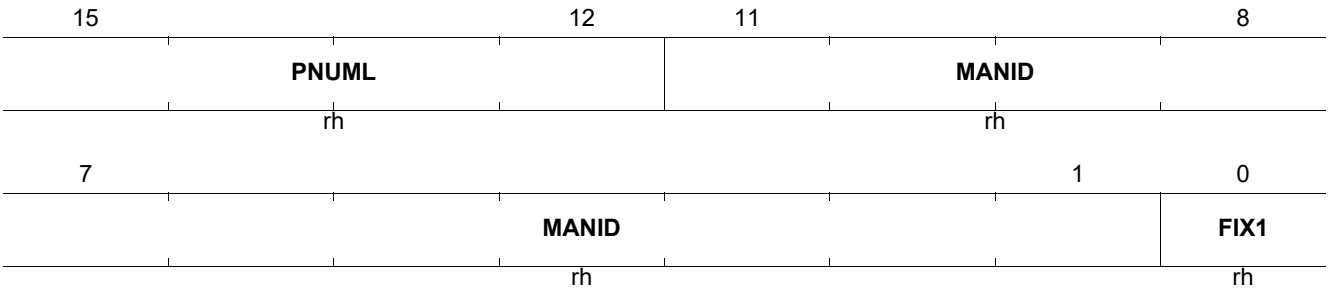
Field	Bits	Type	Description
SRST	15	rwh	**Enable Global Software Reset** Configures the global software reset. Reset is automatically deactivated after some cycles. 0_B **Nil** Global software reset is not issued. 1_B **REQ** Global software reset is triggered.
RD14	14	rw	**Reset Request for Reset Domain RD14** Configures the reset domain 14. Software to decide the required duration. Software reset MGE module. MGE reset type 2 resets all logics excluding register file in MGE module. 0_B **Disabled** MGE software reset type 2 is disabled. 1_B **Enabled** MGE software reset type 2 is enabled.
G0RST	12	rwh	**Enable GPHY0 Reset** Configures the GPHY0 reset. Reset is automatically deactivated after some cycles. 0_B **Nil** GPHY0 reset is not issued. 1_B **REQ** GPHY0 reset is triggered.
RD10	10	rw	**Reset Request for Reset Domain RD10** Configures the reset domain 10. Software to decide the required duration. Software reset GPIO module. 0_B **Disabled** GPIO software reset is disabled. 1_B **Enabled** GPIO software reset is enabled.
RD9	9	rw	**Reset Request for Reset Domain RD9** Configures the reset domain 9. Software to decide the required duration. Software reset MGE module. 0_B **Disabled** MGE software reset is disabled. 1_B **Enabled** MGE software reset is enabled.
RD7	7	rw	**Reset Request for Reset Domain RD7** Configures the reset domain 0. Software to decide the required duration. Software reset CDB. 0_B **Disabled** CDB software reset is disabled. 1_B **Enabled** CDB software reset is enabled.
RD6	6	rw	**Reset Request for Reset Domain RD6** Configures the reset domain 6. Software to decide the required duration. Software reset GPHY Shell. 0_B **Disabled** GPHY Shell software reset is disabled. 1_B **Enabled** GPHY Shell software reset is enabled.
RD5	5	rw	**Reset Request for Reset Domain RD5** Configures the reset domain 5. Software to decide the required duration. Software reset SGMII Shell. 0_B **Disabled** SGMII Shell reset is disabled. 1_B **Enabled** SGMII Shell reset is enabled.
RD4	4	rw	**Reset Request for Reset Domain RD4** Configures the reset domain 4. Software to decide the required duration. 0_B **Disabled** Boot loader reset is disabled. 1_B **Enabled** Boot loader reset is enabled.

Field	Bits	Type	Description
RD3	3	rw	**Reset Request for Reset Domain RD3** Configures the reset domain 3. Software to decide the required duration. Software reset GPHY3 Macro. 0_B **Disabled** GPHY3 Macro software reset is disabled. 1_B **Enabled** GPHY3 Macro software reset is enabled.
RD2	2	rw	**Reset Request for Reset Domain RD2** Configures the reset domain 2. Software to decide the required duration. Software reset GPHY2 Macro. 0_B **Disabled** GPHY2 Macro software reset is disabled. 1_B **Enabled** GPHY2 Macro software reset is enabled.
RD1	1	rw	**Reset Request for Reset Domain RD1** Configures the reset domain 1. Software to decide the required duration. Software reset GPHY1 Macro. 0_B **Disabled** GPHY1 Macro software reset is disabled. 1_B **Enabled** GPHY1 Macro software reset is enabled.
RD0	0	rw	**Reset Request for Reset Domain RD0** Configures the reset domain 0. Software to decide the required duration. Software reset GPHY0 Macro. 0_B **Disabled** GPHY0 Macro software reset is disabled. 1_B **Enabled** GPHY0 Macro software reset is enabled.

MANU ID Register

This shows Manufacturer ID and part number.

MANU_ID	Offset	Reset Value
MANU ID Register	$FA10_H$	1713_H

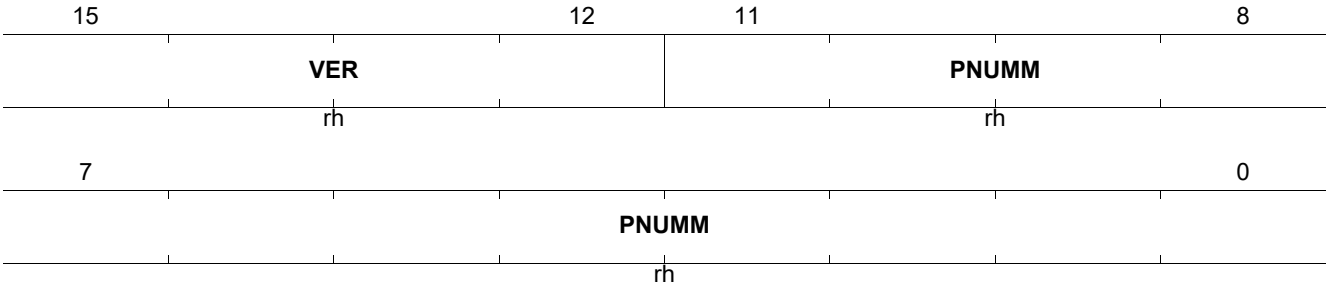


Field	Bits	Type	Description
PNUML	15:12	rh	**Part Number LSB** Part Number LSB
MANID	11:1	rh	**Manufacturer ID** Manufacturer ID, it must be 389_H
FIX1	0	rh	**Fixed to 1** Fixed to 1.

Part Number Register

This shows part number and chip version.

PNUM_ID	Offset	Reset Value
PNUM ID Register	$FA11_H$	$x003_H$

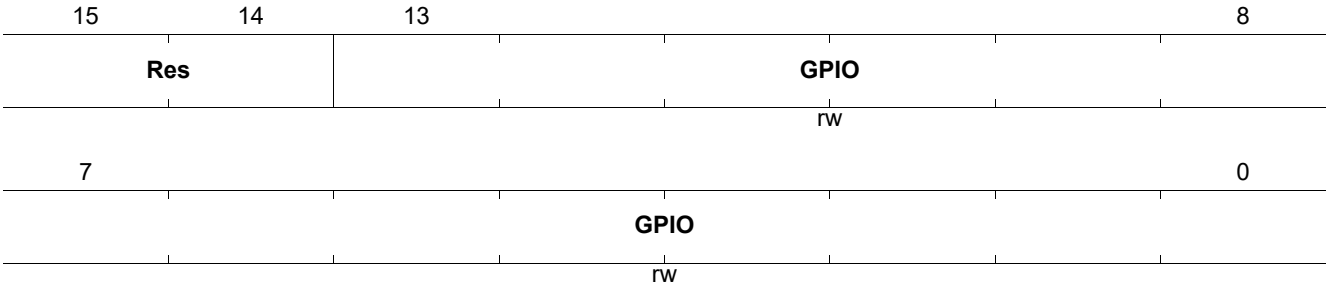


Field	Bits	Type	Description
VER	15:12	rh	**Chip Version** Chip Version ID 0001_B**V1.1** Chip version ID register value is ‘1’ for V1.1. 0010_B**V1.2** Chip version ID register value is ‘2’ for V1.2. 0011_B**V1.3** Chip version ID register value is ‘3’ for V1.3.
PNUMM	11:0	rh	**Part Number MSB** Part Number, Fixed to 003_H

GPIO PAD Driver Strength Control 0 Register

This configures PAD driver strength control.

GPIO_DRIVE0_CFG	Offset	Reset Value
GPIO PAD Driver Strength 0 Control Register	$FA70_H$	$3FFF_H$

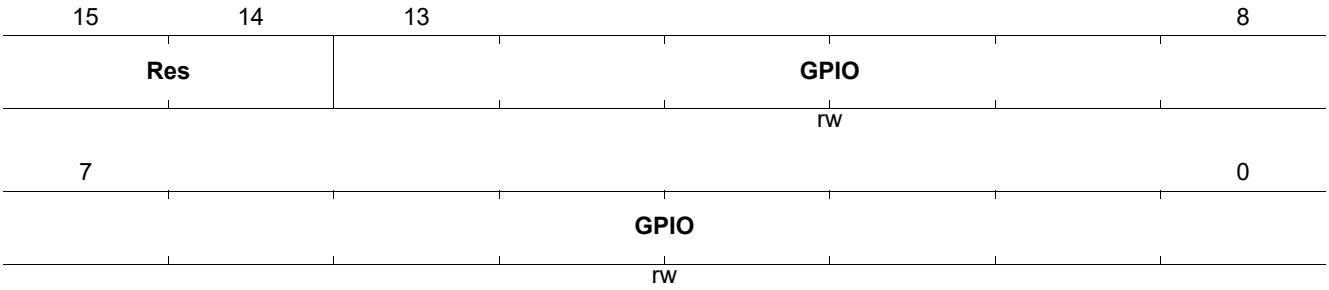


Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO PAD Drive Strength Bit 0** PAD driver strength. 00_B **2mA** PAD drive strength is 2 mA. 01_B **4mA** PAD drive strength is 4 mA. 10_B **8mA** PAD drive strength is 8 mA. 11_B **12mA** PAD drive strength is 12 mA.

GPIO PAD Driver Strength Control 1 Register

This configures PAD driver strength control.

GPIO_DRIVE1_CFG	Offset	Reset Value
GPIO PAD Driver Strength 1 Control Register	$FA71_H$	0000_H

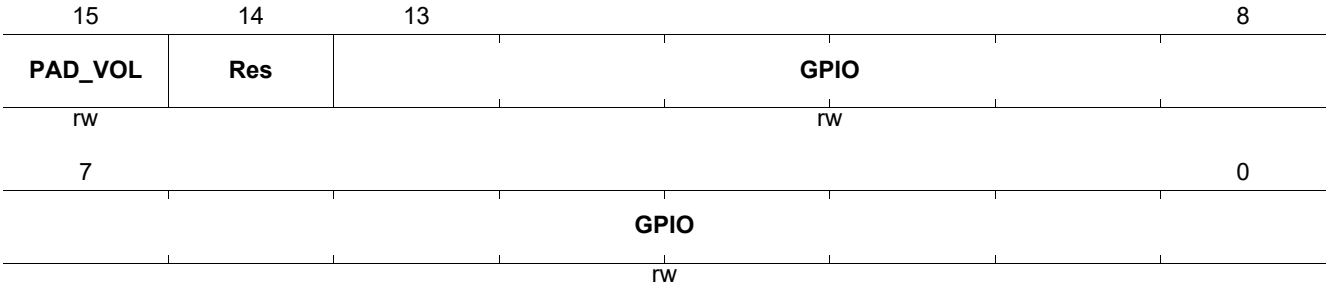


Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO PAD Drive Strength Bit 1** PAD driver strength. 00_B **2mA** PAD drive strength is 2 mA. 01_B **4mA** PAD drive strength is 4 mA. 10_B **8mA** PAD drive strength is 8 mA. 11_B **12mA** PAD drive strength is 12 mA.

GPIO PAD Slew Control Register

This configures GPIO PAD Slew control.

GPIO_SLEW_CFG	Offset	Reset Value
GPIO PAD Slew Control Register	$FA72_H$	0000_H

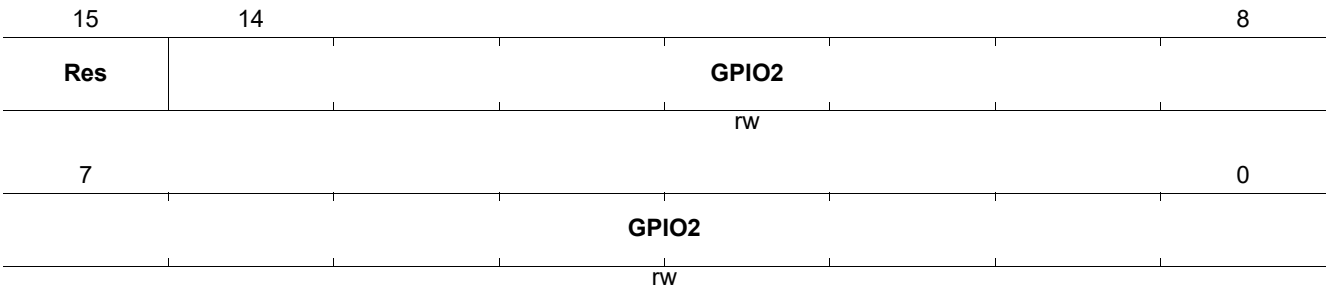


Field	Bits	Type	Description
PAD_VOL	15	rw	**GPIO1 PAD Voltage Supply Level** PAD Slew rate. 0_B **HIGH** GPIO group 1and Reset PAD Voltage supply level is 3.3 V or 2.5 V. 1_B **LOW** GPIO group 1 and Reset PAD Voltage supply level is 1.8 V.
GPIO	13:0	rw	**GPIO PAD Slew Control** PAD slew control. 0_B **Slow** Slow slew. 1_B **Fast** Fast slew.

GPIO2 PAD Driver Strength Control 0 Register

This configures PAD driver strength control.

GPIO2_DRIVE0_CFG	Offset	Reset Value
GPIO2 PAD Driver Strength 0 Control Register	$FA74_H$	$7FFF_H$

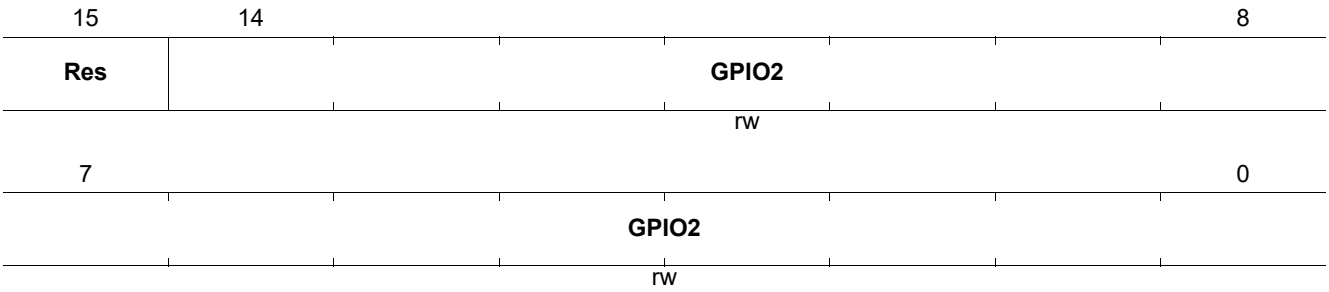


Field	Bits	Type	Description
GPIO2	14:0	rw	**GPIO2 PAD Drive Strength Bit 0** PAD driver strength. 00_B **2mA** PAD drive strength is 2 mA. 01_B **4mA** PAD drive strength is 4 mA. 10_B **8mA** PAD drive strength is 8 mA. 11_B **12mA** PAD drive strength is 12 mA.

GPIO2 PAD Driver Strength Control 1 Register

This configures PAD driver strength control.

GPIO2_DRIVE1_CFG	Offset	Reset Value
GPIO2 PAD Driver Strength 1 Control Register	**$FA75_H$**	**0000_H**

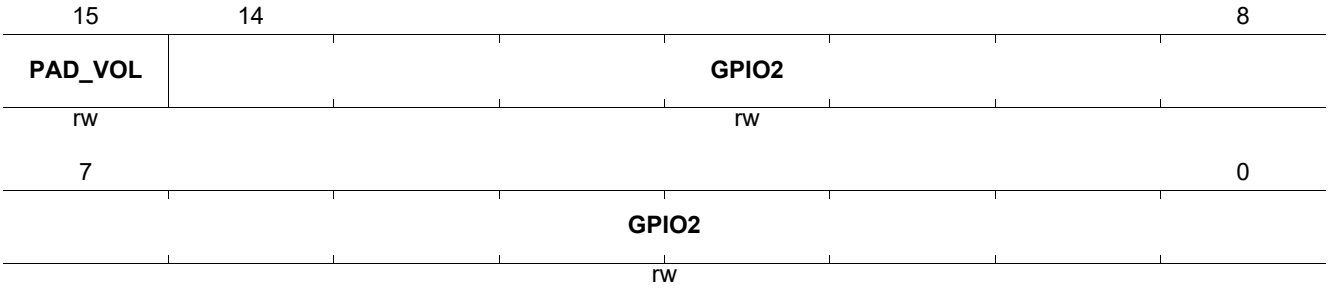


Field	Bits	Type	Description
GPIO2	14:0	rw	**GPIO2 PAD Drive Strength Bit 1** PAD driver strength. 00_B **2mA** PAD drive strength is 2 mA. 01_B **4mA** PAD drive strength is 4 mA. 10_B **8mA** PAD drive strength is 8 mA. 11_B **12mA** PAD drive strength is 12 mA.

GPIO2 PAD Slew Control Register

This configures GPIO2 PAD Slew control.

GPIO2_SLEW_CFG	Offset	Reset Value
GPIO2 Slew Control Register	$FA76_H$	0000_H

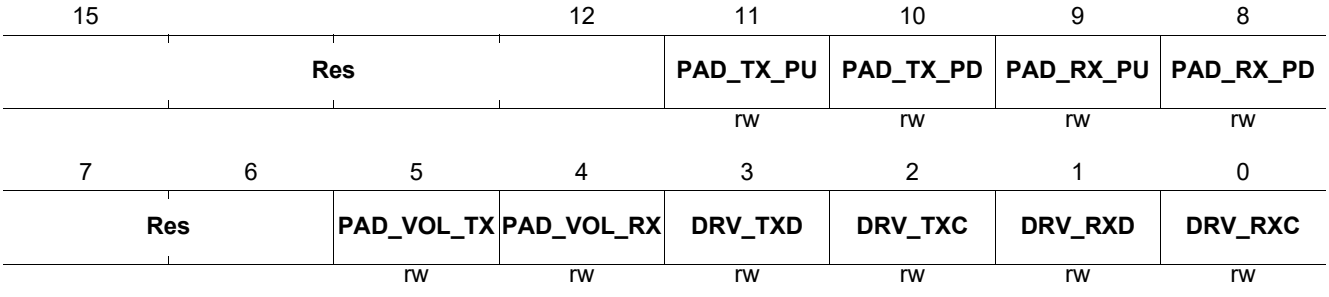


Field	Bits	Type	Description
PAD_VOL	15	rw	**GPIO2 PAD Voltage Supply Level** PAD Slew rate. 0_B **HIGH** GPIO group 2 PAD Voltage supply level is 3.3 V or 2.5 V. 1_B **LOW** GPIO group 2 PAD Voltage supply level is 1.8 V.
GPIO2	14:0	rw	**GPIO PAD Slew Control** PAD slew control. 0_B **Slow** Slow Slew. 1_B **Fast** Fast Slew.

RGMII PAD Slew Control Register

This configures PAD driver strength control.

RGMII_SLEW_CFG	Offset	Reset Value
RGMII PAD Slew Control Register	$FA78_H$	0000_H



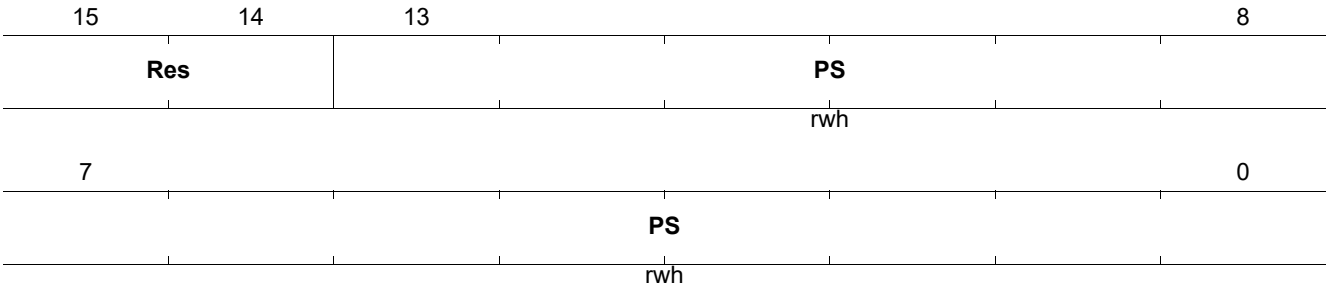
Field	Bits	Type	Description
PAD_TX_PU	11	rw	**RGMII TX PAD Pull Up** Control TX PAD (Including Clock, Data and Control) Pull Up 0_B **DIS** RGMII TX PAD pull up is disabled. 1_B **EN** RGMII TX PAD pull up is enabled.

Field	Bits	Type	Description
PAD_TX_PD	10	rw	**RGMII TX PAD Pull Down** Control TX PAD (Including Clock, Data and Control) Pull Down 0_B **DIS** RGMII TX PAD pull down is disabled. 1_B **EN** RGMII TX PAD pull down is enabled.
PAD_RX_PU	9	rw	**RGMII RX PAD Pull Up** Control RX PAD (Including Clock, Data and Control) Pull Up 0_B **DIS** RGMII RX PAD pull up is disabled. 1_B **EN** RGMII RX PAD pull up is enabled.
PAD_RX_PD	8	rw	**RGMII RX PAD Pull Down** Control RX PAD (Including Clock, Data and Control) Pull Down 0_B **DIS** RGMII RX PAD pull down is disabled. 1_B **EN** RGMII RX PAD pull down is enabled.
PAD_VOL_TX	5	rw	**RGMII TX PAD Voltage Supply Level** TX PAD Voltage Supply 0_B **3.3V** RGMII PAD Voltage supply level is 3.3 V. 1_B **2.5V** RGMII PAD Voltage supply level is 2.5 V.
PAD_VOL_RX	4	rw	**RGMII RX PAD Voltage Supply Level** RX PAD Voltage Supply 0_B **3.3V** RGMII PAD Voltage supply level is 3.3 V. 1_B **2.5V** RGMII PAD Voltage supply level is 2.5 V.
DRV_TXD	3	rw	**RGMII TX Non-Clock PAD Slew Rate** PAD Slew rate. 0_B **Normal** Normal Slew Rate. 1_B **Slow** Slow Slew Rate.
DRV_TXC	2	rw	**RGMII TX Clock Slew Rate** PAD Slew rate. 0_B **Normal** Normal Slew Rate. 1_B **Slow** Slow Slew Rate.
DRV_RXD	1	rw	**RGMII RX Non-Clock PAD Slew Rate** PAD Slew rate. 0_B **Normal** Normal Slew Rate. 1_B **Slow** Slow Slew Rate.
DRV_RXC	0	rw	**RGMII RX Clock Slew Rate** PAD driver strength. 0_B **Normal** Normal Slew Rate. 1_B **Slow** Slow Slew Rate.

Pin-Strapping Register 0

The configuration input pin(s) are sampled and latched at the rising edge of Hardware Reset input. This register cannot be reset by global software reset and module software reset.

PS0	Offset	Reset Value
Pin-Strapping Register	$FA80_H$	$XXXX_H$

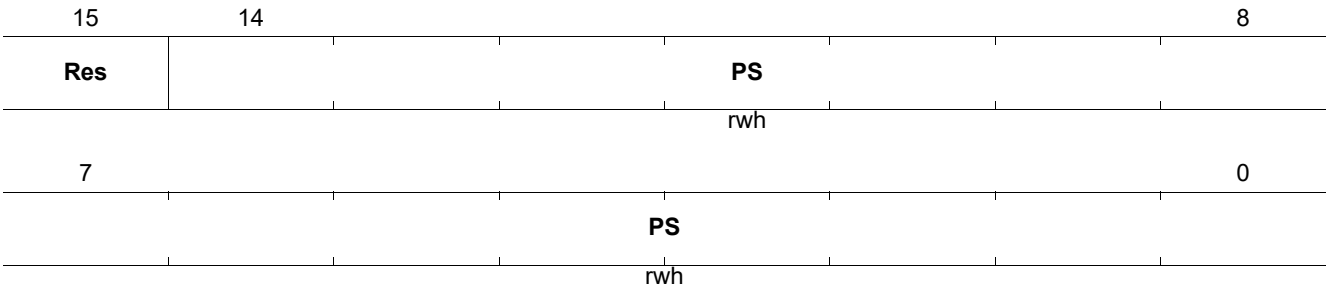


Field	Bits	Type	Description
PS	13:0	rwh	**Pin-Strapping of GPIO0 to GPIO13**

Pin-Strapping Register 1

The configuration input pin(s) are sampled and latched at the rising edge of Hardware Reset input. This register cannot be reset by global software reset and module software reset.

PS1	Offset	Reset Value
Pin-Strapping Register 1	$FA81_H$	$XXXX_H$



Field	Bits	Type	Description
PS	14:0	rwh	**Pin-Strapping of GPIO16 to GPIO30**

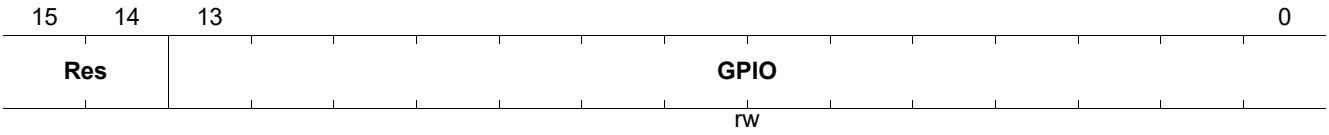
4.1.10 GPIO Registers

The individual control and data bits of each digital parallel port are implemented in a number of registers. Bits with the same meaning and function are assembled together in the same register. Each parallel port consists of a set of registers. The registers are used to configure and use the port as general purpose I/O or alternate function input/output.

GPIO Data Output Register

When a pin is used as general purpose output (GPIO), output data is written into register GPIO_OUT.

GPIO_OUT	Offset	Reset Value
GPIO Data Output Register	$F380_H$	0000_H

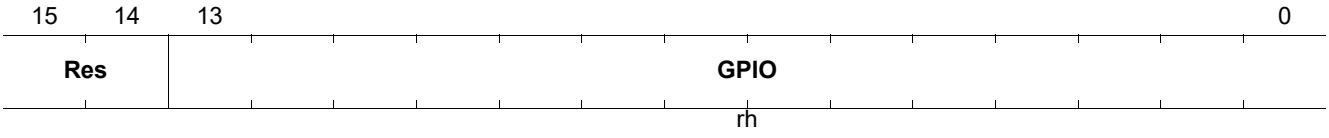


Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Output Value** 0_B **LOW** Output value = 0 *Note: Default value after reset* 1_B **HIGH** Output value = 1

GPIO Data Input Register

The value at a pin can be read through the read-only register GPIO_IN. The data input register GPIO_IN always contains a latched value of the assigned pin.

GPIO_IN	Offset	Reset Value
GPIO Data Input Register	$F381_H$	0000_H



Field	Bits	Type	Description
GPIO	13:0	rh	**GPIO Input Value** 0_B **LOW** Input value = 0 1_B **HIGH** Output value = 1

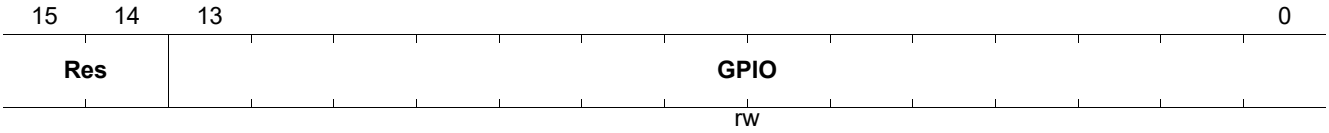
GPIO Direction Register

The direction of port pins can be controlled in the following ways:

- Controlled by Px_DIR register when used for GPIO and controlled by the peripheral when used for alternate function.
- Controlled by Px_DIR register when used as GPIO and fixed direction when used for alternate function.

When the port direction is controlled by the respective direction register Px_DIR, the following encoding is defined.

GPIO_DIR	Offset	Reset Value
GPIO Direction Register	$F382_H$	0000_H



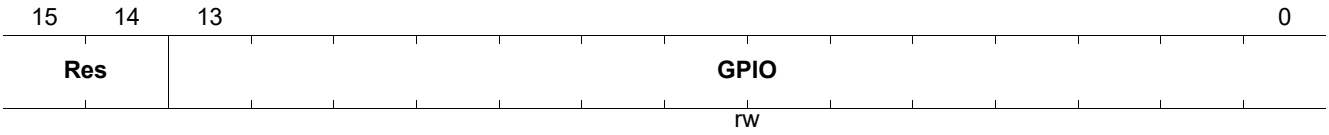
Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Direction Control** 0_B **Input** GPIO is in input mode *Note: Default value after reset* 1_B **Output** GPIO is in output mode

GPIO Alternate Function Select Register 0

Alternate functions are selected via an output multiplexer which can select up to four output lines. This multiplexer can be controlled by the signals of Register **GPIO_ALTSEL0** and 1.

Selection of alternate functions are defined in registers **GPIO_ALTSEL0** and 1.

GPIO_ALTSEL0	Offset	Reset Value
Port 0 Alternate Function Select Register 0	$F383_H$	0000_H



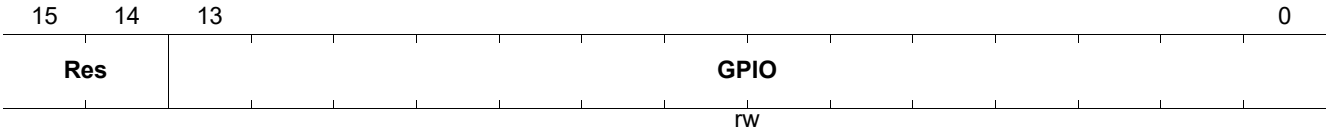
Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Alternate Function Selection LSB** GPIO Alternate Function Selection LSB

GPIO Alternate Function Select Register 1

Alternate functions are selected via an output multiplexer which can select up to four output lines. This multiplexer can be controlled by the signals of Register **GPIO_ALTSEL0** and 1.

Selection of alternate functions are defined in registers **GPIO_ALTSEL0** and 1.

GPIO_ALTSEL1	Offset	Reset Value
Port 0 Alternate Function Select Register 1	$F384_H$	$003C_H$

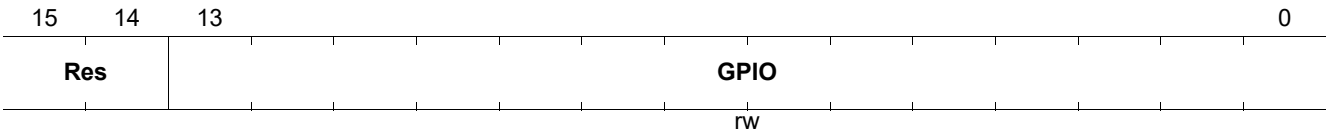


Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Alternate Function Selection MSB** GPIO Alternate Function Selection MSB

GPIO Open Drain Control Register

Each pin in output mode can be switched to Open Drain Mode. When driven with 1, no driver is activated; when driven with 0, the pull-down transistor is activated.

GPIO_OD	Offset	Reset Value
GPIO Open Drain Control Register	$F385_H$	$3FFF_H$



Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Open Drain Mode** 0_B **OD** Open Drain Mode, output is actively driven only for 0 state. 1_B **PP** Normal Mode, output is actively driven for 0 and 1 state.

Port 0 Pull-Up/Pull-Down Select Register

Internal pull-up/pull-down devices can be optionally applied to pin. This offers the possibility to configure the following input characteristics:

- Tristate
- High-impedance with a weak pull-up device
- High-impedance with a weak pull-down device

And the following output characteristics:

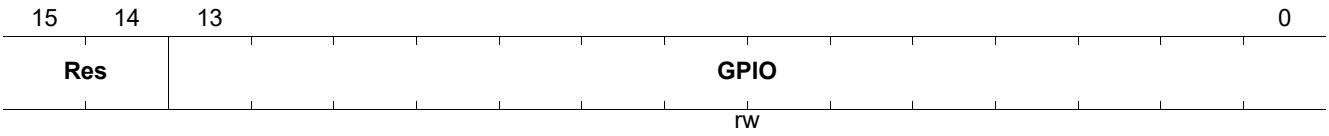
- Push/pull (optional pull-up/pull-down)
- Open drain with internal pull-up
- Open drain with external pull-up

The pull-up/pull-down device can be fixed or controlled via the registers **GPIO_PUDEN**. Register **GPIO_PUDSEL** selects the type of pull-up/pull-down device, while register **GPIO_PUDEN** enables or disables it. The pull-up/pull-down device can be selected pin-wise. The pull-up/pull-down devices are predefined for some pins after reset.

Note: The selected pull-up/pull-down device is enabled by setting the respective bit in the Px_PUDEN register.

GPIO_PUDSEL — **Offset** — **Reset Value**

GPIO Pull-Up/Pull-Down Select Register — **$F386_H$** — **$3FFF_H$**



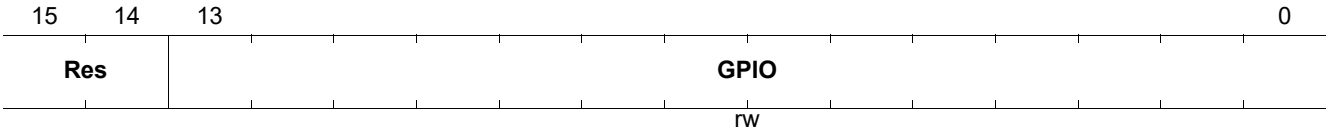
Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Pull Up/Down Mode** 0_B **PD** Internal weak pull down is enabled. 1_B **PU** Internal weak pull up is enabled.

GPIO Pull-Up/Pull-Down Enable Register

See the previous register description.

GPIO_PUDEN — **Offset** — **Reset Value**

GPIO Pull-Up/Pull-Down Enable Register — **$F387_H$** — **$3FFF_H$**

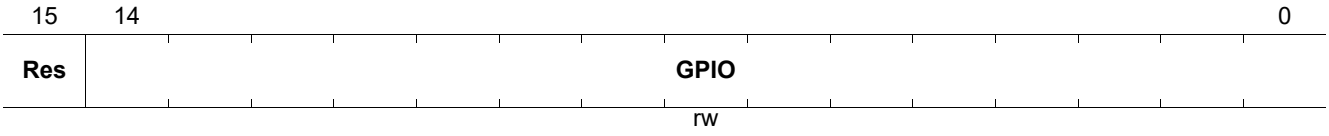


Field	Bits	Type	Description
GPIO	13:0	rw	**GPIO Pull Up/Down Enable** 0_B **Disable** Internal weak pull up/down is disabled. 1_B **Enable** Internal weak pull up/down is enabled.

GPIO2 Data Output Register

When a pin is used as general purpose output (GPIO), output data is written into register GPIO_OUT.

GPIO2_OUT	Offset	Reset Value
GPIO2 Data Output Register	$F390_H$	0000_H

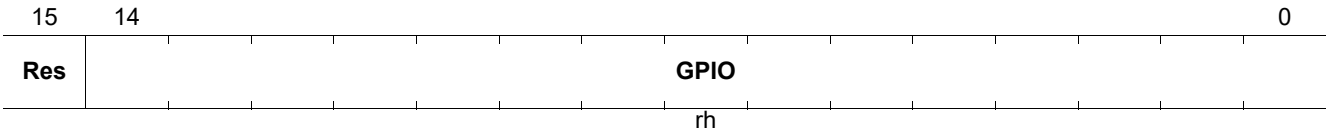


Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Output Value** 0_B **LOW** Output value = 0 *Note: Default value after reset* 1_B **HIGH** Output value = 1

GPIO2 Data Input Register

The value at a pin can be read through the read-only register GPIO_IN. The data input register GPIO_IN always contains a latched value of the assigned pin.

GPIO2_IN	Offset	Reset Value
GPIO2 Data Input Register	$F391_H$	0000_H



Field	Bits	Type	Description
GPIO	14:0	rh	**GPIO Input Value** 0_B **LOW** Input value = 0 1_B **HIGH** Output value = 1

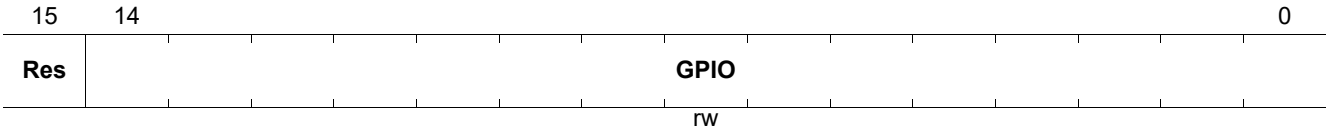
GPIO2 Direction Register

The direction of port pins can be controlled in the following ways:

- Controlled by Px_DIR register when used for GPIO and controlled by the peripheral when used for alternate function
- Controlled by Px_DIR register when used as GPIO and fixed direction when used for alternate function

When the port direction is controlled by the respective direction register Px_DIR, the following encoding is defined.

GPIO2_DIR	Offset	Reset Value
GPIO2 Direction Register	$F392_H$	0000_H



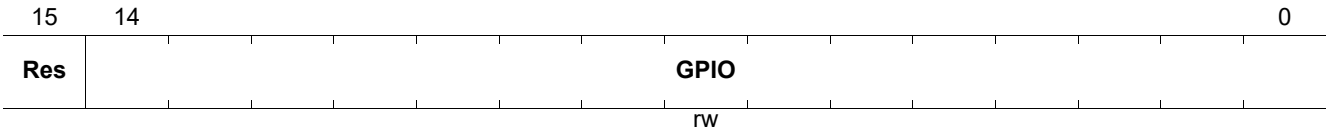
Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Direction Control** 0_B **Input** GPIO is in input mode *Note: Default value after reset* 1_B **Output** GPIO is in output mode

GPIO2 Alternate Function Select Register 0

Alternate functions are selected via an output multiplexer which can select up to four output lines. This multiplexer can be controlled by the signals of Register **GPIO2_ALTSEL0** and 1.

Selection of alternate functions are defined in registers **GPIO2_ALTSEL0** and 1.

GPIO2_ALTSEL0	Offset	Reset Value
Port 2 Alternate Function Select Register 0	$F393_H$	0000_H



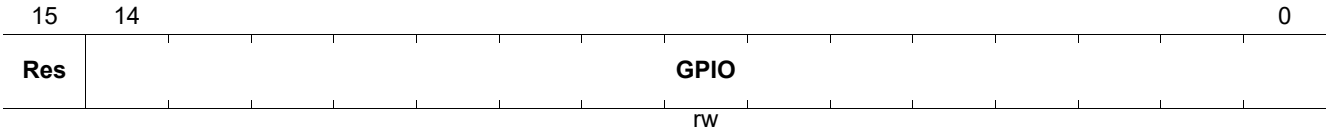
Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Alternate Function Selection LSB** GPIO Alternate Function Selection LSB

GPIO2 Alternate Function Select Register 1

Alternate functions are selected via an output multiplexer which can select up to four output lines. This multiplexer can be controlled by the signals of Register **GPIO2_ALTSEL0** and 1.

Selection of alternate functions are defined in registers **GPIO2_ALTSEL0** and 1.

GPIO2_ALTSEL1	Offset	Reset Value
Port 2 Alternate Function Select Register 1	**$F394_H$**	**0000_H**

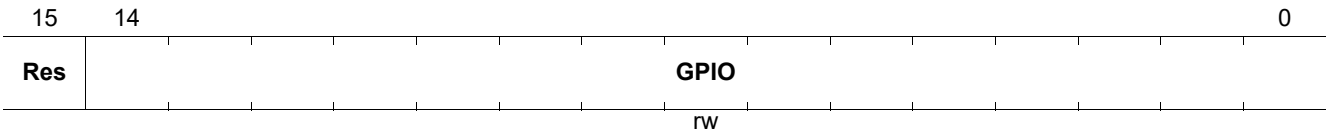


Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Alternate Function Selection MSB** GPIO Alternate Function Selection MSB

GPIO2 Open Drain Control Register

Each pin in output mode can be switched to Open Drain Mode. When driven with 1, no driver is activated; when driven with 0, the pull-down transistor is activated.

GPIO2_OD	Offset	Reset Value
GPIO2 Open Drain Control Register	**$F395_H$**	**$7FFF_H$**



Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Open Drain Mode** 0_B **OD** Open Drain Mode, output is actively driven only for 0 state. 1_B **PP** Normal Mode, output is actively driven for 0 and 1 state.

Port 2 Pull-Up/Pull-Down Select Register

Internal pull-up/pull-down devices can be optionally applied to pin. This offers the possibility to configure the following input characteristics:

- Tristate
- High-impedance with a weak pull-up device
- High-impedance with a weak pull-down device

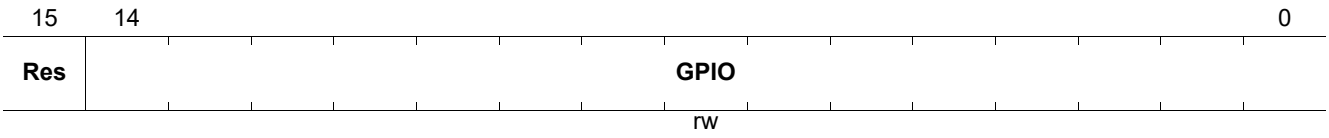
And the following output characteristics:

- Push/pull (optional pull-up/pull-down)
- Open drain with internal pull-up
- Open drain with external pull-up

The pull-up/pull-down device can be fixed or controlled via the registers **GPIO2_PUDEN**. Register **GPIO2_PUDSEL** selects the type of pull-up/pull-down device, while register **GPIO2_PUDEN** enables or disables it. The pull-up/pull-down device can be selected pin-wise. The pull-up/pull-down devices are predefined for some pins after reset.

Note: The selected pull-up/pull-down device is enabled by setting the respective bit in the Px_PUDEN register.

GPIO2_PUDSEL	Offset	Reset Value
GPIO2 Pull-Up/Pull-Down Select Register	**$F396_H$**	**$7FFF_H$**

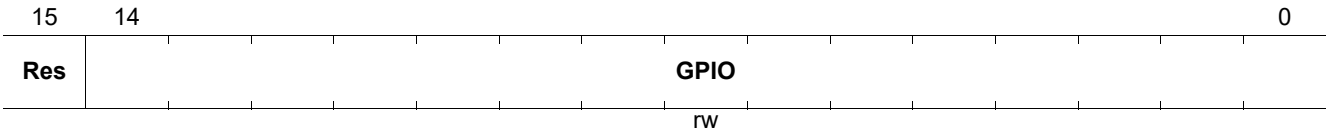


Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Pull Up/Down Mode** 0_B **PD** Internal weak pull down is enabled. 1_B **PU** Internal weak pull up is enabled.

GPIO2 Pull-Up/Pull-Down Enable Register

See the previous register description.

GPIO2_PUDEN	Offset	Reset Value
GPIO2 Pull-Up/Pull-Down Enable Register	**$F397_H$**	**$7FFF_H$**



Field	Bits	Type	Description
GPIO	14:0	rw	**GPIO Pull Up/Down Enable** 0_B **Disable** Internal weak pull up/down is disabled. 1_B **Enable** Internal weak pull up/down is enabled.

4.1.11 ICU Registers

IM0 Interrupt Status Register

Writing a 1 to a bit in the interrupt status register causes this bit to be cleared. Writing 0 to a bit does not change the value of the interrupt request flag. A read action to this register delivers the unmasked captured status of the interrupt request lines.

IM0_ISR	Offset	Reset Value
IM0 Interrupt Status Register	$F3C0_H$	0000_H

15	14	13	12	11	10	9	8
Res				IR11	IR10	Res	
				lhsc	lhsc		

7	6	5	4	3	2	1	0
IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
lhsc	lhsc	lhsc	lhsc	lhsc	lhsc	lhsc	lhsc

Field	Bits	Type	Description
IR11	11	lhsc	**Status of Interrupt Request SGMII** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR10	10	lhsc	**Status of Interrupt Request Packet Extraction** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR7	7	lhsc	**Status of Interrupt Request MGE** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR6	6	lhsc	**Status of Interrupt Request xMII** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR5	5	lhsc	**Status of Interrupt Request GSWIP** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR4	4	lhsc	**Status of Interrupt Request PHY4** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR3	3	lhsc	**Status of Interrupt Request PHY3** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR2	2	lhsc	**Status of Interrupt Request PHY2** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.

Field	Bits	Type	Description
IR1	1	lhsc	**Status of Interrupt Request PHY1** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.
IR0	0	lhsc	**Status of Interrupt Request PHY0** 0_B **Inactive** There is no pending interrupt. 1_B **Active** There is pending interrupt request.

IM0 EINT0 Interrupt Enable Register

Writing 1 to a bit enables the interrupt request line, while writing 0 to a bit disables the associated interrupt request line.

IM0_EINT0_IER	Offset	Reset Value
IM0 EINT0 Interrupt Enable Register	$F3C2_H$	0000_H

15	14	13	12	11	10	9	8
Res				IR11	IR10	Res	
				rw	rw		

7	6	5	4	3	2	1	0
IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
IR11	11	rw	**Interrupt Enable SGMII** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR10	10	rw	**Interrupt Enable Packet Extraction** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR7	7	rw	**Interrupt Enable MGE** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR6	6	rw	**Interrupt Enable xMII** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR5	5	rw	**Interrupt Enable GSWIP** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR4	4	rw	**Interrupt Enable PHY4** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR3	3	rw	**Interrupt Enable PHY3** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.

Field	Bits	Type	Description
IR2	2	rw	**Interrupt Enable PHY2** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR1	1	rw	**Interrupt Enable PHY1** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR0	0	rw	**Interrupt Enable PHY0** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.

IM0 EINT1 Interrupt Enable Register

Writing 1 to a bit enables the interrupt request line, while writing 0 to a bit disables the associated interrupt request line.

IM0_EINT1_IER	Offset	Reset Value
IM0 EINT1 Interrupt Enable Register	$F3C3_H$	0000_H

15	14	13	12	11	10	9	8
Res				IR11	IR10	Res	
				rw	rw		

7	6	5	4	3	2	1	0
IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
rw	rw	rw	rw	rw	rw	rw	rw

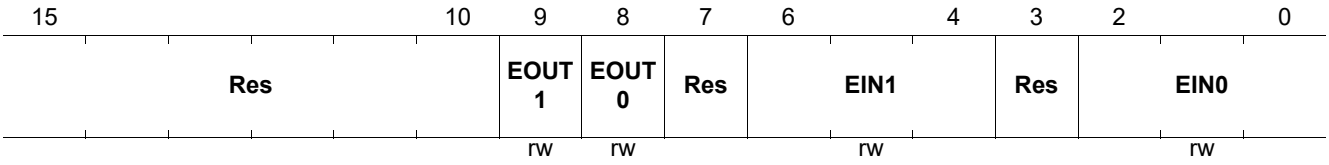
Field	Bits	Type	Description
IR11	11	rw	**Interrupt Enable SGMII** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR10	10	rw	**Interrupt Enable Packet Extraction** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR7	7	rw	**Interrupt Enable MGE** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR6	6	rw	**Interrupt Enable xMII** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR5	5	rw	**Interrupt Enable GSWIP** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR4	4	rw	**Interrupt Enable PHY4** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.

Field	Bits	Type	Description
IR3	3	rw	**Interrupt Enable PHY3** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR2	2	rw	**Interrupt Enable PHY2** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR1	1	rw	**Interrupt Enable PHY1** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.
IR0	0	rw	**Interrupt Enable PHY0** 0_B **Disable** Interrupt request is disabled. 1_B **Active** Interrupt request is enabled.

External Interrupt Control Register

The edge and level detection mechanism of all external interrupt inputs are controlled by register. The polarity of external interrupt outputs are also controlled by register

EIU_EXIN_CONF	Offset	Reset Value
EIU External Interrupt Controller Register	$F3C4_H$	0000_H



Field	Bits	Type	Description
EOUT1	9	rw	**External Interrupt Output EINT1** Configures the external interrupt pin 1 output characteristics. 0_B **High Level** High Active 1_B **Low Level** Low Active
EOUT0	8	rw	**External Interrupt Output EINT0** Configures the external interrupt pin 0 output characteristics. 0_B **High Level** High Active 1_B **Low Level** Low Active

Field	Bits	Type	Description
EIN1	6:4	rw	**External Interrupt Input EINT1** Configures the external interrupt pin 1 input characteristics. 000_B **Edge/Level** Edge and level detection as well as interrupt request generation is disabled 001_B **Rising Edge** Interrupt on rising (positive) edges 010_B **Falling Edge** Interrupt on falling (negative) edges 011_B **Rising/Falling Edge** Both edges, rising and falling edges 100_B **Edge/Level disable** Edge and level detection as well as interrupt request generation is disabled 101_B **High Level** Level detection of high levels 110_B **Low Level** Level detection of low-levels 111_B **Res** reserved
EIN0	2:0	rw	**External Interrupt Input EINT0** Configures the external interrupt pin 0 input characteristics. 000_B **Edge/Level** Edge and level detection as well as interrupt request generation is disabled 001_B **Rising Edge** Interrupt on rising (positive) edges 010_B **Falling Edge** Interrupt on falling (negative) edges 011_B **Rising/Falling Edge** Both edges, rising and falling edges 100_B **Edge/Level disable** Edge and level detection as well as interrupt request generation is disabled 101_B **High Level** Level detection of high levels 110_B **Low Level** Level detection of low-levels 111_B **Res** reserved

4.1.12 LED Registers

This section describes all registers in LED module.

LED Single Color Mode Register

This register configures the LED ground mode or power mode.

LED_MD_CFG	Offset	Reset Value
LED Single Color LED Mode Register	$F3E0_H$	0000_H

15	14	13	12	11	10	9	8
Res	**LED14**	**LED13**	**LED12**	**LED11**	**LED10**	**LED9**	**LED8**
	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
LED7	**LED6**	**LED5**	**LED4**	**LED3**	**LED2**	**LED1**	**LED0**
rw	rw	rw	rw	rw	rw	rw	rw

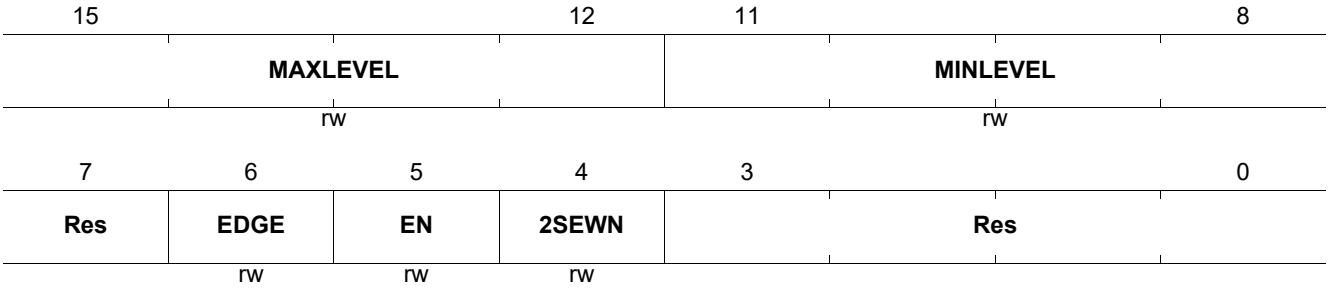
Field	Bits	Type	Description
LED14	14	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED13	13	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED12	12	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED11	11	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED10	10	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED9	9	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED8	8	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED7	7	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode

Field	Bits	Type	Description
LED6	6	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED5	5	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED4	4	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED3	3	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED2	2	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED1	1	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode
LED0	0	rw	**LED Single Color Mode** 0_B **Ground** LED Single Color Ground Mode 1_B **Power** LED Single Color Power Mode

LED Brightness Control Register

This register configures the LED brightness control.

LED_BRT_CTRL	Offset	Reset Value
LED Brightness Control Register	$F3E1_H$	$F430_H$

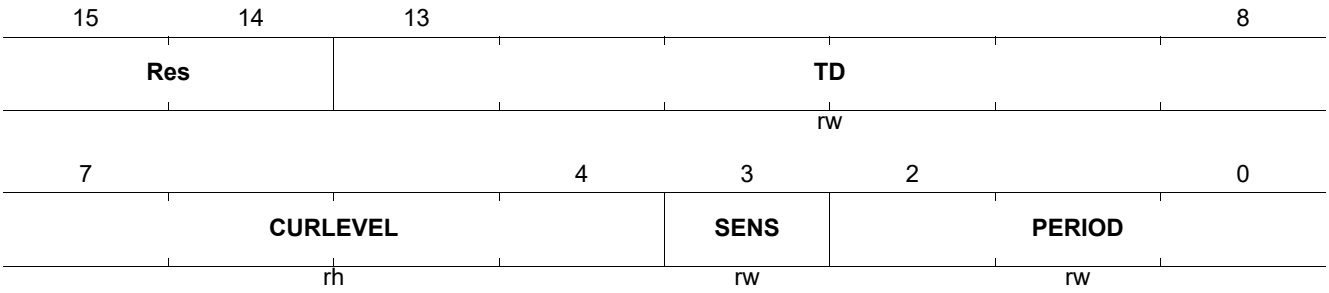


Field	Bits	Type	Description
MAXLEVEL	15:12	rw	**Maximum LED Brightness Value**
MINLEVEL	11:8	rw	**Minimum LED Brightness Value**
EDGE	6	rw	**LED Brightness Switch Edge Detection** 0_B **Falling** Falling Edge 1_B **Rising** Rising Edge
EN	5	rw	**LED Brightness Control Enable** 0_B **Disable** LED brightness control is disabled 1_B **Enable** LED brightness control is enabled
2SEWN	4	rw	**LED Brightness 2 Level Switch Enable** 0_B **Disable** LED brightness control via an external switch is disabled 1_B **Enable** LED brightness control via an external switch is enabled

LED Light Sensing Control Register

This register configures the LED light sensing.

LED_LSENS_CTRL	Offset	Reset Value
LED Light Sensing Control Register	$F3E2_H$	$0D09_H$



Field	Bits	Type	Description
TD	13:8	rw	**The Number of Slots for Discharge**
CURLEVEL	7:4	rh	**Current Brightness Level**
SENS	3	rw	**LED Sensing Enable** 0_B **Disable** LED sensing is disabled 1_B **Enable** LED sensing is enabled
PERIOD	2:0	rw	**LED Sensing Period** 000_B **1000** 1000 ms 001_B **500** 500 ms 010_B **333** 333 ms 011_B **250** 250 ms 100_B **200** 200 ms 101_B **167** 167 ms 110_B **142** 142 ms 111_B **125** 125 ms

4.2 SGMII_Registers

This section defines all the registers required to operate the SGMII module.

Table 56 Registers Address Space

Module	Base Address	End Address	Note
SGMII_TBI	300_H	$3FF_H$	
SGMII_PCS	400_H	$4FF_H$	
SGMII_PHY	000_H	$1FF_H$	
SGMII_MACRO	200_H	$2FF_H$	

Table 57 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
SGMII_Registers, SGMII_TBI: TBI Submodule Register File			
SGMII_TBI_TXANEGH	SGMII Transmit Auto-Negotiation High Byte	$D300_H$	232
SGMII_TBI_TXANEGL	SGMII Transmit Auto-Negotiation Low Byte	$D301_H$	233
SGMII_TBI_RXANEGH	SGMII Receive Auto-Negotiation High Byte(15:8)	$D302_H$	234
SGMII_TBI_RXANEGL	SGMII Receive Auto-Negotiation Low Byte(7:0)	$D303_H$	235
SGMII_TBI_ANEGCTL	SGMII Auto-Negotiation Control Bits	$D304_H$	236
SGMII_TBI_TBICTL	SGMII TBI Control Bits	$D305_H$	238
SGMII_TBI_TBICTLT	SGMII TBI Control Bits TX	$D306_H$	240
SGMII_TBI_TBITEST	SGMII TBI Test Control Bits	$D307_H$	241
SGMII_TBI_RXERR	SGMII RX Error Counter	$D308_H$	242
SGMII_TBI_TBISTAT	SGMII TBI Status	$D309_H$	243
SGMII_TBI_LPSTAT	SGMII Link Partner Status	$D30A_H$	244
SGMII_TBI_ISTAT	SGMII Interrupt Status	$D30B_H$	245
SGMII_TBI_IMASK	SGMII Interrupt Mask	$D30C_H$	246
SGMII_TBI_TX_FSM_STAT	SGMII Transmitter State	$D30D_H$	247
SGMII_TBI_RX_FSM_STAT	SGMII Receiver State	$D30E_H$	248
SGMII_Registers, SGMII_PCS: SGMII PCS Register File			
SGMII_PCS_CFG	SGMII PCS Configuration	$D400_H$	249
SGMII_PCS_RXB_CTL	SGMII Receive Buffer Control	$D401_H$	250
SGMII_PCS_RXB_CFG	SGMII Receive Buffer Configuration	$D402_H$	251
SGMII_PCS_RXB_STAT	SGMII PCS Receive Buffer Status	$D403_H$	252
SGMII_PCS_TXB_CTL	SGMII PCS Transmit Buffer Control	$D404_H$	253
SGMII_PCS_TXB_CFG	SGMII PCS Transmit Buffer Configuration	$D405_H$	254
SGMII_PCS_TXB_STAT	SGMII PCS Transmit Buffer Status	$D406_H$	255
SGMII_Registers, SGMII_PHY: SGMII_PHY Registers			

Table 57 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
SGMII_PHY_RESETN	SGMII PHY Reset	$D000_H$	256
SGMII_PHY_MPLL_CFG1	SGMII PHY MPLL CFG1	$D001_H$	257
SGMII_PHY_MPLL_CFG2	SGMII PHY MPLL CFG2	$D002_H$	258
SGMII_PHY_RX0_CFG1	SGMII PHY RX0 CFG1	$D003_H$	259
SGMII_PHY_RX0_CFG2	SGMII PHY RX0 CFG2	$D004_H$	260
SGMII_PHY_TX0_CFG1	SGMII PHY TX0 CFG1	$D005_H$	261
SGMII_PHY_TX0_CFG2	SGMII PHY TX0 CFG2	$D006_H$	262
SGMII_PHY_TX0_CFG3	SGMII PHY TX0 CFG3	$D007_H$	263
SGMII_PHY_MISC	SGMII PHY MISC	$D008_H$	264
SGMII_PHY_HWBU_CTRL	SGMII PHY HWBU CTRL	$D009_H$	265
SGMII_PHY_STATUS	SGMII PHY STATUS	$D00A_H$	266
SGMII_PHY_D	SGMII PHY D	$D100_H$	267
SGMII_PHY_A	SGMII PHY A	$D101_H$	268
SGMII_PHY_C	SGMII PHY C	$D102_H$	269
SGMII_PHY_WATCHDOG_CTRL	SGMII PHY WATCHDOG CONTROL	$D111_H$	270
SGMII_PHY_WATCHDOG_TIMER	SGMII PHY WATCHDOG TIMER	$D112_H$	270
SGMII_Registers, SGMII_MACRO_REGISTERS: SGMII_MACRO Registers			
SGMII_MACRO_SGMII_CTRL1	SGMII Macro SGMII CTRL1	$D201_H$	272
SGMII_MACRO_CLK_CTRL	SGMII Macro Clock Control	$D20F_H$	273
SGMII_MACRO_RESETN	SGMII Macro Reset Control	$D200_H$	271

The register is addressed wordwise.

Table 58 Register Access Types

Mode	Symbol
Interrupt status register, latching high, cleared by writing a ONE	lhsc
Hardware status, read-only	rh
Read/write register with input from and output to hardware	rwh
Standard read/write register with output to hardware	rw

4.2.1 SGMII_TBI: TBI Submodule Register File

This section defines all the registers required to operate the SGMII_TBI module.[1)]

SGMII Transmit Auto-Negotiation High Byte

This register holds the part of the control word transmitted during ANEG.

SGMII_TBI_TXANEGH	Offset	Reset Value
SGMII Transmit Auto-Negotiation High Byte	$D300_H$	0000_H

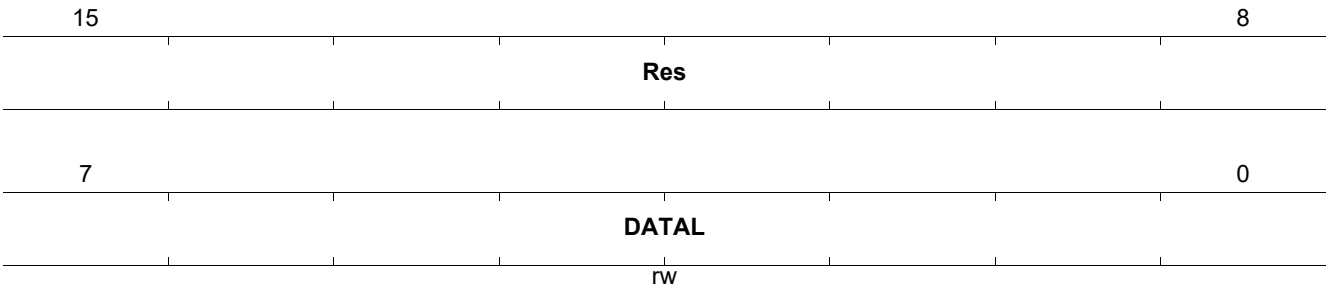
Field	Bits	Type	Description
NP	7	rw	**Next Page** The NP bit is set up the external Next Page function to indicate whether or not this is the last page to be transmitted 0_B **LAST** Last Page 1_B **NEXT** Additional next page to follow
DATAH	5:0	rw	**Higher Data or Control Bits for Auto-Negotiation** This is the upper byte of the transmitted control word during ANEG

1) Generated by REFIGE v1.4 - Beta Release XIV

SGMII Transmit Auto-Negotiation Low Byte

This register holds part of the control word transmitted during ANEG.

SGMII_TBI_TXANEGL	Offset	Reset Value
SGMII Transmit Auto-Negotiation Low Byte	$D301_H$	0000_H



Field	Bits	Type	Description
DATAL	7:0	rw	**Lower Data or Control Bits for Auto-Negotiation** The SGMII_TBI_TXANEGL must be written after SGMII_TBI_TXANEGH. Writing to SGMII_TBI_TXANEGH register updates the tx_config_reg(15:0) (described in cl 36 of the standard). When Next Page function is supported, the controller must write to NP bit in SGMII_TBI_TXANEGH to go to NEXT_PAGE_WAIT state in ANEG FSM after ANEG Interrupt.

SGMII Receive Auto-Negotiation High Byte(15:8)

This register holds part of the control word received during ANEG.

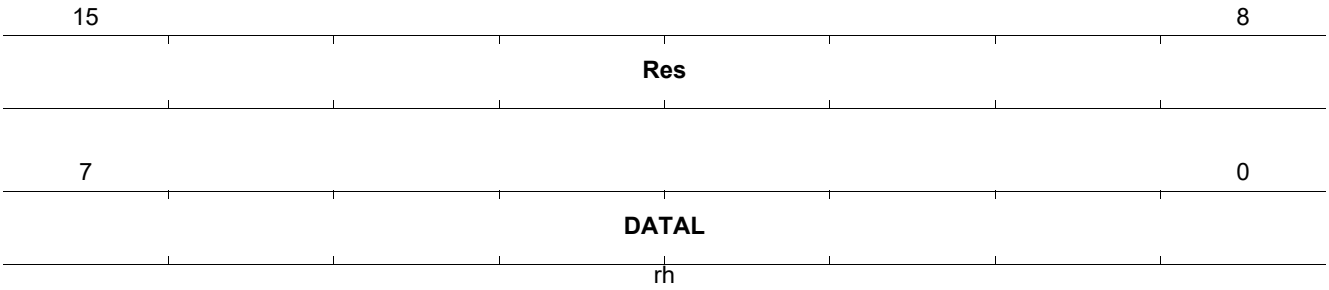
SGMII_TBI_RXANEGH	Offset	Reset Value
SGMII Receive Auto-Negotiation High Byte(15:8)	$D302_H$	0000_H

Field	Bits	Type	Description
NP	7	rh	**Next Page** The NP bit is used by the Next Page function to indicate whether or not this is the last page 0_B **LAST** Last Page 1_B **NEXT** Additional next page to follow
ACK	6	rh	**Acknowledge** 0_B **NAK** No Acknowledge received 1_B **ACK** Acknowledge received
DATAH	5:0	rh	**Higher Data or Control Bits for Auto-Negotiation** This is the upper byte of the received control word during ANEG

SGMII Receive Auto-Negotiation Low Byte(7:0)

This register holds part of the control word received during ANEG.

SGMII_TBI_RXANEGL	Offset	Reset Value
SGMII Receive Auto-Negotiation Low Byte(7:0)	$D303_H$	0000_H

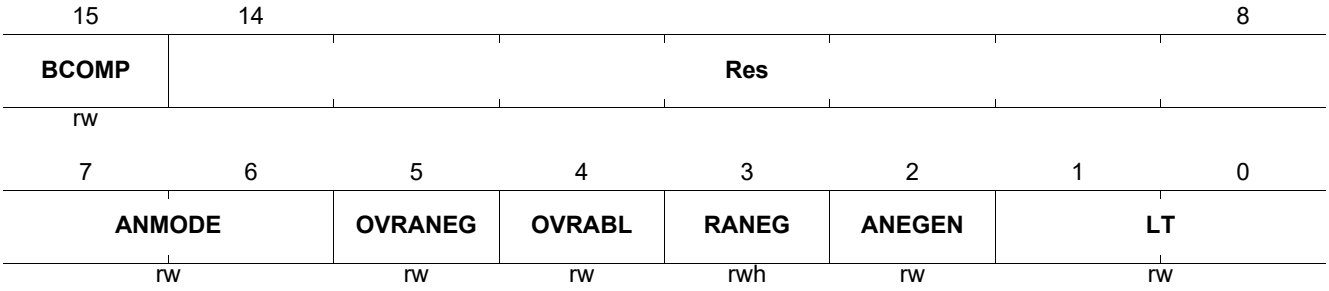


Field	Bits	Type	Description
DATAL	7:0	rh	**Lower Data or Control Bits for Auto-Negotiation** This is the lower byte of the received control word during ANEG

SGMII Auto-Negotiation Control Bits

This register holds the bits that control the ANEG process.

SGMII_TBI_ANEGCTL	Offset	Reset Value
SGMII Auto-Negotiation Control Bits	$D304_H$	$00B2_H$



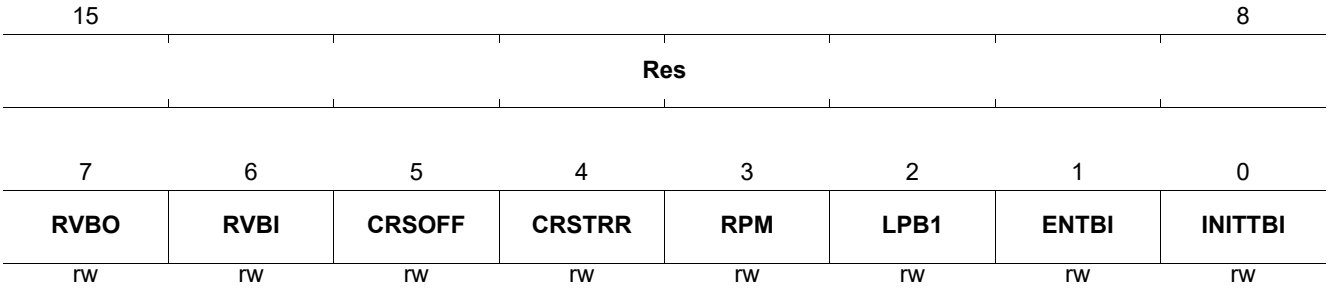
Field	Bits	Type	Description
BCOMP	15	rw	**Backwards Compatibility Control** ANEG FSM switches from COMPLETE_ACKNOWLEDGE to NEXT_PAGE_WAIT only when LP's NP ability is activated (among other conditions). Retains earlier ANEG FSM operating mode, where LP's NP ability is not considered in changing state COMPLETE_ACKNOWLEDGE to NEXT_PAGE_WAIT state. 0_B **INCOMP** Backwards incompatible mode 1_B **COMP** Backwards compatible mode
ANMODE	7:6	rw	**ANEG Mode** 00_B **RESERVED** RESERVED 01_B **SGMII_1000BX** 1000BASE-X mode: ANEG done as defined by 1000BASE-X. 10_B **SGMII_PHY** SGMII PHY mode: ANEG done as defined by SGMII standard, as PHY. 11_B **SGMII_MAC** SGMII MAC mode: ANEG done as defined by SGMII standard, as MAC.
OVRANEG	5	rw	**Override Ability for ANEG Control** 0_B **HW_INT** Hardware mode: ANEG Mode, Enable ANEG and restart ANEG are taken from interface signals AN_MODE_I, AN_EN_I and AN_RS_I respectively 1_B **OVERRIDE** Register Mode: ANEG Mode, Enable ANEG and restart ANEG are taken from bits ANMODE, ANEGEN, RANEG of this register

Field	Bits	Type	Description
OVRABL	4	rw	**Override Ability for tx_config_reg** Ability values are taken from Hardware Interface SGMII (PHY mode only): AN_FD_I and AN_HD_I to form duplex mode bit; TR_DR_I to form speed bit 1000BASE-X: AN_FD_I and AN_HD_I to form FD and HD bits; AN_PS_I form PS1 and PS2 bits; AN_RF_I form RF1 and RF2 bits Note: Other tx_config_reg bits are set to '0' in this mode The tx_config_reg values are taken from Register TXANEGH and TXANEGL 0_B **HW_INT** Hardware mode: Ability Values are taken from Interface Signals 1_B **OVERRIDE** Register Mode: Override, Ability Values are taken from Registers
RANEG	3	rwh	**Restart Auto-Negotiation Process** Bit is cleared by hardware after FSM restarts. 0_B **NORMAL** Normal operation 1_B **RESTART** Restart auto-negotiation process
ANEGEN	2	rw	**Auto-Negotiation Enable** Enable auto-negotiation for TBI Interface. 0_B **DISABLE** Auto-negotiation is disabled 1_B **ENABLE** Auto-negotiation is enabled
LT	1:0	rw	**Link Timer Value** Link timer values for TBI ANEG FSM. Required value for standard TBI is 10 ms. Required value for SGMII is 1.6 ms (Reset value). 00_B **T_10US** Timer Delay is 10 µs (Simulation) 01_B **T_1_6MS** Timer Delay is 1.6 ms (SGMII) 10_B **T_5MS** Timer Delay is 5 ms 11_B **T_10MS** Timer Delay is 10 ms (TBI)

SGMII TBI Control Bits

This register holds the bits that control the TBI operations.

SGMII_TBI_TBICTL	Offset	Reset Value
SGMII TBI Control Bits	$D305_H$	0001_H



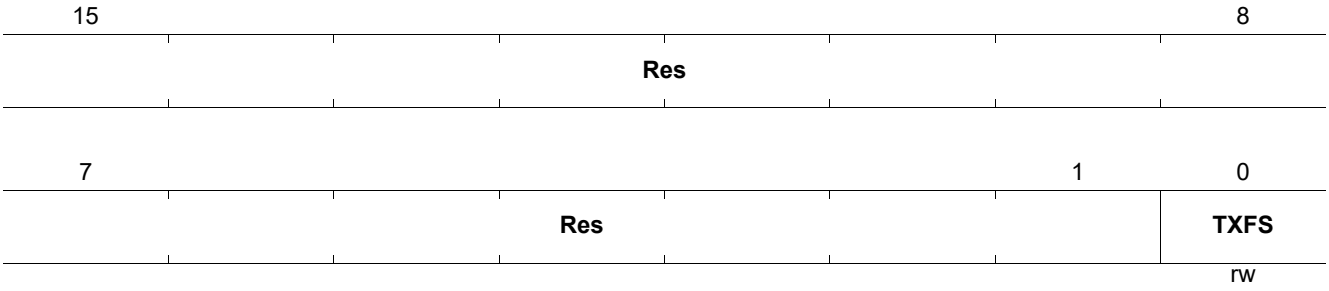
Field	Bits	Type	Description
RVBO	7	rw	**Reverse Bit Order Output** Output of 10 Bit encoder is (9:0) or (0:9) 0_B **NORMAL** 10 Bit Output according to Standard 1_B **REVERS** 10 Bit Output with reversed Bit Order
RVBI	6	rw	**Reverse Bit Order Input** Input for 10 Bit decoder is (9:0) or (0:9) 0_B **NORMAL** 10 Bit Input according to Standard 1_B **REVERS** 10 Bit Input with reversed Bit Order
CRSOFF	5	rw	**Carrier Sense Off** CRS output on GMII interface can be switched off especially for device which have trouble with that in Half Duplex mode . 0_B **ON** Carrier Sense is always generated in HD and FD 1_B **OFF** Carrier Sense is never generated, forced to 0
CRSTRR	4	rw	**Carrier Sense Extension for Sequence T/R/R/K28.5** Select Generation of Carrier Extension in Case of TBI Sequence /T/R/R/K28.5 according to Figure 36-7b of IEEE Std 802.3. 0_B **NO** No Generate Carrier Extension 1_B **YES** Generate Carrier Extension
RPM	3	rw	**Repeater Mode of TBI** Enable Repeater Operation for TBI Interface. Repeater Mode: CRS is only asserted in response to receive activity. Normal Operation: CRS is asserted in response to either transmit ore receive. 0_B **NORMAL** Normal operation 1_B **REPEATER** Repeater mode enabled

Field	Bits	Type	Description
LPB1	2	rw	**Loopback Mode of TBI** Enable Digital Loopback Operation. NOTE: For proper loopback operation, in addition to setting this bit, the digital loop in the PMA must be activated. For this, it is required to set the following bits in the PMA: en_txilpbk and rxlbi_en. See the SYNOPSYS* documentation for further information. 0_B **NORMAL** Normal operation 1_B **LOOPBACK** Loopback enabled
ENTBI	1	rw	**Enable of TBI Interface** Set to 1 for normal TBI operation, when set to DISABLE the RX and TX FSMs are frozen. 0_B **DISABLE** TBI Interface is disabled 1_B **ENABLE** TBI Interface is enabled
INITTBI	0	rw	**Reset of TBI FSM** Reset TBI Interface. 0_B **NORMAL** Normal operation 1_B **INIT** Initialization of TBI

SGMII TBI Control Bits TX

This register holds the bits that control the TBI operations.

SGMII_TBI_TBICTLT	Offset	Reset Value
SGMII TBI Control Bits TX	$D306_H$	0000_H

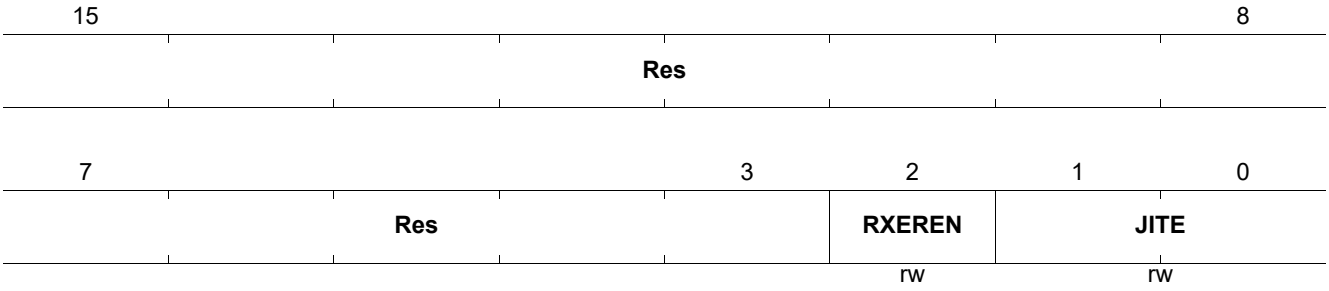


Field	Bits	Type	Description
TXFS	0	rw	**Transmit False Carrier Insertion** When enabled, defines a non-standard TX_FLASE_CARRIER state in PCS transmit ordered_set FSM in between XMIT_DATA and START_OF_PACKET states, which is entered in case TX_EN_I = '0' and TX_ER_I = '1'. See Figure 36-5 of IEEE Std 802.3. 0_B **NO** No False Carrier Insertion 1_B **YES** False Carrier Insertion

SGMII TBI Test Control Bits

This register holds the bits to enable some test features of the TBI.

SGMII_TBI_TBITEST	Offset	Reset Value
SGMII TBI Test Control Bits	$D307_H$	0000_H

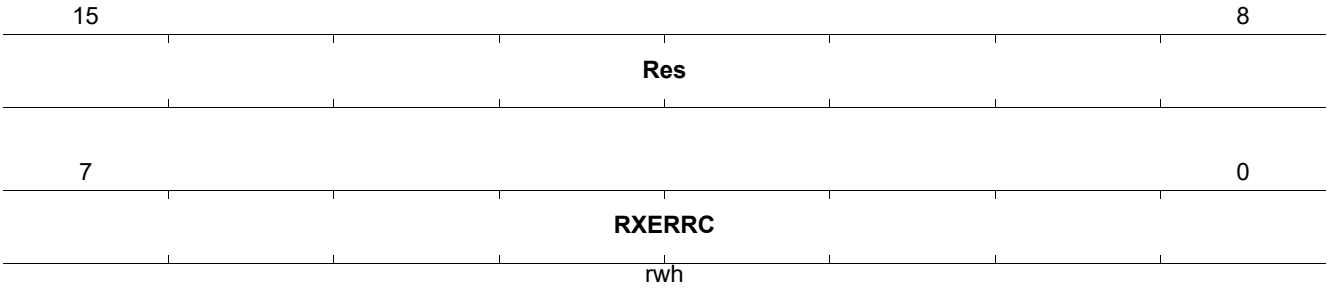


Field	Bits	Type	Description
RXEREN	2	rw	**Enable RX Error Counter** When enabled, the errors from 8b10b Decoder are counted 0_B **DSIABLE** RX Error Counter is disabled 1_B **ENABLE** RX Error Counter is enabled
JITE	1:0	rw	**Jitter Test pattern for Transmit** When set, the test pattern according to IEEE Std 802.3 chapter 36 A are transmitted. 00_B **NO** Normal Function 01_B **HIGH** Transmit High Frequency test pattern 36A.1 10_B **LOW** Transmit Low Frequency test pattern 36A.2 11_B **MIXED** Transmit Mixed Frequency test pattern 36A.3

SGMII RX Error Counter

This register holds the count of errors as seen by the 8b10b decoder.

SGMII_TBI_RXERR	Offset	Reset Value
SGMII RX Error Counter	$D308_H$	0000_H

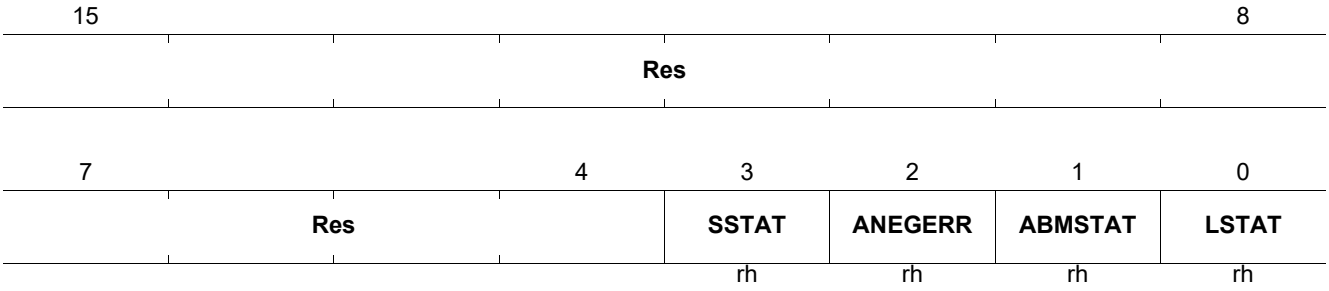


Field	Bits	Type	Description
RXERRC	7:0	rwh	**RX Error Counter** When enabled the receive errors detected by the 8b10b Decoder are counted. The register is cleared by read.

SGMII TBI Status

This register holds the status bits of the TBI FSMs.

SGMII_TBI_TBISTAT	Offset	Reset Value
SGMII TBI Status	$D309_H$	0000_H

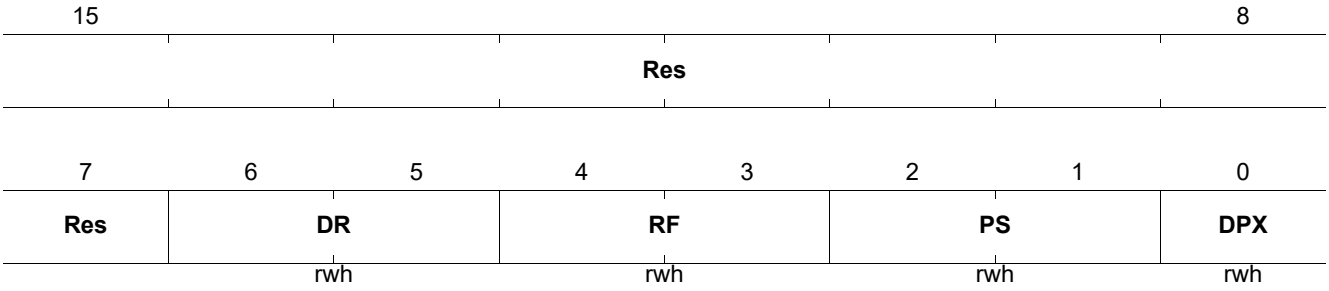


Field	Bits	Type	Description
SSTAT	3	rh	**Sync Status of the TBI Sync FSM** Status of the TBI Sync FSM as defined in figure 36-9 of 802.3 0_B **NOK** Sync Status of TBI is not OK 1_B **OK** Sync Status of TBI is OK
ANEGERR	2	rh	**Auto-Negotiation Error** Error Bit set when Abilities of local device and link partner do not match and cannot be resolved by the RESOLVE_PRIORIY function during auto-negotiation, when auto-negotiation is enabled. Not valid for SGMII mode. 0_B **NO_ERROR** No auto-negotiation error 1_B **ERROR** Auto-negotiation Error
ABMSTAT	1	rh	**Ability Match of TBI** Ability match status when auto-negotiation is enabled. 0_B **NOK** Auto-negotiation State Machine ability does not match 1_B **OK** Auto-negotiation State Machine ability match
LSTAT	0	rh	**Link Status of TBI** Indicates whether the ANEG FSM advanced to the LINK_OK status or not when auto-negotiation is enabled 0_B **NOK** Auto-negotiation State Machine is not in LINK_OK state 1_B **OK** Auto-negotiation State Machine is in LINK_OK state

SGMII Link Partner Status

This register carries information about the link partner obtained via ANEG.

SGMII_TBI_LPSTAT	Offset	Reset Value
SGMII Link Partner Status	$D30A_H$	0000_H

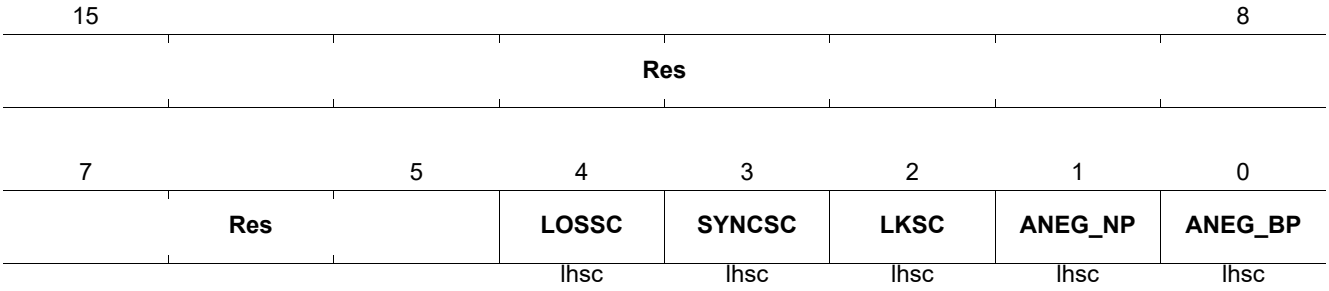


Field	Bits	Type	Description
DR	6:5	rwh	**SGMII Data Rate** SGMII Data Rate at link partner, set by HW when OVRABL is DISABLED and ANEG is enabled by HW or SW, only valid in SGMII Mode 00_B **DR10** Data Rate is 10 Mbps 01_B **DR100** Data Rate is 100 Mbps 10_B **DR1000** Data Rate is 1000 Mbps 11_B **INVALID** Not SGMII Mode
RF	4:3	rwh	**Remote Fault** Remote Fault Status at link partner, set by HW when OVRABL is DISABLED and ANEG is enabled by HW or SW 00_B **LINK_OK** No Error, link OK 01_B **LINK_FAIL** Link Failure, Link Down in SGMII Mode 10_B **OFFLINE** Offline, not used in SGMII Mode 11_B **ANEG_ERROR** Auto-negotiation error, not used in SGMII Mode
PS	2:1	rwh	**Pause Capability** Pause Status after auto-negotiation Priority Resolution at link partner, set by HW when OVRABL is DISABLED and ANEG is enabled by HW or SW 00_B **NO** No Pause 01_B **RECEIVE** Receive PAUSE 10_B **TRANSMIT** Transmit PAUSE 11_B **BOTH** Receive and Transmit PAUSE
DPX	0	rwh	**Duplex Status** Duplex Status after auto-negotiation Priority Resolution, set by HW when OVRABL is DISABLED and ANEG is enabled by HW or SW 0_B **HD** Half Duplex Mode 1_B **FD** Full Duplex Mode

SGMII Interrupt Status

This register carries information about the source of interrupt from the macro.

SGMII_TBI_ISTAT	Offset	Reset Value
SGMII Interrupt Status	$D30B_H$	0000_H

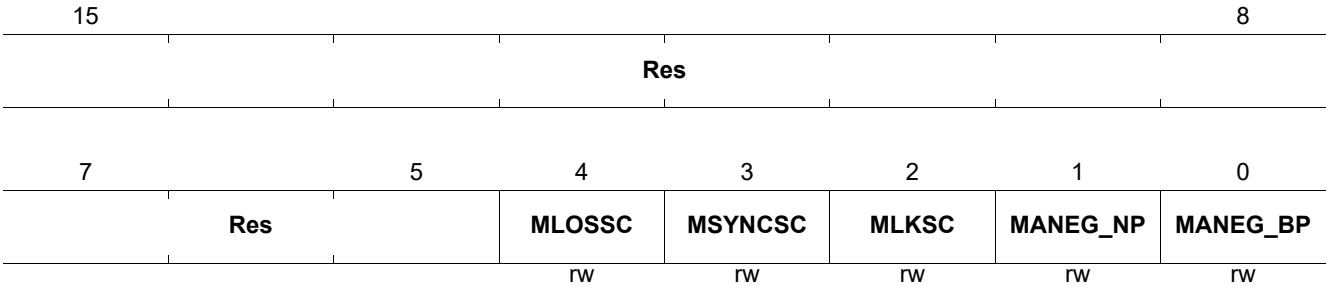


Field	Bits	Type	Description
LOSSC	4	lhsc	**Los Status Change** The current status of the los signal has changed. Interrupt cleared by writing a 1.
SYNCSC	3	lhsc	**Sync Status Change** The current status of the Synch state machine has changed. Interrupt cleared by writing a 1.
LKSC	2	lhsc	**Link Status Change** The current status of the link has changed either from OK to not OK or vice versa. Interrupt cleared by writing a 1.
ANEG_NP	1	lhsc	**Auto-Negotiation Interrupt Next Page** Interrupt generated from auto-negotiation when in COMPLETE_ACKNOWLEDGE state and a next page has been transferred. Firmware must write a fresh value to SGMII_TBI_TXANEGx with NP bit set before timer expires, when another next page operation is required i.e., for the ANEG FSM to move from COMPLETE_ACKNOWLEDGE to NEXT_PAGE_WAIT. Else the FSM moves to IDLE_DETECT state. Interrupt cleared by writing a '1'.
ANEG_BP	0	lhsc	**Auto-Negotiation Interrupt Base Page** Interrupt generated from auto-negotiation FSM when in COMPLETE_ACKNOWLEDGE state and the base page has been transferred; Firmware must write a fresh value to SGMII_TBI_TXANEGx with NP set before the timer expires, when next page operation is required i.e., for the ANEG FSM to move from COMPLETE_ACKNOWLEDGE to NEXT_PAGE_WAIT. Else the FSM moves to IDLE_DETECT state. Interrupt cleared by writing a '1'.

SGMII Interrupt Mask

This register carries mask bits for the interrupts described in SGMI_TBI_ISTAT.

SGMII_TBI_IMASK	Offset	Reset Value
SGMII Interrupt Mask	$D30C_H$	$001F_H$

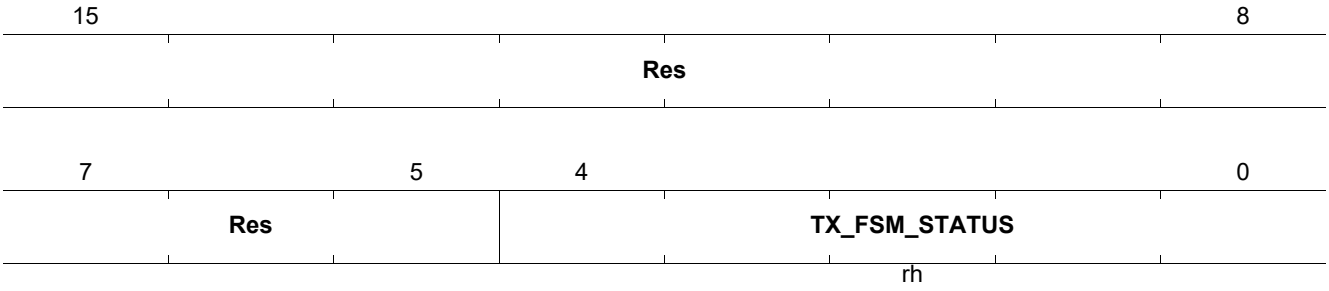


Field	Bits	Type	Description
MLOSSC	4	rw	**LOS Status Change** 0_B **UMASK** Unmask LOSSC Interrupt 1_B **MASK** Mask LOSSC Interrupt
MSYNCSC	3	rw	**Sync Status Change** 0_B **UMASK** Unmask SYNCSC Interrupt 1_B **MASK** Mask SYNCSC Interrupt
MLKSC	2	rw	**Link Status Change** 0_B **UMASK** Unmask LKSC Interrupt 1_B **MASK** Mask LKSC Interrupt
MANEG_NP	1	rw	**Mask Auto-Negotiation Next Page** 0_B **UMASK** Unmask auto-negotiation interrupt 1_B **MASK** Mask auto-negotiation interrupt
MANEG_BP	0	rw	**Mask Auto-Negotiation Base Page** 0_B **UMASK** Unmask auto-negotiation interrupt 1_B **MASK** Mask auto-negotiation interrupt

SGMII Transmitter State

This register indicates the status of the transmit FSM.

SGMII_TBI_TX_FSM_STAT	Offset	Reset Value
SGMII Transmitter State	$D30D_H$	0000_H

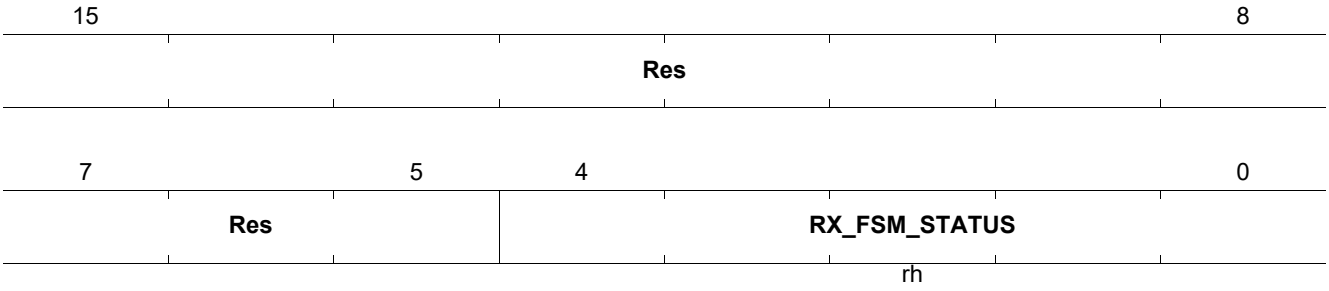


Field	Bits	Type	Description
TX_FSM_STATUS	4:0	rh	**State of Transmit FSM** 00000_B**RESET_TX** Reset txstate 00001_B**TX_TEST_TRANSMIT** Check xmit state 00010_B**CONFIGURATION_ST** Send config part 00011_B**IDLE_TX** Send idle 00100_B**XMIT_DATA** Send indication for tx data 00101_B**TX_START_OF_PACKET** Send sfd 00110_B**TX_DATA** Send data 00111_B**TX_END_OF_PACKET_NOEXT** Send epd 01000_B**END_OF_PACKET_EXT** Send end of packet at txeven is zero and err is zero 01001_B**EPD2_NOEXT** Align to txeven is zero 01010_B**EPD3** Send R when txeven is one 01011_B**EXTEND_BY_1** Send r for carrier ext 01100_B**CARRIER_EXTEND** Err is one then send sfd or send start of err 01101_B**ALIGN_ERR_START** Send error at txeven 01110_B**START_ERROR** Send start of error at one 01111_B**TX_DATA_ERROR** Send error data 10000_B**TX_FALSE_CARRIER** Send false carrier

SGMII Receiver State

This register indicates the status of the receive FSM.

SGMII_TBI_RX_FSM_STAT	Offset	Reset Value
SGMII Receiver State	$D30E_H$	0000_H



Field	Bits	Type	Description
RX_FSM_STATUS	4:0	rh	**State of Receive FSM** 00000_B**RESET** Reset state 00001_B**LINK_FAILED** Link failed 00010_B**WAIT_FOR_K** Wait for comma state 00011_B**RX_K** Received comma 00100_B**RX_CB** Received config bit 00101_B**RX_CC** Received config1 bit 00110_B**RX_CD** Received config2 bit 00111_B**RX_INVALID** Received data is invalid 01000_B**IDLE_D** Idle state 01001_B**FALSE_CARRIER** False carrier detection 01010_B**START_OF_PACKET** Start of packet detected 01011_B**EARLY_END** Early end of packet detected 01100_B**TRI_RRI** Packet termination received correctly 01101_B**TRR_EXTEND** Packet termination received correctly with carrier extend&check epd 01110_B**TRR_EXTEND_A** Packet termination received correctly with carrier extend 01111_B**PACKET_BURST_RRS** Receiving packet burst 10000_B**EXTEND_ERR** Carrier extend err 10001_B**RX_DATA_ERROR** Receiving wrong data 10010_B**RX_DATA** Receiving data

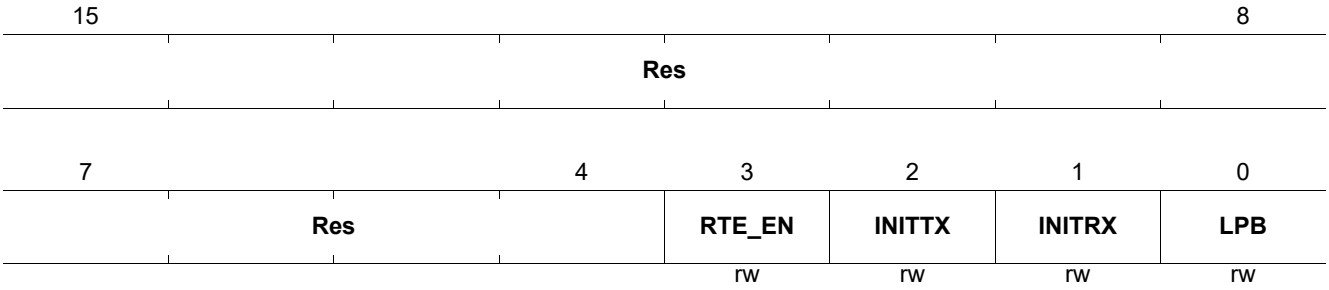
4.2.2 SGMII_PCS: SGMII PCS Register File

This section defines all the registers required to operate the SGMII_PCS module.

SGMII PCS Configuration

This register contains configuration bits for the PCS.

SGMII_PCS_CFG	Offset	Reset Value
SGMII PCS Configuration	$D400_H$	0000_H

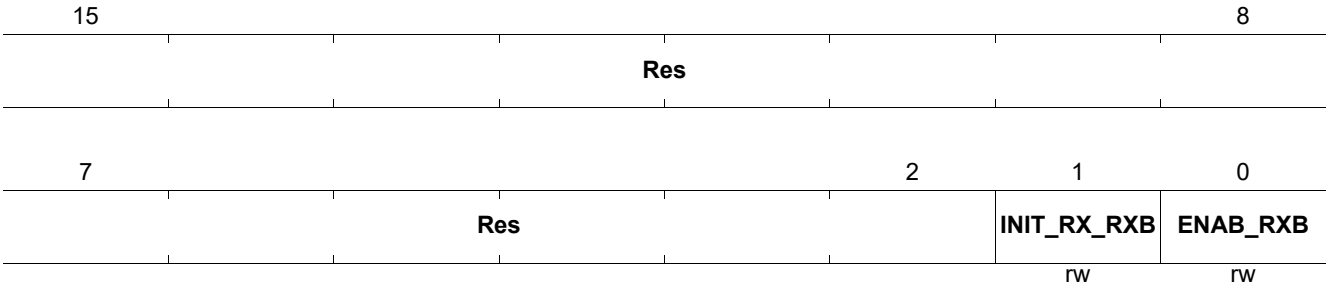


Field	Bits	Type	Description
RTE_EN	3	rw	**RTE Enable** Used to enable/disable real time Ethernet support. 0_B **DISABLE** Disable RTE 1_B **ENABLE** Enable RTE
INITTX	2	rw	**INIT SGMII TX Path** Used to reset all transmit operations. 0_B **NORMAL** Normal Operation TX 1_B **INIT** Reset TX Path
INITRX	1	rw	**INIT SGMII RX Path** Used to reset all receive operations. 0_B **NORMAL** Normal Operation TX 1_B **INIT** Reset RX Path
LPB	0	rw	**Loop Back RX to TX Path** Used to loop data from receive buffer to transmit buffer (PCS SGMII loop). 0_B **NORMAL** Normal Operation TX 1_B **LOOP** Loop back RX to TX Path

SGMII PCS Receive Buffer Control

Used to control the RX buffer operation.

SGMII_PCS_RXB_CTL	Offset	Reset Value
SGMII Receive Buffer Control	$D401_H$	0001_H

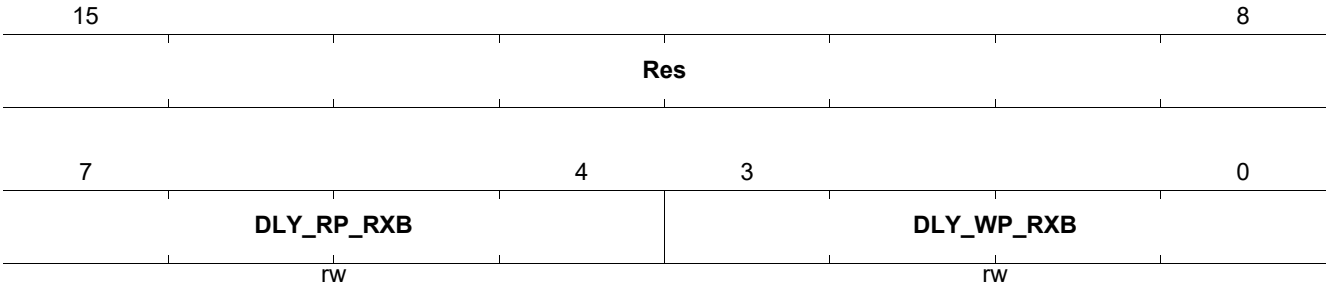


Field	Bits	Type	Description
INIT_RX_RXB	1	rw	**Initialize RX Buffer** Used to reset the RX buffer and associated pointers. 0_B **NORMAL** RX Buffer and pointers are normally operating 1_B **ACTIVE** RX Buffer and pointers are initialized
ENAB_RXB	0	rw	**Enable RX Buffer** When this control bit is disabled, the RX Buffer is disabled. The current transfer is NOT affected. This bit is used for the clock-gating. 0_B **DISABLE** RX Buffer is disabled 1_B **ENABLE** RX Buffer is enabled

SGMII PCS Receive Buffer Configuration

Used to configure the RX buffer operation.

SGMII_PCS_RXB_CFG	Offset	Reset Value
SGMII Receive Buffer Configuration	$D402_H$	0040_H

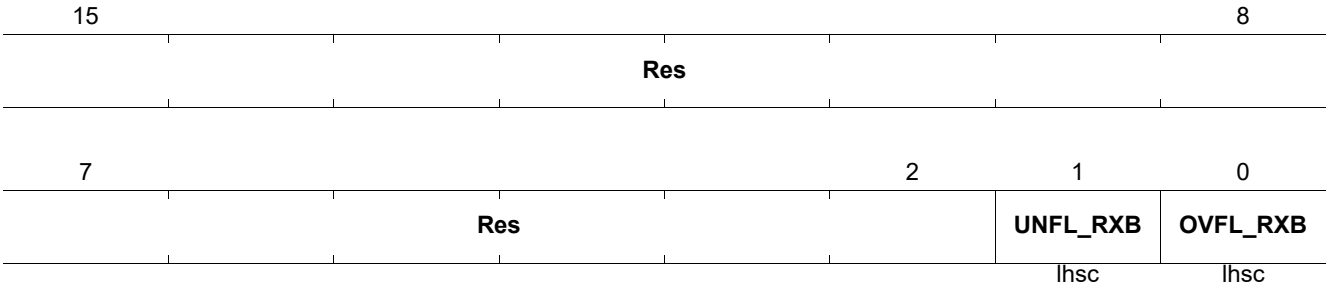


Field	Bits	Type	Description
DLY_RP_RXB	7:4	rw	**Synch Delay** This register is used to configure the value of write pointer at which the Read pointer is released from its reset value of 0. Actual time of first increment is set by internal synch delays.
DLY_WP_RXB	3:0	rw	**Initial Delay** This register is used to configure the initial delay of the write pointer in the RXB. This delay must be larger than zero to support negative frequency offsets. This delay must be smaller than max to support positive frequency offsets.

SGMII PCS Receive Buffer Status

Indicates the status of the RX buffer.

SGMII_PCS_RXB_STAT	Offset	Reset Value
SGMII PCS Receive Buffer Status	$D403_H$	0000_H

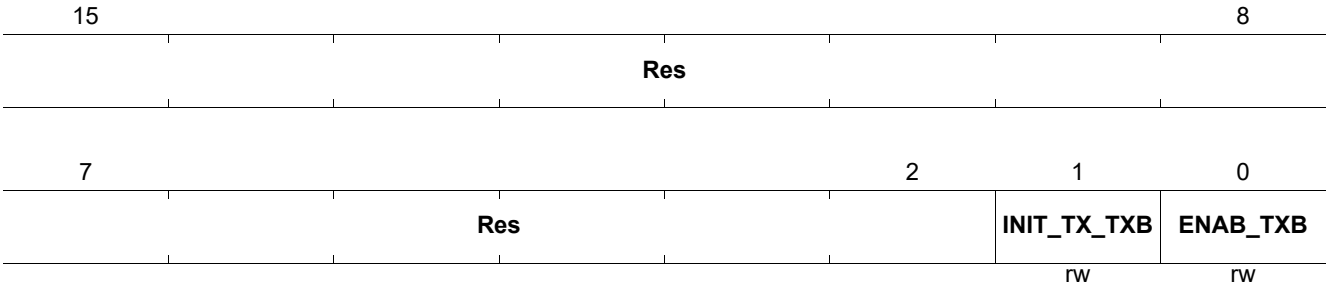


Field	Bits	Type	Description
UNFL_RXB	1	lhsc	**Underflow Indicator** 0_B **NONE** Underflow never detected 1_B **ONCE** Underflow occurred at least once
OVFL_RXB	0	lhsc	**Overflow Indicator** 0_B **NONE** Overflow never detected 1_B **ONCE** Overflow occurred at least once

SGMII PCS Transmit Buffer Control

Used to control the TX buffer operation

SGMII_PCS_TXB_CTL	Offset	Reset Value
SGMII PCS Transmit Buffer Control	$D404_H$	0001_H

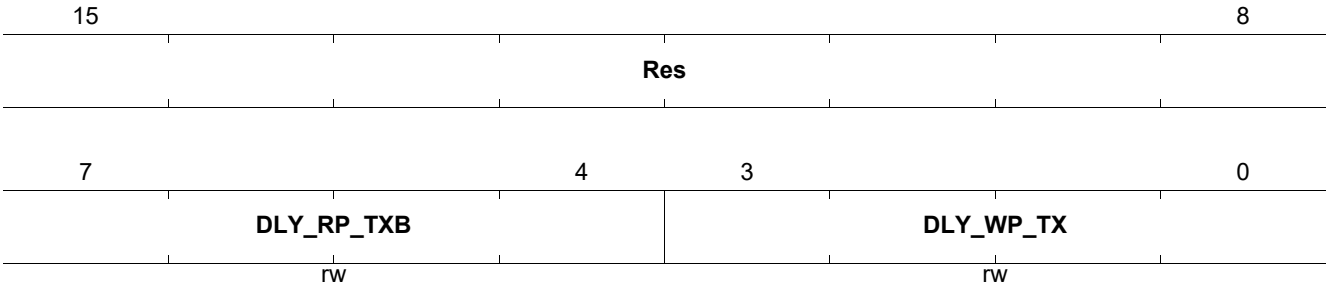


Field	Bits	Type	Description
INIT_TX_TXB	1	rw	**Initialize TX Buffer** Used to reset the TX buffer and associated pointers. 0_B **NORMAL** TXB is normally operating 1_B **ACTIVE** TXB is initialized
ENAB_TXB	0	rw	**Enable TX Buffer** When this control bit is disabled the TX Buffer is disabled. The current transfer is NOT affected. This bit is used for the clock-gating. 0_B **DISABLE** TX Buffer is disabled 1_B **ENABLE** TX Buffer is enabled

SGMII PCS Transmit Buffer Configuration

Used to configure the TX buffer operation.

SGMII_PCS_TXB_CFG	Offset	Reset Value
SGMII PCS Transmit Buffer Configuration	$D405_H$	0040_H

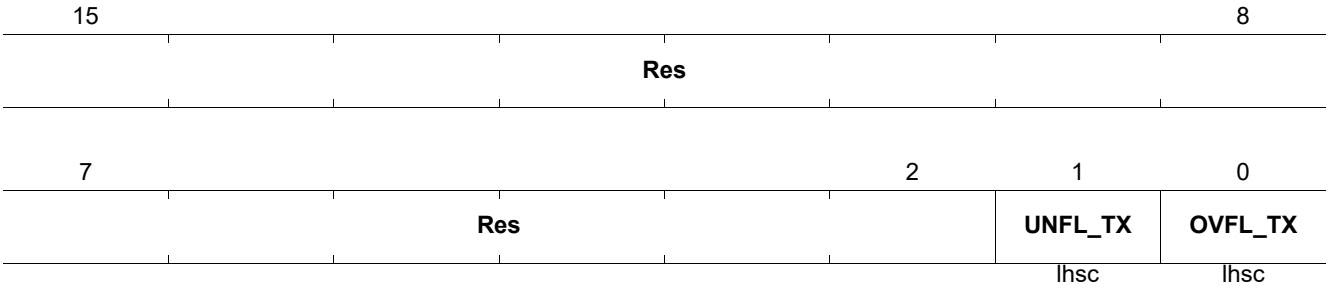


Field	Bits	Type	Description
DLY_RP_TXB	7:4	rw	**Synch Delay** This register is used to configure the value of write pointer at which the Read pointer is released from its reset value of 0. Actual time of first increment is set by internal synch delays
DLY_WP_TX	3:0	rw	**Initial Delay** This register is used to configure the initial delay of the WRITE POINTER in the TXB. This delay must be larger than zero to support negative frequency offsets. This delay must be smaller than max to support positive frequency offsets.

SGMII PCS Transmit Buffer Status

Indicates the status of the TX buffer.

SGMII_PCS_TXB_STAT	Offset	Reset Value
SGMII PCS Transmit Buffer Status	$D406_H$	0000_H



Field	Bits	Type	Description
UNFL_TX	1	lhsc	**Underflow Indicator** 0_B **NONE** Underflow never detected 1_B **ONCE** Underflow occurred at least once
OVFL_TX	0	lhsc	**Overflow Indicator** 0_B **NONE** Overflow never detected 1_B **ONCE** Overflow occurred at least once

4.2.3 SGMII_PHY: SGMII_PHY Registers

This section defines all the registers required to operate the SGMII_PHY module.

SGMII PHY Reset

Used to configure SGMII PHY Reset.

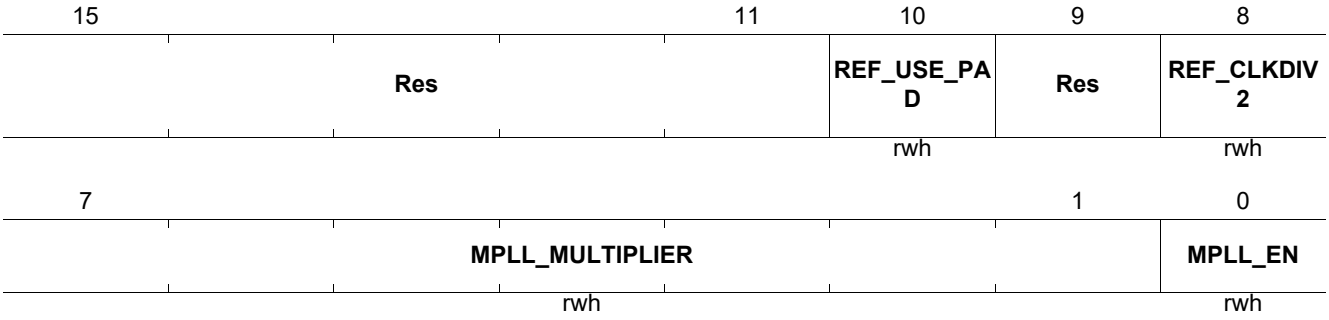
SGMII_PHY_RESETN	Offset	Reset Value
SGMII PHY Reset	$D000_H$	0001_H

Field	Bits	Type	Description
RESET_N	0	rwh	**RESET_N** Asynchronous active low reset. 0_B **RESET** Reset is triggered. 1_B **NOT_RESET** Reset is not triggered.

SGMII PHY MPLL CFG1

Used to configure SGMII PHY MPLL.

SGMII_PHY_MPLL_CFG1	Offset	Reset Value
SGMII PHY MPLL CFG1	$D001_H$	0000_H

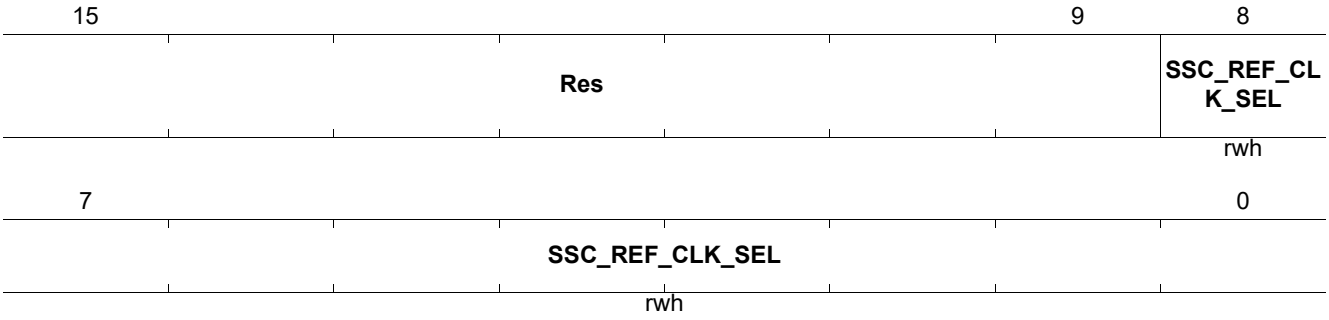


Field	Bits	Type	Description
REF_USE_PAD	10	rwh	**MPLL Input Clock Mode** 0_B **USE_ALT** On chip ALT clock is used as MPLL input clock. 1_B **USE_EXT_PAD** External reference pad clock is used as MPLL input clock.
REF_CLKDIV2	8	rwh	**Input Clock Frequency Division Enable** 0_B **DISABLE** Input reference clock frequency divide by 2 is disabled. 1_B **ENABLE** Input reference clock frequency divide by 2 is enabled.
MPLL_MULTIPLIER	7:1	rwh	**MPLL Frequency Multiplier** MPLL Frequency Multiplier Control
MPLL_EN	0	rwh	**MPLL Enable** 0_B **DISABLE** MPLL is disabled. 1_B **ENABLE** MPLL is enabled.

SGMII PHY MPLL CFG2

Used to configure SGMII PHY MPLL.

SGMII_PHY_MPLL_CFG2	Offset	Reset Value
SGMII PHY MPLL CFG2	$D002_H$	0000_H



Field	Bits	Type	Description
SSC_REF_CLK_SEL	8:0	rwh	**Spread Spectrum Reference Clock Config** Spread Spectrum Reference Clock shifting for non-integer input reference frequencies to MPLL.

SGMII PHY RX0 CFG1

Used to configure SGMII PHY Receiver.

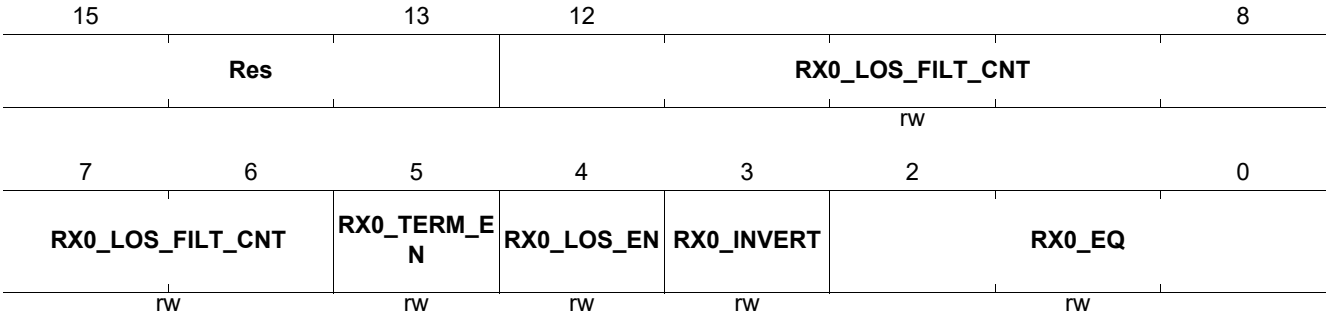
SGMII_PHY_RX0_CFG1	Offset	Reset Value
SGMII PHY RX0 CFG1	$D003_H$	0000_H

Field	Bits	Type	Description
RX0_RESET	5	rwh	**Active High Receiver Reset** 0_B **NOT_RESET** Receiver is not in reset state. 1_B **RESET** Receiver is in reset state.
RX0_RATE	4:3	rwh	**RX Data Rate** 00_B **DIV1** MPLL_Baud_clk 01_B **DIV2** MPLL_Baud_clk/2 10_B **DIV4** MPLL_Baud_clk/4 11_B **RES** Reserved
RX0_PLL_EN	2	rwh	**RX PLL Enable** 0_B **DISABLE** RX PLL is disabled. 1_B **ENABLE** RX PLL is enabled.
RX0_DATA_EN	1	rwh	**RX Data Enable** 0_B **DISABLE** RX Data Enable is disabled. 1_B **ENABLE** RX Data Enable is enabled.
RX0_ALIGN_EN	0	rwh	**RX Align Enable** 0_B **DISABLE** RX Align Enable is disabled. 1_B **ENABLE** RX Align Enable is enabled.

SGMII PHY RX0 CFG2

Used to configure SGMII PHY Receiver.

SGMII_PHY_RX0_CFG2	Offset	Reset Value
SGMII PHY RX0 CFG2	$D004_H$	0532_H



Field	Bits	Type	Description
RX0_LOS_FILT_CNT	12:6	rw	**Loss of Signal Filter Count** It configures the number of cycles that raw LOS must remain high for rx0_los to assert.
RX0_TERM_EN	5	rw	**RX Receiver Termination** 0_B **DISABLE** RX Receiver Termination removed. 1_B **ENABLE** RX Receiver Termination is present.
RX0_LOS_EN	4	rw	**LOS of Signal Detector Enable** 0_B **DISABLE** LOS of Signal Detector is disabled. 1_B **ENABLE** LOS of Signal Detector is enabled.
RX0_INVERT	3	rw	**RX Data Invert Control** 0_B **DISABLE** Incoming data on rx0_data[19:0] is NOT inverted. 1_B **ENABLE** Incoming data on rx0_data[19:0] is inverted.
RX0_EQ	2:0	rw	**Receiver Equalization Setting** "010_B" is recommended setting. May vary from system to system.

SGMII PHY TX0 CFG1

Used to configure SGMII PHY Transmitter.

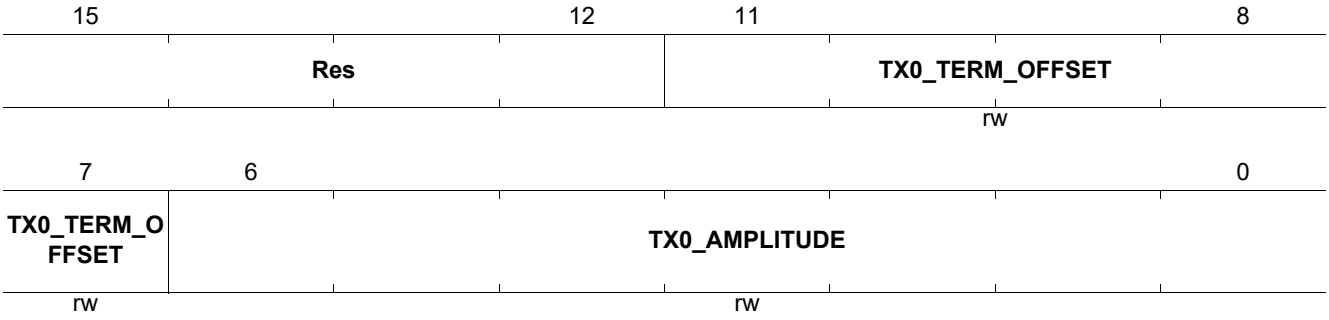
SGMII_PHY_TX0_CFG1	Offset	Reset Value
SGMII PHY TX0 CFG1	$D005_H$	0000_H

Field	Bits	Type	Description
TX0_RESET	5	rwh	**Active High Transmitter Reset** 0_B **NOT_RESET** NO Reset State 1_B **RESET** Reset State
TX0_RATE	4:3	rwh	**TX Data Rate** 00_B **DIV1** MPLL_Baud_clk 01_B **DIV2** MPLL_Baud_clk/2 10_B **DIV4** MPLL_Baud_clk/4 11_B **RES** Reserved
TX0_EN	2	rwh	**TX Enable** 0_B **DISABLE** TX is not enabled 1_B **ENABLE** TX is enabled
TX0_DATA_EN	1	rwh	**TX Data Enable** 0_B **DISABLE** TX data is disabled. 1_B **ENABLE** TX data is enabled.
TX0_CM_EN	0	rwh	**TX Common Mode Voltage Enable** 0_B **DISABLE** TX Common Mode Voltage is disabled 1_B **ENABLE** TX Common Mode Voltage is enabled

SGMII PHY TX0 CFG2

Used to configure SGMII PHY Transmitter.

SGMII_PHY_TX0_CFG2	Offset	Reset Value
SGMII PHY TX0 CFG2	$D006_H$	$007F_H$

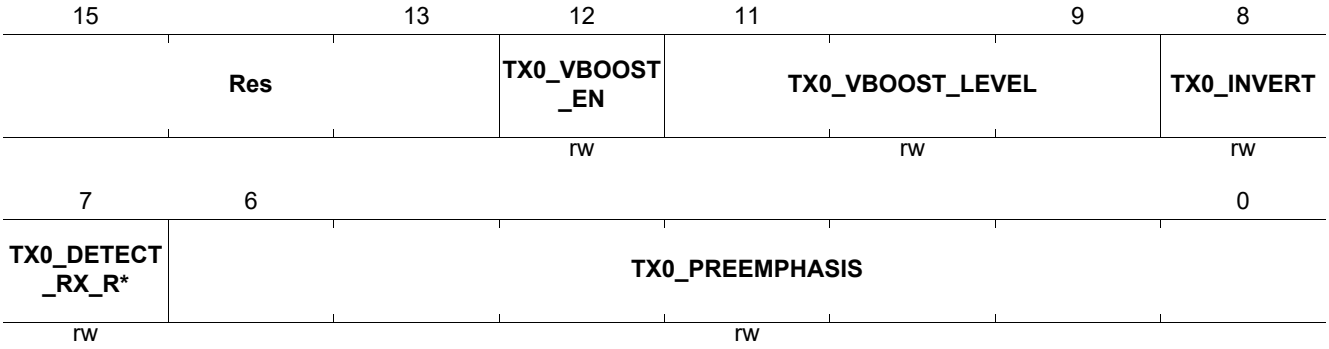


Field	Bits	Type	Description
TX0_TERM_OFFSET	11:7	rw	**TX Termination Offset** Transmitter Termination Offset
TX0_AMPLITUDE	6:0	rw	**TX Amplitude Control** Transmitter Amplitude Control

SGMII PHY TX0 CFG3

Used to configure SGMII PHY Transmitter.

SGMII_PHY_TX0_CFG3	Offset	Reset Value
SGMII PHY TX0 CFG3	$D007_H$	0800_H

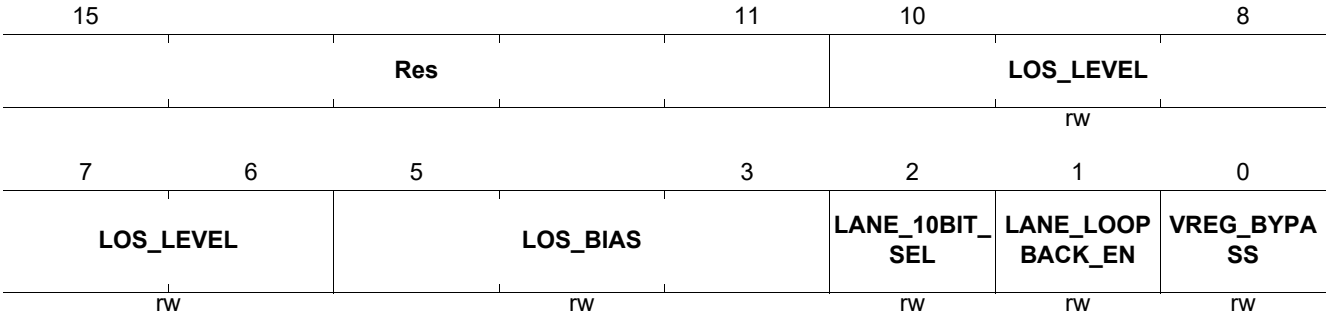


Field	Bits	Type	Description
TX0_VBOOST_EN	12	rw	**TX Vboost Enable** 0_B **DISABLE** TX Vboost is disabled. 1_B **ENABLE** TX Vboost is enabled.
TX0_VBOOST_LEVEL	11:9	rw	**TX Vboost Level Control** 011_B **Level3** Launch amplitude of 0.844 V 100_B **Level4** Launch amplitude of 1.008 V 101_B **Level5** Launch amplitude of 1.156 V
TX0_INVERT	8	rw	**TX Data Inversion** 0_B **DISABLE** TX Data is NOT inverted. 1_B **ENABLE** TX Data is inverted
TX0_DETECT_RX_REQ	7	rw	**Remote Receiver Detection Request Enable** 0_B **DISABLE** Remote receiver detection request is disabled 1_B **ENABLE** Remote receiver detection request is enabled (must remain high till rx_detect_ack asserts)
TX0_PREEMPHASIS	6:0	rw	**TX Preemphasis Configuration** Control Transmitter Preemphasis used by transmitter driver

SGMII PHY MISC

Used to configure SGMII PHY.

SGMII_PHY_MISC	Offset	Reset Value
SGMII PHY MISC	$D008_H$	0254_H

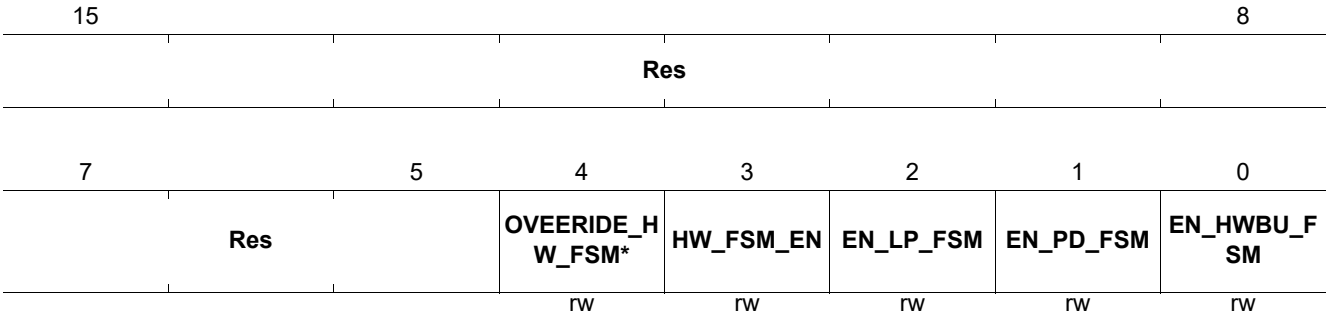


Field	Bits	Type	Description
LOS_LEVEL	10:6	rw	**LOS Sensitivity Level** LOSS of Signal Detector Sensitivity Level Control
LOS_BIAS	5:3	rw	**LOS Threshold Level** LOSS of Signal Detector Threshold Level Control 000_B **RES** Reserved 001_B **Level1** 120 mV 010_B **Level2** 135 mV 011_B **Level3** 150 mV 100_B **Level4** 45 mV 101_B **Level5** 60 mV 110_B **Level6** 75 mV 111_B **Level7** 90 mV
LANE_10BIT_SEL	2	rw	**10 Bit Mode Enable** 0_B **DISABLE** 10 Bit mode is disabled. 1_B **ENABLE** 10 Bit mode is enabled.
LANE_LOOPBACK_EN	1	rw	**TX to RX Loopback Enable** 0_B **DISABLE** TX-to-RX Loopback is disabled. 1_B **ENABLE** TX-to-RX Loopback is enabled.
VREG_BYPASS	0	rw	**Voltage Regulator Bypass Enable** 0_B **DISABLE** 3.3 V Regulator Bypass is disabled. 1_B **ENABLE** 3.3 V Regulator Bypass is enabled. 2.5 V external supply is applied to VDDH.

SGMII PHY HWBU CTRL

Used to configure SGMII PHY.

SGMII_PHY_HWBU_CTRL	Offset	Reset Value
SGMII PHY HWBU CTRL	$D009_H$	0008_H

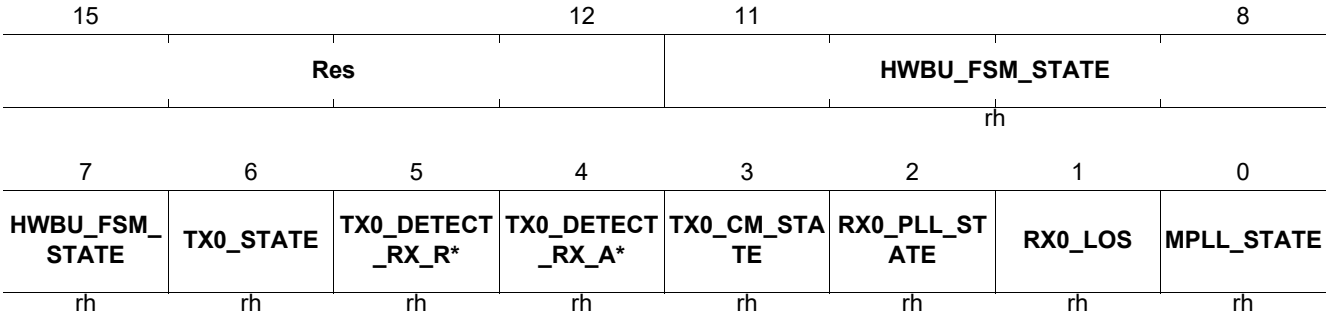


Field	Bits	Type	Description
OVEERIDE_HW_FSM_EN	4	rw	**Hardware Bringup FSM Override Enable** 0_B **DISABLE** Hardware bringup FSM override is disabled. Hardware bringup FSM enable is controlled by top level software. 1_B **ENABLE** Hardware bringup FSM override is enabled. Hardware bringup FSM enable is controlled by hardware bringup state machine.
HW_FSM_EN	3	rw	**Hardware Bringup FSM Enable** 0_B **DISABLE** Bit 0 (SGMII PHY HWBU CTRL.EN_HWBU_FSM) of this register is used as a FSM disable. 1_B **ENABLE** SGMII Macro input pin "en_hwbu_fsm" is used as FSM enable.
EN_LP_FSM	2	rw	**Hardware Bringup Low Power FSM Enable** 0_B **DISABLE** Hardware bringup low power FSM is disabled. 1_B **ENABLE** Hardware bringup low power FSM is enabled.
EN_PD_FSM	1	rw	**Hardware Bringup Power Down FSM Enable** 0_B **DISABLE** Hardware bringup power down FSM is disabled. 1_B **ENABLE** Hardware bringup power down FSM is enabled.
EN_HWBU_FSM	0	rw	**Hardware Bringup FSM Enable** 0_B **DISABLE** Hardware bringup FSM is disabled. 1_B **ENABLE** Hardware bringup FSM is enabled.

SGMII PHY STATUS

Used to store SGMII PHY status.

SGMII_PHY_STATUS	Offset	Reset Value
SGMII PHY STATUS	$D00A_H$	0000_H

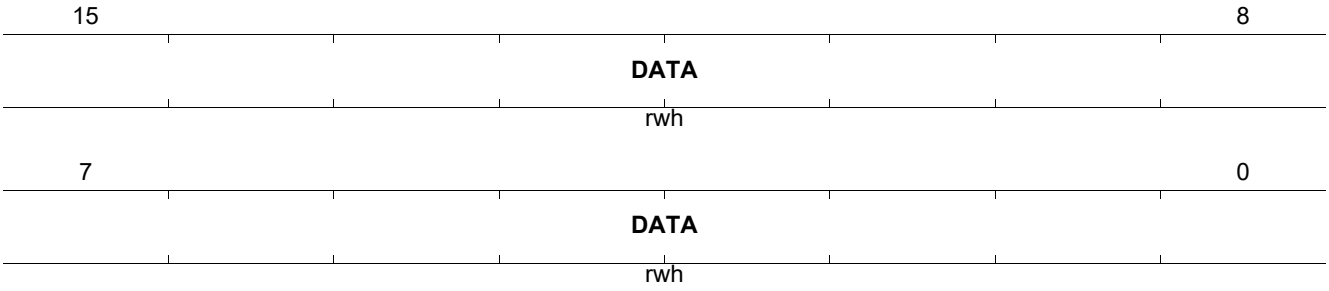


Field	Bits	Type	Description
HWBU_FSM_STATE	11:7	rh	**Hardware Bringup FSM State** Indicates status of hardware bringup FSM state
TX0_STATE	6	rh	**TX State** Indicates Transmitter is ready to Sample transmitter clock and data
TX0_DETECT_RX_RESULT	5	rh	**Detection of Receiver** Indicates detection of receiver result when asserted along with tx0_detect_rx_ack
TX0_DETECT_RX_ACK	4	rh	**Detection of Receiver Acknowledgment** Indicates detection of receiver acknowledgment.
TX0_CM_STATE	3	rh	**TX CM Acknowledgment** Indicates acknowledgment to TX CM enable
RX0_PLL_STATE	2	rh	**RX PLL State** Indicates acknowledgment to RX0 PLL enable
RX0_LOS	1	rh	**RX Loss of Signal Status** Indicates RX0 loss of signal
MPLL_STATE	0	rh	**MPLL State** Indicates acknowledgment to MPLL enable

SGMII PHY D

Used to configure/store data for read and write transaction.

SGMII_PHY_D	Offset	Reset Value
SGMII PHY D	$D100_H$	0000_H

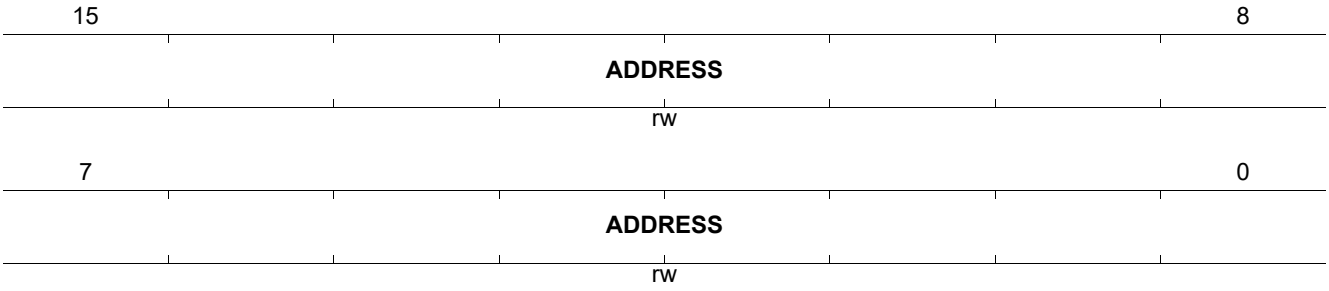


Field	Bits	Type	Description
DATA	15:0	rwh	**Data** When a XAUI control read transaction has completed, the return value may be read from here. When a XAUI control write transaction is to be performed the desired write data must be written here prior to issuing a write via SGMII_PHY_C.

SGMII PHY A

Used to configure address for read and write transaction.

SGMII_PHY_A	Offset	Reset Value
SGMII PHY A	$D101_H$	0000_H

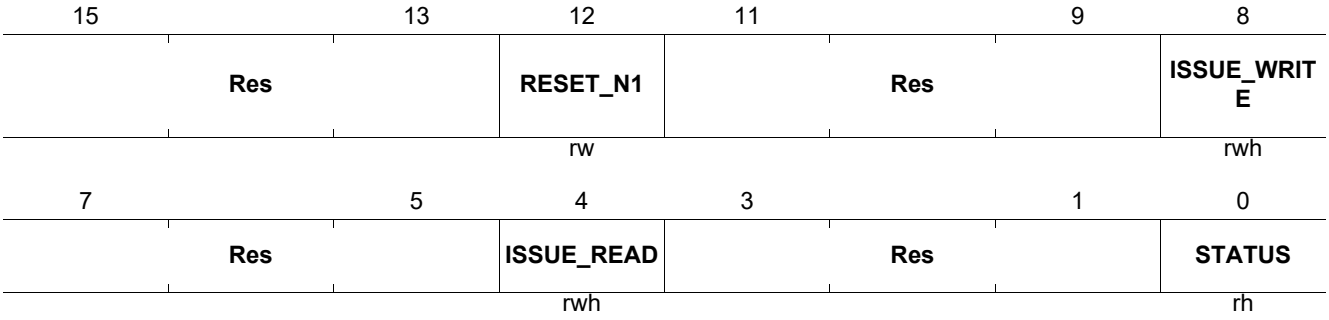


Field	Bits	Type	Description
ADDRESS	15:0	rw	**Address** When a XAUI control read or write transaction is to be performed, the desired address must be written here. Values written here are available for reading back.

SGMII PHY C

Used to configure read and write transaction control

SGMII_PHY_C	Offset	Reset Value
SGMII PHY C	$D102_H$	1000_H



Field	Bits	Type	Description
RESET_N1	12	rw	**Active Low Reset** Active low asynchronous reset to PDI2CR statemachine.Write 1b'0 to reset.
ISSUE_WRITE	8	rwh	**Start Write Access** When written to a one, the XAUI address stored in SGMII_PHY_A is written with the data value stored in SGMII_PHY_D.
ISSUE_READ	4	rwh	**Start Read Access** When written to a one, the XAUI address stored in SGMII_PHY_A is read from the XAUI module, and the result deposited in SGMII_PHY_D. This bit auto clears.
STATUS	0	rh	**Status** When a register transaction to the XAUI is initiated, this bit auto clears to 0. When the transaction is completed this register is then set to 1. After initiation of a XAUI read or write, firmware must poll for this bit to be a 1. This bit stays at 1 until reset or until a new transaction is initiated.

SGMII PHY WATCHDOG CONTROL

Used to configure watchdog control.

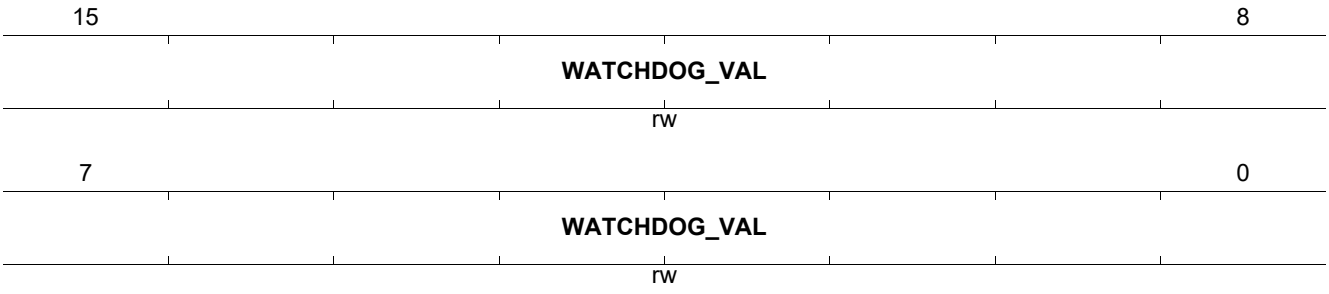
SGMII_PHY_WATCHDOG_CTRL	Offset	Reset Value
SGMII PHY WATCHDOG CONTROL	$D111_H$	0000_H

Field	Bits	Type	Description
WATCHDOG_EN	1	rw	**Watchdog Enable** Enable watchdog timer.
WATCHDOG_ERR	0	rh	**Watchdog Error Value** Watchdog reset state machine.

SGMII PHY WATCHDOG TIMER

Used to configure watchdog timer.

SGMII_PHY_WATCHDOG_TIMER	Offset	Reset Value
SGMII PHY WATCHDOG TIMER	$D112_H$	$FFFF_H$



Field	Bits	Type	Description
WATCHDOG_VAL	15:0	rw	**Watchdog Timer Value** Watchdog timer value

4.2.4 SGMII_MACRO_REGISTERS: SGMII_MACRO Registers

This section defines all the registers required to operate the SGMII_MACRO module.[1)]

SGMII Macro Reset Control

Hold bits that control top level resets of the macro.

SGMII_MACRO_RESETN	Offset	Reset Value
SGMII Macro Reset Control	$D200_H$	0003_H

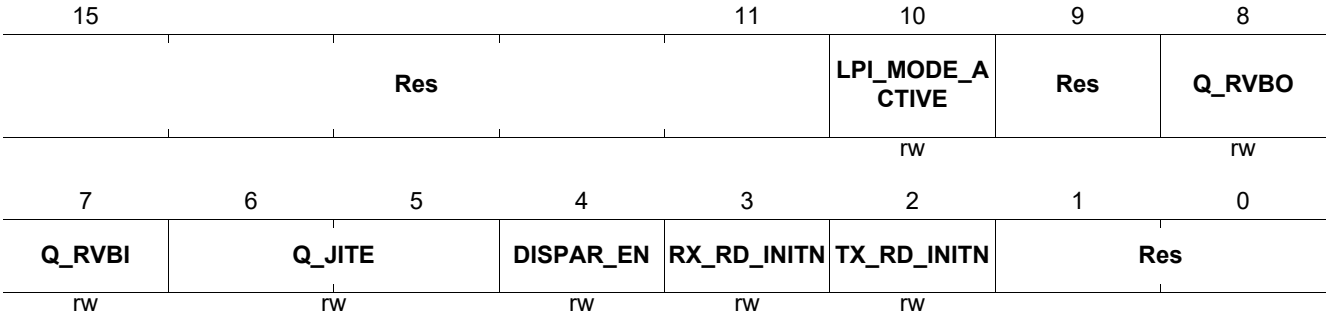
Field	Bits	Type	Description
SGMII_PCS_ RESETN	1	rw	**SGMII_PCS_RESETN** Resets all PCS operations of the SGMII Macro. 0_B **RESET** RESET 1_B **NOT_RESET** NO_RESET
SGMII_PHY_ RESETN	0	rw	**SGMII_PHY_RESETN** Resets all operations related to the SGMII_PHY Macro. 0_B **RESET** RESET 1_B **NOT_RESET** NO_RESET

1) Generated by REFIGE v1.4 - Beta Release XIV

SGMII Macro SGMII CTRL1

Used to configure SGMII interface mode.

SGMII_MACRO_SGMII_CTRL1	Offset	Reset Value
SGMII Macro SGMII CTRL1	$D201_H$	$020C_H$

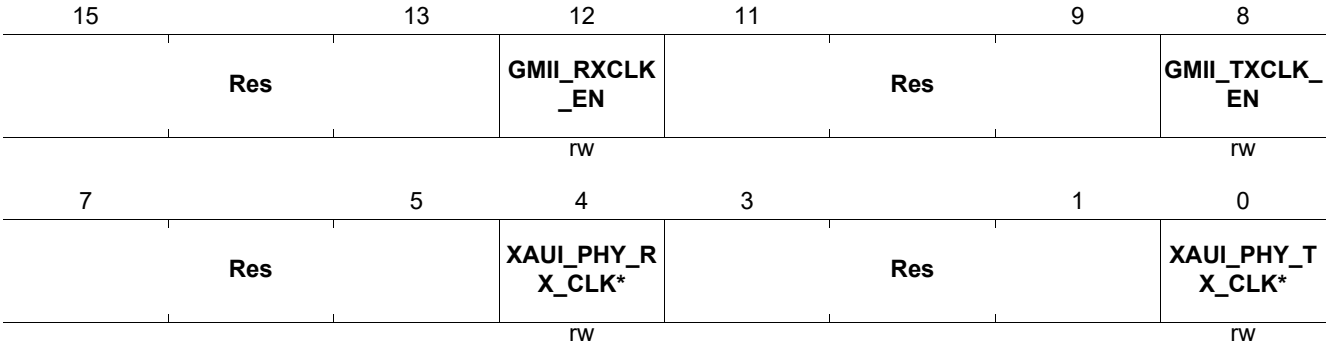


Field	Bits	Type	Description
LPI_MODE_ACTIVE	10	rw	**LPI Mode Enable** 0_B **DISABLE** LPI mode is disabled. 1_B **ENABLE** LPI mode is enabled.
Q_RVBO	8	rw	**Reverse Bit Order Output** 0_B **DISABLE** Reverse bit order output is disabled. 1_B **ENABLE** Reverse bit order output is enabled.
Q_RVBI	7	rw	**Reverse Bit Order Input** 0_B **DISABLE** Reverse bit order input is disabled. 1_B **ENABLE** Reverse bit order input is enabled.
Q_JITE	6:5	rw	**TX Jitter Test Pattern** 00_B **NO** Normal Function 01_B **HIGH** Transmit high frequency test pattern 36A.1 10_B **LOW** Transmit low frequency test pattern 36A.2 11_B **MIXED** Transmit mixed frequency test pattern 36A.3
DISPAR_EN	4	rw	**Disparity Enable** 0_B **DISABLE** Disparity is disabled. 1_B **ENABLE** Disparity is enabled.
RX_RD_INITN	3	rw	**RX Running Disparity** 0_B **INIT0** RX Running Disparity is initialized to '0'. 1_B **INIT1** RX Running Disparity is initialized to '1'.
TX_RD_INITN	2	rw	**TX Running Disparity** 0_B **INIT0** TX Running Disparity is initialized to '0'. 1_B **INIT1** TX Running Disparity is initialized to '1'.

SGMII Macro Clock Control

Controls gating of various SGMII macro clocks.

SGMII_MACRO_CLK_CTRL	Offset	Reset Value
SGMII Macro Clock Control	$D20F_H$	1111_H



Field	Bits	Type	Description
GMII_RXCLK_EN	12	rw	**GMII RX Clock Enable** Enables the GMII RX clock to PCS layer 0_B **DISABLE** RX clock is disabled 1_B **ENABLE** RX clock is enabled
GMII_TXCLK_EN	8	rw	**GMII TX Clock Enable** Enables the GMII Tx clock to PCS layer 0_B **DISABLE** TX clock is disabled 1_B **ENABLE** TX clock is enabled
XAUI_PHY_RX_CLK_EN	4	rw	**PMD/PMA Core's RX Clock Enable** Enables the PMD/PMA Core's RX data clock to PCS layer 0_B **DISABLE** RX clock is disabled. 1_B **ENABLE** RX clock is enabled.
XAUI_PHY_TX_CLK_EN	0	rw	**PMD/PMA Core's RX Clock Enable** Enables the PMD/PMA Core's Tx data clock to PCS layer 0_B **DISABLE** TX clock is disabled. 1_B **ENABLE** TX clock is enabled.

4.3 PHY MDIO Registers

This section defines all the registers required to operate the REGISTERS module.[1)]

Table 59 Registers Address Space

Module	Base Address	End Address	Note
REGISTERS	00_H	60_H	

Table 60 Registers Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
PHY MDIO Registers, STD: Standard Management Registers			
CTRL	Control	00_H	9040_H
STAT	Status Registers	01_H	7949_H
PHYID1	PHY Identifier 1	02_H	$D565_H$
PHYID2	PHY Identifier 2	03_H	$A401_H$
AN_ADV	Auto-Negotiation Advertisement	04_H	$01E1_H$
AN_LPA	Auto-Negotiation Link-Partner Ability	05_H	0000_H
AN_EXP	Auto-Negotiation Expansion	06_H	0004_H
AN_NPTX	Auto-Negotiation Next-Page Transmit Register	07_H	2001_H
AN_NPRX	Auto-Negotiation Link-Partner Received Next-Page Register	08_H	2001_H
GCTRL	Gigabit Control Register	09_H	0300_H
GSTAT	Gigabit Status Register	$0A_H$	0000_H
RES11	Reserved	$0B_H$	0000_H
RES12	Reserved	$0C_H$	0000_H
MMDCTRL	MMD Access Control Register	$0D_H$	0000_H
MMDDATA	MMD Access Data Register	$0E_H$	0000_H
XSTAT	Extended Status Register	$0F_H$	3000_H
PHY MDIO Registers, PHY: PHY-Specific Management Registers			
PHYPERF	Physical Layer Performance Status	10_H	$80FF_H$
PHYSTAT1	Physical Layer Status 1	11_H	0000_H
PHYSTAT2	Physical Layer Status 2	12_H	0000_H
PHYCTL1	Physical Layer Control 1	13_H	0003_H
PHYCTL2	Physical Layer Control 2	14_H	8006_H
ERRCNT	Error Counter	15_H	0000_H
MIISTAT	Media-Independent Interface Status	18_H	0000_H
IMASK	Interrupt Mask Register	19_H	0000_H
ISTAT	Interrupt Status Register	$1A_H$	0000_H
LED	LED Control Register	$1B_H$	$0F00_H$
TPGCTRL	Test-Packet Generator Control	$1C_H$	0000_H

1) Generated by REFIGE v1.4 - Beta Release XIV

Table 60 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
TPGDATA	Test-Packet Generator Data	$1D_H$	$00AA_H$
FWV	Firmware Version Register	$1E_H$	8304_H
RES1F	Reserved	$1F_H$	0000_H

The register is addressed wordwise.

Table 61 Register Access Types

Mode	Symbol	Internal Hardware Configuration		
		Type	Behavior	Arbitration
Status Register, Latch-High	ROLH	RWRE	AUTO_PDI	CLROR
Status Register, Latch-Low	ROLL	WOR	AUTO_HW	CLROR
Status Register, Self-Clearing	ROSC	WOR	AUTO_PDI	CLROR
Read-Write Register	RW	RWR	AUTO_PDI	-
Read-Write Register, Self-Clearing	RWSC	RWR	AUTO_PDI	CLROR
Status Register	RO	WOR	AUTO_PDI	-

4.3.1 STD: Standard Management Registers

This section describes the IEEE 802.3 standard management registers.

Control

This register controls the main functions of the PHY. Refer to IEEE 802.3 22.2.4.1.

CTRL	Offset	Reset Value
Control	00_H	9040_H

15	14	13	12	11	10	9	8
RST	**LB**	**SSL**	**ANEN**	**PD**	**ISOL**	**ANRS**	**DPLX**
rwsc	rw	rw	rw	rw	rw	rwsc	rw

7	6	5					0
COL	**SSM**	**RES**					
rw	rw	ro					

Field	Bits	Type	Description
RST	15	RWSC	**Reset** Resets the PHY to its default state. Active links are terminated. This is a self-clearing bit set to zero by the hardware after reset has been done. Refer to IEEE 802.3 22.2.4.1.1. 0_B **NORMAL** Normal operational mode 1_B **RESET** Resets the device
LB	14	RW	**Loopback** This mode enables looping back of MII data from the transmit to the receive direction. No data is transmitted to the medium via MDI. The device operates at the selected speed. The collision signal remains de-asserted unless otherwise forced by the collision test. Refer to IEEE 802.8-2008 22.2.4.1.2. 0_B **NORMAL** Normal operational mode 1_B **ENABLE** Closes the loopback from TX to RX at xMII
SSL	13	RW	**Forced Speed Selection LSB** This bit only takes effect when the auto-negotiation process is disabled, that is, bit CTRL. ANEN is set to zero. This is the LSB (CTRL.SSL) of the forced speed-selection register SS. In conjunction with the MSB (CTRL.SSM), the following encodings are valid: SS=0: 10 Mbps SS=1: 100 Mbps SS=2: 1000 Mbps SS=3: Reserved

Field	Bits	Type	Description
ANEN	12	RW	**Auto-Negotiation Enable** Allows enabling and disabling of the auto-negotiation process capability of the PHY. When enabled, the force bits for duplex mode (CTRL.DPLX) and the speed selection (CTRL.SSM, CTRL.SSL) become inactive. Otherwise, the force bits define the PHY operation. Refer to IEEE 802.3 22.2.4.1.4. 0_B **DISABLE** Disable the auto-negotiation protocol 1_B **ENABLE** Enable the auto-negotiation protocol
PD	11	RW	**Power Down** Forces the device into a power-down state where power consumption is the bare minimum required to still maintain the MII management interface communication. When activating the power-down functionality, the PHY terminates active data links. None of the xMII interface work in power-down mode. Refer to IEEE 802.3 22.2.4.1.5. 0_B **NORMAL** Normal operational mode 1_B **POWERDOWN** Forces the device into power-down mode
ISOL	10	RW	**Isolation Mode** The isolation mode isolates the PHY from the MAC. MAC interface inputs are ignored, whereas MAC interface outputs are set to tristate (high-impedance). Refer to IEEE 802.3 22.2.4.1.6. 0_B **NORMAL** Normal operational mode 1_B **ISOLATE** Isolates the PHY from the MAC
ANRS	9	RWSC	**Restart Auto-Negotiation** Restarts the auto-negotiation process on the MDI. This bit does not take any effect when auto-negotiation is disabled using (CTRL.ANEN). This bit is self-clearing after the auto-negotiation process is initiated. Refer to IEEE 802.3 22.2.4.1.7. 0_B **NORMAL** Stay in current mode 1_B **RESTART** Restart auto-negotiation
DPLX	8	RW	**Forced Duplex Mode** This bit only takes effect when the auto-negotiation process is disabled, that is, bit CTRL.ANEN is set to zero. This bit controls the forced duplex mode. It allows forcing of the PHY into full or half-duplex mode. This bit does not take effect in loop-back mode, that is, when bit CTRL.LB is set to one. Refer to IEEE 802.3 22.2.4.1.8. 0_B **HD** Half duplex 1_B **FD** Full duplex
COL	7	RW	**Collision Test** Allows$WORKAREA/units/mdio/source testing of the COL signal at the xMII interface. When the collision test is enabled, the state of the TX_EN signal is looped back to the COL signal within a minimum latency time. Refer to IEEE 802.3 22.2.4.1.9. 0_B **DISABLE** Normal operational mode 1_B **ENABLE** Activates the collision test
SSM	6	RW	**Forced Speed Selection MSB** Refer to the description of SSL. Refer also to IEEE 802.3-2008 22.2.4.1.3.
RES	5:0	RO	**Reserved** Write as zero, ignore on read.

Status Registers

This register contains status and capability information about the device. All bits are read-only. A write access by the MAC does not have any effect. Refer to IEEE 802.3 22.2.4.2.

STAT	Offset	Reset Value
Status Registers	01_H	7949_H

15	14	13	12	11	10	9	8
CBT4	**CBTXF**	**CBTXH**	**XBTF**	**XBTH**	**CBT2F**	**CBT2H**	**EXT**
ro	ro	ro	ro	ro	ro	ro	ro
7	6	5	4	3	2	1	0
RES	**MFPS**	**ANOK**	**RF**	**ANAB**	**LS**	**JD**	**XCAP**
ro	ro	ro	rolh	ro	roll	rolh	ro

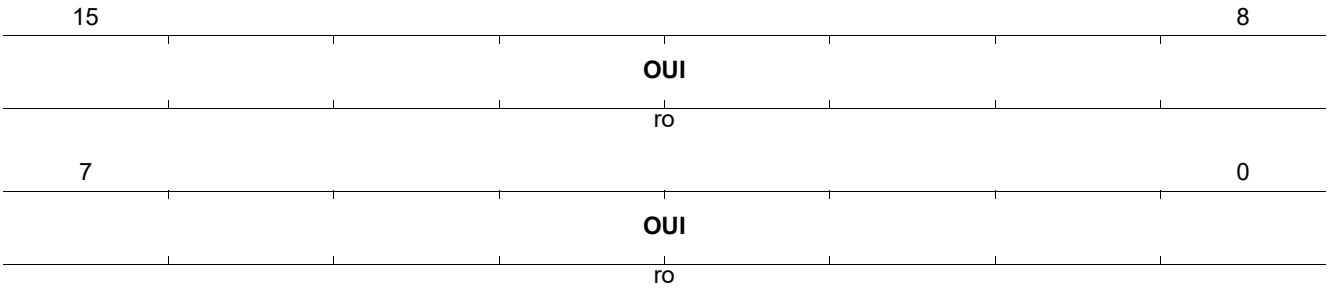
Field	Bits	Type	Description
CBT4	15	RO	**IEEE 100BASE-T4** Specifies the 100BASE-T4 ability. Refer to IEEE 802.3 22.2.4.2.1. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBTXF	14	RO	**IEEE 100BASE-TX Full-Duplex** Specifies the 100BASE-TX full-duplex ability. Refer to IEEE 802.3 22.2.4.2.2. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBTXH	13	RO	**IEEE 100BASE-TX Half-Duplex** Specifies the 100BASE-TX half-duplex ability. Refer to IEEE 802.3 22.2.4.2.3. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
XBTF	12	RO	**IEEE 10BASE-T Full-Duplex** Specifies the 10 BASE-T full-duplex ability. Refer to IEEE 802.3 22.2.4.2.4. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
XBTH	11	RO	**IEEE 10BASE-T Half-Duplex** Specifies the 10BASE-T half-duplex ability. Refer to IEEE 802.3 22.2.4.2.5. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBT2F	10	RO	**IEEE 100BASE-T2 Full-Duplex** Specifies the 100BASE-T2 full-duplex ability. Refer to IEEE 802.3 22.2.4.2.6. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBT2H	9	RO	**IEEE 100BASE-T2 Half-Duplex** Specifies the 100BASE-T2 half-duplex ability. Refer to IEEE 802.3 22.2.4.2.7. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode

Field	Bits	Type	Description
EXT	8	RO	**Extended Status** The extended status registers are used to specify 1000 Mbps speed capabilities in the register XSTAT. Refer to IEEE 802.3 22.2.4.2.16. 0_B **DISABLED** No extended status information available in register 15 1_B **ENABLED** Extended status information available in register 15
RES	7	RO	**Reserved** Ignore when read.
MFPS	6	RO	**Management Preamble Suppression** Specifies the MF preamble suppression ability. Refer to IEEE 802.3 22.2.4.2.9. 0_B **DISABLED** PHY requires management frames with preamble 1_B **ENABLED** PHY accepts management frames without preamble
ANOK	5	RO	**Auto-Negotiation Completed** Indicates whether the auto-negotiation process is completed or in progress. Refer to IEEE 802.3 22.2.4.2.10. 0_B **RUNNING** Auto-negotiation process is in progress 1_B **COMPLETED** Auto-negotiation process is completed
RF	4	ROLH	**Remote Fault** Indicates the detection of a remote fault event. Refer to IEEE 802.3 22.2.4.2.11. 0_B **INACTIVE** No remote fault condition detected 1_B **ACTIVE** Remote fault condition detected
ANAB	3	RO	**Auto-Negotiation Ability** Specifies the auto-negotiation ability. Refer to IEEE 802.3 22.2.4.2.12. 0_B **DISABLED** PHY is not able to perform auto-negotiation 1_B **ENABLED** PHY is able to perform auto-negotiation
LS	2	ROLL	**Link Status** Indicates the link status of the PHY to the link partner. Refer to IEEE 802.3 22.2.4.2.13. 0_B **INACTIVE** The link is down. No communication with link partner possible. 1_B **ACTIVE** The link is up. Data communication with link partner is possible.
JD	1	ROLH	**Jabber Detect** Indicates that a jabber event has been detected. Refer to IEEE 802.3 22.2.4.2.14. 0_B **NONE** No jabber condition detected 1_B **DETECTED** Jabber condition detected
XCAP	0	RO	**Extended Capability** Indicates the availability and support of extended capability registers. Refer to IEEE 802.3 22.2.4.2.15. 0_B **DISABLED** Only base registers are supported 1_B **ENABLED** Extended capability registers are supported

PHY Identifier 1

This is the first of two PHY identification registers containing the MSBs of a 32-bit code. This code specifies the Organizationally Unique Identifier (OUI), and the vendor model and revision number.

PHYID1	Offset	Reset Value
PHY Identifier 1	02_H	$D565_H$

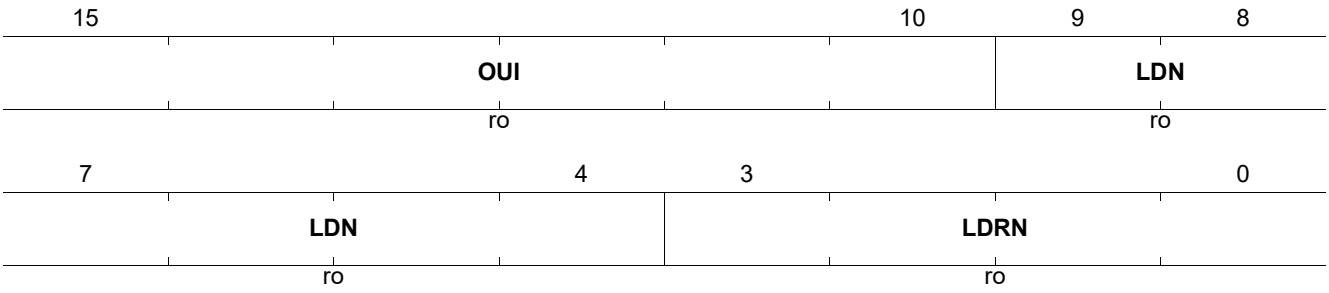


Field	Bits	Type	Description
OUI	15:0	RO	**Organizationally Unique Identifier Bits 3:18** This register holds the bits 3:18 of the OUI code for MaxLinear Inc., which is specified to be OUI=AC-9A-96. Refer to IEEE 802.3 22.2.4.3.1.

PHY Identifier 2

This is the second of 2 PHY identification registers containing the LSBs of a 32-bit code. This code specifies the Organizationally Unique Identifier (OUI), and the vendor model and revision number. Refer to IEEE 802.3 22.2.4.3.1.

PHYID2	Offset	Reset Value
PHY Identifier 2	03_H	$A401_H$



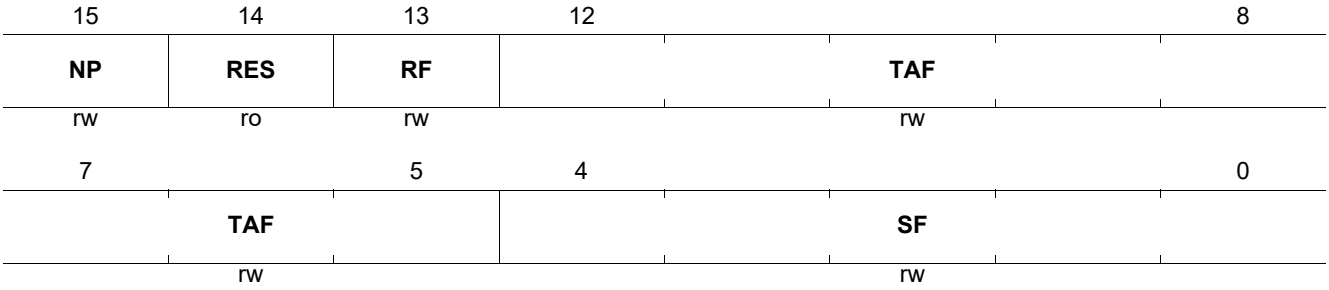
Field	Bits	Type	Description
OUI	15:10	RO	**Organizationally Unique Identifier Bits 19:24** This register holds the bits 19:24 of the OUI code for MaxLinear Inc., which is specified to be OUI=AC-9A-96.
LDN	9:4	RO	**Device Number** Specifies the device number to distinguish between several different products.

Field	Bits	Type	Description
LDRN	3:0	RO	**Device Revision Number** Specifies the device revision number to distinguish between several versions of this device.

Auto-Negotiation Advertisement

This register contains the advertised abilities of the PHY during auto-negotiation. Refer also to IEEE 802.3 28.2.4.1.3, as well as IEEE 802.3 Table 28-2.

AN_ADV	Offset	Reset Value
Auto-Negotiation Advertisement	**04_H**	**$01E1_H$**



Field	Bits	Type	Description
NP	15	RW	**Next Page** Next-page indication is encoded in bit AN_ADV.NP regardless of the selector field value or link code word encoding. The PHY always advertises NP when a 1000BASE-T mode is advertised during auto-negotiation. Refer to IEEE 802.3 28.2.1.2.6. 0_B **INACTIVE** No next page(s) follow(s) 1_B **ACTIVE** Additional next page(s) follow(s)
RES	14	RO	**Reserved** Write as zero, ignore on read.
RF	13	RW	**Remote Fault** The remote fault bit allows indication of a fault to the link partner. Refer to IEEE 802.3 28.2.1.2.4. 0_B **NONE** No remote fault is indicated 1_B **FAULT** A remote fault is indicated

Field	Bits	Type	Description
TAF	12:5	RW	**Technology Ability Field** The technology ability field is an eight-bit wide field containing information indicating supported technologies as defined by the following constants specific to the selector field value. These bits are mapped to individual technologies so that abilities are advertised in parallel for a single selector field value. In converter mode, the field is always forced to value 0x60. The TAF encoding for the IEEE 802.3 selector (AN_ADV.SF=0x1) is described in IEEE 802.3 Annex 28B.2 and in Annex 28D. Refer also to IEEE 802.3 28.2.1.2.2. 00000001_B**XBT_HDX** Advertise 10BASE-T half duplex 00000010_B**XBT_FDX** Advertise 10BASE-T full duplex 00000100_B**DBT_HDX** Advertise 100BASE-TX half duplex 00001000_B**DBT_FDX** Advertise 100BASE-TX full duplex 00010000_B**DBT4** Advertise 100BASE-T4 00100000_B**PS_SYM** Advertise symmetric pause 01000000_B**PS_ASYM** Advertise asymmetric pause 10000000_B**RES** Reserved for future technologies
SF	4:0	RW	**Selector Field** The selector field is a five-bit wide field for encoding 32 possible messages. Selector field encoding definitions are shown in IEEE 802.3 Annex 28A. Combinations not specified are reserved for future use. Reserved combinations of the selector field are not to be transmitted. Refer also to IEEE 802.3 28.2.1.2.1. 00001_B**IEEE802DOT3** Select the IEEE 802.3 technology

Auto-Negotiation Link-Partner Ability

All of the bits in the auto-negotiation link-partner ability register are read-only. A write to the auto-negotiation link-partner ability register has no effect. This register contains the advertised ability of the link partner. Refer to IEEE 802.3 Tables 28-3 and 28-4. The bit definitions are a direct representation of the received link-code word. Refer to IEEE 802.3 Figure 28-7 and IEEE 802.3 22.2.4.3.3.

AN_LPA	Offset	Reset Value
Auto-Negotiation Link-Partner Ability	05_H	0000_H

15	14	13	12	11	10	9	8
NP	ACK	RF	TAF				
ro	ro	ro	ro				

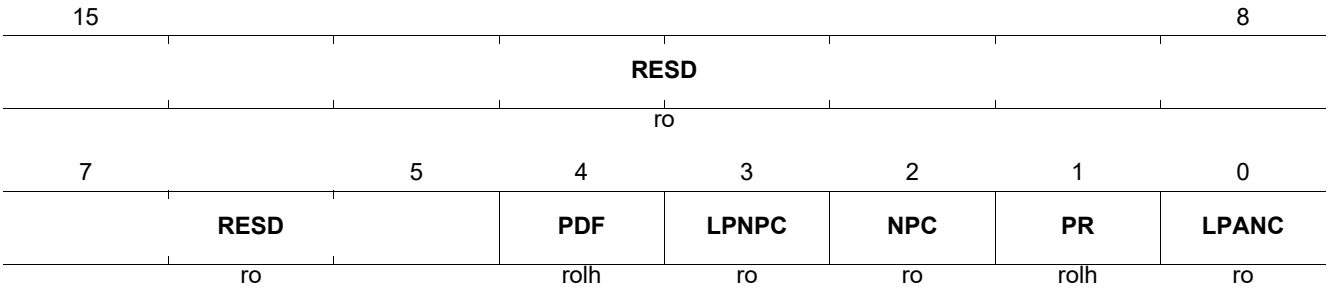
7	6	5	4	3	2	1	0
TAF			SF				
ro			ro				

Field	Bits	Type	Description
NP	15	RO	**Next Page** Next-page request indication from the link partner. Refer to IEEE 802.3 28.2.1.2.6. 0_B **INACTIVE** No next page(s) follow (s) 1_B **ACTIVE** Additional next pages follow (s)
ACK	14	RO	**Acknowledge** Acknowledgment indication from the link partner's link-code word. Refer to IEEE 802.3 28.2.1.2.5. 0_B **INACTIVE** The device did not successfully receive its link partner's link code word 1_B **ACTIVE** The device has successfully received its link partner's link-code word
RF	13	RO	**Remote Fault** Remote fault indication from the link partner. Refer to IEEE 802.3 28.2.1.2.4. 0_B **NONE** Remote fault is not indicated by the link partner 1_B **FAULT** Remote fault is indicated by the link partner
TAF	12:5	RO	**Technology Ability Field** Indicates the link-partner capabilities as received from the link partner's link-code word. Refer to IEEE 802.3 28.2.1.2.2. 00000001_B**XBT_HDX** Link partner advertised 10BASE-T half duplex 00000010_B**XBT_FDX** Link partner advertised 10BASE-T full duplex. 00000100_B**DBT_HDX** Link partner advertised 100BASE-TX half duplex 00001000_B**DBT_FDX** Link partner advertised 100BASE-TX full duplex 00010000_B**DBT4** Link partner advertised 100BASE-T4 00100000_B**PS_SYM** Link partner advertised symmetric pause 01000000_B**PS_ASYM** Link partner advertised asymmetric pause 10000000_B**RES** Reserved for future technologies; must be zero
SF	4:0	RO	**Selector Field** The selector field represents one of the 32 possible messages. It must fit to the advertised selector field in AN_ADV.SF. Selector field encoding definitions are shown in IEEE 802.3 Annex 28A. 00001_B**IEEE802DOT3** Select the IEEE 802.3 technology

Auto-Negotiation Expansion

This is the auto-negotiation expansion register indicating the status of the link partner's auto-negotiation. Refer to IEEE 802.3 28.2.4.1.5.

AN_EXP	Offset	Reset Value
Auto-Negotiation Expansion	06_H	0004_H

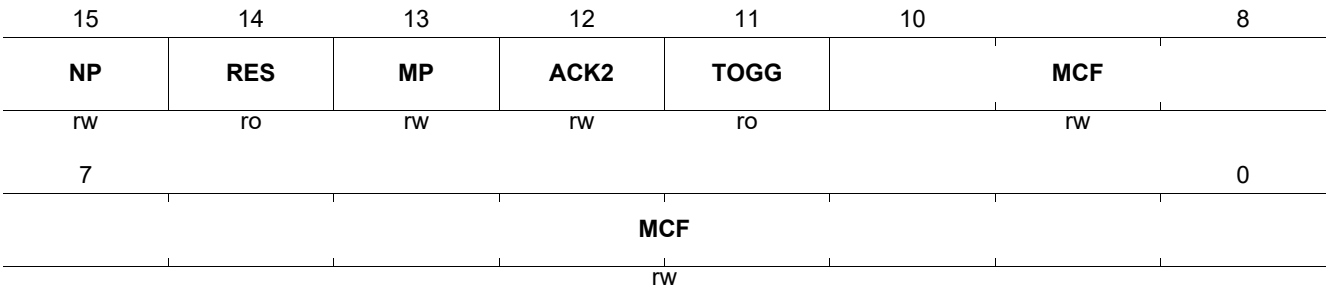


Field	Bits	Type	Description
RESD	15:5	RO	**Reserved** Write as zero, ignore on read.
PDF	4	ROLH	**Parallel Detection Fault** This bit latches high. It is set to zero upon read of AN_EXP. Refer to IEEE 802.3 28.2.4.1.5. 0_B **NONE** A fault has not been detected via the parallel detection function 1_B **FAULT** A fault has been detected via the parallel detection function
LPNPC	3	RO	**Link Partner Next-Page Capable** Refer to IEEE 802.3 28.2.4.1.5. 0_B **UNABLE** Link partner is unable to exchange next pages 1_B **CAPABLE** Link partner is capable of exchanging next pages
NPC	2	RO	**Next-Page Capable** Refer to IEEE 802.3 28.2.4.1.5. 0_B **UNABLE** Local Device is unable to exchange next pages 1_B **CAPABLE** Local device is capable of exchanging next pages
PR	1	ROLH	**Page Received** This bit latches high. It is set to zero upon read of AN_EXP. Refer to IEEE 802.3 28.2.4.1.5. 0_B **NONE** A new page has not been received 1_B **RECEIVED** A new page has been received
LPANC	0	RO	**Link Partner Auto-Negotiation Capable** Refer to IEEE 802.3 28.2.4.1.5. 0_B **UNABLE** Link partner is unable to auto-negotiate 1_B **CAPABLE** Link partner is auto-negotiation capable

Auto-Negotiation Next-Page Transmit Register

The auto-negotiation next-page transmit register contains the next-page link-code word to be transmitted when next-page ability is supported. On power-up, this register contains the default value of 0x2001, which represents a message page with the message code set to the null message. Refer also to IEEE 802.3 28.2.4.1.6.

AN_NPTX	Offset	Reset Value
Auto-Negotiation Next-Page Transmit Register	07_H	2001_H

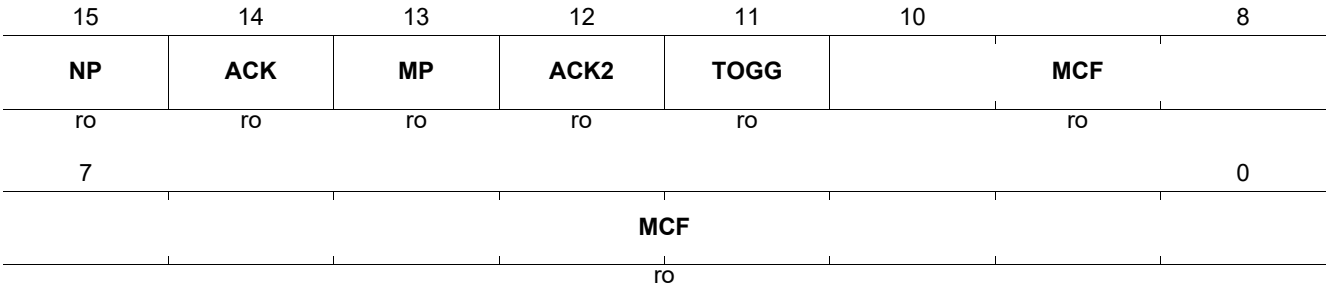


Field	Bits	Type	Description
NP	15	RW	**Next Page** Refer to IEEE 802.3 28.2.3.4. 0_B **INACTIVE** Last page 1_B **ACTIVE** Additional next page(s) follow(s)
RES	14	RO	**Reserved** Write as zeros, ignore on read.
MP	13	RW	**Message Page** Indicates that the content of MCF is either an unformatted page or a formatted message. Refer to IEEE 802.3 28.2.3.4. 0_B **UNFOR** Unformatted page 1_B **MESSG** Message page
ACK2	12	RW	**Acknowledge 2** Refer to IEEE 802.3 28.2.3.4. 0_B **INACTIVE** Device cannot comply with message 1_B **ACTIVE** Device complies with message
TOGG	11	RO	**Toggle** Refer to IEEE 802.3 28.2.3.4. 0_B **ZERO** Previous value of the transmitted link-code word was equal to logic ONE 1_B **ONE** Previous value of the transmitted link-code word was equal to logic ZERO
MCF	10:0	RW	**Message or Unformatted Code Field** Refer to IEEE 802.3 28.2.3.4.

Auto-Negotiation Link-Partner Received Next-Page Register

The auto-negotiation link-partner received next-page register contains the next-page link-code word received from the link partner. Refer to IEEE 802.3 28.2.4.1.7.

AN_NPRX	Offset	Reset Value
Auto-Negotiation Link-Partner Received Next-Page Register	08_H	2001_H

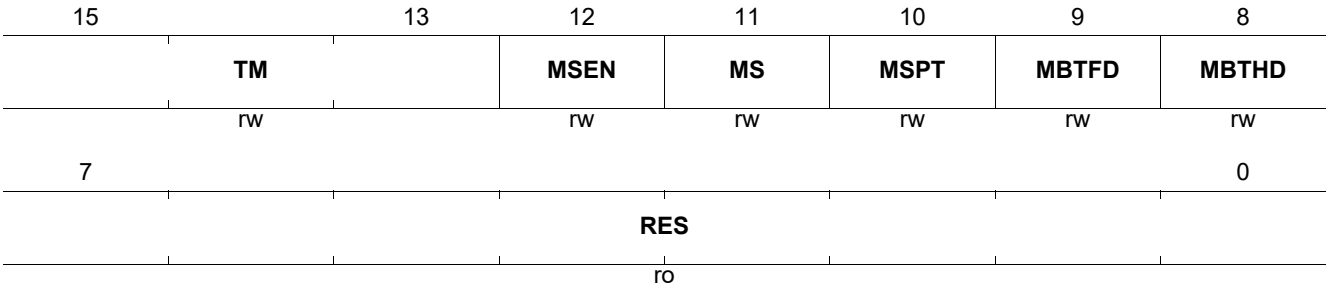


Field	Bits	Type	Description
NP	15	RO	**Next Page** Refer to IEEE 802.3 28.2.3.4. 0_B **INACTIVE** No next pages to follow 1_B **ACTIVE** Additional next page(s) follow(s)
ACK	14	RO	**Acknowledge** Refer to IEEE 802.3 28.2.3.4. 0_B **INACTIVE** The device did not successfully receive its link partner's link-code word 1_B **ACTIVE** The device has successfully received its link partner's link-code word
MP	13	RO	**Message Page** Indicates that the content of MCF is either an unformatted page or a formatted message. Refer to IEEE 802.3 28.2.3.4. 0_B **UNFOR** Unformatted page 1_B **MESSG** Message page
ACK2	12	RO	**Acknowledge 2** Refer to IEEE 802.3 28.2.3.4. 0_B **INACTIVE** Device cannot comply with message 1_B **ACTIVE** Device complies with message
TOGG	11	RO	**Toggle** Refer to IEEE 802.3 28.2.3.4. 0_B **ZERO** Previous value of the transmitted link-code word was equal to logic ONE 1_B **ONE** Previous value of the transmitted link-code word was equal to logic ZERO
MCF	10:0	RO	**Message or Unformatted Code Field** Refer to IEEE 802.3 28.2.3.4.

Gigabit Control Register

This is the control register used to configure the Gigabit Ethernet behavior of the PHY. Refer to IEEE 802.3 40.5.1.1.

GCTRL	Offset	Reset Value
Gigabit Control Register	09_H	0300_H



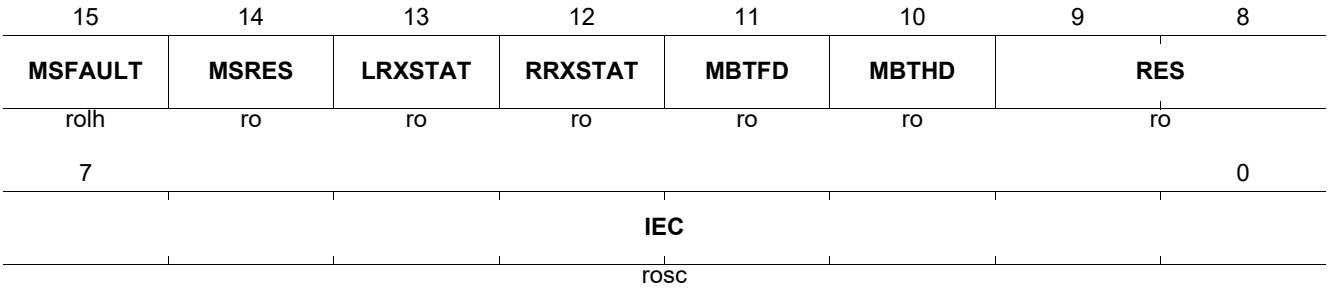
Field	Bits	Type	Description
TM	15:13	RW	**Transmitter Test Mode** This register field allows enabling of the standard transmitter test modes. Refer also to IEEE 802.3-2008 Table 40-7. 000_B **NOP** Normal operation 001_B **WAV** Test mode 1 transmit waveform test 010_B **JITM** Test mode 2 transmit jitter test in MASTER mode 011_B **JITS** Test mode 3 transmit jitter test in SLAVE mode 100_B **DIST** Test mode 4 transmitter distortion test 101_B **RESD0** Reserved, operations not identified. 110_B **CDIAG** Cable diagnostics. 111_B **ABIST** Analog build in self-test
MSEN	12	RW	**Master/Slave Manual Configuration Enable** Refer also to IEEE 802.3-2008 40.5.1.1. 0_B **DISABLED** Disable master/slave manual configuration value 1_B **ENABLED** Enable master/slave manual configuration value
MS	11	RW	**Master/Slave Config Value** Allows forcing of master or slave mode manually when AN_GCTRL.MSEN is set to logical one. Refer also to IEEE 802.3-2008 40.5.1.1. 0_B **SLAVE** Configure PHY as SLAVE during master/slave negotiation, only when AN_GCTRL.MSEN is set to logical one 1_B **MASTER** Configure PHY as MASTER during master/slave negotiation, only when AN_GCTRL.MSEN is set to logical one
MSPT	10	RW	**Master/Slave Port Type** Defines whether the PHY advertises itself as a multi- or single-port device, which in turn impacts the master/slave resolution function. Refer also to IEEE 802.3-2008 40.5.1.1. 0_B **SPD** Single-port device 1_B **MPD** Multi-port device

Field	Bits	Type	Description
MBTFD	9	RW	**1000BASE-T Full-Duplex** Advertises the 1000BASE-T full-duplex capability; always forced to 1 in converter mode. Refer also to IEEE 802.3 40.5.1.1. 0_B **DISABLED** Advertise PHY as not 1000BASE-T full-duplex capable 1_B **ENABLED** Advertise PHY as 1000BASE-T full-duplex capable
MBTHD	8	RW	**1000BASE-T Half-Duplex** Advertises the 1000BASE-T half-duplex capability; always forced to 1 in converter mode. Refer to IEEE 802.3 40.5.1.1. 0_B **DISABLED** Advertise PHY as not 1000BASE-T half-duplex capable 1_B **ENABLED** Advertise PHY as 1000BASE-T half-duplex capable
RES	7:0	RO	**Reserved** Write as zero, ignore on read.

Gigabit Status Register

This is the status register used to reflect the Gigabit Ethernet status of the PHY. Refer also to IEEE 802.3-2008 40.5.1.1.

GSTAT	Offset	Reset Value
Gigabit Status Register	$0A_H$	0000_H



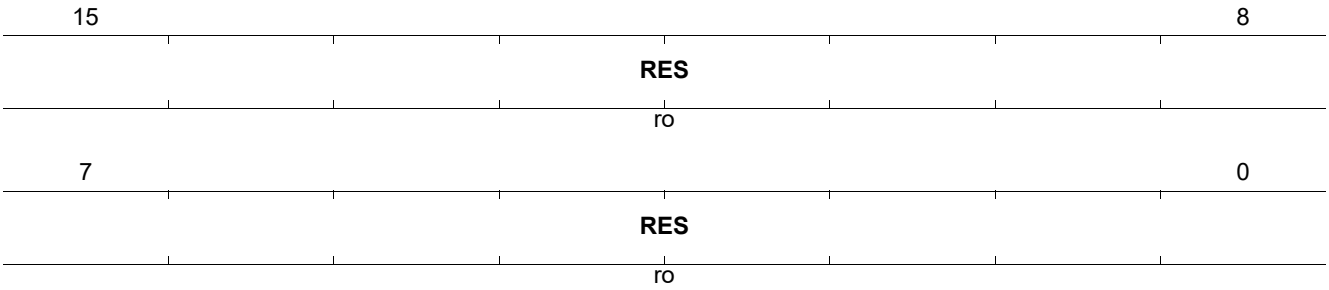
Field	Bits	Type	Description
MSFAULT	15	ROLH	**Master/Slave Manual Configuration Fault** This is a latching high bit. It is cleared upon each read of GSTAT. This bit self clears on auto-negotiation enable or auto-negotiation complete. This bit is set to active high when the number of failed master/slave resolutions reaches 7. Refer also to IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. 0_B **OK** Master/slave manual configuration resolved successfully 1_B **NOK** Master/slave manual configuration resolved with a fault
MSRES	14	RO	**Master/Slave Configuration Resolution** Refer to IEEE 802.3 40.5.1.1 register 10 in Table 40-3. 0_B **SLAVE** Local PHY configuration resolved to SLAVE 1_B **MASTER** Local PHY configuration resolved to MASTER

Field	Bits	Type	Description
LRXSTAT	13	RO	**Local Receiver Status** Indicates the status of the local receiver. Refer also to IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. 0_B **NOK** Local receiver not OK 1_B **OK** Local receiver OK
RRXSTAT	12	RO	**Remote Receiver Status** Indicates the status of the remote receiver. Refer also to IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. **Constants** 0_B **NOK** Remote receiver not OK 1_B **OK** Remote receiver OK
MBTFD	11	RO	**Link-Partner Capable of Operating 1000BASE-T Full-Duplex** Refer also to IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. **Constants** 0_B **DISABLED** Link partner is not capable of operating 1000BASE-T full-duplex 1_B **ENABLED** Link partner is capable of operating 1000BASE-T full-duplex
MBTHD	10	RO	**Link-Partner Capable of Operating 1000BASE-T Half-Duplex** Refer also to IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. **Constants** 0_B **DISABLED** Link partner is not capable of operating 1000BASE-T half-duplex 1_B **ENABLED** Link partner is capable of operating 1000BASE-T half-duplex
RES	9:8	RO	**Reserved** Write as zero, ignore on read.
IEC	7:0	ROSC	**Idle Error Count** Indicates the idle error count. This field contains a cumulative count of the errors detected when the receiver is receiving idles and PMA_TXMODE. Indicate is equal to SEND_N (indicating that both local and remote receiver status have been detected to be OK). The counter is incremented every symbol period that rxerror_status is equal to ERROR. These bits are reset to all zeros when the GSTAT register is read by the management function or upon execution of the PCS reset function, and are to be held at all ones in case of overflow.

Reserved

Reserved. In IEEE 802.3-2008, this register is used for Power-Sourcing-Equipment (PSE) control functions. Refer to IEEE 802.3-2008 33.6.1.1. These are not supported by this PHY.

RES11	Offset	Reset Value
Reserved	$0B_H$	0000_H

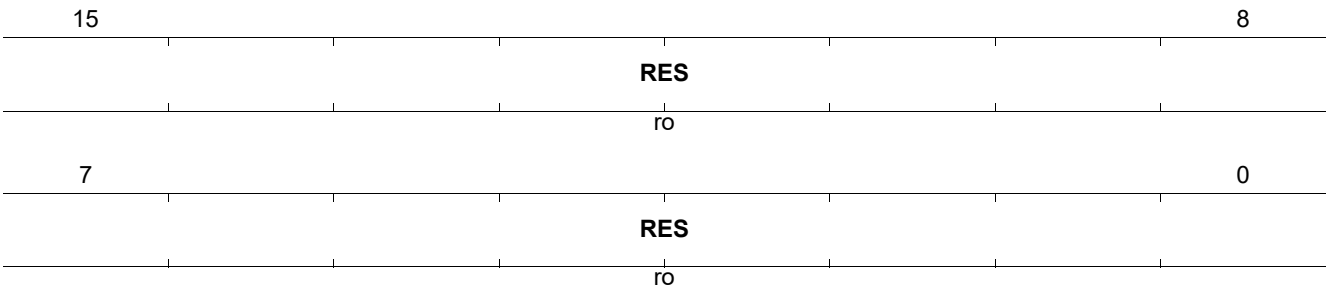


Field	Bits	Type	Description
RES	15:0	RO	**Reserved** Write as zero, ignored on read.

Reserved

Reserved. In IEEE 802.3-2008, this register is used for Power-Sourcing-Equipment (PSE) status functions. Refer to IEEE 802.3-2008 33.6.1.2. These are not supported by this PHY.

RES12	Offset	Reset Value
Reserved	$0C_H$	0000_H

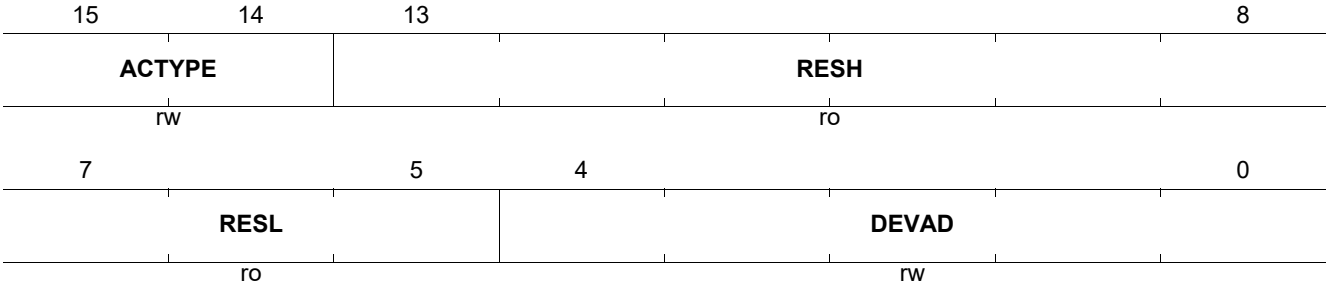


Field	Bits	Type	Description
RES	15:0	RO	**Reserved** Write as zero, ignored on read.

MMD Access Control Register

The MMD access control register is used in conjunction with the MMDDATA register to access the MMD register space. Each MMD maintains its own individual address register, as described in IEEE 802.3-2008 clause 45.2.8. The DEVAD field directs any accesses of register MMDDATA to the appropriate MMD as described in IEEE 802.3-2008 clause 45.2. For additional insight into the operation and use of the MMD registers, refer to IEEE 802.3-2008 clause 22.2.4.3.11, Annex 22D and clause 45.2.

MMDCTRL	Offset	Reset Value
MMD Access Control Register	$0D_H$	0000_H



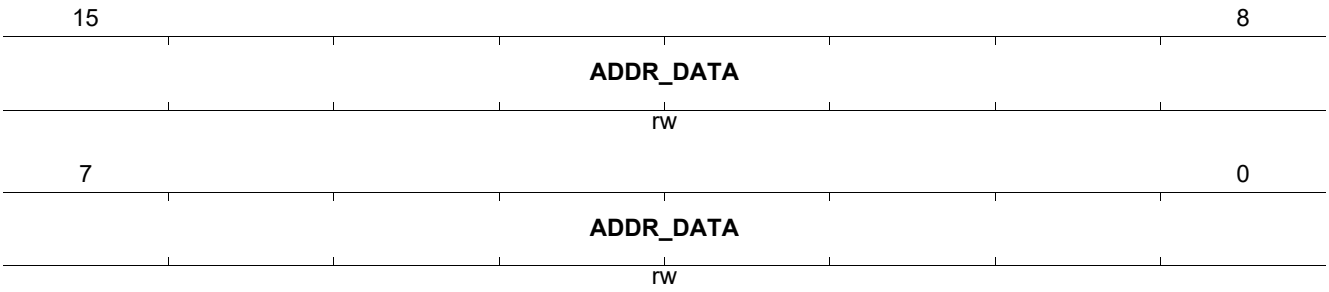
Field	Bits	Type	Description
ACTYPE	15:14	RW	**Access Type Function** When the access of register MMDDATA is an address access (ACTYPE=0) then it is directed to the address register within the MMD associated with the value in the DEVAD field. Otherwise, both the DEVAD field and the MMD's address register direct the register MMDDATA data accesses to the appropriate registers within that MMD. The function field can be set to any of the constants defined (ADDRESS, DATA, DATA_PI, DATA_PIWR). 00_B **ADDRESS** Accesses to register MMDDATA access the MMD individual address register 01_B **DATA** Accesses to register MMDDATA access the register within the MMD selected by the value in the MMD address register 10_B **DATA_PI** Accesses to register MMDDATA access the register within the MMD selected by the value in the MMD address register. After this access is complete, for both read and write accesses, the value in the MMD address field is incremented. 11_B **DATA_PIWR** Accesses to register MMDDATA access the register within the MMD selected by the value in the MMD address register. After this access is complete, for write accesses only, the value in the MMD address field is incremented. For read accesses, the value in the MMD address field is not modified.
RESH	13:8	RO	**Reserved** Write as zero, ignored on read.
RESL	7:5	RO	**Reserved** Write as zero, ignored on read.

Field	Bits	Type	Description
DEVAD	4:0	RW	**Device Address** The DEVAD field directs any accesses of register MMDDATA to the appropriate MMD as described in IEEE 802.3-2008 clause 45.2.

MMD Access Data Register

The MMD access data register is used in conjunction with the MMD access control (MMDCTRL) register to access the MMD register space. For more information on MMD access, refer to IEEE 802.3-2008 clause 22.2.4.3.12, clause 45.2 and Annex 22D.

MMDDATA	Offset	Reset Value
MMD Access Data Register	$0E_H$	0000_H

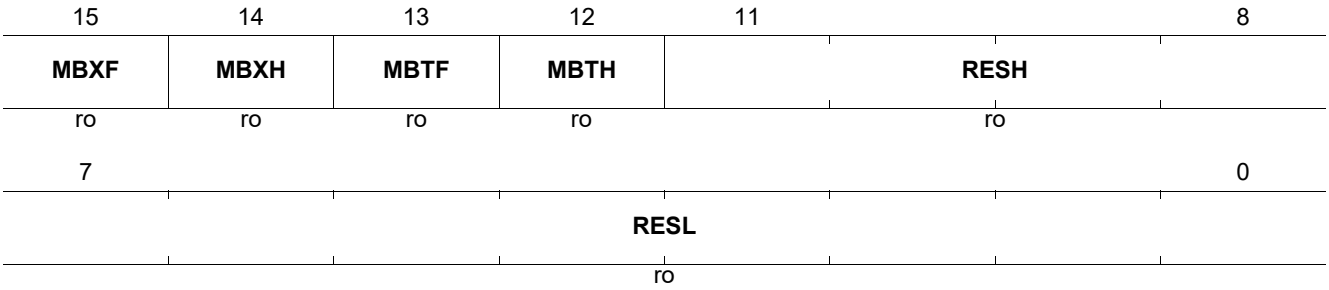


Field	Bits	Type	Description
ADDR_DATA	15:0	RW	**Address or Data Register** This register accesses either a specific MMD address register or the data content of the MMD register to which this address register points. Which of the functions is currently valid is defined by the MMDCTRL register.

Extended Status Register

This register contains extended status and capability information about the PHY. All bits are read-only. A write access does not have any effect.

XSTAT	Offset	Reset Value
Extended Status Register	$0F_H$	3000_H



Field	Bits	Type	Description
MBXF	15	RO	**1000BASE-X Full-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-X full-duplex. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
MBXH	14	RO	**1000BASE-X Half-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-X half-duplex. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
MBTF	13	RO	**1000BASE-T Full-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-T full-duplex. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
MBTH	12	RO	**1000BASE-T Half-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-T full-duplex. 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
RESH	11:8	RO	**Reserved** Ignore when read.
RESL	7:0	RO	**Reserved** Ignore when read.

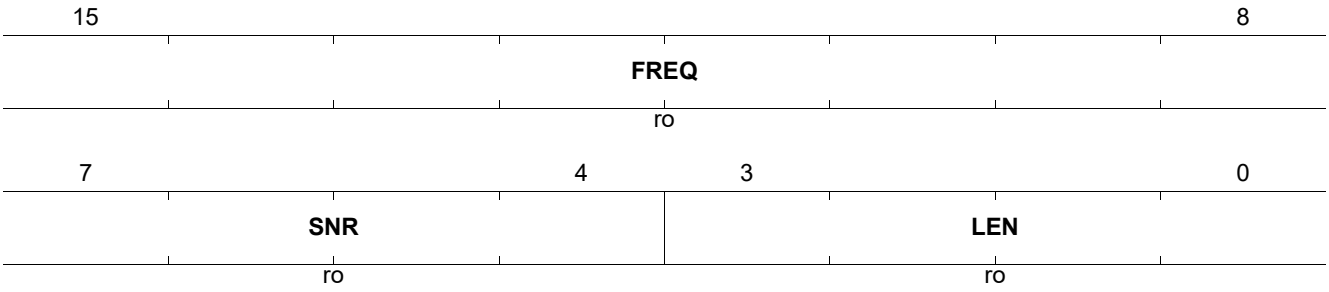
4.3.2 PHY: PHY-Specific Management Registers

This section describes the PHY-specific management registers.

Physical Layer Performance Status

This register reports the PHY performance in the current mode of operation. The content of this register is only valid when the link is up.

PHYPERF	Offset	Reset Value
Physical Layer Performance Status	10_H	$80FF_H$

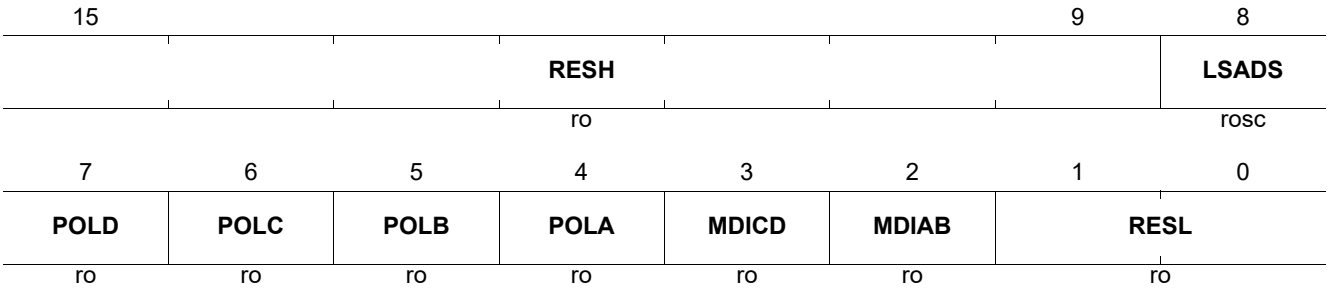


Field	Bits	Type	Description
FREQ	15:8	RO	**Frequency Offset of Link-Partner [ppm]** This register fields reports the measured frequency offset of the receiver in ppm as a signed 2's complement number. A value of -128 (0x80) indicates an invalid number.
SNR	7:4	RO	**Receive SNR Margin [dB]** This register field reports the measured SNR margin of the receiver in dB. The value saturates at a 14-dB SNR margin for very short links and 0 dB for very long links. A value of 15 indicates an invalid number. 1111_B**INVALID** Invalid value
LEN	3:0	RO	**Estimated Loop Length (Valid During Link-Up)** This register field reports the estimated loop length compared to a virtually ideal CAT5e straight cable. The unit is LEN x 10m. A value of 15 indicates an invalid number.

Physical Layer Status 1

This register reports PHY lock information, for example link-up, polarity reversals and port mapping. The content of this register is only valid when the link is up.

PHYSTAT1	Offset	Reset Value
Physical Layer Status 1	11_H	0000_H



Field	Bits	Type	Description
RESH	15:9	RO	**Reserved** Write as zero, ignored on read.
LSADS	8	ROSC	**Link-Speed Auto-Downspeed Status** Monitors the status of the link speed auto-downspeed controlled in PHYCTL1.LDADS 0_B **NORMAL** Did not perform any link speed auto-downspeed 1_B **DETECTED** Detected an auto-downspeed
POLD	7	RO	**Receive Polarity Inversion Status on Port D** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion detected
POLC	6	RO	**Receive Polarity Inversion Status on Port C** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion detected
POLB	5	RO	**Receive Polarity Inversion Status on Port B** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion detected
POLA	4	RO	**Receive Polarity Inversion Status on Port A** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion detected
MDICD	3	RO	**Mapping of MDI Ports C and D** 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode
MDIAB	2	RO	**Mapping of MDI Ports A and B** 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode
RESL	1:0	RO	**Reserved** Write as zero, ignored on read.

Physical Layer Status 2

This register reports PHY lock information, for example, pair skews in the GbE mode. The content of this register is only valid when the link is up.

PHYSTAT2	Offset	Reset Value
Physical Layer Status 2	12_H	0000_H

15	14	12	11	10	8
RESD	SKEWD		RESC	SKEWC	
ro	ro		ro	ro	

7	6	4	3	2	0
RESB	SKEWB		RESA	SKEWA	
ro	ro		ro	ro	

Field	Bits	Type	Description
RESD	15	RO	**Reserved** Write as zero, ignored on read.
SKEWD	14:12	RO	**Receive Skew on Port D** The skew is reported as an unsigned number of symbol periods.
RESC	11	RO	**Reserved** Write as zero, ignored on read.
SKEWC	10:8	RO	**Receive Skew on Port C** The skew is reported as an unsigned number of symbol periods.
RESB	7	RO	**Reserved** Write as zero, ignored on read.
SKEWB	6:4	RO	**Receive Skew on Port B** The skew is reported as an unsigned number of symbol periods.
RESA	3	RO	**Reserved** Write as zero, ignored on read.
SKEWA	2:0	RO	**Receive Skew on Port A** The skew is reported as an unsigned number of symbol periods.

Physical Layer Control 1

This register controls the PHY functions.

PHYCTL1	Offset	Reset Value
Physical Layer Control 1	13_H	0003_H

15	14	13	12	11	10	9	8
TLOOP			TXOFF	TXADJ			
rw			rw	rw			

7	6	5	4	3	2	1	0
POLD	POLC	POLB	POLA	MDICD	MDIAB	TXEEE10	AMDIX
rw	rw	rw	rw	rw	rw	ro	rw

Field	Bits	Type	Description
TLOOP	15:13	RW	**Test Loop** Configures predefined test loops. 000_B **OFF** Test loops are switched off - normal operation. 001_B **NETL** Near-end test loop 010_B **FETL** Far-end test loop 011_B **ECHO** Echo test loop 100_B **RJTL** RL45 connector test loop 101_B **FETLS** Standalone Far-end test loop. No dependency on TX_CLK and RX_CLK on the (G)MII interface
TXOFF	12	RW	**Transmitter Off** This register bit allows turning off of the transmitter. This feature might be useful for return loss measurements. 0_B **ON** Transmitter is on 1_B **OFF** Transmitter is off
TXADJ	11:8	RW	**Transmit Level Adjustment** Transmit-level adjustment can be used to fine tune the transmit amplitude of the PHY. The amplitude adjustment is valid for all supported speed modes. The adjustment is performed in digits. One digit represents 3.125 percent of the nominal amplitude. The scaling factor is gain = 1 + signed(TXADJ)*2^-7.
POLD	7	RW	**Transmit Polarity Inversion Status on Port D** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion
POLC	6	RW	**Transmit Polarity Inversion Status on Port C** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion
POLB	5	RW	**Transmit Polarity Inversion Control on Port B** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion

Field	Bits	Type	Description
POLA	4	RW	**Transmit Polarity Inversion Control on Port A** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion
MDICD	3	RW	**Mapping of MDI Ports C and D** 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode
MDIAB	2	RW	**Mapping of MDI Ports A and B** 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode
TXEEE10	1	RO	**Transmit Energy-Efficient Ethernet 10BASE-Te Amplitude** This register bit allows enabling of the 10BASE-Te energy-efficient mode transmitting only with a 1.75 V nominal amplitude. 0_B **DISABLED** Transmit the 10Base-T amplitude, that is, 2.3 V 1_B **ENABLED** Transmit the 10BASE-Te amplitude, that is, 1.75 V
AMDIX	0	RW	**PHY Performs Auto-MDI/MDI-X or Uses Manual MDI/MDI-X** 0_B **MANUAL** PHY uses manual MDI/MDI-X 1_B **AUTO** PHY performs Auto-MDI/MDI-X

Physical Layer Control 2

This register controls the PHY functions.

PHYCTL2 **Offset** **Reset Value**

Physical Layer Control 2 **14_H** **8006_H**

15	14	13	9	8
LSADS		**RESH**		**STICKY**
rw		ro		rw

7	5	4	3	2	1	0
RESL		**ADCR**		**PSCL**	**ANPD**	**Res**
ro		rw		rw	rw	

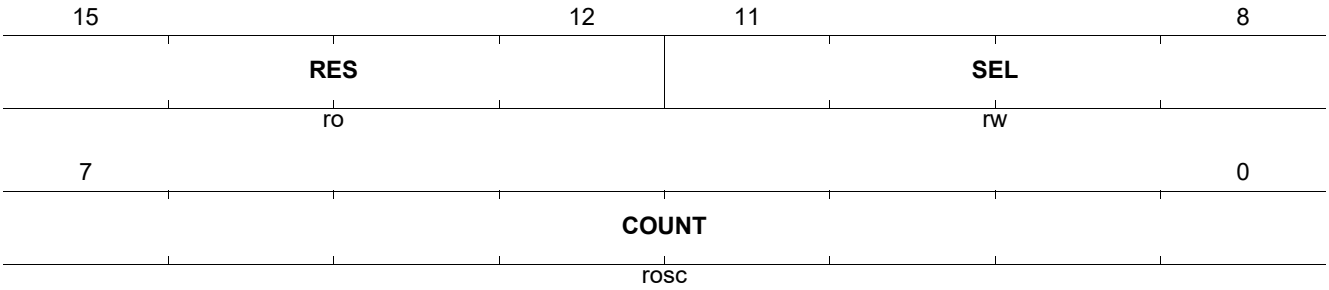
Field	Bits	Type	Description
LSADS	15:14	RW	**Link Speed Auto-Downspeed Control Register** Link speed auto-downspeed is a functionality which allows an Ethernet link to be established even in non-standard harsh cable environments. **Constants applicable for GSW140A3MC, GSW140A3LC devices** 00_B **ADS1** Do not perform auto-downspeed of link speed 01_B **ADS2** Perform auto-downspeed of link speed after 4 consecutive failed link-ups. 10_B **ADS3** Perform auto-downspeed of link speed after 6 consecutive failed link-ups. 11_B **ADS4** Perform auto-downspeed of link speed after 8 consecutive failed link-ups.

Field	Bits	Type	Description
RESH	13:9	RO	**Reserved** Write as zero, ignored on read.
STICKY	8	RW	**Sticky-Bit Handling** Allows enabling/disabling of the sticky-bit handling for all PHY-specific MDIO register bits of type RW, except for the TPGCTRL register. This means that the current content of these registers is left untouched during a software reset when sticky-bit handling is enabled. 0_B **OFF** Sticky-bit handling is disabled 1_B **ON** Sticky-bit handling is enabled
RESL	7:5	RO	**Reserved** Write as zero, ignored on read.
ADCR	4:3	RW	**ADC Resolution Boost** Allows for the ADC resolution to be increased. 00_B **DEFAULT** Default ADC resolution. 01_B **BOOST** ADC resolution boost.
PSCL	2	RW	**Power-Consumption Scaling Depending on Link Quality** Allows enabling/disabling of the power-consumption scaling dependent on the link quality. 0_B **OFF** PSCL is disabled 1_B **ON** PSCL is enabled
ANPD	1	RW	**Auto-Negotiation Power Down** Allows enabling/disabling of the power-down modes during auto-negotiation looking for a link partner. 0_B **OFF** ANPD is disabled 1_B **ON** ANPD is enabled

Error Counter

This register controls the error counter. It allows the number of errors detected in the PHY to be counted for monitoring purposes.

ERRCNT	Offset	Reset Value
Error Counter	15_H	0000_H

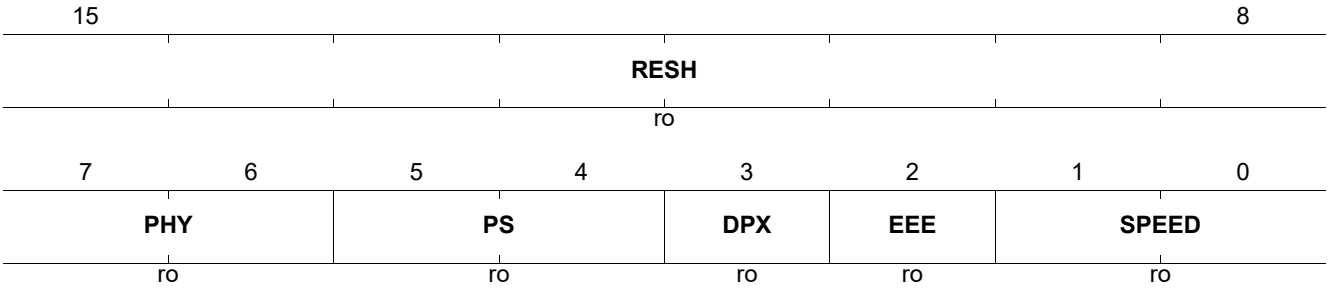


Field	Bits	Type	Description
RES	15:12	RO	**Reserved** Write as zero, ignored on read.
SEL	11:8	RW	**Select Error Event** Configures the error/event to which the error counter is sensitive. 0000_B**RXERR** Receive errors are counted 0001_B**RXACT** Receive frames are counted 0010_B**ESDERR** ESD errors are counted 0011_B**SSDERR** SSD errors are counted 0100_B**TXERR** Transmit errors are counted 0101_B**TXACT** Transmit frames events get counted 0110_B**COL** Collision events get counted 1000_B**NLD** Number of Link Down get counted 1001_B**NDS** Number of auto-downspeed get counted
COUNT	7:0	ROSC	**Counter State** This counter state is updated each time the selected error event has been detected. The counter state is reset every time a read operation on this register is performed or the error event is changed. The counter saturates at value 0xFF.

Media-Independent Interface Status

This register contains status information of the MII interface.

MIISTAT	Offset	Reset Value
Media-Independent Interface Status	18_H	0000_H



Field	Bits	Type	Description
RESH	15:8	RO	**Reserved** Write as zero, ignored on read.
PHY	7:6	RO	**Active PHY Interface** 00_B **TP** The twisted-pair interface is the active PHY interface 01_B **FIBER** The fiber interface is the active PHY interface 10_B **MII2** The second MII interface is the active PHY interface 11_B **SGMII** The SGMII interface is the active PHY interface
PS	5:4	RO	**Resolved Pause Status for Flow Control** 00_B **NONE** No PAUSE 01_B **TX** Transmit PAUSE 10_B **RX** Receive PAUSE 11_B **TXRX** Both transmit and receive PAUSE
DPX	3	RO	**Duplex mode at which the MII currently operates.** 0_B **HDX** Half duplex 1_B **FDX** Full duplex
EEE	2	RO	**Resolved Energy-Efficient Ethernet Mode** 0_B **OFF** EEE is disabled after auto-negotiation resolution 1_B **ON** EEE is enabled after auto-negotiation resolution
SPEED	1:0	RO	**PHY Speed at which the MII Currently Operates.** 00_B **TEN** 10 Mbps 01_B **FAST** 100 Mbps 10_B **GIGA** 1000 Mbps 11_B **FRE** FRE mode

Interrupt Mask Register

This register defines the mask for the Interrupt Status Register (ISTAT). Each masked interrupt is able to activate the MDINT pin to the management device. The information about the interrupt source can be extracted by reading the ISTAT register. A read operation on the ISTAT register simultaneously clears the interrupts, deactivating MDINT.

IMASK	Offset	Reset Value
Interrupt Mask Register	19_H	0000_H

15	14	13	12	11	10	9	8
WOL	MSRE	NPRX	NPTX	ANE	ANC	AMBF	LOR
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
RESL		ADSC	MDIPC	MDIXC	DXMC	LSPC	LSTC
ro		rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
WOL	15	RW	**Wake-On-LAN Event Mask** When active and masked in IMASK, the MDINT is activated upon detection of a valid Wake-On-LAN event. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MSRE	14	RW	**Master/Slave Resolution Error Mask** When active, MDINT is activated upon detection of a master/slave resolution error during a 1000BASE-T auto-negotiation. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
NPRX	13	RW	**Next Page Received Mask** When active, MDINT is activated upon reception of a next page in STD.AN_NPRX. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
NPTX	12	RW	**Next Page Transmitted Mask** When active, MDINT is activated upon transmission of the currently stored next page in STD.AN_NPTX. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
ANE	11	RW	**Auto-Negotiation Error Mask** When active, MDINT is activated upon detection of an auto-negotiation error. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

Field	Bits	Type	Description
ANC	10	RW	**Auto-Negotiation Complete Mask** When active, MDINT is activated upon completion of the auto-negotiation process. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
AMBF	9	RW	**MDIO Handling Fault** When active, MDINT is activated upon detection that the MDIO handling FIFO has overflowed and as such flushed and init by FW. This must indicate that one or more of the MDIO transactions before this event may be lost. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LOR	8	RW	**SyncE Lost Of Reference** When active, MDINT is activated upon detection that the SyncE reference clock is lost. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
RESL	7:6	RO	**Reserved** Write as zeros, ignore on read.
ADSC	5	RW	**Link-Speed Auto-Downspeed Detect Mask** When active, MDINT is activated upon detection of a link speed auto-downspeed event. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MDIPC	4	RW	**MDI Polarity Change Detect Mask** When active, MDINT is activated upon detection of an MDI polarity change event. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MDIXC	3	RW	**MDIX Change Detect Mask** When active, MDINT is activated upon detection of an MDI/MDIX cross-over change event. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
DXMC	2	RW	**Duplex Mode Change Mask** When active, MDINT is activated upon detection of full- or half-duplex change. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LSPC	1	RW	**Link Speed Change Mask** When active, MDINT is activated upon detection of link speed change. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LSTC	0	RW	**Link State Change Mask** When active, MDINT is activated upon detection of link status change. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

Interrupt Status Register

This register defines the Interrupt Status Register (ISTAT). Each masked interrupt (IMASK) is able to activate the MDINT pin to the management device. The information about the interrupt source can be extracted by reading the ISTA register. A read operation on the ISTAT register simultaneously clears the interrupts and this deactivates MDINT.

ISTAT	Offset	Reset Value
Interrupt Status Register	$1A_H$	0000_H

15	14	13	12	11	10	9	8
WOL	MSRE	NPRX	NPTX	ANE	ANC	AMBF	LOR
rolh	rolh	rolh	rolh	rolh	rolh	rw	rolh

7	6	5	4	3	2	1	0
RESL		ADSC	MDIPC	MDIXC	DXMC	LSPC	LSTC
rolh		rolh	rolh	rolh	rolh	rolh	rolh

Field	Bits	Type	Description
WOL	15	ROLH	**Wake-On-LAN Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of a valid Wake-On-LAN event. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MSRE	14	ROLH	**Master/Slave Resolution Error Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of a master/slave resolution error during a 1000BASE-T auto-negotiation. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
NPRX	13	ROLH	**Next Page Received Interrupt Status** When active and masked in IMASK, the MDINT is activated upon reception of a next page in STD.AN_NPRX. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
NPTX	12	ROLH	**Next Page Transmitted Interrupt Status** When active and masked in IMASK, the MDINT is activated upon transmission of the currently stored next page in STD.AN_NPTX. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
ANE	11	ROLH	**Auto-Negotiation Error Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of an auto-negotiation error. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

Field	Bits	Type	Description
ANC	10	ROLH	**Auto-Negotiation Complete Interrupt Status** When active and masked in IMASK, the MDINT is activated upon completion of the auto-negotiation process. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
AMBF	9	RW	**MDIO Handling Fault** When active and masked in IMASK, MDINT is activated upon detection that the MDIO handling FIFO has overflowed and as such flushed and init by FW. This must indicate that one or more of the MDIO transactions before this event may be lost. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LOR	8	ROLH	**SyncE Lost Of Reference** When active and masked in IMASK, MDINT is activated upon detection that the SyncE reference clock is lost. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
RESL	7:6	ROLH	**Reserved** Write as zeros, ignore on read.
ADSC	5	ROLH	**Link Speed Auto-Downspeed Detect Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of a link speed auto-downspeed event. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MDIPC	4	ROLH	**MDI Polarity Change Detect Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of an MDI polarity change event. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MDIXC	3	ROLH	**MDIX Change Detect Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of an MDI/MDIX cross-over change event. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
DXMC	2	ROLH	**Duplex Mode Change Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of a full or half-duplex change. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LSPC	1	ROLH	**Link Speed Change Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of link speed change. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

Field	Bits	Type	Description
LSTC	0	ROLH	**Link State Change Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of link status change. 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

LED Control Register

This register contains control bits to allow for direct access to the LEDs. A directly controlled LED must disable the integrated LED function as specified by the more sophisticated LED control registers in page LED.

LED	Offset	Reset Value
LED Control Register	$1B_H$	$0F00_H$

15	14	13	12	11	10	9	8
RESH				LED3EN	LED2EN	LED1EN	LED0EN
ro				rw	rw	rw	rw

7	6	5	4	3	2	1	0
RESL				LED3DA	LED2DA	LED1DA	LED0DA
ro				rw	rw	rw	rw

Field	Bits	Type	Description
RESH	15:12	RO	**Reserved** Write as zero, ignored on read.
LED3EN	11	RW	**Enable the integrated function of LED3** Write a logic 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED3DA. 0_B **DISABLE** Disables the integrated LED function 1_B **ENABLE** Enables the integrated LED function
LED2EN	10	RW	**Enable the integrated function of LED2** Write a logic 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED2DA. 0_B **DISABLE** Disables the integrated LED function 1_B **ENABLE** Enables the integrated LED function
LED1EN	9	RW	**Enable the Integrated Function of LED1** Write a logic 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED1DA. 0_B **DISABLE** Disables the integrated LED function 1_B **ENABLE** Enables the integrated LED function
LED0EN	8	RW	**Enable the Integrated Function of LED0** Write a logic 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED0DA. 0_B **DISABLE** Disables the integrated LED function 1_B **ENABLE** Enables the integrated LED function

Field	Bits	Type	Description
RESL	7:4	RO	**Reserved** Write as zero, ignored on read.
LED3DA	3	RW	**Direct Access to LED3** Write a logic 1 to this bit to illuminate the LED. LED3EN must be set to logic zero. 0_B **OFF** Switch off the LED 1_B **ON** Switch on the LED
LED2DA	2	RW	**Direct Access to LED2** Write a logic 1 to this bit to illuminate the LED. LED2EN must be set to logic zero. 0_B **OFF** Switch off the LED 1_B **ON** Switch on the LED
LED1DA	1	RW	**Direct Access to LED1** Write a logic 1 to this bit to illuminate the LED. LED1EN must be set to logic zero. 0_B **OFF** Switch off the LED 1_B **ON** Switch on the LED
LED0DA	0	RW	**Direct Access to LED0** Write a logic 1 to this bit to illuminate the LED. LED0EN must be set to logic zero. 0_B **OFF** Switch off the LED 1_B **ON** Switch on the LED

Test-Packet Generator Control

This register controls the operation of the integrated Test-Packet Generator (TPG). This module is only used for testing purposes.

TPGCTRL	Offset	Reset Value
Test-Packet Generator Control	$1C_H$	0000_H

15	14	13	12	11	10	9	8
CHSEL		MODE	BURST4EN	IPGL		TYPE	
rw		rw	rw	rw		rw	

7	6		4	3	2	1	0
RESL1	SIZE			MOPT		START	EN
ro	rw			rw		rw	rw

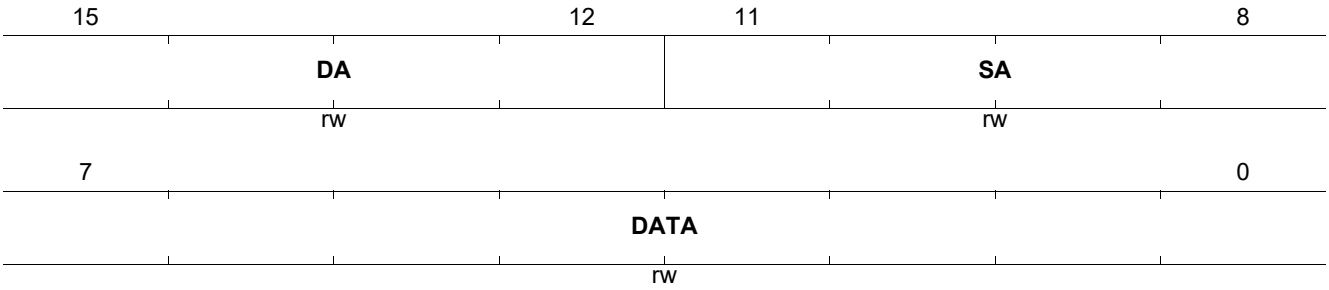
Field	Bits	Type	Description
CHSEL	15:14	RW	**Channel Selection** There are 4 channels in the IP which can be selected for debug data dumping. This field is not used in case BURST4EN=1 && MOPT=1 (auto-channel burst). 00_B **CHA** Channel A is selected 01_B **CHB** Channel B is selected 10_B **CHC** Channel C is selected 11_B **CHD** Channel D is selected
MODE	13	RW	**TPG Mode** Configures the packet generation mode . 0_B **CONTINUOUS** Send packets continuously 1_B **SINGLE** Send a single packet. Also used to send a single burst of 4 packets in debug dumping when selected.
BURST4EN	12	RW	**Burst of 4 Packets Enable** When Enabled, this indicates to the packet generator to auto-select based on MOPT the debug data configuration per packet in the burst of 4. When MOPT=0, then the packets are generated capturing for the selected ASP channel, the polyphases 0,1,2,3 respectively. When MOPT=1, then the packets are generated capturing for the selected DVC option, the channels A,B,C,D respectively. This leads to a burst of 4 packets when MODE=SINGLE. In case MODE=1(continuous), then we get packets where every group of 4 packets are generated according to the MOPT selection. 0_B **DISABLE** Disable 1_B **ENABLE** Enable burst of 4 packet generation
IPGL	11:10	RW	**Inter-Packet Gap Length** Configures the length of the inter-packet gap in bit times. 00_B **BT48** Length is 48 bit times 01_B **BT96** Length is 96 bit times 10_B **BT960** Length is 960 bit times 11_B **BT9600** Length is 9600 bit times
TYPE	9:8	RW	**Packet Data Type** Configures the packet data type to be either predefined, byte increment or random. When predefined, the content of the register TPGDATA is used repetitively. 00_B **RANDOM** Use random data as the packet content 01_B **BYTEINC** Use byte increment as the packet content 10_B **PREDEF** Use pre-defined content of the register TPGDATA 11_B **DBGDATA** Use Dbg data as packet content. Additional Configuration is taken from TPGDATA
RESL1	7	RO	**Reserved** Write as zero, ignore on read.

Field	Bits	Type	Description
SIZE	6:4	RW	**Packet Size** Configures the size of the generated Ethernet packets in bytes. The size includes DA, SA, length/type, payload and FCS. 000_B **L64** Packet length is 64 bytes. 001_B **L2048** Packet length is 2048 bytes (jumbo frames). 010_B **L256** Packet length is 256 bytes. 011_B **L4096** Packet length is 4096 bytes (jumbo frames). 100_B **L1024** Packet length is 1024 bytes. 101_B **L1518** Packet length is 1518 bytes. 110_B **L9000** Packet length is 9000 bytes (jumbo frames). 111_B **RANDOM** Packet length is randomized between upper sizes without jumbo frames.
MOPT	3:2	RW	**Mux Option** Additional Mux Selection Options depending on the value of DVC in TPGDATA[3:0]. 00_B **MOPT0** BURST4EN=1: auto-polyphase selected, BURST4EN=0 && DVC=0b1001: DBG SYNC Data Gen, otherwise sub-DVC-mode selection 01_B **MOPT1** BURST4EN=1: auto-channel selected, BURST4EN=0 && DVC=0b1001: DBG Trace Data, otherwise sub-DVC-mode selection 10_B **MOPT2** sub-DVC-mode selection 11_B **MOPT3** sub-DVC-mode selection
START	1	RW	**Start or Stop TPG Data Generation.** Starts the TPG data generation. Depending on the MODE, the TPG sends only 1 single packet or chunks of 10,000 packets until stopped. 0_B **STOP** Stops the TPG data generation 1_B **START** Starts the TPG data generation
EN	0	RW	**Enable the TPG** Enables the TPG for data generation. 0_B **DISABLE** Disables the TPG 1_B **ENABLE** Enables the TPG

Test-Packet Generator Data

Specifies the payload data to be used when sending a non-random data packet. All payload data bytes are sent with this value.

TPGDATA	Offset	Reset Value
Test-Packet Generator Data	$1D_H$	$00AA_H$

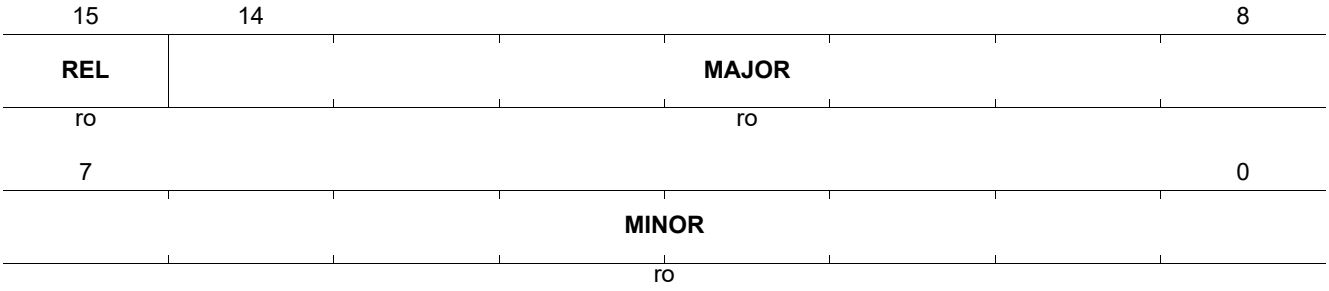


Field	Bits	Type	Description
DA	15:12	RW	**Destination Address** Configures the destination address nibble. The Source Address builds up to 00-03-19-FF-FF-F[DA].
SA	11:8	RW	**Source Address** Configures the source address nibble. The source address builds up to 00-03-19-FF-FF-F[SA].
DATA	7:0	RW	**Data Byte to be Transmitted** This is the content of the payload bytes in the frame in case it is selected to send constant data. When it is selected to send debug data, this byte has additional configuration as seen in the constants listed here. The bit masks are listed here. Refer to the related section for more details on the configuration. 00001111_B**DVC** Select the debug data to be dump 00010000_B**RESERVED** Reserved 01100000_B**PREC2** For reduce precision, select the options with bits [6:5] 10000000_B**PREC** select whether to take full precision('1') of reduce precision '0' at bit 7

Firmware Version Register

This register contains the version of the PHY firmware.

FWV	Offset	Reset Value
Firmware Version Register	**$1E_H$**	**8304_H**

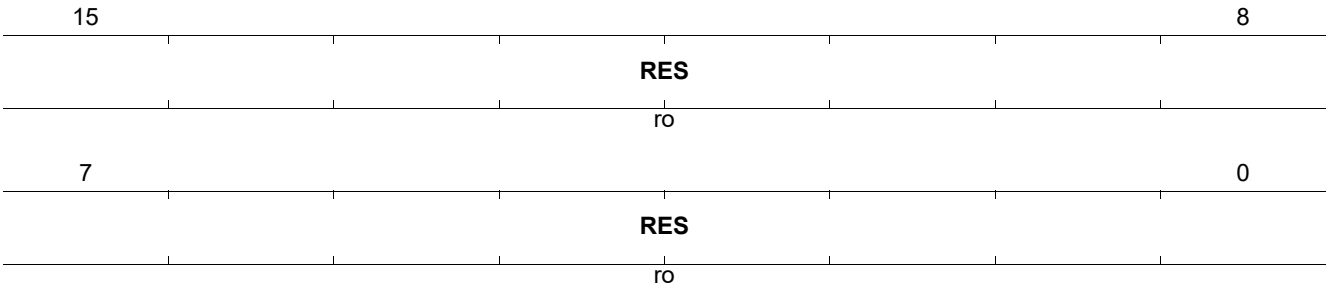


Field	Bits	Type	Description
REL	15	RO	**Release Indication** This parameter indicates either a test or a release version. 0_B **TEST** Indicates a test version 1_B **RELEASE** Indicates a released version
MAJOR	14:8	RO	**Major Version Number** Specifies the main version release number of the firmware.
MINOR	7:0	RO	**Minor Version Number** Specifies the sub-version release number of the firmware.

Reserved

Reserved.

RES1F	Offset	Reset Value
Reserved	**$1F_H$**	**0000_H**



Field	Bits	Type	Description
RES	15:0	RO	**Reserved** Write as zero, ignored on read.

4.4 PHY MMD Registers

This section defines all the registers required to operate the MMD_REGISTERS module.[1)]

Table 62 Registers Address Space

Module	Base Address	End Address	Note
MMD_REGISTERS	000000_H	$1FFFFF_H$	

Table 63 Registers Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
PHY MMD Registers, PMAPMD: Standard PMAPMD Registers for MMD=0x01			
TIMESYNC_CAP	PMAPMD TimeSync Capability Indication	01.1800_H	0000_H
PHY MMD Registers, EEE: Standard EEE Registers for MMD=0x03			
EEE_CTRL1	EEE Control Register 1	03.0000_H	0000_H
EEE_STAT1	EEE Status Register 1	03.0001_H	0000_H
EEE_CAP	EEE Capability Register	03.0014_H	0006_H
EEE_WAKERR	EEE Status Register 1	03.0016_H	0000_H
PHY MMD Registers, ANEG: Standard Auto-Negotiation Registers for MMD=0x07			
EEE_AN_ADV	EEE Auto-Negotiation Advertisement Register	$07.003C_H$	0000_H
EEE_AN_LPADV	EEE Auto-Negotiation Link-Partner Advertisement Register	$07.003D_H$	0000_H
PHY MMD Registers, INTERNAL: Internal Address Space (MMD=0x1F)			
LEDCH	LED Configuration	$1F.01E0_H$	$00C5_H$
LEDCL	LED Configuration	$1F.01E1_H$	0067_H
LED0H	Configuration for LED Pin 0	$1F.01E2_H$	0070_H
LED1H	Configuration for LED Pin 1	$1F.01E4_H$	0020_H
LED2H	Configuration for LED Pin 2	$1F.01E6_H$	0040_H
LED3H	Configuration for LED Pin 3	$1F.01E8_H$	0040_H
LED0L	Configuration for LED Pin 0	$1F.01E3_H$	0003_H
LED1L	Configuration for LED Pin 1	$1F.01E5_H$	0000_H
LED2L	Configuration for LED Pin 2	$1F.01E7_H$	0000_H
LED3L	Configuration for LED Pin 3	$1F.01E9_H$	0020_H
EEE_RXERR_LINK_FAIL_H	High Byte of the EEE Link-Fail Counter	$1F.01EA_H$	0000_H
EEE_RXERR_LINK_FAIL_L	Low Byte of the EEE Link-Fail Counter	$1F.01EB_H$	0000_H
WOLCTRL	Wake-On-LAN Control Register	$1F.0781_H$	0000_H
WOLAD0	Wake-On-LAN Address Byte 0	$1F.0783_H$	0000_H
WOLAD1	Wake-On-LAN Address Byte 1	$1F.0784_H$	0000_H
WOLAD2	Wake-On-LAN Address Byte 2	$1F.0785_H$	0000_H

1) Generated by REFIGE v1.4 - Beta Release XIV

Table 63 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
WOLAD3	Wake-On-LAN Address Byte 3	$1F.0786_H$	0000_H
WOLAD4	Wake-On-LAN Address Byte 4	$1F.0787_H$	0000_H
WOLAD5	Wake-On-LAN Address Byte 5	$1F.0788_H$	0000_H
WOLPW0	Wake-On-LAN SecureON Password Byte 0	$1F.0789_H$	0000_H
WOLPW1	Wake-On-LAN SecureON Password Byte 1	$1F.078A_H$	0000_H
WOLPW2	Wake-On-LAN SecureON Password Byte 2	$1F.078B_H$	0000_H
WOLPW3	Wake-On-LAN SecureON Password Byte 3	$1F.078C_H$	0000_H
WOLPW4	Wake-On-LAN SecureON Password Byte 4	$1F.078D_H$	0000_H
WOLPW5	Wake-On-LAN SecureON Password Byte 5	$1F.078E_H$	0000_H
PD_CTL	Configuration for Synchronous Ethernet	$1F.07FE_H$	0000_H

The register is addressed wordwise.

Table 64 Register Access Types

Mode	Symbol	Internal Hardware Configuration		
		Type	Behavior	Arbitration
Status Register, Latch-High	ROLH	WOR	AUTO_PDI	CLROR
Status Register, Latch-Low	ROLL	WOR	AUTO_PDI	CLROR
Status Register, Self-Clearing	ROSC	WOR	AUTO_PDI	CLROR
Read-Write Register	RW	RWR	AUTO_PDI	-
Read-Write Register, Self-Clearing	RWSC	RWR	AUTO_PDI	CLROR
Status Register	RO	WOR	AUTO_PDI	-

4.4.1 PMAPMD: Standard PMAPMD Registers for MMD=0x01

This section describe the registers for support of IEEE 802.3BF indication for TimeSync (a.k.a SyncT interface in this IP).

PMAPMD TimeSync Capability Indication

PMAPMD TimeSync Capability indication Register. This IP does not support providing data path delay information. It is provided to enhance compatibility

TIMESYNC_CAP	Offset	Reset Value
PMAPMD TimeSync Capability Indication	01.1800_H	0000_H

Field	Bits	Type	Description
TXDEL	1	RO	**Transmit Data Path Delay Information** PHY indicates whether it is capable of providing the minimum and maximum data path delay information. 0_B **NONE** PHY do not have this capability 1_B **CAPABLE** min and max TX data path delay available
RXDEL	0	RO	**Receive Data Path Delay Information** PHY indicates whether it is capable of providing the minimum and maximum data path delay information. 0_B **NONE** PHY do not have this capability 1_B **CAPABLE** min and max RX data path delay available

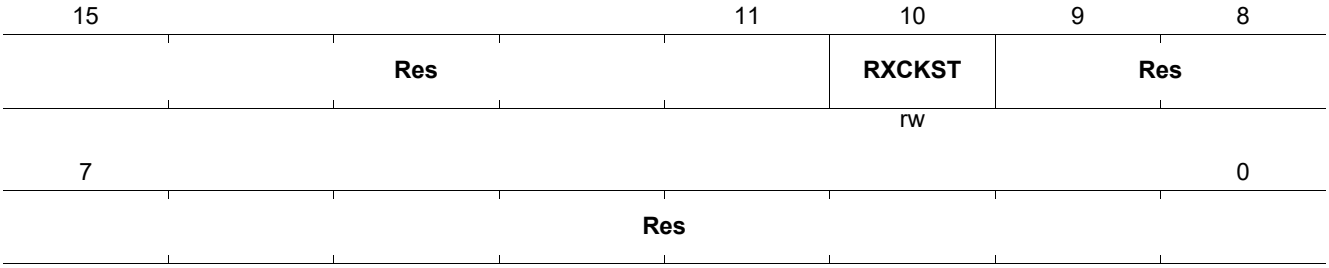
4.4.2 EEE: Standard EEE Registers for MMD=0x03

This section describes the EEE registers for MMD device 0x03.

EEE Control Register 1

EEE Control Register 1.

EEE_CTRL1	Offset	Reset Value
EEE Control Register 1	03.0000_H	0000_H

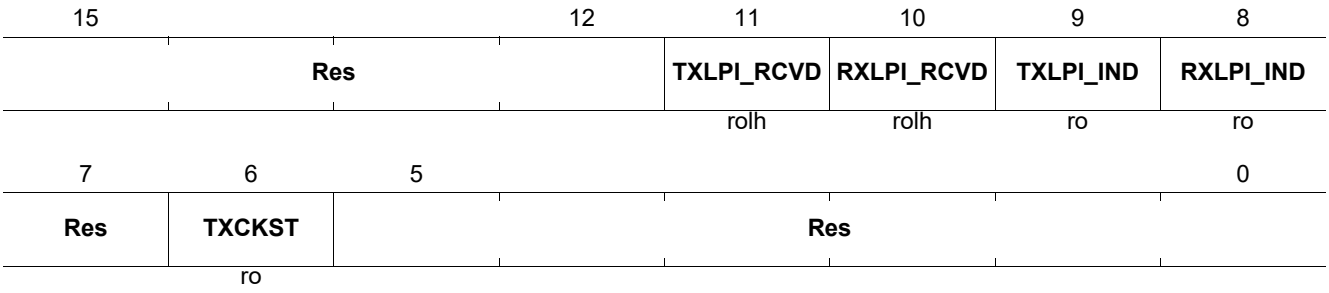


Field	Bits	Type	Description
RXCKST	10	RW	**Receive Clock Stoppable** The MAC can set this bit to active to allow the PHY to stop the clocking during the LPI_MODE. 0_B **DISABLE** The PHY must not stop the xMII clock during LPI_MODE 1_B **ENABLE** The PHY can stop the xMII clock during LPI_MODE

EEE Status Register 1

EEE Status Register 1.

EEE_STAT1	Offset	Reset Value
EEE Status Register 1	03.0001_H	0000_H



Field	Bits	Type	Description
TXLPI_RCVD	11	ROLH	**TXLPI Received** 0_B **INACTIVE** LPI has not been received 1_B **ACTIVE** LPI has been received

Field	Bits	Type	Description
RXLPI_RCVD	10	ROLH	**RXLPI Received** 0_B **INACTIVE** LPI has not been received 1_B **ACTIVE** LPI has been received
TXLPI_IND	9	RO	**TXLPI Indication** 0_B **INACTIVE** LPI is currently inactive 1_B **ACTIVE** LPI is currently active
RXLPI_IND	8	RO	**RXLPI Indication** 0_B **INACTIVE** LPI is currently inactive 1_B **ACTIVE** LPI is currently active
TXCKST	6	RO	**Transmit Clock Stoppable** Indicate whether PHY is able to accept a stopped transmit clock during LPI_MODE. MAC may choose to stop the clocking during LPI_MODE when this bit is set to active. 0_B **DISABLE** The PHY is not able to accept stopped transmit clocks (default) 1_B **ENABLE** The PHY is able to accept a stopped transmit clock during LPI_MODE

EEE Capability Register

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type.

EEE_CAP	Offset	Reset Value
EEE Capability Register	03.0014_H	0006_H

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res	EEE_10GBKR	EEE_10GBKX4	EEE_1000BKX	EEE_10GBT	EEE_1000BT	EEE_100BTX	Res
r	ro	ro	ro	ro	ro	ro	r

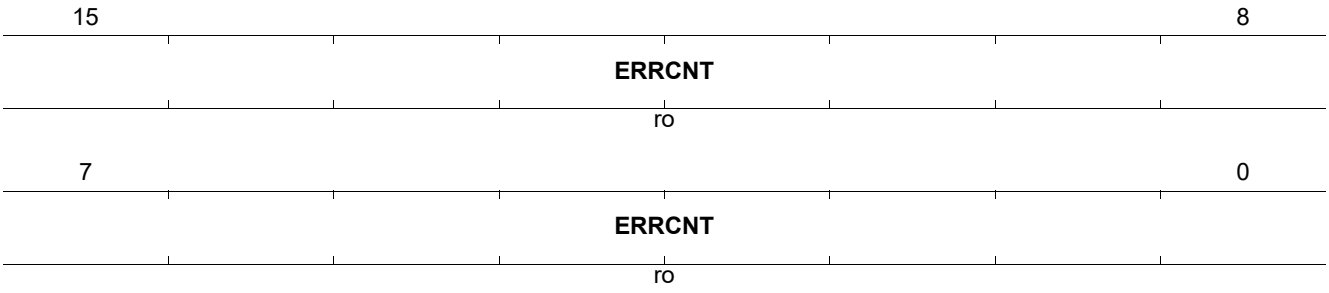
Field	Bits	Type	Description
EEE_10GBKR	6	RO	**Support of 10GBASE-KR EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBKX4	5	RO	**Support of 10GBASE-KX4 EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BKX	4	RO	**Support of 1000BASE-KX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE

Field	Bits	Type	Description
EEE_10GBT	3	RO	**Support of 10GBASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BT	2	RO	**Support of 1000BASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_100BTX	1	RO	**Support of 100BASE-TX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE

EEE Status Register 1

Not Specified

EEE_WAKERR	Offset	Reset Value
EEE Status Register 1	**03.0016_H**	**0000_H**



Field	Bits	Type	Description
ERRCNT	15:0	RO	**EEE Wake Error Counter** This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and may occur during a refresh or a wake-up as defined by the PHY. This 16-bit counter is reset to all zeroes when the EEE wake error counter is read by the management function or upon execution of the PCS reset. It is held at all ones in case of overflow.

4.4.3 ANEG: Standard Auto-Negotiation Registers for MMD=0x07

This register file contains the auto-negotiation registers for MMD device 0x07 (only supporting EEE specifics).

EEE Auto-Negotiation Advertisement Register

This register defines the EEE advertisement sent in the unformatted next page following an EEE technology message code as defined in 28C.12. The 11 bits (7.60.10 to 7.60.0) in the EEE advertisement register correspond to the bits in the unformatted next page. For PHYs that negotiate extended next-page support, the 11 bits (7.60.10 to 7.60.0) in the EEE advertisement register correspond to bits U10 to U0 respectively of the extended next-page unformatted code field.

EEE_AN_ADV	Offset	Reset Value
EEE Auto-Negotiation Advertisement Register	$07.003C_H$	0000_H

15	14	13	12	11	10	9	8
Res							

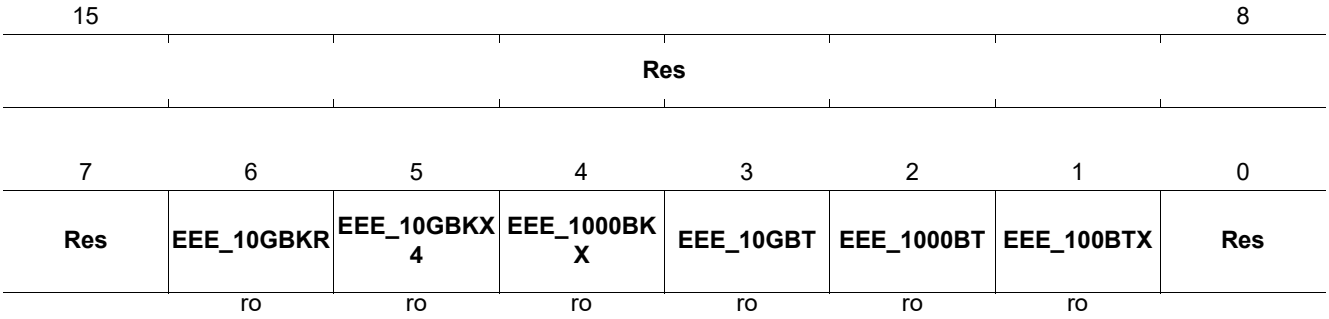
7	6	5	4	3	2	1	0
Res	EEE_10GBKR	EEE_10GBKX4	EEE_1000BKX	EEE_10GBT	EEE_1000BT	EEE_100BTX	Res
	ro	ro	ro	ro	rw	rw	

Field	Bits	Type	Description
EEE_10GBKR	6	RO	**Support of 10GBASE-KR EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBKX4	5	RO	**Support of 10GBASE-KX4 EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BKX	4	RO	**Support of 1000BASE-KX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBT	3	RO	**Support of 10GBASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BT	2	RW	**Support of 1000BASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_100BTX	1	RW	**Support of 100BASE-TX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE

EEE Auto-Negotiation Link-Partner Advertisement Register

All of the bits in the EEE LP advertisement register are read only. A write operation to the EEE LP advertisement register has no effect. After the AN process has been completed, this register reflects the contents of the link partner's EEE advertisement register. The definitions are the same as for the EEE AN advertisement register.

EEE_AN_LPADV	Offset	Reset Value
EEE Auto-Negotiation Link-Partner Advertisement Register	$07.003D_H$	0000_H



Field	Bits	Type	Description
EEE_10GBKR	6	RO	**Support of 10GBASE-KR EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBKX4	5	RO	**Support of 10GBASE-KX4 EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BKX	4	RO	**Support of 1000BASE-KX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBT	3	RO	**Support of 10GBASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BT	2	RO	**Support of 1000BASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_100BTX	1	RO	**Support of 100BASE-TX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE

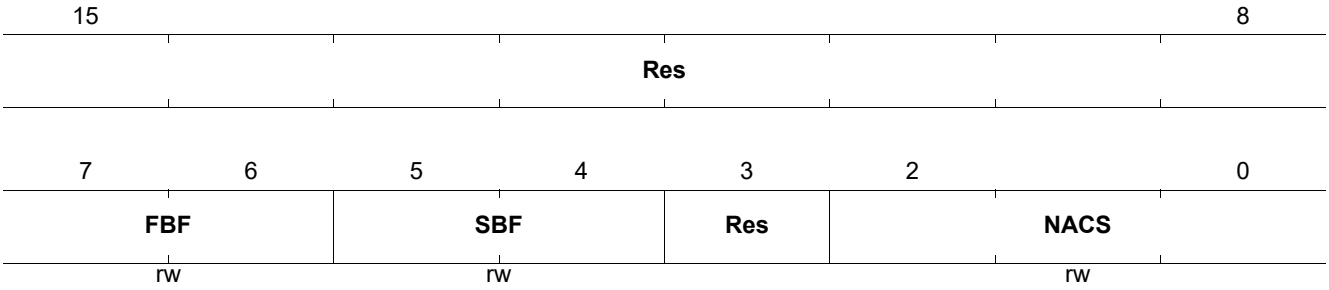
4.4.4 INTERNAL: Internal Address Space (MMD=0x1F)

This register file contains the PHY internal address space (MMD=0x1F).

LED Configuration

This register must be used to configure the complex functions of the LED behavior. Complex functions are of a higher priority than direct LED functions as of registers MMD.INTERNAL.LEDxH/L. When the PHY enters a state defined to activate complex LED functions, all LEDs are controlled according to the type of the complex function.

LEDCH	Offset	Reset Value
LED Configuration	$1F.01E0_H$	$00C5_H$



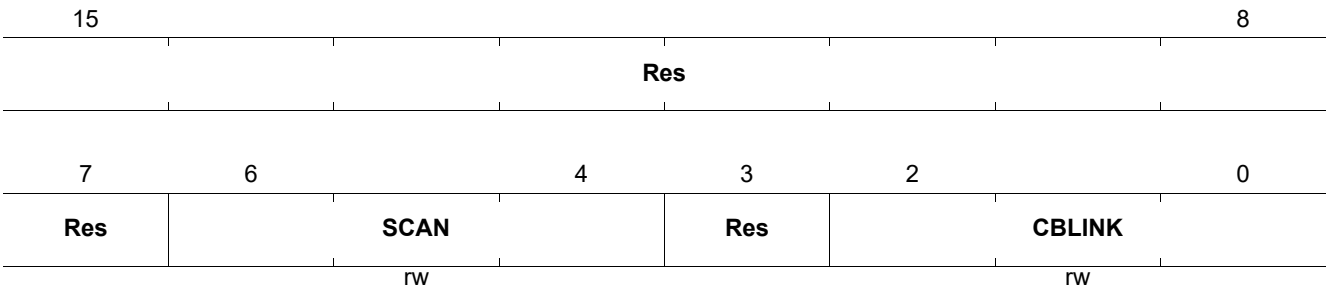
Field	Bits	Type	Description
FBF	7:6	RW	**Fast Blink Frequency** This register must be used to configure the fast-blinking frequency. This setting implicitly defines the pulse-stretching width. 00_B **F02HZ** 2 Hz blinking frequency 01_B **F04HZ** 4 Hz blinking frequency 10_B **F08HZ** 8 Hz blinking frequency 11_B **F16HZ** 16 Hz blinking frequency
SBF	5:4	RW	**Slow Blink Frequency** This register must be used to configure the slow-blinking frequency. 00_B **F02HZ** 2 Hz blinking frequency 01_B **F04HZ** 4 Hz blinking frequency 10_B **F08HZ** 8 Hz blinking frequency 11_B **F16HZ** 16 Hz blinking frequency

Field	Bits	Type	Description
NACS	2:0	RW	**Inverse of SCAN Function** This configuration defines in which state the "complex SCAN" must be activated. The complex SCAN performs running off which turns back and forth between the first and last LED. The speed is dependent on the MMD.INTERNAL.LEDCH.FBF setting. 000_B **NONE** No Function 001_B **LINK** Complex function enabled when link is up 010_B **PDOWN** Complex function enabled when device is powered-down 011_B **EEE** Complex function enabled when device is in EEE mode 100_B **ANEG** Complex function enabled when auto-negotiation is running 101_B **ABIST** Complex function enabled when analog self-test is running 110_B **CDIAG** Complex function enabled when cable diagnostics are running 111_B **TEST** Complex function enabled when test mode is running

LED Configuration

The register must be used to configure the complex functions of the LED behavior. Complex functions are of a higher priority than direct LED functions as of registers MMD.INTERNAL.LEDxH/L. When the PHY enters a state defined to activate complex LED functions all LEDs are controlled according to the type of the complex function.

LEDCL	Offset	Reset Value
LED Configuration	**$1F.01E1_H$**	**0067_H**

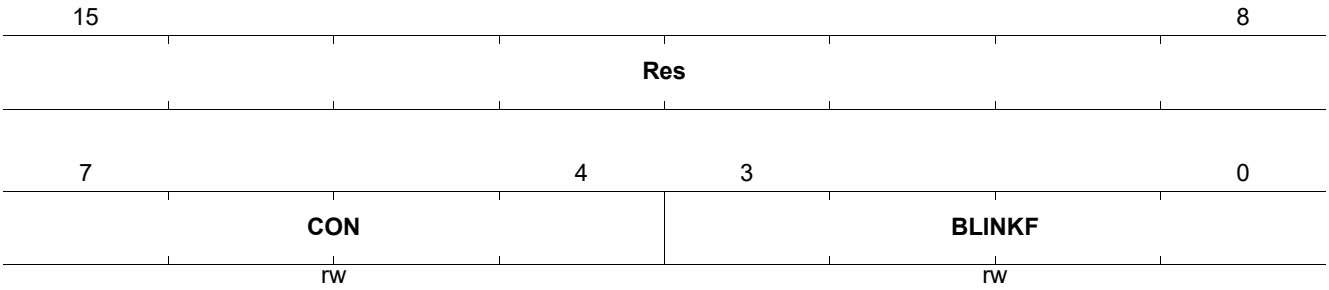


Field	Bits	Type	Description
SCAN	6:4	RW	**Complex SCAN Configuration** This configuration defines in which state the "complex SCAN" must be activated. The complex SCAN performs running on which turns back and forth between the first and last LED. The speed is dependent on the MMD.INTERNAL.LEDCH.FBF setting. 000_B **NONE** No Function 001_B **LINK** Complex function enabled when link is up 010_B **PDOWN** Complex function enabled when device is powered-down 011_B **EEE** Complex function enabled when device is in EEE mode 100_B **ANEG** Complex function enabled when auto-negotiation is running 101_B **ABIST** Complex function enabled when analog self-test is running 110_B **CDIAG** Complex function enabled when cable diagnostics are running 111_B **TEST** Complex function enabled when test mode is running
CBLINK	2:0	RW	**Complex Blinking Configuration** This configuration defines in which state the "complex blinking" must be activated. The complex blinking performs a blinking at the fast-blinking frequency on all LEDs simultaneously. This function can be used to indicate a special mode of the PHY such as cable-diagnostics or test. The speed is dependent on the MMD.INTERNAL.LEDCH.FBF setting. 000_B **NONE** No Function 001_B **LINK** Complex function enabled when link is up 010_B **PDOWN** Complex function enabled when device is powered-down 011_B **EEE** Complex function enabled when device is in EEE mode 100_B **ANEG** Complex function enabled when auto-negotiation is running 101_B **ABIST** Complex function enabled when analog self-test is running 110_B **CDIAG** Complex function enabled when cable diagnostics are running 111_B **TEST** Complex function enabled when test mode is running

Configuration for LED Pin 0

This register configures the behavior of the LED depending on pre-defined states or events the PHY has entered into or raised. Since more than one event/state can be active at the same time, more than one function might apply simultaneously. The priority from highest to lowest is given by the order PULSE, BLINKS, BLINKF, CON.

LED0H	Offset	Reset Value
Configuration for LED Pin 0	$1F.01E2_H$	0070_H



Field	Bits	Type	Description
CON	7:4	RW	**Constant On Configuration** The Constant-ON field selects in which PHY states the LED is constantly on. 0000_B**NONE** LED does not light up constantly 0001_B**LINK10** LED is on when link is 10 Mbps 0010_B**LINK100** LED is on when link is 100 Mbps 0011_B**LINK10X** LED is on when link is 10/100 Mbps 0100_B**LINK1000** LED is on when link is 1000 Mbps 0101_B**LINK10_0** LED is on when link is 10/1000 Mbps 0110_B**LINK100X** LED is on when link is 100/1000 Mbps 0111_B**LINK10XX** LED is on when link is 10/100/1000 Mbps 1000_B**PDOWN** LED is on when device is powered-down 1001_B**EEE** LED is on when device is in EEE mode 1010_B**ANEG** LED is on when auto-negotiation is running 1011_B**ABIST** LED is on when analog self-test is running 1100_B**CDIAG** LED is on when cable diagnostics are running 1101_B**COPPER** LED is on when the COPPER interface is selected 1110_B**FIBER** LED is on when the FIBER or an interface other than copper is selected 1111_B**RESERVED** Reserved for future use

Field	Bits	Type	Description
BLINKF	3:0	RW	**Fast Blinking Configuration** The Blink-F Field selects in which PHY states the LED blinks with the pre-defined fast frequency. 0000_B**NONE** No Blinking 0001_B**LINK10** Blink when link is 10 Mbps 0010_B**LINK100** Blink when link is 100 Mbps 0011_B**LINK10X** Blink when link is 10/100 Mbps 0100_B**LINK1000** Blink when link is 1000 Mbps 0101_B**LINK10_0** Blink when link is 10/1000 Mbps 0110_B**LINK100X** Blink when link is 100/1000 Mbps 0111_B**LINK10XX** Blink when link is 10/100/1000 Mbps 1000_B**PDOWN** Blink when device is powered-down 1001_B**EEE** Blink when device is in EEE mode 1010_B**ANEG** Blink when auto-negotiation is running 1011_B**ABIST** Blink when analog self-test is running 1100_B**CDIAG** Blink when cable diagnostics are running

Similar Registers

The following registers are identical to the Register **LED0H** defined above.

Table 65 Similar Registers

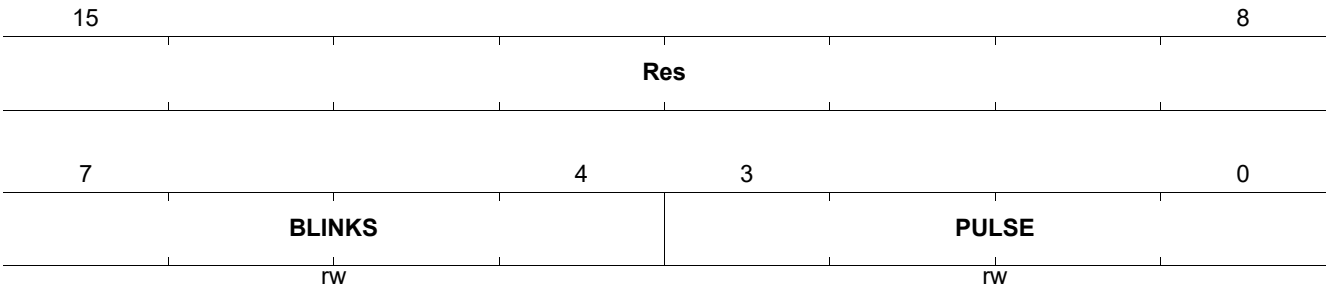
Register Short Name	Register Long Name	Offset Address	Reset Value
LED1H	Configuration for LED Pin 1	$1F.01E4_H$	0020_H
LED2H	Configuration for LED Pin 2	$1F.01E6_H$	0040_H
LED3H	Configuration for LED Pin 3	$1F.01E8_H$	0040_H

Configuration for LED Pin 0

This register configures the behavior of the LED depending on pre-defined states or events the PHY has entered into or raised. Since more than one event or state can be active at the same time, more than one function might apply simultaneously. The priority from highest to lowest is given by the order PULSE, BLINKS, BLINKF, CON.

LED0L **Offset** **Reset Value**

Configuration for LED Pin 0 **$1F.01E3_H$** **0003_H**



Field	Bits	Type	Description
BLINKS	7:4	RW	**Slow Blinking Configuration** The Blink-S field selects in which PHY states the LED blinks with the pre-defined slow frequency. 0000_B**NONE** No Blinking 0001_B**LINK10** Blink when link is 10 Mbps 0010_B**LINK100** Blink when link is 100 Mbps 0011_B**LINK10X** Blink when link is 10/100 Mbps 0100_B**LINK1000** Blink when link is 1000 Mbps 0101_B**LINK10_0** Blink when link is 10/1000 Mbps 0110_B**LINK100X** Blink when link is 100/1000 Mbps 0111_B**LINK10XX** Blink when link is 10/100/1000 Mbps 1000_B**PDOWN** Blink when device is powered-down 1001_B**EEE** Blink when device is in EEE mode 1010_B**ANEG** Blink when auto-negotiation is running 1011_B**ABIST** Blink when analog self-test is running 1100_B**CDIAG** Blink when cable diagnostics are running
PULSE	3:0	RW	**Pulsing Configuration** The pulse field is a mask field by which certain events can be combined, e.g. TXACT|RXACT, to generate a pulse on the LED in case such an event has been detected. 0000_B**NONE** No pulsing 0001_B**TXACT** Transmit activity 0010_B**RXACT** Receive activity 0100_B**COL** Collision 1000_B**RES** Reserved

Similar Registers

The following registers are identical to the Register **LED0L** defined above.

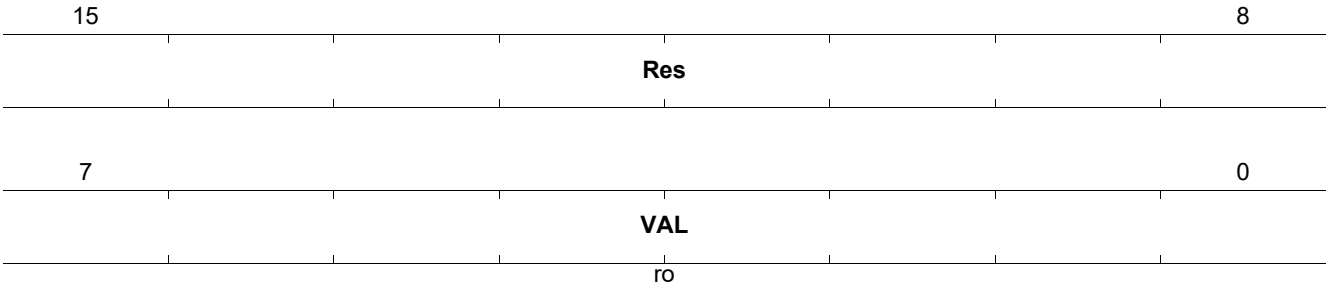
Table 66 Similar Registers

Register Short Name	Register Long Name	Offset Address	Reset Value
LED1L	Configuration for LED Pin 1	$1F.01E5_H$	0000_H
LED2L	Configuration for LED Pin 2	$1F.01E7_H$	0000_H
LED3L	Configuration for LED Pin 3	$1F.01E9_H$	0020_H

High Byte of the EEE Link-Fail Counter

High Byte of the EEE Link-Fail Counter.

EEE_RXERR_LINK_FAIL_H	Offset	Reset Value
High Byte of the EEE Link-Fail Counter	$1F.01EA_H$	0000_H

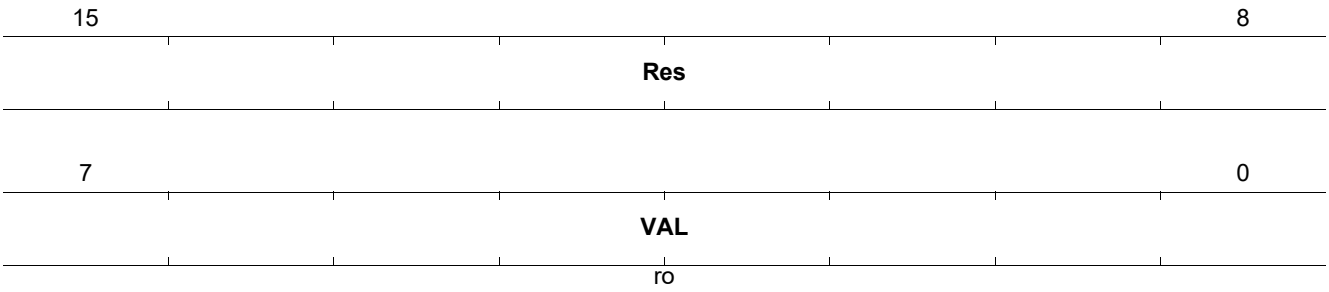


Field	Bits	Type	Description
VAL	7:0	RO	**VAL** High byte of the EEE_RXERR_LINK_FAIL counter. A read access to the low byte also clears the high byte of this counter.

Low Byte of the EEE Link-Fail Counter

Low Byte of the EEE Link-Fail Counter.

EEE_RXERR_LINK_FAIL_L	Offset	Reset Value
Low Byte of the EEE Link-Fail Counter	$1F.01EB_H$	0000_H

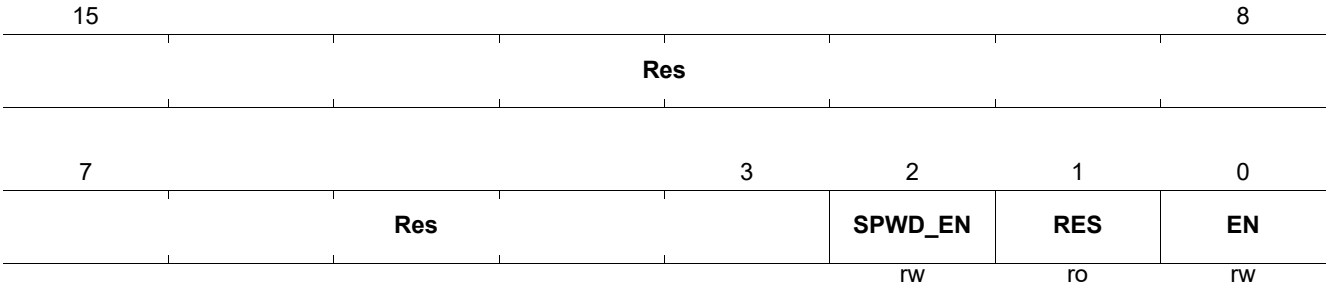


Field	Bits	Type	Description
VAL	7:0	RO	**VAL** Low byte of the EEE_RXERR_LINK_FAIL counter. A read access to this byte also clears the high byte of this counter.

Wake-On-LAN Control Register

Wake-On-LAN Control Register.

WOLCTRL	Offset	Reset Value
Wake-On-LAN Control Register	$1F.0781_H$	0000_H

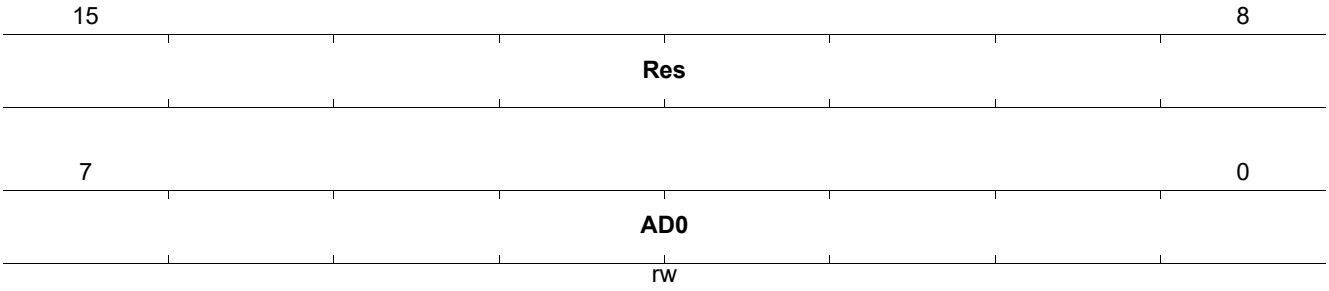


Field	Bits	Type	Description
SPWD_EN	2	RW	**Secure-ON Password Enable** When enabled, checks for the Secure-ON password after the 16 MAC address repetitions. 0_B **DISABLED** Secure-On password check is disabled 1_B **ENABLED** Secure-On password check is enabled
RES	1	RO	**Reserved** Must always be written to zero!
EN	0	RW	**Wake-On-LAN Enable** When Wake-On-LAN is enabled, the PHY scans for the configured magic packet and indicates its reception via the register bit ISTAT.WOL, and optionally also via interrupt. 0_B **DISABLED** Wake-On-LAN functionality is disabled 1_B **ENABLED** Wake-On-LAN functionality is enabled

Wake-On-LAN Address Byte 0

Wake-On-LAN Address Byte 0.

WOLAD0	Offset	Reset Value
Wake-On-LAN Address Byte 0	$1F.0783_H$	0000_H



Field	Bits	Type	Description
AD0	7:0	RW	**Address Byte 0** Defines byte 0 of the WOL-designated MAC address to which the PHY is sensitive.

Similar Registers

The following registers are identical to the Register **WOLAD0** defined above.

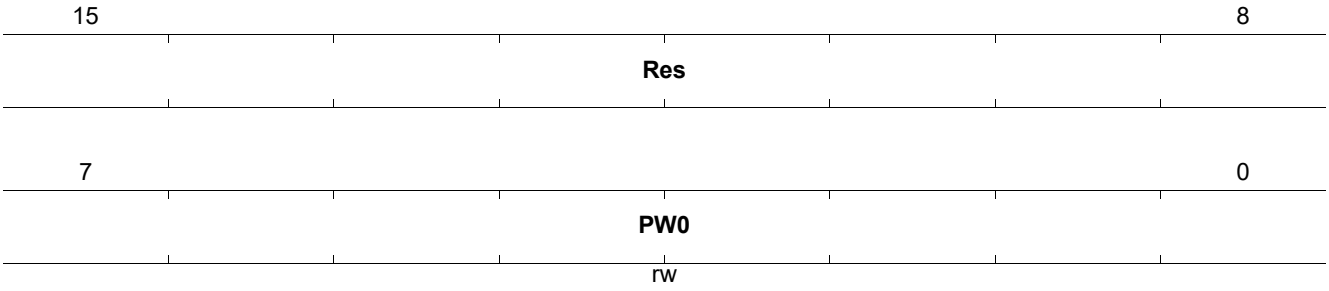
Table 67 Similar Registers

Register Short Name	Register Long Name	Offset Address	Reset Value
WOLAD1	Wake-On-LAN Address Byte 1	$1F.0784_H$	0000_H
WOLAD2	Wake-On-LAN Address Byte 2	$1F.0785_H$	0000_H
WOLAD3	Wake-On-LAN Address Byte 3	$1F.0786_H$	0000_H
WOLAD4	Wake-On-LAN Address Byte 4	$1F.0787_H$	0000_H
WOLAD5	Wake-On-LAN Address Byte 5	$1F.0788_H$	0000_H

Wake-On-LAN SecureON Password Byte 0

Wake-On-LAN SecureON Password Byte 0.

WOLPW0	Offset	Reset Value
Wake-On-LAN SecureON Password Byte 0	$1F.0789_H$	0000_H



Field	Bits	Type	Description
PW0	7:0	RW	**SecureON Password Byte 0** Defines byte 0 of the WOL-designated SecureON password to which the PHY is sensitive.

Similar Registers

The following registers are identical to the Register **WOLPW0** defined above.

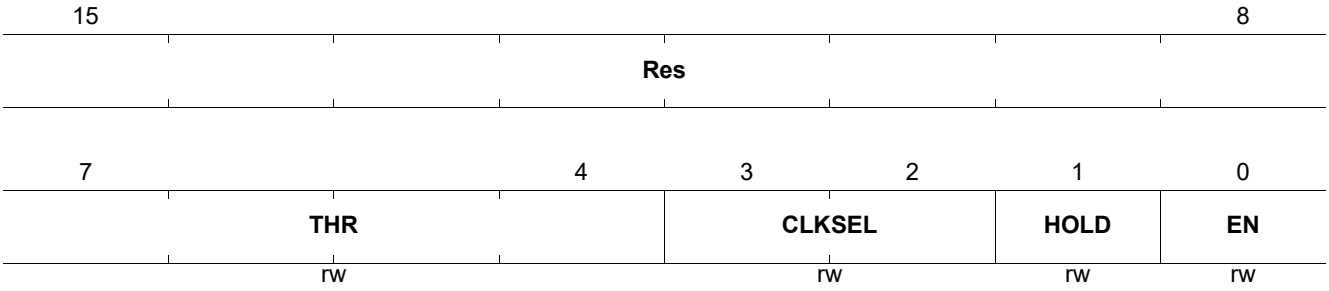
Table 68 Similar Registers

Register Short Name	Register Long Name	Offset Address	Reset Value
WOLPW1	Wake-On-LAN SecureON Password Byte 1	$1F.078A_H$	0000_H
WOLPW2	Wake-On-LAN SecureON Password Byte 2	$1F.078B_H$	0000_H
WOLPW3	Wake-On-LAN SecureON Password Byte 3	$1F.078C_H$	0000_H
WOLPW4	Wake-On-LAN SecureON Password Byte 4	$1F.078D_H$	0000_H
WOLPW5	Wake-On-LAN SecureON Password Byte 5	$1F.078E_H$	0000_H

Configuration for Synchronous Ethernet

This register allow management configuration of the SyncE clocking reference

PD_CTL	Offset	Reset Value
Configuration for Synchronous Ethernet	$1F.07FE_H$	0000_H



Field	Bits	Type	Description
THR	7:4	RW	**THR** Control the Threshold for detection of Lost of Reference clock.
CLKSEL	3:2	RW	**CLKSEL** This enable management selection of the type of reference clock we are receiving 00_B **AN1** Reference clock is 8 kHz. Special request for AN application 01_B **EEC1** Reference clock is 2.048 MHz according to EEC-Option 1 10_B **EEC2** Reference clock is 1.544 MHz according to EEC-Option 2 11_B **AN2** Reserved
HOLD	1	RW	**HOLD** Force the SyncE into HOLD over mode. This is the mode we enter when we detect Lost of reference. To hold the adapted Frequency so that we are able to sustain the reference clock generation within error of 4.6ppm. 0_B **NORM** HW control of the entry/exit of Hold-Over mode 1_B **FHOLD** Force Hold Over mode
EN	0	RW	**EN** Enable Synchronous Ethernet Support 0_B **DISABLE** Normal Ethernet operation 1_B **ENABLE** SyncE is enabled

5 Electrical Characteristics

This chapter defines the electrical characteristics to which the Gigabit Ethernet Switch device conforms.

Note: This chapter is subject to change.

5.1 Absolute Maximum Ratings

Table 69 shows the absolute maximum ratings for the Gigabit Ethernet Switch.

Attention: Stresses above the maximum values listed in this table may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.

Table 69 Absolute Limit Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage Temperature Limits	T_{STG}	-55.0	–	125.0	°C	–
Moisture Level 3 Temperature Limits	T_{ML3}	–	–	260.0	°C	According to IPS J-STD 020
DC Voltage Limits on VDDP Pins	V_{DDP}	-0.5	–	+3.6	V	–
DC Voltage Limits on VDDH Pins	V_{DDH}	-0.5	–	+3.6	V	–
DC Voltage Limits on VDDA Pins	V_{DDA}	-0.5	–	+3.6	V	–
DC Voltage Limits on VDDR Pins	V_{DDR}	-0.5	–	+3.6	V	–
DC Voltage Limits on VDDL Pins	V_{DDL}	-0.5	–	+1.26	V	–
DC Voltage Limits on VDDS Pins	V_{DDS}	-0.5	–	+1.26	V	–
DC Voltage Limits on VDD Pins	V_{DD}	-0.5	–	+1.26	V	–
DC Voltage Limits on Any Other Pins[1] With Respect to Ground	V_{DC}	-0.5	–	V_{DDx}+0.5	V	Unless specified otherwise
ESD HBM Robustness	$V_{ESD,HBM}$	–	–	1000.0	V	According to ANSI/ESDA/JEDEC JS-001-2014
ESD CDM Robustness	$V_{ESD,CDM}$	–	–	250.0	V	According to JEDEC JESD22-C101

1) This means any pin which is not a supply pin out of one of the domains: V_{DDP}, V_{DDA}, V_{DDH}, V_{DDR}, V_{DDL}, V_{DD}.

5.2 Operating Range

Table 70 defines the limit values of voltages and temperature which may be applied to guarantee proper operation of the Gigabit Ethernet Switch.

Table 70 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature Under Bias	T_A	0	–	70.0	°C	–
Junction Temperature	T_j	–	–	125.0	°C	–
Pad Supply Voltage	V_{DDP}	3.13	3.30	3.47	V	3.3 V supply
High Supply Voltage	V_{DDH}	3.13	3.30	3.47	V	3.3 V supply
XO High Supply Voltage	V_{DDA}	3.13	3.30	3.47	V	3.3 V supply
RGMII PAD Supply Voltage	V_{DDR}	3.13	3.30	3.47	V	3.3 V supply
		2.37	2.50	2.63	V	2.5 V supply
Low Supply Voltage	V_{DDL}	1.05	1.10	1.15	V	1.1 V supply
SGMII Low Supply Voltage	V_{DDS}	1.05	1.10	1.15	V	1.1 V supply
Core Supply Voltage	V_{DD}	1.05	1.10	1.15	V	1.1 V supply
Digital Input Voltage (Except RGMII Pins)	V_{ID}	-0.30	–	V_{DDP}+0.3	V	–
Digital Input Voltage (RGMII Pins)	V_{ID}	0.00	–	V_{DDR}	V	–
XTAL1 Input Voltage	V_{ID}	-0.30	–	V_{DDA}+0.3	V	–
Ground	V_{SS}	0.00	0.00	0.00	V	–

Attention: Operations above the max. values listed here for extended periods can adversely affect long-term reliability of the device.

5.3 Power Consumption

Attention: The Reset Request Register (RST_REQ) bits 2 and 3 must always be written as '1'.

Table 71 Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MAX POWER CASE: 4-GPHY-ports 1G link+traffic, 100m cable; SGMII+ trafic, RGMII traffic						
	I_{DDH}	–	260	280	mA	V_{DDH} = 3.3 V, T_A = 25 °C
	I_{DDL}	–	420	450	mA	V_{DDL} = 1.1 V, T_A = 25 °C
	$I_{DD/DDS}$	–	760	840	mA	$V_{DD/DDS}$ = 1.1 V, T_A = 25 °C
	$I_{DDP/DDR/DDA}$	–	7	10	mA	$V_{DDP/DDR/DDA}$ = 3.3 V, T_A = 25 °C
10m POWER CASE: 4-GPHY-ports 1G link+traffic, 10m cable; SGMII+ traffic, RGMII traffic						
	I_{DDH}	–	260	280	mA	V_{DDH} = 3.3 V, T_A = 25 °C
	I_{DDL}	–	380	430	mA	V_{DDL} = 1.1 V, T_A = 25 °C
	$I_{DD/DDS}$	–	660	750	mA	$V_{DD/DDS}$ = 1.1 V, T_A = 25 °C
	$I_{DDP/DDR/DDA}$	–	7	10	mA	$V_{DDP/DDR/DDA}$ = 3.3 V, T_A = 25 °C
100BASE-T POWER CASE: 4-GPHY-ports 100Mbps link+traffic, 100m cable; SGMII+ traffic, RGMII traffic						
	I_{DDH}	–	120	140	mA	V_{DDH} = 3.3 V, T_A = 25 °C
	I_{DDL}	–	200	220	mA	V_{DDL} = 1.1 V, T_A = 25 °C
	$I_{DD/DDS}$	–	300	350	mA	$V_{DD/DDS}$ = 1.1 V, T_A = 25 °C
	$I_{DDP/DDR/DDA}$	–	7	10	mA	$V_{DDP/DDR/DDA}$ = 3.3 V, T_A = 25 °C
EEE NO-TRAFFIC POWER CASE: 4-GPHY-ports 1G link no-traffic, SGMII+ IDLE, RGMII IDLE						
	I_{DDH}	–	65	80	mA	V_{DDH} = 3.3 V, T_A = 25 °C
	I_{DDL}	–	160	180	mA	V_{DDL} = 1.1 V, T_A = 25 °C
	$I_{DD/DDS}$	–	370	410	mA	$V_{DD/DDS}$ = 1.1 V, T_A = 25 °C
	$I_{DDP/DDR/DDA}$	–	7	10	mA	$V_{DDP/DDR/DDA}$ = 3.3 V, T_A = 25 °C
NO-LINK POWER CASE: 4-GPHY-ports no-link+trafic, SGMII+ IDLE, RGMII IDLE						
	I_{DDH}	–	55	60	mA	V_{DDH} = 3.3 V, T_A = 25 °C
	I_{DDL}	–	80	90	mA	V_{DDL} = 1.1 V, T_A = 25 °C
	$I_{DD/DDS}$	–	240	270	mA	$V_{DD/DDS}$ = 1.1 V, T_A = 25 °C
	$I_{DDP/DDR/DDA}$	–	7	10	mA	$V_{DDP/DDR/DDA}$ = 3.3 V, T_A = 25 °C
RESET POWER CASE: 4-GPHY-ports Reset, SGMII+ Reset, RGMII Reset						
	I_{DDH}	–	23	30	mA	V_{DDH} = 3.3 V, T_A = 25 °C
	I_{DDL}	–	7	10	mA	V_{DDL} = 1.1 V, T_A = 25 °C
	$I_{DD/DDS}$	–	10	15	mA	$V_{DD/DDS}$ = 1.1 V, T_A = 25 °C
	$I_{DDP/DDR/DDA}$	–	1	3	mA	$V_{DDP/DDR/DDA}$ = 3.3 V, T_A = 25 °C

5.4 DC Characteristics

The following sections investigate the DC characteristics of the Gigabit Ethernet Switch external interfaces.

5.4.1 Digital Interfaces

This section defines the DC characteristics of the digital interfaces.

5.4.1.1 GPIO Interfaces

This section defines the DC characteristics of the GPIO Interface comprised of the following interfaces.

- MDIO
- SPI
- UART
- Interrupts
- Clock Outputs
- General Purpose IO
- LED
- JTAG

Table 72 summarizes the DC characteristics for V_{DDP}=3.3 V.

Table 72 DC Characteristics of the GPIO Interfaces (VDDP=3.3V)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	0.7*V_{DDP}	–	V_{DDP}+0.3	V	–
Input Low Voltage	V_{IL}	–0.3	–	0.3*V_{DDP}	V	–
Output High Voltage	V_{OH}	V_{DDP}-0.4	–	–	V	I_{OH}= 2, 4, 8, 12 mA
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL}= 2, 4, 8, 12 mA

5.4.1.2 RGMII Transmit Interface

This section defines the DC characteristics of the RGMII transmit Interface. Table 73 summarizes the DC characteristics valid for V_{DDR}=2.5 V and V_{DDR}=3.3 V.

Table 73 DC Characteristics of the Transmit RGMII Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output High Voltage	V_{OH}	2.1	–	V_{DDR}+0.3	V	5 pF
Output Low Voltage	V_{OL}	0	–	0.5	V	5 pF

5.4.1.3 RGMII Receive Interface

This section defines the DC characteristics of the RGMII receive Interface. Table 74 summarizes the DC characteristics valid for V_{DDR}=2.5 V and V_{DDR}=3.3 V.

Table 74 DC Characteristics of the Receive RGMII Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	1.7	–	–	V	–
Input Low Voltage	V_{IL}		–	0.7	V	–

5.5 AC Characteristics

The following sections describe the AC characteristics of the external interfaces. The load capacitors are according to the specific interface standard. All non-specified interfaces use 30 pF as assumed loading.

5.5.1 Reset

Gigabit Ethernet Switch supports an asynchronous hardware reset HRSTN. **Table 75** lists the timing requirements on the HRSTN pin to the GSW140. **Figure 50** depicts the signal sequence waveforms illustrating the timings.

It is recommended that the voltage 3.3 V powers up before voltage 1.1 V. Voltage 1.1 V must never be higher than voltage 3.3 V ramp. Voltage 1.1 V must power up within t_{up} after 3.3 V powers up. After the power-supply settling time, all primary input signals to the GSW140 must be defined. In particular, this is valid for the device reset HRSTN. This reset must be held for a t_{reset} time. After releasing the reset, the integrated PLL locks on the reference clock and the device boots up.

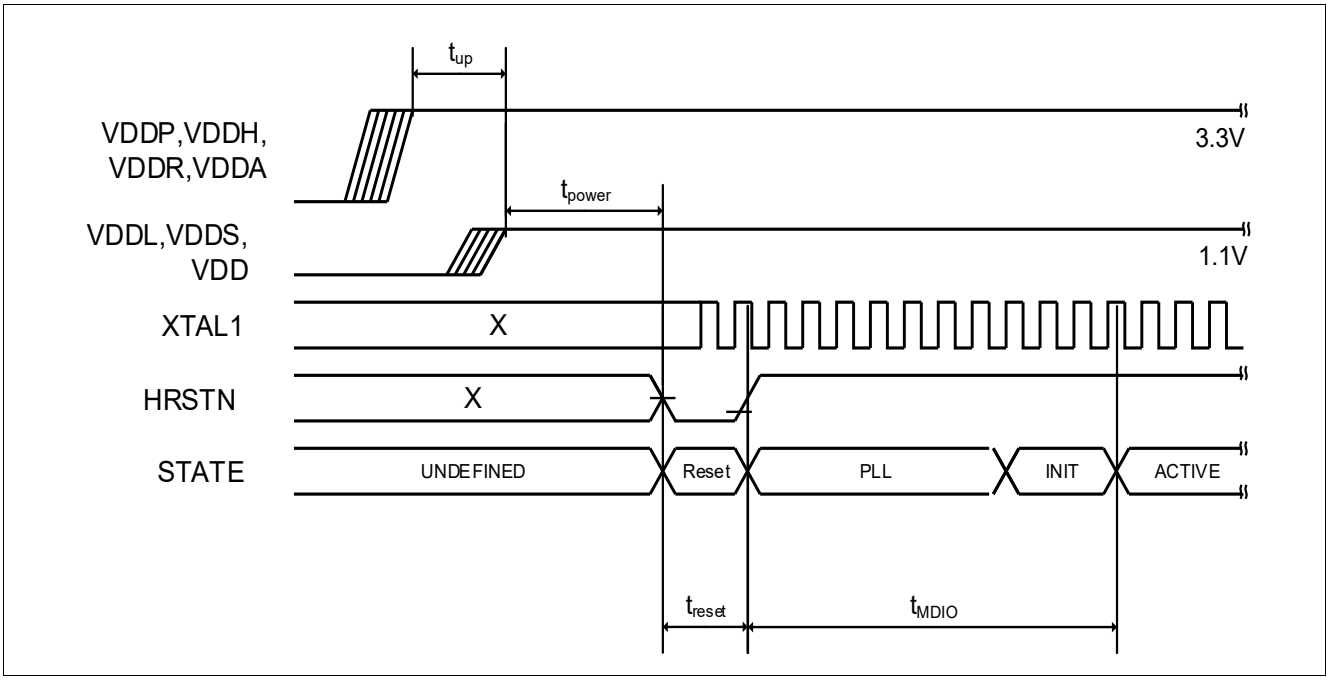


Figure 50 Timing Diagram for the GSW140 Reset Sequence

Table 75 AC Characteristics of the HRSTN Pin

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply Sequence Time	t_{up}	–	–	100.0	ms	–
Power Supply Settling Time	t_{power}	–	–	50.0	ms	–
Reset Time	t_{reset}	200.0	–	–	ms	–
First MDIO Access after Reset Release	t_{MDIO}	300.0	–	–	ms	–

5.5.2 Power Supply

Table 76 lists the AC characteristics of the power supplies.

Table 76 AC Characteristics of the Power Supply

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply Ripple on VDDL	R_{VDDL}	–	–	30.0	mV	Peak value
Power Supply Ripple on VDDS	R_{VDDL}	–	–	30.0	mV	Peak value
Power Supply Ripple on VDD	R_{VDD}	–	–	30.0	mV	Peak value
Power Supply Ripple on VDDP	R_{VDDP}	–	–	100.0	mV	Peak value
Power Supply Ripple on VDDH	R_{VDDH}	–	–	30.0	mV	Peak value
Power Supply Ripple on VDDA	R_{VDDH}	–	–	30.0	mV	Peak value
Power Supply Ripple on VDDR	R_{VDDR}	–	–	100.0	mV	Peak value

5.5.3 Input Clock

Table 77 lists the input clock requirements when not using a crystal, i.e. when an external reference clock is injected into the XTAL1 pin of the Gigabit Ethernet Switch, e.g. nominal frequency, frequency deviation, duty cycle and signal characteristics. When a crystal is applied to generate the reference clock using the integrated XO, the clock requirements stated here are explicitly met as long as the specification for the crystal is satisfied.

Table 77 AC Characteristics of Input Clock on XTAL1 pin

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency with 25 MHz Input	f_{clk25}	–	25.0	–	MHz	–
Frequency with 40 MHz Input	f_{clk40}	–	40.0	–	MHz	–
Frequency Deviation		-50.0	–	+50.0	ppm	–
Duty Cycle		45.0	50.0	55.0	%	–
XTAL1 Input Swing		0.9	-	V_{DDA}	V	–
Rise/Fall-Times		–	–	2.0	ns	-

5.5.4 Output Clock

Table 78 lists the output clock requirements on the GPC pin from the Gigabit Ethernet Switch, e.g. nominal frequency, frequency deviation, duty cycle and signal characteristics.

Table 78 AC Characteristics of Output Clock on GPC pin

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Deviation		-50.0	–	+50.0	ppm	–
Duty Cycle		45.0	50.0	55.0	%	–
Rise/Fall-Times		–	–	2.0	ns	10 pF load

5.5.5 MDIO Interface

Figure 51 shows a timing diagram of the MDIO interface for a clock cycle in the read-, write- and turnaround-modus, respectively. The timing measures are annotated. Table 79 summarizes the defined absolute values.

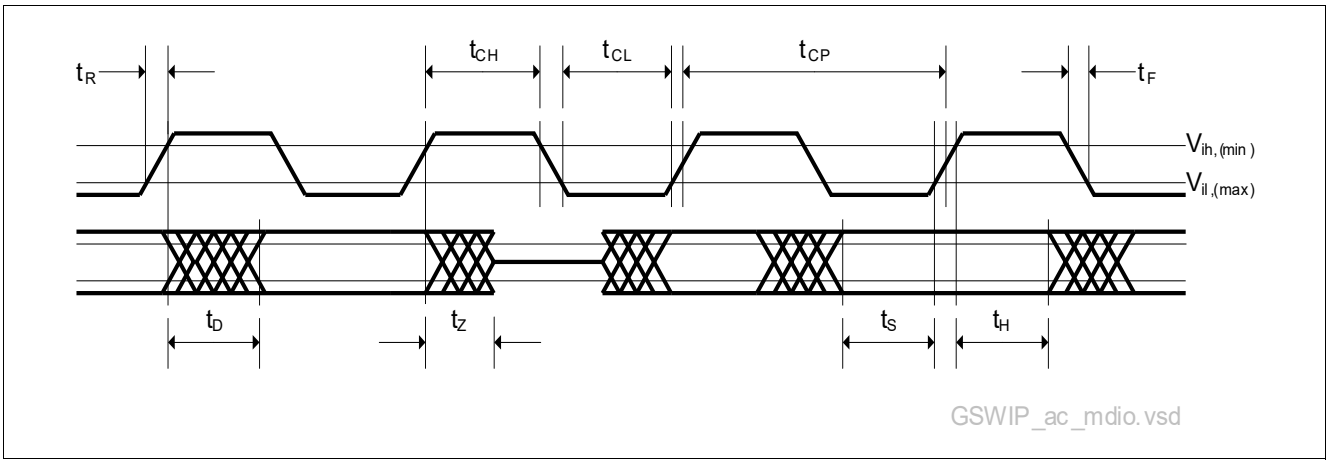


Figure 51 Timing Diagram for the MDIO Interface

Table 79 Timing Characteristics of the MDIO Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MDC High Time	t_{CH}	10.0	–	–	ns	Given timings are all subject to the MDC at the pin of the Gigabit Ethernet Switch.
MDC Low Time	t_{CL}	10.0	–	–	ns	
MDC Clock Period	t_{CP}	58.8	400.0	–	ns	
MDC Clock Frequency[1)]	t_{CP}	–	2.5	17.0	MHz	
MDC Rise Time	t_R	–	–	5.0	ns	
MDC Fall Time	t_F	–	–	5.0	ns	
MDIO Input Setup Time subject to ↑ MDC	t_S	10.0	–	–	ns	Gigabit Ethernet Switch receive
MDIO Input Hold Time subject to ↑ MDC	t_H	0.0	–	–	ns	Gigabit Ethernet Switch receive
MDIO Output Delay subject to ↑ MDC	t_D	10.0	–	t_{CP}-10	ns	Gigabit Ethernet Switch transmit
Standard @2.5 MHz						
MDIO Output Delay subject to ↑ MDC	t_D	0.0	–	300.0	ns	PHY transmit
MDIO Output Setup Time subject to ↑ MDC	t_S	10.0	–	–	ns	MAC transmit
MDIO Output Hold Time subject to ↑ MDC	t_H	10.0	–	–	ns	MAC transmit

1) MDC clock supports range of frequencies, up to 25 MHz. Default/typical frequency is 2.5 MHz.

5.5.6 SMDIO Interface

Figure 52 shows a timing diagram of the SMDIO interface for a clock cycle in the read-, write- and turnaround-modus, respectively. The timing measures are annotated. Table 80 summarizes the defined absolute values.

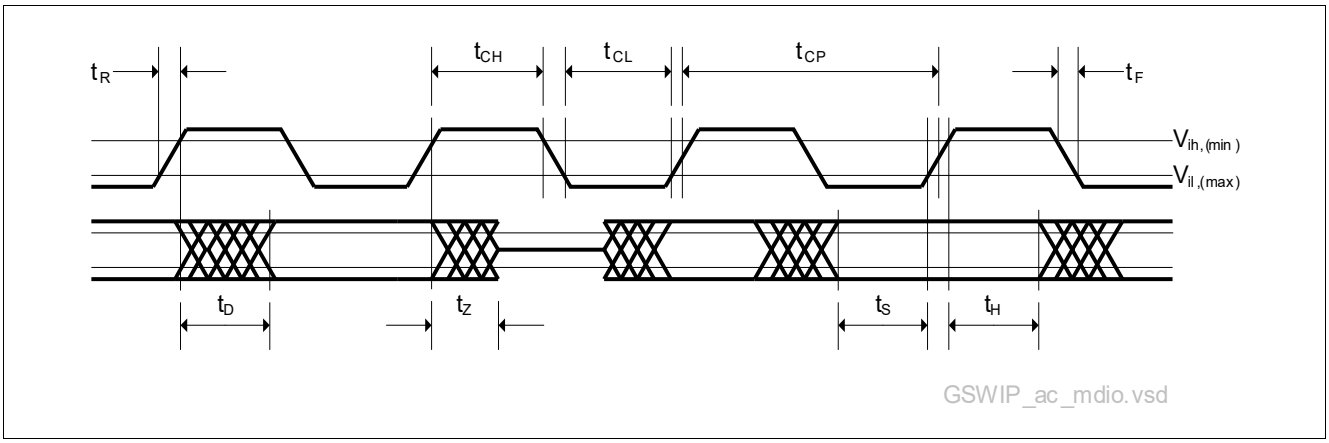


Figure 52 Timing Diagram for the SMDIO Interface

Table 80 Timing Characteristics of the SMDIO Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MDC High Time	t_{CH}	10.0	–	–	ns	Given timings are all subject to the MDC at the pin of the Gigabit Ethernet Switch.
MDC Low Time	t_{CL}	10.0	–	–	ns	
MDC Clock Period	t_{CP}	40.0	400.0	–	ns	
MDC Clock Frequency[1)]	t_{CP}	–	2.5	25.0	MHz	
MDC Rise Time	t_R	–	–	5.0	ns	
MDC Fall Time	t_F	–	–	5.0	ns	
MDIO Input Setup Time subject to ↑ MDC	t_S	10.0	–	–	ns	Gigabit Ethernet Switch receive
MDIO Input Hold Time subject to ↑ MDC	t_H	10.0	–	–	ns	Gigabit Ethernet Switch receive
MDIO Output Delay Time subject to ↑ MDC	t_D	0.0	–	10	ns	Gigabit Ethernet Switch transmit
Standard @2.5 MHz						
MDIO Output Delay subject to ↑ MDC	t_D	0.0	–	300.0	ns	PHY transmit
MDIO Output Setup Time subject to ↑ MDC	t_S	10.0	–	–	ns	MAC transmit
MDIO Output Hold Time subject to ↑ MDC	t_H	10.0	–	–	ns	MAC transmit

1) MDC clock supports range of frequencies, up to 25 MHz. Default/typical frequency is 2.5 MHz.

5.5.7 RGMII Interface Timing Characteristics

The following sections investigate the timing characteristics of the xMII interfaces.

5.5.7.1 RGMII Interface

This section investigates the timing characteristics of the RGMII interface at the Gigabit Ethernet Switch. Unless no HSTL voltages are supported, this interface is conform to the RGMII specification v1.3 and v2.0. The RGMII interface can operate at speeds of 10 Mbps, 100 Mbps and 1000 Mbps.

Timing Characteristics

Figure 53 shows the timing diagram of the RGMII interface at the Gigabit Ethernet Switch. **Table 81** characterizes the timing requirements. The setup and hold times are subject to the internal version of the TX_CLK/RX_CLK which is the external clock delayed by the integrated delay and adjustable in steps of 0.5ns via PCDU register configuration. When the integrated delay is not used, e.g. because its implemented externally by PCB wire delays, it must be set to zero in which case all the timings are related directly to the TX_CLK/RX_CLK at the pin.

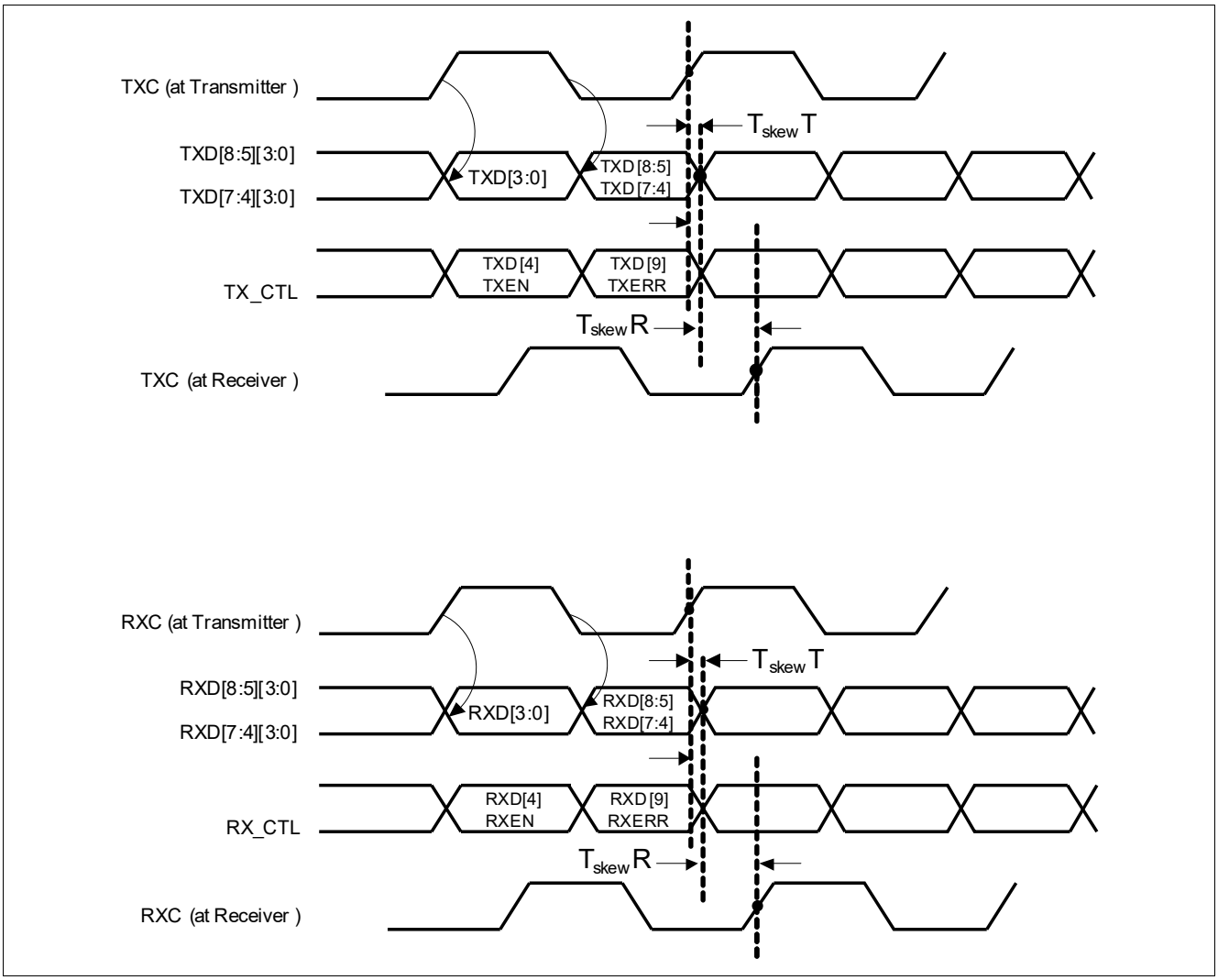


Figure 53 Timing Diagram of the RGMII

Table 81 Timing Characteristics of the RGMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock Frequency (RX_CLK/TX_CLK)	f_{CLK}	-50ppm	125.0	+ 50ppm	MHz	For 1000 Mbps speed.
		-50ppm	25.0	+ 50ppm	MHz	For 100 Mbps speed.
		-50ppm	2.5	+ 50ppm	MHz	For 10 Mbps speed.
Clock Period (RX_CLK/TX_CLK)	t_{CP}	7.2	8.0	8.8	ns	For 1000 Mbps speed.
		36.0	40.0	44.0	ns	For 100 Mbps speed.
		360.0	400.0	440.0	ns	For 10 Mbps speed.
Duty Cycle[1)]	t_H/t_{CP}, t_L/t_{CP}	45.0	50.0	55.0	%	Speed independent
Clock Rise Time (RX_CLK/TX_CLK)	t_R	–	–	750.0	ps	20% → 80%
Clock Fall Time (RX_CLK/TX_CLK)	t_F	–	–	750.0	ps	80% → 20%
Clock to Data Skew at Transmitter	t_{SkewT}	-0.5	0.0	0.5	ns	
Clock to Data Skew at Receiver	t_{SkewR}	1	1.8	2.6	ns	
Integrated Receive Clock Delay	t_{ID}	0.0	k*0.5	3.5	ns	Adjustable via registers

1) Duty Cycle may be stretched/shrunk during speed changes. Such an even last no longer than three t_{CP} at lowest speed.

5.5.7.2 SGMII Interface

This section describes the AC characteristics of the SGMII Interface on the GSW140. This interface conforms to the CEI-6G-SR Specification, as defined in **[3]**. The SGMII interface can operate at 3.125 Gbaud (maximum). The maximum net data-rate is 2500 Mbps.

5.5.7.2.1 Transmit Timing Characteristics

Figure 54 shows the timing diagram of the transmit SGMII interface at the GSW140. **Table 82** specifies the timing requirements.

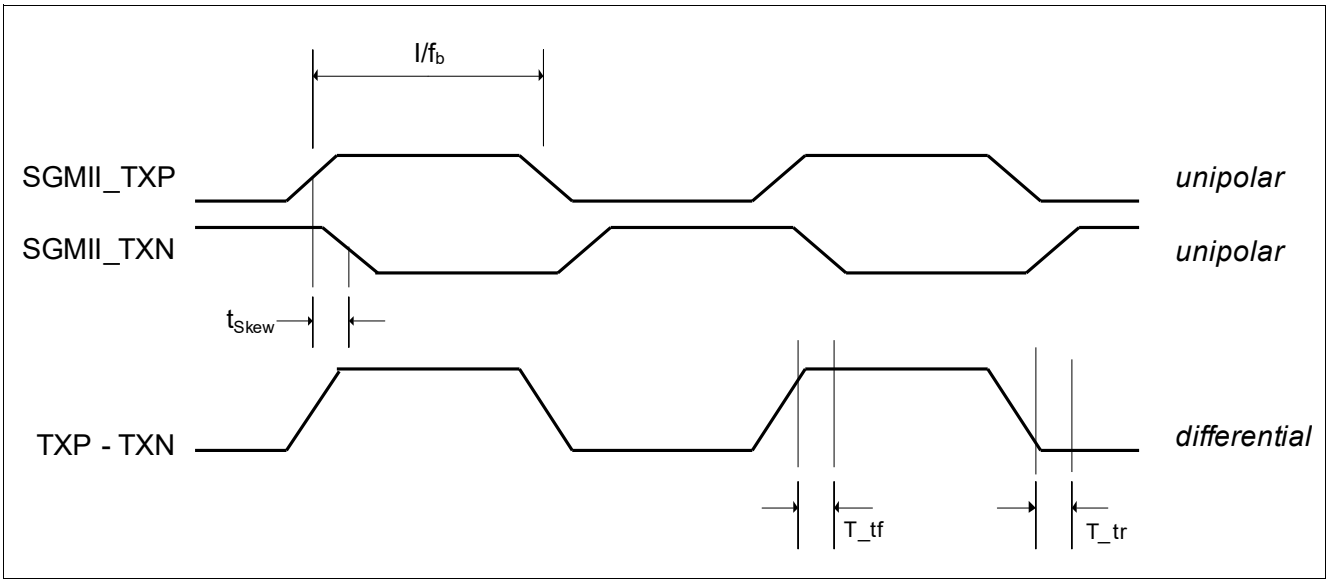


Figure 54 Transmit Timing Diagram of the SGMII (Shows Alternating Data Sequence)

Table 82 Transmit Timing Characteristics of the SGMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transmit Baud Rate	f_b	-100 ppm	f_b	+ 100 ppm	Mbaud	f_b = 1.25/2.5/3.125 Gbaud
Differential Transmit Rise Time	T_tr	30 ps	–	0.25 UI	–	20% → 80%[1)]
Differential Transmit Fall Time	T_rf	30 ps	–	0.25 UI	–	80% → 20%
Output Timing Jitter	T_TJ	–	–	0.30	UI_{pp}	[2)]
Time Skew Between Pairs	t_{Skew}	–	–	15	ps	–
Output Differential Voltage	V_{OD}	400	–	1600	mV	Peak-peak amplitude
Output Impedance (Differential)	R_O	80	100	120	Ω	–

1) $UI = I/f_b$
2) Refer to **[3]** for details.

5.5.7.2.2 Receive Timing Characteristics

Figure 55 shows the timing diagram of the receive SGMII interface on the GSW140. **Table 83** specifies the timing requirements.

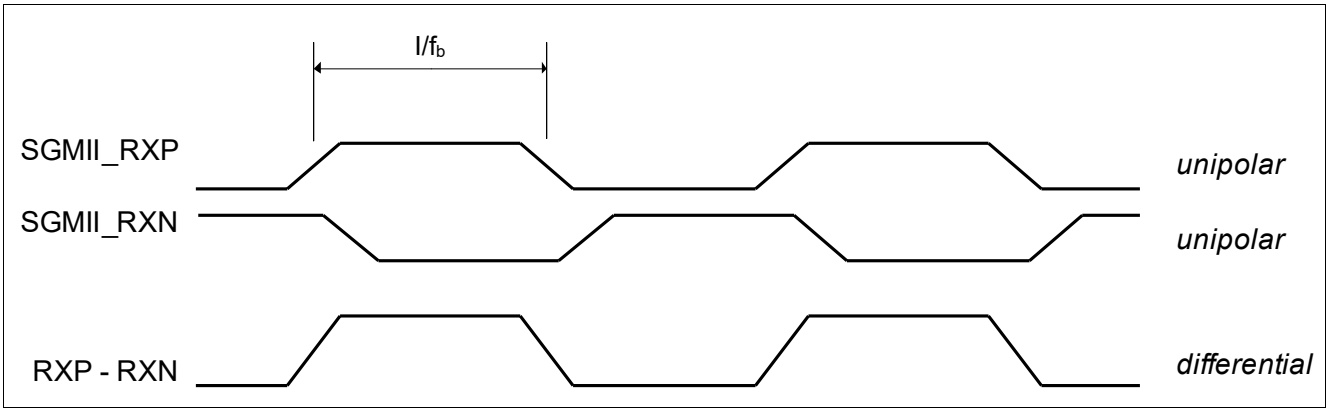


Figure 55 Receive Timing Diagram of the SGMII (Alternating Data Input Sequence)

Table 83 Receive Timing Characteristics of the SGMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive Baud Rate	f_b	-100 ppm	f_b	+ 100 ppm	Mbaud	f_b = 1.25/2.5/3.125 Gbaud
Receive Data Jitter Tolerance	R_TJ	–	–	0.6	UI_{pp} [1)]	–
Input Differential Voltage	V_{ID}	200	–	1600	mV	peak-peak amplitude
Input Impedance (Differential)	R_I	80	100	120	Ω	–

1) Refer to **[3]** for details.

5.5.8 Test Interface

The test interface is used for boundary scan.

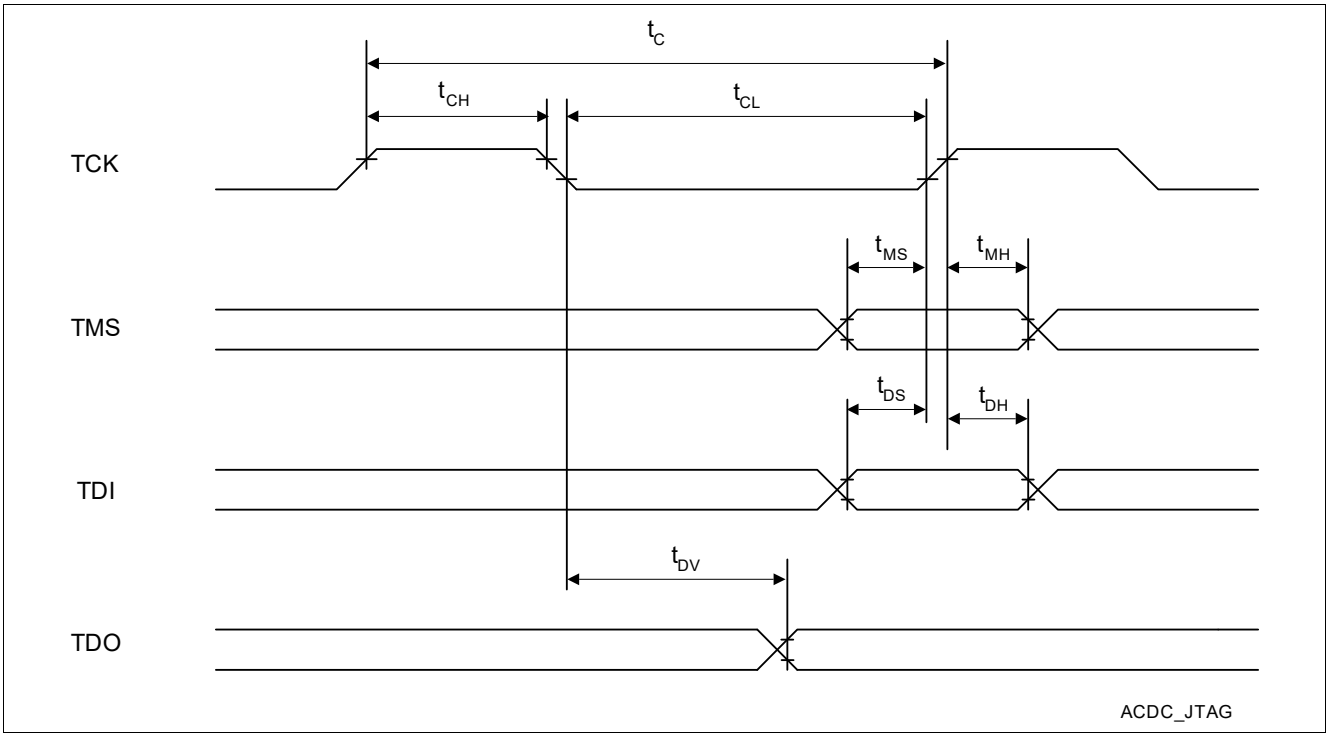


Figure 56 Test Interface Timing

Table 84 and Table 85 describe the timing values.

Table 84 Test Interface Clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK Clock Period	t_C	100	–	–	ns	–
TCK High Time	t_{CH}	40	–	–	ns	–
TCK Low Time	t_{CL}	40	–	–	ns	–

Table 85 JTAG Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TMS Setup Time	t_{MS}	40	–	–	ns	–
TMS Hold Time	t_{MH}	40	–	–	ns	–
TDI Setup Time	t_{DS}	40	–	–	ns	–
TDI Hold Time	t_{DH}	40	–	–	ns	–
Hold: $\overline{\text{TRST}}$ After TCK	t_{HD}	10	–	–	ns	–
TDO Valid Delay	t_{DV}	–	–	60	ns	–

5.5.9 Crystal Specification

In the reference design, the crystal is attached to the Gigabit Ethernet Switch SoC and must follow the specifications found in **Table 86**.

Table 86 Specification of the Crystal

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency with 25 MHz Input	f_{clk25}	–	25.0	–	MHz	–
Frequency with 40 MHz Input	f_{clk40}	–	40.0	–	MHz	–
Total Frequency Stability	–	-50	–	+50	ppm	Refer to sum of all effects: eg. general tolerance, aging, temperature dependency
Series Resonant Resistance	–	–	–	40	Ω	–
Drive Level	–	0.08	0.10	0.2	mW	–
Load Capacitance	C_L	16	-	30	pF	–
Shunt Capacitance	C_0	–	-	7	pF	–

5.5.10 Transformers (Magnetics)

GSW140 supports both types of common mode choke on the PHY side or Line side transformer configuration. **Figure 57** and **Figure 58** show these configurations.

Note: Refer to the electrical isolation requirement before using the Integrated MagJacks transformer.

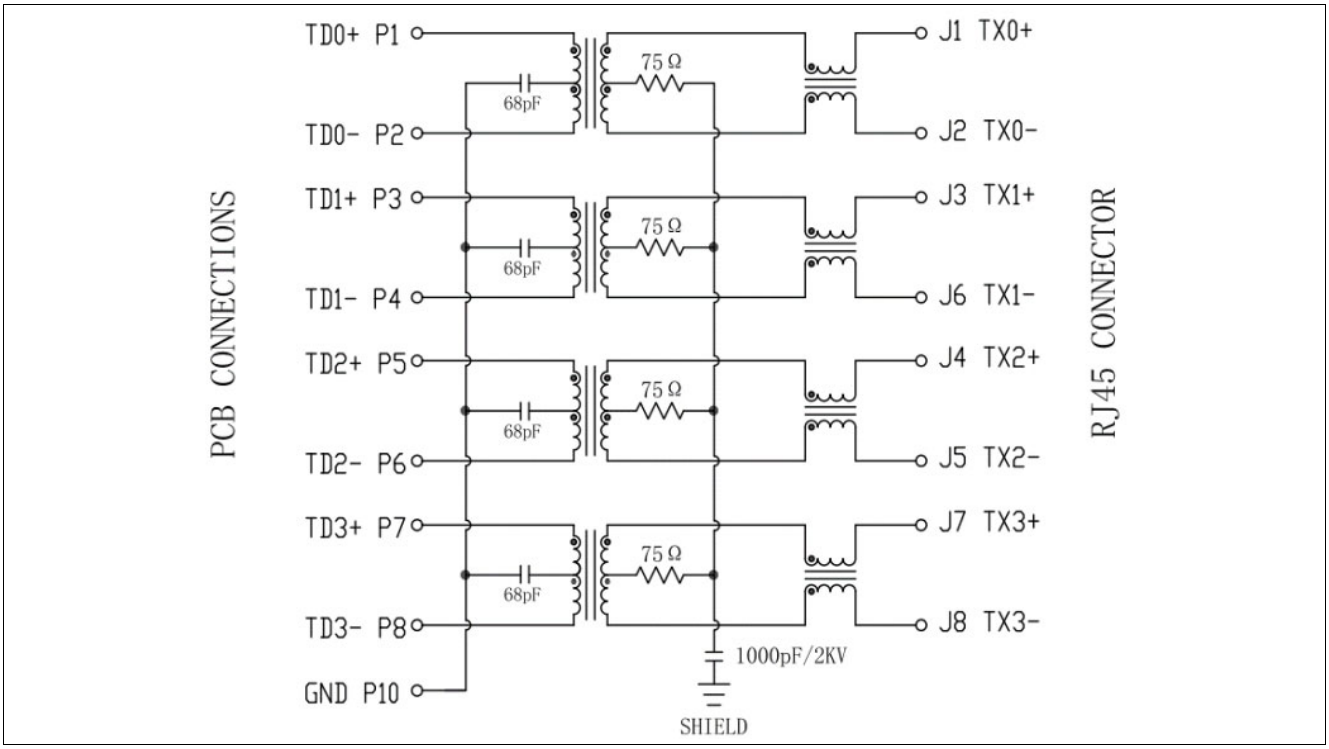


Figure 57 Schematic of a Transformer with CMC on Line

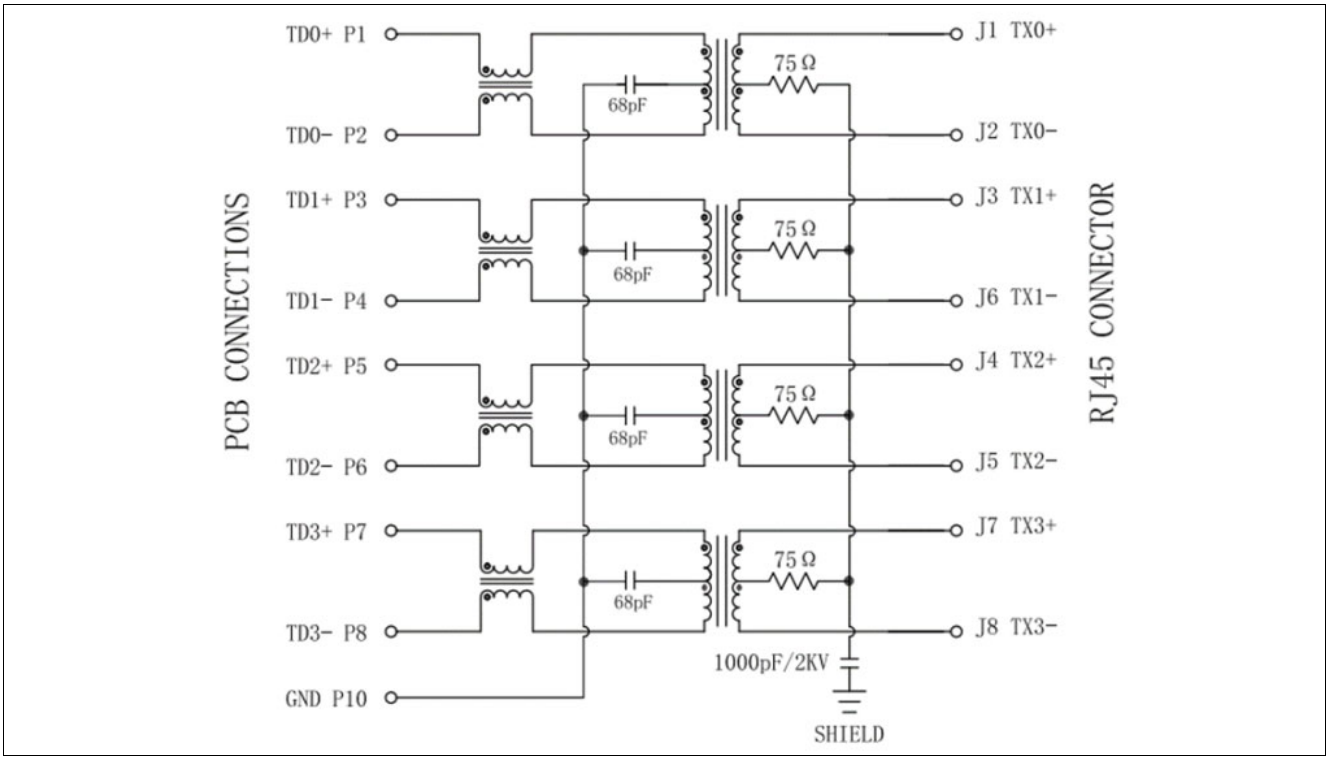


Figure 58 Schematic of a Transformer with CMC on PHY Side

Table 87 specifies the electrical characteristics of the supported transformer devices. The listed specifications guarantee proper operation according to IEEE 802.3.

Table 87 Electrical Characteristics for Supported Transformers (Magnetics)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Turns ratio	1:tr	0.95	1.00	1.05		±5%
Differential-to-common-mode rejection	DCMR	43	–	–	dB	30 MHz
		37	–	–	dB	60 MHz
		33	–	–	dB	100 MHz
Crosstalk attenuation	CTA	45	–	–	dB	30 MHz
		40	–	–	dB	60 MHz
		35	–	–	dB	100 MHz
Insertion loss	IL	–	–	1	dB	0.1 MHz ≤ f ≤ 100 MHz
Return loss	RL	18.0	–	–	dB	1 MHz ≤ f ≤ 30 MHz
		14.0	–	–	dB	31 MHz ≤ f ≤ 40 MHz
		13.0	–	–	dB	41 MHz ≤ f ≤ 50 MHz
		12.0	–	–	dB	51 MHz ≤ f ≤ 80 MHz
		10.0	–	–	dB	81 MHz ≤ f ≤ 100 MHz

Note: These characteristics represent the bare minimum for achieving standard performance. Since the transformer significantly impacts the link performance, it is possible to increase the loop reach by selecting transformers with improved parameters.

6 Package Outline

The product is assembled in a package which complies with regulations requiring lead free material.

6.1 PG-MRQFN-105 Package

This section describes the PG-MRQFN-105 package.

Table 88 JEDEC Thermal Resistance PG-MRQFN-105 Package Parameters

Item	Description/Value
Package Type	PG-MRQFN-105
Thermal Resistance Junction to Ambient (Reference to JEDEC JESD51-2)	$R_{th,\ JA}$ = 18.15 K/W Psi_{JCTop} = 0.21 K/W Psi_{JB} = 7.10 K/W
Thermal Resistance Junction to Case (Reference to JEDEC JESD15-3)	$R_{th,\ JCtop}$ = 20.42 K/W
	$R_{th,\ JB}$ = 5.51 K/W

Note: The 4-layer PCB is used and the number of PCB Thermal Vias is 14.

Figure 59 and **Figure 60** show the package outline and dimensions.

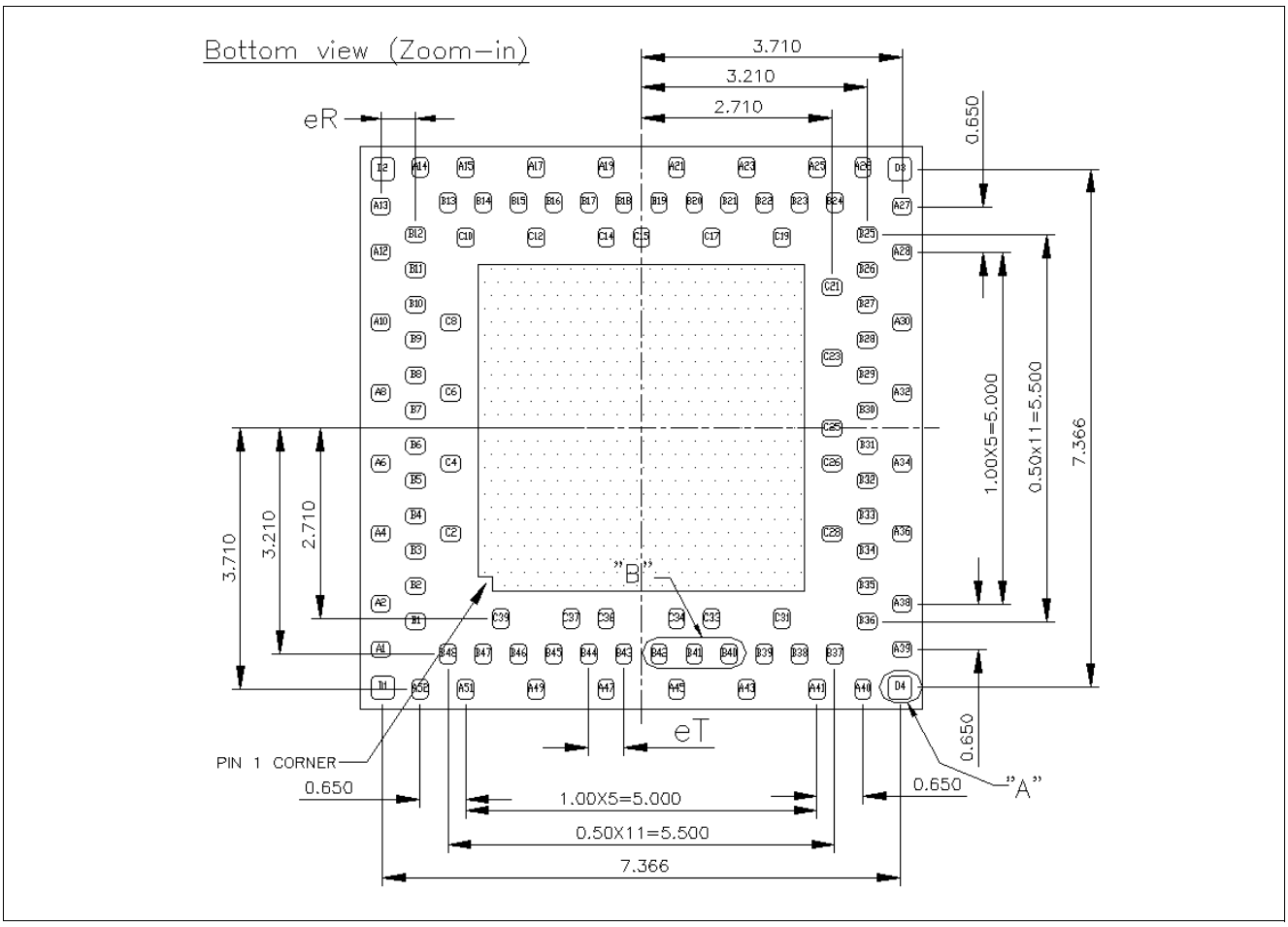
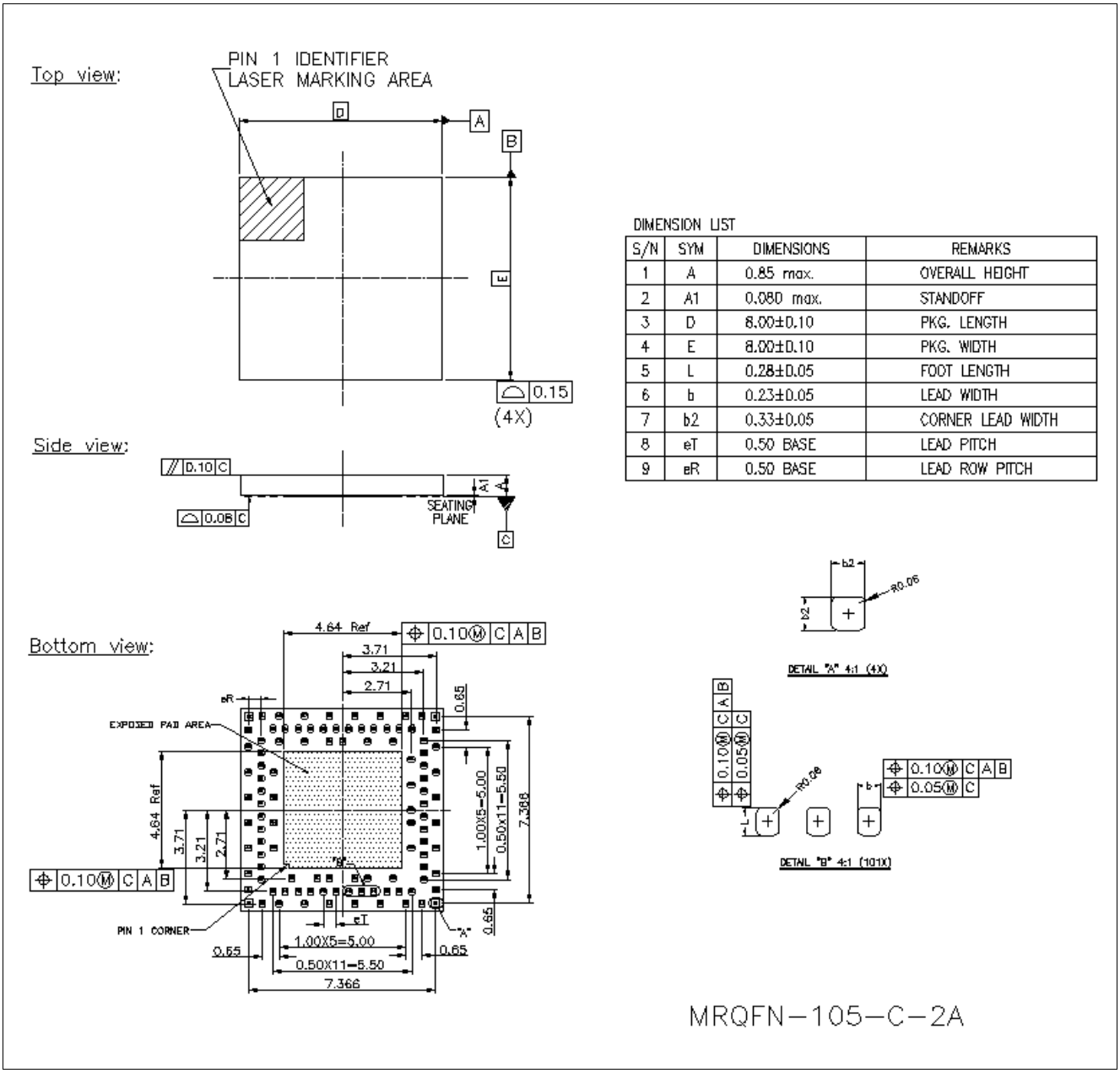


Figure 59 MRQFN 8 mm x 8 mm Package Outline



DIMENSION LIST

S/N	SYM	DIMENSIONS	REMARKS
1	A	0.85 max.	OVERALL HEIGHT
2	A1	0.080 max.	STANDOFF
3	D	8.00±0.10	PKG. LENGTH
4	E	8.00±0.10	PKG. WIDTH
5	L	0.28±0.05	FOOT LENGTH
6	b	0.23±0.05	LEAD WIDTH
7	b2	0.33±0.05	CORNER LEAD WIDTH
8	eT	0.50 BASE	LEAD PITCH
9	eR	0.50 BASE	LEAD ROW PITCH

Figure 60 MRQFN 8 mm x 8 mm Package Dimensions

6.2 LGA-105 Package

This section describes the LGA-105 package.

Table 89 JEDEC Thermal Resistance LGA-105 Package Parameters

Item	Description/Value
Package Type	LGA-105
Thermal Resistance Junction to Ambient (Reference to JEDEC JESD51-2)	$R_{th,\ JA}$ = 25.53 K/W Psi_{JCTop} = 0.24 K/W Psi_{JB} = 14.47 K/W
Thermal Resistance Junction to Case (Reference to JEDEC JESD15-3)	$R_{th,\ JCtop}$ = 20.49 K/W
	$R_{th,\ JB}$ = 10.96 K/W

Note: The 4-layer PCB is used and the number of PCB Thermal Vias is 14.

Figure 61 and **Figure 62** show the package outline and dimensions.

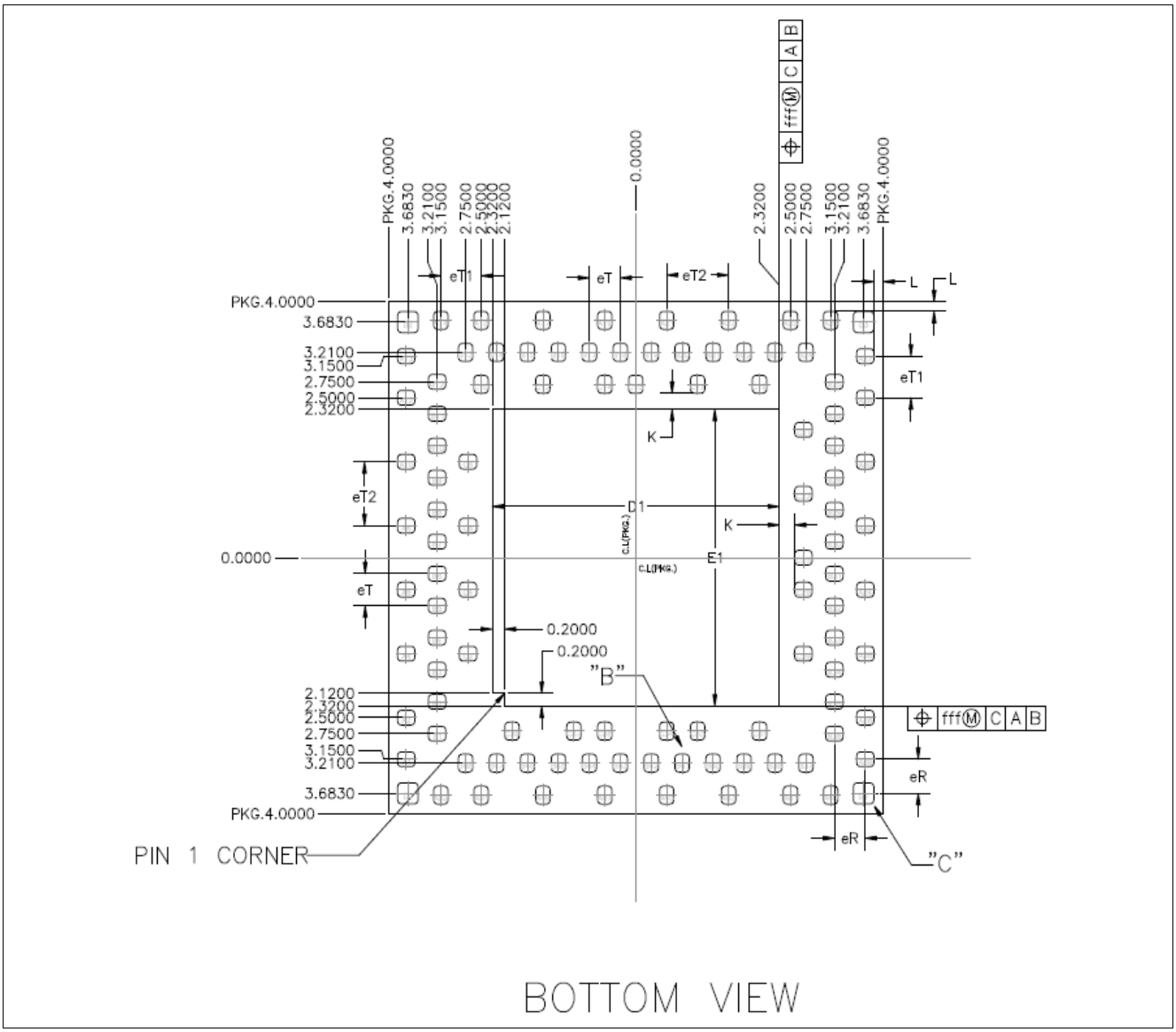
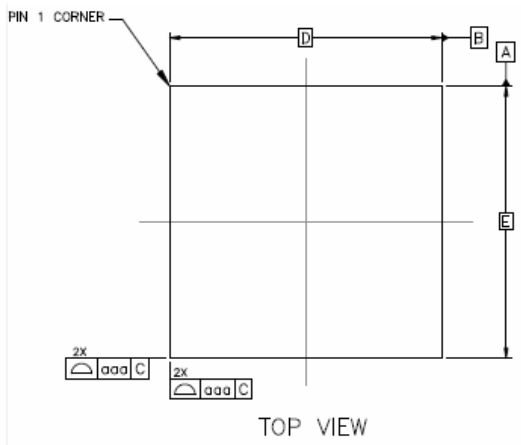
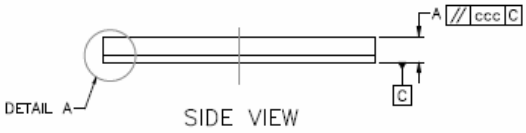


Figure 61 LGA 8 mm x 8 mm Package Outline

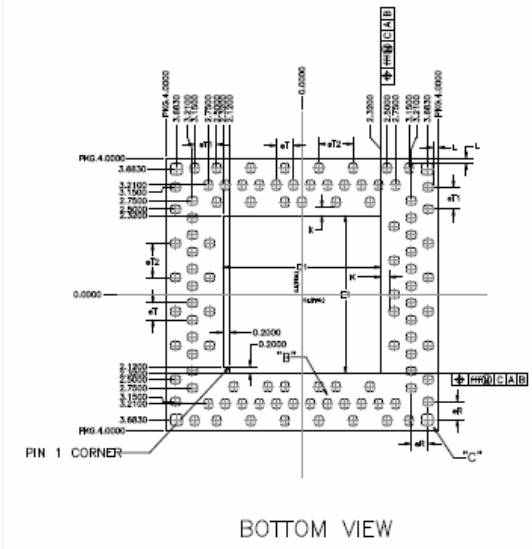


TOP VIEW

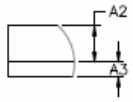


SIDE VIEW

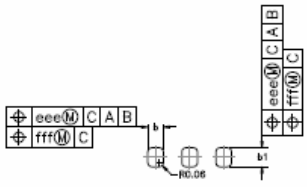
FOR CUSTOMER ONLY				
PACKAGE TYPE		LGA		
PIN COUNT		105		
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.65	0.75	0.85
STAND OFF	A1	–	–	–
MOLD THICKNESS	A2	–	0.54 BSC	–
MATERIAL THICKNESS	A3	0.17	0.21	0.25
PACKAGE SIZE	D	7.90	8.00	8.10
	E	7.90	8.00	8.10
LEAD PITCH	eT1		0.65 BSC	
LEAD WIDTH	b	0.18	0.23	0.28
EP SIZE	D1	4.54	4.64	4.74
	E1	4.54	4.64	4.74
PACKAGE EDGE PROFILE	aaa		0.15	
SUBSTRATE FLATNESS	bbb		0.10	
MOLD FLATNESS	ccc		0.08	
LEAD COPLANARITY	ddd		0.05	
LEAD POSITION OFFSET (PACKAGE)	eee		0.08	
LEAD POSITION OFFSET (LEAD)	fff		0.10	
LEAD LENGTH	L	0.10	0.15	0.20
	b1	0.23	0.28	0.33
	b2	0.28	0.33	0.38
	eT		0.50 BSC	
	eT2		1.00 BSC	
	eR		0.50 BSC	
	K	0.20	0.25	0.30



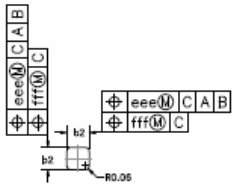
BOTTOM VIEW



DETAIL A (2:1)



DETAIL "B" (2:1)(10IX)



DETAIL "C" (2:1)(4X)

Figure 62 LGA 8 mm x 8 mm Package Dimensions

6.3 Chip Identification and Ordering Information

Figure 63 shows an example of the marking pattern on the Gigabit Ethernet Switch (GSW140) device. The actual chip marking may differ slightly from the illustration.

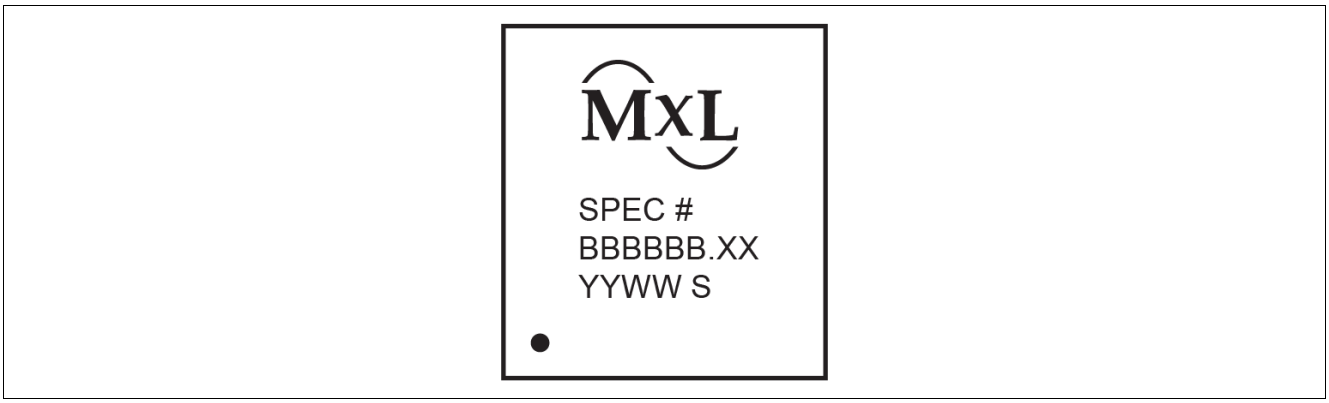


Figure 63 Example of Chip Marking

Table 90 explains the chip marking information and Table 91 provides chip ordering information.

Table 90 Chip Marking Pattern

Marking	Description
Text Line 1	MaxLinear Logo
Text Line 2	Spec. Number - See Table 91
Text Line 3	Wafer Lot Number
Text Line 4	Date Code (YYWW) and Assembly Site Code (S)

Table 91 Product Naming

Product Name	Former Intel Sales Code	Ordering Code	S-Spec#	Package
GSW140	MMID 963956	GSW140A3MC	SLMHB	PG-MRQFN-105
GSW140	MMID 910007	GSW140A3LC	SL007	LGA-105

Literature References

[1] Ethernet Switch GSW140/GSW145 Reference Board V1.2.x Hardware Design Guide Rev. 2.0 (in preparation)

[2] Ethernet Switch GSW140/GSW145 Reference Board V1.2.x Getting Started Rev. 2.0 (in preparation)

[3] Common Electrical I/O (CEI) – Electrical and Jitter Interoperability agreements for 6G+ bps and 11G+ bps I/O (IA # OIF-CEI-02.0) 28th February 2005