19-4681; Rev 1; 3/10

EVALUATION KIT AVAILABLE

Multi-Output Power Supplies with VCOM Amplifier and High-Voltage Gamma Reference for LCD TVs

General Description

The MAX17126/MAX17126A generate all the supply rails for thin-film transistor liquid-crystal display (TFT LCD) TV panels operating from a regulated 12V input. They include a step-down and a step-up regulator, a positive and a negative charge pump, an operational amplifier, a high-accuracy high-voltage gamma reference, and a high-voltage switch control block. The MAX17126/MAX17126A can operate from input voltages from 8V to 16.5V and is optimized for an LCD TV panel running directly from 12V supplies.

The step-up and step-down switching regulators feature internal power MOSFETs and high-frequency operation allowing the use of small inductors and capacitors, resulting in a compact solution. The step-up regulator provides TFT source driver supply voltage, while the step-down regulator provides the system with logic supply voltage. Both regulators use fixed-frequency current-mode control architectures, providing fast load-transient response and easy compensation. A current-limit function for internal switches and output-fault shutdown protects the step-up and step-down power supplies against fault conditions. The MAX17126/MAX17126A provide soft-start functions to limit inrush current during startup. In addition, the MAX17126/MAX17126A integrate a control block that can drive an external p-channel MOSFET to sequence power to source drivers.

The positive and negative charge-pump regulators provide TFT gate-driver supply voltages. Both output voltages can be adjusted with external resistive voltage-dividers. A logic-controlled, high-voltage switch block allows the manipulation of the positive gate-driver supply.

The MAX17126/MAX17126A include one high-current operational amplifier designed to drive the LCD backplane (VCOM). The amplifier features high output current (±200mA), fast slew rate (45V/µs), wide bandwidth (20MHz), and rail-to-rail outputs.

Also featured in the MAX17126/MAX17126A is a high-accuracy, high-voltage adjustable reference for gamma correction.

The MAX17126/MAX17126A are available in a small (7mm x 7mm), ultra-thin (0.8mm), 48-pin thin QFN package and operate over the -40°C to +85°C temperature range.

Applications

LCD TV Panels

Features

- **8.0V to 16.5V IN Supply-Voltage Range**
- **Selectable Frequency (500kHz/750kHz)**
- **Current-Mode Step-Up Regulator**
  - **Fast Load-Transient Response**
  - **High-Accuracy Output Voltage (1.0%)**
  - **Built-In 20V, 4.2A, 100mΩ MOSFET**
  - **High Efficiency**
  - **Adjustable Soft-Start**
  - **Adjustable Current Limit**
  - **Low Duty-Cycle Operation (13.2V_{IN} - 13.5V AVDD)**
- **Current-Mode Step-Down Regulator**
  - **Fast Load-Transient Response**
  - **Built-In 20V, 3.2A, 100mΩ MOSFET**
  - **High Efficiency**
  - **3ms Internal Soft-Start**
- **Adjustable Positive Charge-Pump Regulator**
- **Adjustable Negative Charge-Pump Regulator**
- **Integrated High-Voltage Switch with Adjustable Turn-On Delay**
- **High-Speed Operational Amplifier**
  - **±200mA Short-Circuit Current**
  - **45V/µs Slew Rate**
- **High-Accuracy Reference for Gamma Buffer**
  - **±1% Feedback Voltage**
  - **Up to 30mA Load Current**
  - **Low-Dropout Voltage 0.5V at 60mA**
- **External p-Channel Gate Control for AVDD Sequencing**
- **PGOOD Comparator**
- **Input Undervoltage Lockout and Thermal-Overload Protection**
- **48-Pin, 7mm x 7mm, Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17126ETM+	-40°C to +85°C	48 Thin QFN-EP*
MAX17126AETM+	-40°C to +85°C	48 Thin QFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

INVL, IN2, VOP, EN, FSEL to GND .....-0.3V to +24V
PGND, OGND, CPGND to GND .....-0.3V to +0.3V
DLY1, GVOFF, THR, VL to GND .....-0.3V to +7.5V
REF, FBP, FBN, FB1, FB2, COMP, SS, CLIM,
PGOOD, VDET, VREF_FB, OUT to GND.....-0.3V, (V_L+ 0.3)
GD, GD_I to GND.....-0.3V to +24V
LX1 to PGND.....-0.3V to +24V
OPP, OPN, OPO to OGND..... -0.3V to VOP + 0.3V
DRVP to CPGND ..... -0.3V to SUPP + 0.3V
DRVN to CPGND.....-0.3V to SUPN + 0.3V
LX2 to PGND.....-0.7 to (IN2 + 0.3V)
SUPN to GND.....-0.3V to (IN2 + 0.3V)
SUPP to GND .....-0.3V to (GD_I + 0.3V)
BST to VL.....-0.3V to +30V
VGH to GND.....-0.3V to +40V
VGHM, DRN to GND ..... -0.3V, VGH + 0.3V
VGHM to DRN .....-0.3V to +40V
VREF_I to GND.....-0.3V to +24V
VREF_O to GND.....-0.3V, (V_{REF_I} + 0.3)V
REF Short Circuit to GND.....Continuous
RMS LX1 Current (total for both pins).....3.2 A
RMS PGND CURRENT (total for both pins).....3.2 A
RMS IN2 Current (total for both pins) .....3.2 A
RMS LX2 Current (total for both pins).....3.2 A
RMS DRVN, DRVP Current 0.8A
RMS VL Current.....50mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFN
(derated 38.5mW/°C above +70°C).....3076.9mW
Junction Temperature .....+160°C
Storage Temperature Range..... -65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{INVL}= V_{IN2} = 12V, V_{VOP} = V_{VREF_I} = 15V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
INVL, IN2 Input-Voltage Range		8		16.5	V
INVL + IN2 Quiescent Current	Only LX2 switching (V_{FB1} = V_{FBP} = 1.5V, V_{FBN} = 0V) EN = VL, FSEL = high		8.5	20	mA
INVL + IN2 Standby Current	LX2 not switching (V_{FB1} = V_{FB2} = V_{FBP} = 1.5V, V_{FBN} = 0V), EN = VL, FSEL = high		24	5	mA
SMPS Operating Frequency	FSEL = INVL or high impedance	630	750	870	kHz
	FSEL = GND	420	500	580	
INVL Undervoltage-Lockout Threshold	INVL rising, 150mV typical hysteresis	6.0	7.0	8.0	V
VL REGULATOR					
VL Output Voltage	I_{VL} = 25mA, V_{FB1} = V_{FB2} = V_{FBP} = 1.1V, V_{FBN} = 0.4V (all regulators switching)	4.85	5	5.15	V
VL Undervoltage-Lockout Threshold	VL rising, 50mV typical hysteresis	3.5	3.9	4.3	V
REFERENCE					
REF Output Voltage	No external load	1.2375	1.250	1.2625	V
REF Load Regulation	0V < I_{LOAD} < 50µA			5	mV
REF Sink Current	In regulation	10			µA
REF Undervoltage-Lockout Threshold	Rising edge, 250mV typical hysteresis		1.0	1.2	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{INVL}= V_{IN2} = 12V, V_{VOP} = V_{VREF_I} = 15V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
STEP-DOWN REGULATOR						
OUT Voltage in Fixed Mode	FB2 = GND, no load (Note 1)	0°C < T_A = +85°C	3.25	3.3	3.35	V
		T_A = +25°C	3.267		3.333	
FB2 Voltage in Adjustable Mode	V_{OUT} = 2.5V, no load (Note 1)	0°C < T_A = +85°C	1.23	1.25	1.27	V
		T_A = +25°C	1.2375		1.2625	
FB2 Adjustable Mode Threshold Voltage	Dual Mode™ comparator		0.10	0.15	0.20	V
Output Voltage Adjust Range			1.5		5	V
FB2 Fault-Trip Level	Falling edge		0.96	1.0	1.04	V
FB2 Input Leakage Current	V_{FB2} = 1.25V		50	125	200	nA
DC Load Regulation	0V < I_{LOAD} < 2A			0.5		%
DC Line Regulation	No load, 10.8V < V_{IN2} < 13.2V			0.1		%/V
LX2-to-IN2 nMOS Switch On-Resistance				100	200	mΩ
LX2-to-GND2 nMOS Switch On-Resistance			6	10	23	Ω
BST-to-VL pMOS Switch On-Resistance			40	30	110	Ω
Low-Frequency Operation OUT Threshold	LX2 only			0.8		V
Low-Frequency Operation Switching Frequency	FSEL = INVL			125		kHz
	FSEL = GND			83		
LX2 Positive Current Limit	MAX17126		2.50	3.20	3.90	A
	MAX17126A		3.0	3.5	4.0	
Soft-Start Ramp Time	Zero to full limit			3		ms
Maximum Duty Factor			70	78	85	%
Minimum Duty Factor Char/Design Limit Only					10	%
STEP-UP REGULATOR						
Output Voltage Range			VIN		20	V
Oscillator Maximum Duty Cycle			70	78	85	%
FB1 Regulation Voltage	FB1 = COMP, C_{COMP} = 1nF		1.2375	1.25	1.2625	V
FB1 Fault Trip Level	Falling edge		0.96	1.0	1.04	V
FB1 Load Regulation	0V < I_{LOAD} < full			0.5		%
FB1 Line Regulation	10.8V < V_{IN} < 13.2V			0.08		%/V
FB1 Input Bias Current	V_{FB1} = 1.25V		30	125	200	nA
FB1 Transconductance	ΔI = ±2.5µA at COMP, FB1 = COMP		150	320	560	µS
FB1 Voltage Gain	FB1 to COMP			1400		V/V
LX1 Leakage Current	V_{FB1} = 1.5V, V_{LX1} = 20V			10	40	µA

Dual Mode is a trademark of Maxim Integrated Products, Inc.

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{INVL}= V_{IN2} = 12V, V_{VOP} = V_{VREF_I} = 15V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LX1 Current Limit	V_{FB1} = 1.1V, R_{CLIM} = unconnected	3.6	4.2	4.8	A
	V_{FB1} = 1.1V, with R_{CLIM} at CLIM pin	-20%	4.2 - (68k/ R_{CLIM})	+20%	
CLIM Voltage	R_{CLIM} = 60.5kΩ	0.56	0.625	0.69	V
Current-Sense Transresistance		0.19	0.21	0.25	V/A
LX1 On-Resistance			100	185	mΩ
Soft-Start Period	C_{SS} < 200pF		16		ms
SS Charge Current	V_{SS} = 1.2V	4	5	6	µA
POSITIVE CHARGE-PUMP REGULATORS					
GD_I Input Supply Range		8.0		20	V
GD_I Input Supply Current	V_{FBP} = 1.5V (not switching)		0.15	0.3	mA
GD_I Overvoltage Threshold	GD_I rising, 250mV typical hysteresis (Note 2)	20.1	21	22	V
FBP Regulation Voltage		1.2375	1.25	1.2625	V
FBP Line Regulation Error	V_{SUP} = 11V to 16V, not in dropout			0.2	%/V
FBP Input Bias Current	V_{FBP} = 1.5V, T_A = +25°C	-50		+50	nA
DRVP p-Channel MOSFET On-Resistance			1.5	3	Ω
DRVP n-Channel MOSFET On-Resistance			1	2	Ω
FBP Fault Trip Level	Falling edge	0.96	1.0	1.04	V
Positive Charge-Pump Soft-Start Period	7-bit voltage ramp with filtering to prevent high peak currents 500kHz frequency		4		ms
	750kHz frequency		3		ms
NEGATIVE CHARGE-PUMP REGULATORS					
FBN Regulation Voltage	V_{REF} - V_{FBN}	0.99	1.00	1.01	V
FBN Input Bias Current	V_{FBN} = 0mV, T_A = +25°C	-50		+50	nA
FBN Line Regulation Error	V_{IN2} = 11V to 16V, not in dropout			0.2	%/V
DRVN P_{CH} On-Resistance			1.5	3	Ω
DRVN N_{CH} On-Resistance			1	2	Ω
FBN Fault Trip Level	Rising edge	720	800	880	mV
Negative Charge-Pump Soft-Start Period	7-bit voltage ramp with filtering to prevent high peak currents 500kHz frequency		3		ms
	750kHz frequency		2		
AVDD SWITCH GATE CONTROL					
GD to GD_I Pullup Resistance	EN = GND		25	50	Ω
GD Output Sink Current	EN = VL	5	10	15	µA
GD Done Threshold	EN = VL, V_{GD_I} - V_{GD}	5	6	7	V
OPERATIONAL AMPLIFIERS					
VOP Supply Range		8		20	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{INVL}= V_{IN2} = 12V, V_{VOP} = V_{VREF_I} = 15V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VOP Overvoltage Fault Threshold	V_{VOP} = rising, hysteresis = 200mV (Note 2)	20.1	21	22	V
VOP Supply Current	Buffer configuration, V_{OPP} = V_{OPN} = VOP/2, no load		2	4	mA
Input Offset Voltage	2V < (V_{OPP}, V_{OPN}) < (V_{VOP} - 2V)		3	14	mV
Input Bias Current	2V < (V_{OPP}, V_{OPN}) < (V_{VOP} - 2V)	-1		+1	µA
Input Common-Mode Voltage Range		0		VOP	V
Input Common-Mode Rejection Ratio	2V < (V_{OPP}, V_{OPN}) < (V_{VOP} - 2V)		80		dB
Output Voltage Swing High	I_{OPO} = 25mA	VOP - 320	VOP - 150		mV
Output Voltage Swing Low	I_{OPO} = -25mA		150	300	mV
Large-Signal Voltage Gain	2V < (V_{OPP}, V_{OPN}) < (V_{OP} - 2V)		80		dB
Slew Rate	2V < (V_{OPP}, V_{OPN}) < (V_{OP} - 2V)		45		V/µs
-3dB Bandwidth	2V < (V_{OPP}, V_{OPN}) < (V_{OP} - 2V)		20		MHz
Short-Circuit Current	Short to V_{VOP}/2, sourcing	200			mA
	Short to V_{VOP}/2, sinking	200			
HIGH-VOLTAGE SWITCH ARRAY					
VGH Supply Range				35	V
VGH Supply Current			150	300	µA
VGHM-to-VGH Switch On-Resistance	V_{DLY1} = 2V, GVOFF = VL		5	10	Ω
VGHM-to-VGH Switch Saturation Current	V_{VGH} - V_{VGHM} > 5V	150	390		mA
VGHM-to-DRN Switch On-Resistance	V_{DLY1} = 2V, GVOFF = GND		20	50	Ω
VGHM-to-DRN Switch Saturation Current	V_{VGHM} - V_{DRN} > 5V	75	200		mA
VGHM-to-GND Switch On-Resistance	DLY1 = GND	1.0	2.5	4.0	kΩ
GVOFF Input Low Voltage				0.6	V
GVOFF Input High Voltage		1.6			V
GVOFF Input Current	V_{GVOFF} = 0V or VL, T_A = +25°C	-1		+1	µA
GVOFF-to-VGHM Rising Propagation Delay	1kΩ from DRN to CPGND, V_{GVOFF} = 0V to VL step, no load on VGHM, measured from GVOFF = 2V to VGHM = 20%		100		ns
GVOFF-to-VGHM Falling Propagation Delay	1kΩ from DRN to CPGND, V_{GVOFF} = VL to 0V step, no load on VGHM, DRN falling, no load on DRN and VGHM, measured from V_{GVOFF} = 0.6V to VGHM = 80%		200		ns
THR-to-VGHM Voltage Gain		9.4	10	10.6	V/V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{INVL}= V_{IN2} = 12V, V_{VOP} = V_{VREF_I} = 15V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SEQUENCE CONTROL					
EN Pulldown Resistance			1		MΩ
DLY1 Charge Current	V_{DLY1} = 1V; when DLY1 cap is not used, there is no delay	6	8	10	µA
EN, DLY1 Turn-On Threshold		1.19	1.25	1.31	V
DLY1 Discharge Switch On-Resistance	EN = GND or fault tripped		10		Ω
FBN Discharge Switch On-Resistance	(EN = GND and INVL < UVLO) or fault tripped		3		kΩ
GAMMA REFERENCE					
VREF_I Input-Voltage Range		10		18.0	V
VREF_I Input Bias Current	No load		125	250	µA
VREF_O Dropout Voltage	I_{VREF_O} = 60mA		0.25	0.5	V
VREF_FB Regulation Voltage	V_{VREF_I} = 13.5V, 1mA ≤ I_{VREF_O} ≤ 30mA, V_{VREF_O} = 9.5V	1.243	1.250	1.256	V
	V_{VREF_I} from 10V to 18V, I_{VREF_O} = 20mA, V_{VREF_O} = 9.5V			≤ 0.9	mV/V
VREF_O Maximum Output Current		60			mA
PGOOD FUNCTION					
VDET Threshold	VDET rising	1.274	1.3	1.326	V
VDET Hysteresis			50		mV
VDET Input Bias Current		50	175	300	nA
PGOOD Output Voltage	VDET = AGND, I_{PGOOD} = 1mA			0.4	V
FAULT DETECTION					
Duration-to-Trigger Fault	For UVP only		50		ms
Step-Up Short-Circuit Protection	FB1 falling edge	0.36 x V_{REF}	0.4 x V_{REF}	0.44 x V_{REF}	V
Step-Down Short-Circuit Protection	Adjustable mode FB2 falling	0.18 x V_{REF}	0.2 x V_{REF}	0.22 x V_{REF}	V
	Fixed mode OUT falling, internal feedback divider voltage	0.18 x V_{REF}	0.2 x V_{REF}	0.22 x V_{REF}	
Positive Charge-Pump Short-Circuit Protection	FBP falling edge	0.36 x V_{REF}	0.4 x V_{REF}	0.44 x V_{REF}	V
Negative Charge-Pump Short-Circuit Protection	V_{REF} - V_{FBN}	0.4	0.45	0.5	V
Thermal-Shutdown Threshold	Latch protection		+160		°C

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{INVL}= V_{IN2} = 12V, V_{VOP} = V_{VREF_I} = 15V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING FREQUENCY SELECTION					
FSEL Input Low Voltage	500kHz			0.6	V
FSEL Input High Voltage	750kHz	1.6			V
FSEL Pullup Resistance			1		MΩ

ELECTRICAL CHARACTERISTICS

(V_{INVL} = V_{IN2} = 12V, V_{VOP} = V_{VREF_I} = 15V, **T_A = -40°C to +85°C**.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
INVL, IN2 Input-Voltage Range		8		16.5	V
SMPS Operating Frequency	FSEL = INVL or high impedance	630		870	kHz
	FSEL = GND	420		580	
INVL Undervoltage-Lockout Threshold	INVL rising, 150mV typical hysteresis	6.0		8.0	V
VL REGULATOR					
VL Output Voltage	I_{VL} = 25mA, V_{FB1} = V_{FB2} = V_{FB} = 1.1V, V_{FBN} = 0.4V (all regulators switching)	4.85		5.15	V
VL Undervoltage-Lockout Threshold	VL rising, 50mV typical hysteresis	3.5		4.3	V
REFERENCE					
REF Output Voltage	No external load	1.235		1.265	V
REF Undervoltage-Lockout Threshold	Rising edge, 25mV typical hysteresis			1.2	V
STEP-DOWN REGULATOR					
OUT Voltage in Fixed Mode	FB2 = GND, no load (Note 1)	3.267		3.333	V
FB2 Voltage in Adjustable Mode	V_{OUT} = 2.5V, no load (Note 1)	1.2375		1.2625	V
FB2 Adjustable Mode Threshold Voltage	Dual-mode comparator	0.10		0.20	V
Output Voltage Adjust Range		1.5		5	V
FB2 Fault Trip Level	Falling edge	0.96		1.04	V
LX2-to-IN2 nMOS Switch On-Resistance				200	mΩ
LX2-to-GND2 nMOS Switch On-Resistance		6		23	Ω
BST-to-VL pMOS Switch On-Resistance		40		110	Ω
LX2 Positive Current Limit	MAX17126	2.50		3.90	A
	MAX17126A	3.0		4.0	
Maximum Duty Factor		70		85	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{INVL} = V_{IN2} = 12V, V_{VOP} = V_{VREF_I} = 15V, **T_A = -40°C to +85°C**.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STEP-UP REGULATOR					
Output-Voltage Range		VIN		20	V
Oscillator Maximum Duty Cycle		70		85	%
FB1 Regulation Voltage	FB1 = COMP, C_{COMP} = 1nF	1.2375		1.2625	V
FB1 Fault Trip Level	Falling edge	0.96		1.04	V
FB1 Transconductance	ΔI = ±2.5µA at COMP, FB1 = COMP	150		560	µS
LX1 Input Bias Current	V_{FB1} = 1.5V, V_{LX1} = 20V			40	µA
LX1 Current Limit	V_{FB1} = 1.1V, R_{CLIM} = unconnected	3.6		4.8	A
	V_{FB1} = 1.1V , with R_{CLIM} at CLIM pin, limit = 3.5A - (60.5K/R_{CLIM})	-20%		+20%	
CLIM Voltage	R_{CLIM} = 60.5kΩ	0.56		0.69	V
Current-Sense Transresistance		0.19		0.25	V/A
LX1 On-Resistance				185	mΩ
SS Charge Current	V_{SS} = 1.2V	4		6	µA
POSITIVE CHARGE-PUMP REGULATORS					
GD_I Input Supply Range		8.0		20	V
GD_I Input Supply Current	V_{FBP} = 1.5V (not switching)			0.2	mA
GD_I Overvoltage Threshold	GD_I rising, 250mV typical hysteresis (Note 2)	20.1		22	V
FBP Regulation Voltage		1.243		1.256	V
FBP Line Regulation Error	V_{SUP} = 11V to 16V, not in dropout			0.2	%/V
DRVP p-Channel MOSFET On-Resistance				3	Ω
DRVP n-Channel MOSFET On-Resistance				1	Ω
FBP Fault Trip Level	Falling edge	0.96		1.04	V
NEGATIVE CHARGE-PUMP REGULATORS					
FBN Regulation Voltage	V_{REF} - V_{FBN}	0.99		1.01	V
FBN Line Regulation Error	V_{IN2} = 11V to 16V, not in dropout			0.2	%/V
DRVN P_{CH} On-Resistance				3	Ω
DRVN N_{CH} On-Resistance				1	Ω
FBN Fault Trip Level	Rising edge	720		880	mV
AVDD SWITCH GATE CONTROL					
GD Output Sink Current	EN = VL	5		15	µA
GD Done Threshold	EN = VL, VGD_I - VGD	5		7	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{INVL} = V_{IN2} = 12V, V_{VOP} = V_{VREF_I} = 15V, **T_A = -40°C to +85°C**.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATIONAL AMPLIFIERS					
VOP Supply Range		8		20	V
VOP Overvoltage Fault Threshold	V_{OP} = rising, hysteresis = 200mV (Note 2)	20.1		22	V
VOP Supply Current	Buffer configuration, V_{OPP} = V_{OPN} = V_{OP}/2, no load			4	mA
Input Offset Voltage	2V < (V_{OPP}, V_{OPN}) < (V_{OP} - 2V)			14	mV
Input Common-Mode Voltage Range		0		OVIN	V
Output Voltage Swing High	I_{OPO} = 25mA	VOP - 320			mV
Output Voltage Swing Low	I_{OPO} = -25mA			300	mV
Short-Circuit Current	Short to V_{OPO}/2, sourcing	200			mA
	Short to V_{OPO}/2, sinking	200			
HIGH-VOLTAGE SWITCH ARRAY					
VGH Supply Range				35	V
VGH Supply Current				300	µA
VGHM-to-VGH Switch On-Resistance	V_{DLY1} = 2V, GVOFF = VL			10	Ω
VGHM-to-VGH Switch Saturation Current	V_{VGH} - V_{VGHM} > 5V	150			mA
VGHM-to-DRN Switch On-Resistance	V_{DLY1} = 2V, GVOFF = GND			50	Ω
VGHM-to-DRN Switch Saturation Current	V_{VGHM} - V_{DRN} > 5V	75			mA
VGHM-to-GND Switch On-Resistance	DLY1 = GND	1.0		4.0	kΩ
GVOFF Input Low Voltage				0.6	V
GVOFF Input High Voltage		1.6			V
THR-to-VGHM Voltage Gain		9.4		10.6	V/V
SEQUENCE CONTROL					
EN Input Low Voltage				0.6	V
EN Input High Voltage		1.6			V
DLY1 Charge Current	V_{DLY1} = 1V; when DLY1 cap is not used, there is no delay	6		10	µA
DLY1 Turn-On Threshold		1.19		1.31	V

Multi-Output Power Supplies with VCOM Amplifier and High-Voltage Gamma Reference for LCD TVs

ELECTRICAL CHARACTERISTICS (continued)

(V_{INVL} = V_{IN2} = 12V, V_{VOP} = V_{VREF_I} = 15V, **T_A = -40°C to +85°C**.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GAMMA REFERENCE					
VREF_I Input Voltage Range		10		18.0	V
VREF_I Undervoltage Lockout	VREF_I rising			5.2	V
VREF_I Input Bias Current	No load			250	µA
VREF_O Dropout Voltage	I_{VREF_O} = 60mA			0.5	V
VREF_FB Regulation Voltage	V_{REF_I} = 13.5V, 1mA ≤ I_{VREF_O} ≤ 30mA	1.2375		1.2625	V
	V_{REF_I} from 10V to 18V, I_{VREF_O} = 20mA			≤ 0.9	mV/V
VREF_O Maximum Output Current		60			mA
PGOOD FUNCTION					
VDET Threshold	VDET rising	1.274		1.326	V
PGOOD Output Voltage	VDET = AGND, I_{PGOOD} = 1mA			0.4	V
FAULT DETECTION					
Step-Up Short-Circuit Protection	FB1 falling edge	0.36 x V_{REF}		0.44 x V_{REF}	V
Step-Down Short-Circuit Protection	Adjustable mode FB2 falling	0.18 x V_{REF}		0.22 x V_{REF}	V
	Fixed mode OUT falling, internal feedback divider voltage	0.18 x V_{REF}		0.22 x V_{REF}	V
Positive Charge-Pump Short-Circuit Protection	FBP falling edge	0.36 x V_{REF}		0.44 x V_{REF}	V
Negative Charge-Pump Short-Circuit Protection	V_{REF} - V_{FBN}	0.4		0.5	V
SWITCHING FREQUENCY SELECTION					
FSEL Input Low Voltage	500kHz			0.6	V
FSEL Input High Voltage	750kHz	1.6			V

Note 1: When the step-down inductor is in continuous conduction (EN = VL or heavy load), the output voltage has a DC regulation level lower than the error comparator threshold by 50% of the output voltage ripple. In discontinuous conduction (EN = GND with light load), the output voltage has a DC regulation level higher than the error comparator threshold by 50% of the output voltage ripple.

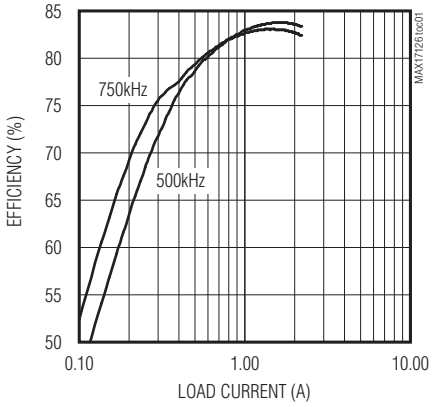
Note 2: Disables boost switching if either GD_I or VOP exceeds the threshold. Switching resumes when no threshold is exceeded.

Note 3: Specifications to T_A = -40°C are guaranteed by design, not production tested.

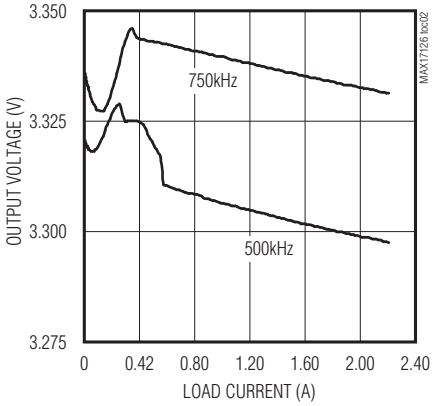
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

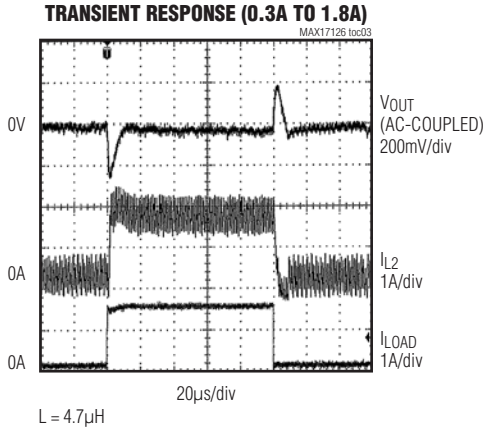
STEP-DOWN REGULATOR EFFICIENCY vs. LOAD CURRENT



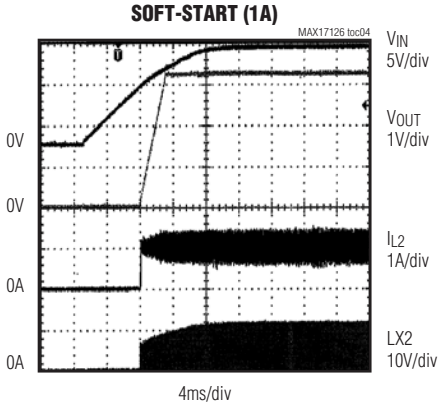
STEP-DOWN REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



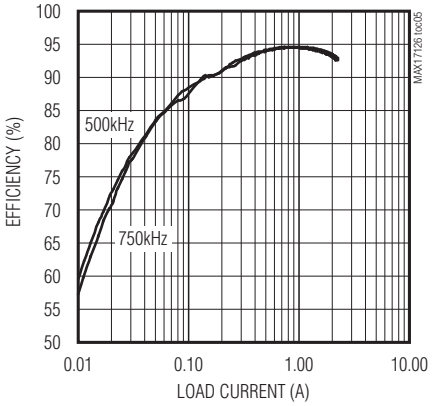
STEP-DOWN REGULATOR LOAD TRANSIENT RESPONSE (0.3A TO 1.8A)



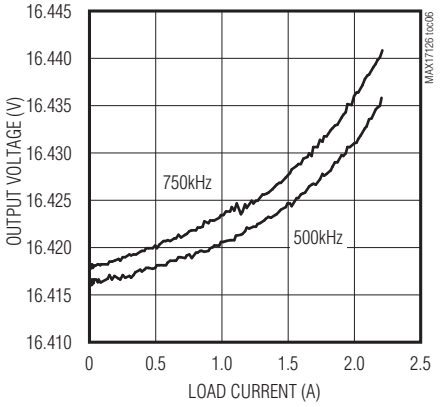
STEP-DOWN REGULATOR HEAVY-LOAD SOFT-START (1A)



STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT



STEP-UP REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT

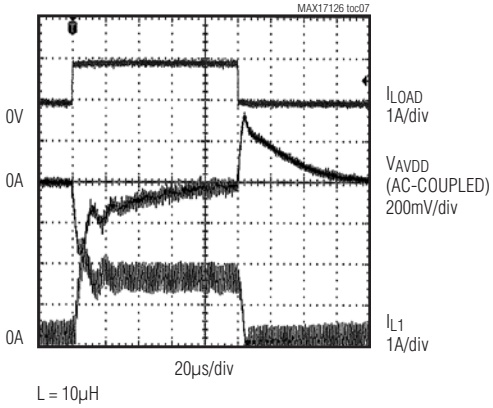


Multi-Output Power Supplies with VCOM Amplifier and High-Voltage Gamma Reference for LCD TVs

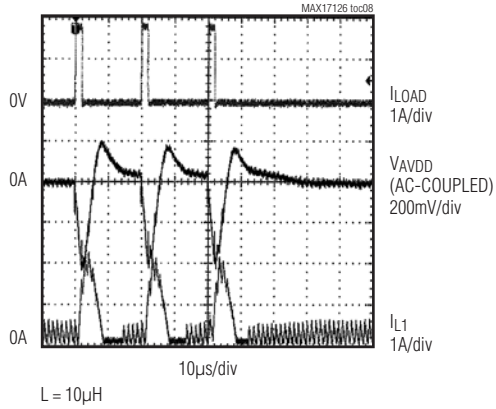
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

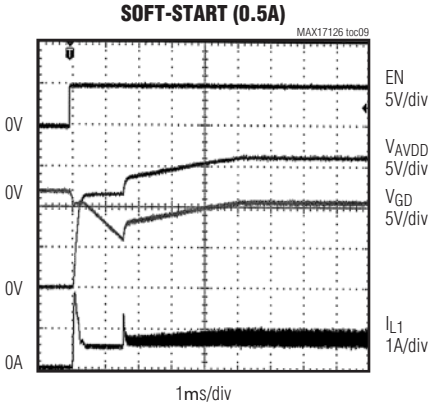
STEP-UP REGULATOR LOAD TRANSIENT RESPONSE (0.1A TO 1.1A)



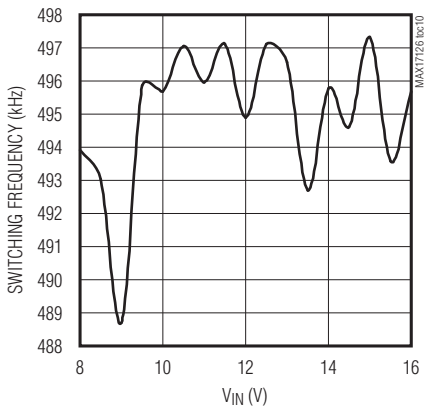
STEP-UP REGULATOR PULSED LOAD TRANSIENT RESPONSE (0.1A TO 1.9mA)



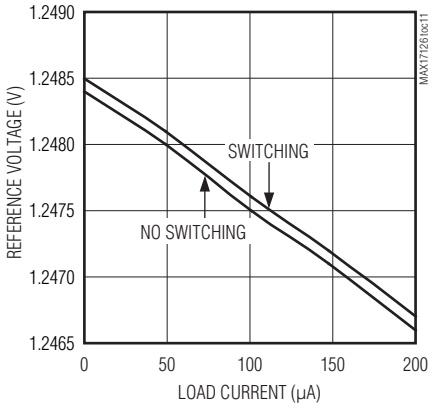
STEP-UP REGULATOR HEAVY LOAD SOFT-START (0.5A)



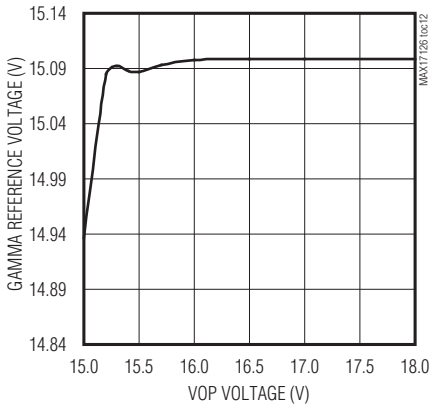
SWITCHING FREQUENCY vs. INPUT VOLTAGE



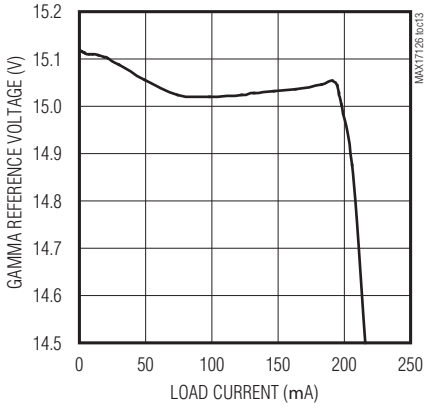
REFERENCE VOLTAGE LOAD REGULATION



GAMMA REFERENCE LINE REGULATION (LOAD = 20mA)



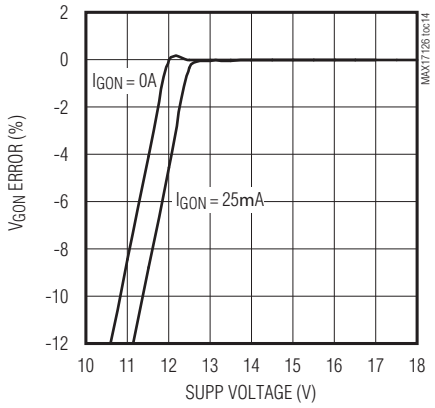
GAMMA REFERENCE LOAD REGULATION (V_{REF} = 16V)



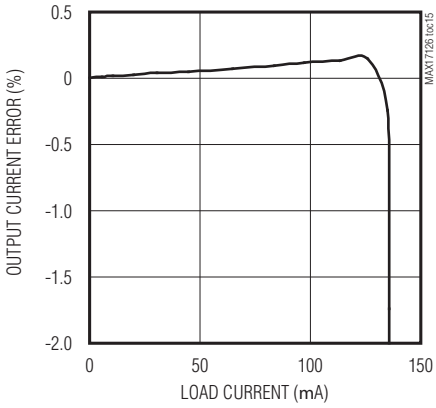
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

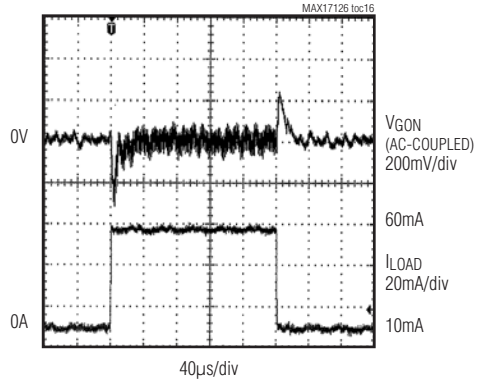
POSITIVE CHARGE-PUMP REGULATOR NORMALIZED LINE REGULATION



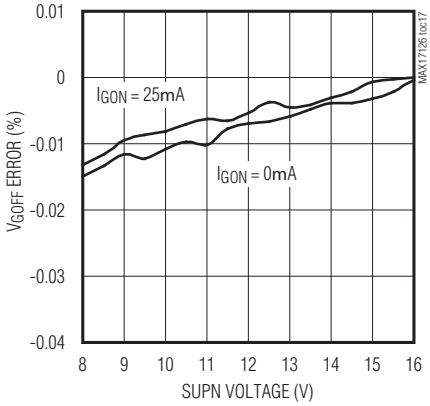
POSITIVE CHARGE-PUMP REGULATOR NORMALIZED LOAD REGULATION



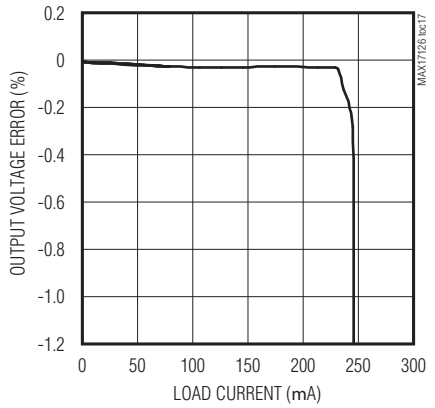
POSITIVE CHARGE-PUMP REGULATOR LOAD-TRANSIENT RESPONSE



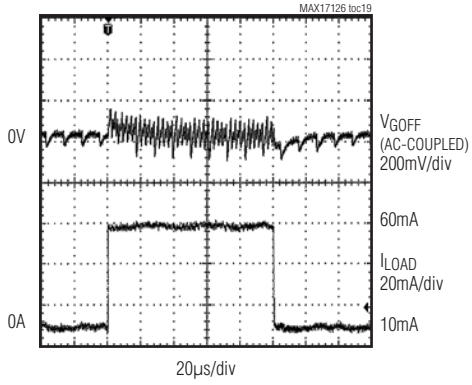
NEGATIVE CHARGE-PUMP REGULATOR NORMALIZED LINE REGULATION



NEGATIVE CHARGE-PUMP REGULATOR NORMALIZED LOAD REGULATION



NEGATIVE CHARGE-PUMP REGULATOR LOAD TRANSIENT RESPONSE

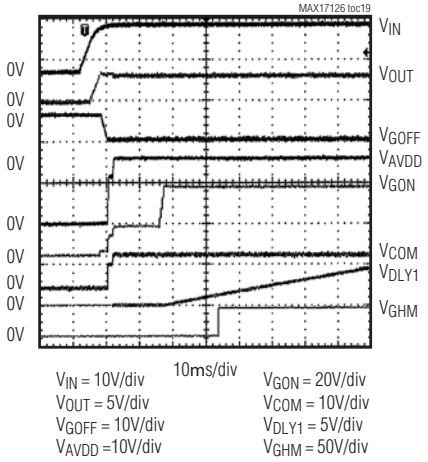


Multi-Output Power Supplies with VCOM Amplifier and High-Voltage Gamma Reference for LCD TVs

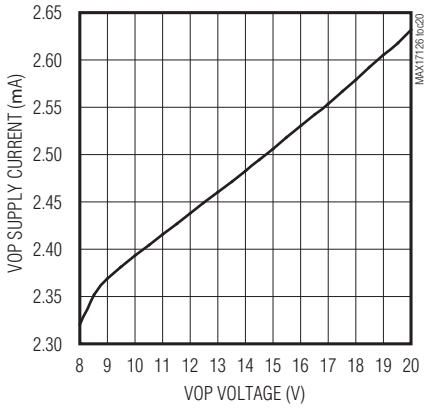
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

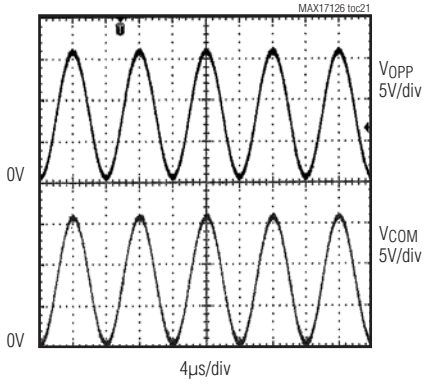
POWER-UP SEQUENCE OF ALL SUPPLY OUTPUTS



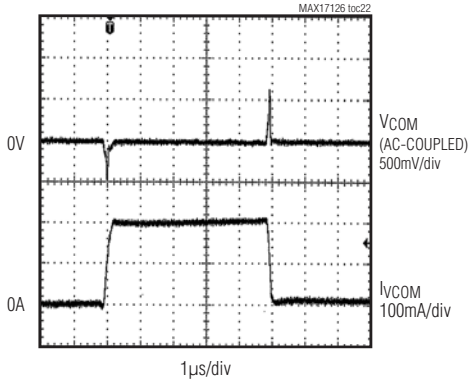
OP AMP SUPPLY CURRENT vs. SUPPLY VOLTAGE



OPERATIONAL AMPLIFIER RAIL-TO-RAIL INPUT/OUTPUT WAVEFORMS



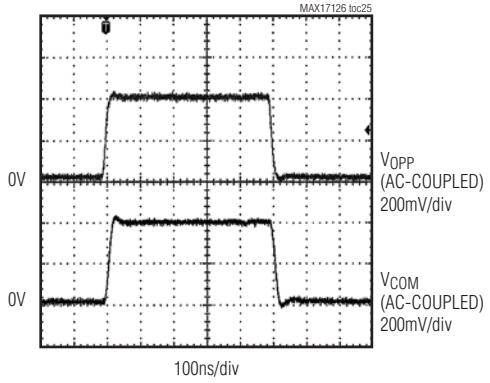
OPERATIONAL AMPLIFIER LOAD TRANSIENT RESPONSE



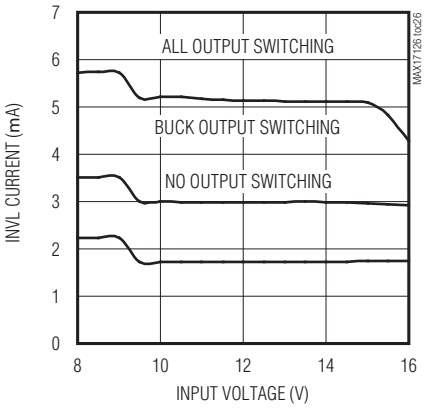
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

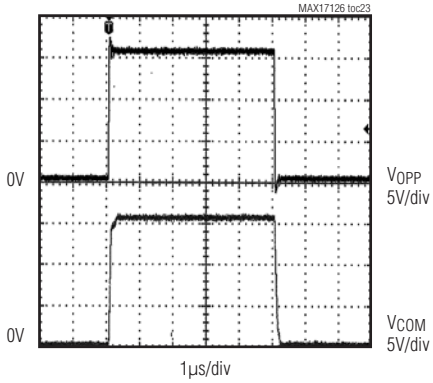
OPERATIONAL AMPLIFIER SMALL-SIGNAL STEP RESPONSE



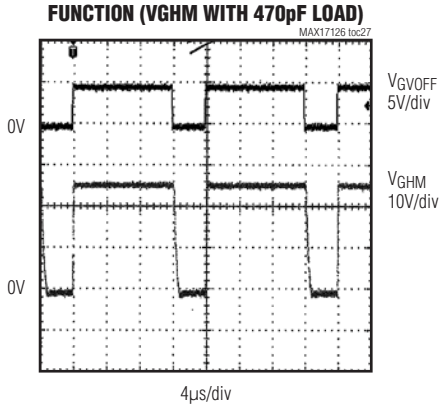
VIN SUPPLY CURRENT vs. VIN VOLTAGE



OPERATIONAL AMPLIFIER LARGE-SIGNAL STEP RESPONSE



HIGH-VOLTAGE SWITCH CONTROL FUNCTION (VGHM WITH 470pF LOAD)



Multi-Output Power Supplies with VCOM Amplifier and High-Voltage Gamma Reference for LCD TVs

Pin Description

PIN	NAME	FUNCTION
1	VREF_I	Gamma Reference Input
2	VOP	Operational Amplifier Power Supply
3	OGND	Operational Amplifier Power Ground
4	OPP	Operational Amplifier Noninverting Input
5	OPN	Operational Amplifier Inverting Input
6	OPO	Operational Amplifier Output
7	PGOOD	Input voltage power-good open-drain output pulled high to VL or 3.3V through 10kΩ resistor.
8	GVOFF	High-Voltage Switch-Control Block Timing Control Input. See the *High-Voltage Switch Control* section for details.
9	EN	Enable Input. Enable is high, turns on step-up converter and positive charge pump.
10	FB2	Step-Down Regulator Feedback Input. Connect FB2 to GND to select the step-down converter's 3.3V fixed mode. For adjustable mode, connect FB2 to the center of a resistive voltage-divider between the step-down regulator output (OUT) and GND to set the step-down regulator output voltage. Place the resistive voltage-divider within 5mm of FB2.
11	OUT	Step-Down Regulator Output Voltage Sense. Connect OUT to step-down regulator output.
12	N.C.	Not Connected
13, 14	LX2	Step-Down Regulator Switching Node. LX2 is the source of the internal n-channel MOSFET connected between IN2 and LX2. Connect the inductor and Schottky catch diode to both LX2 pins and minimize the trace area for lowest EMI.
15	BST	Step-Down Regulator Bootstrap Capacitor Connection. Power supply for high-side gate driver. Connect a 0.1µF ceramic capacitor from BST to LX2.
16, 17	IN2	Step-Down Regulator Power Input. Drain of the internal n-channel MOSFET connected between IN2 and LX2.
18, 44	GND	Analog Ground
19	VDET	Voltage-Detector Input. Connects VDET to the center of a resistor voltage-divider between input voltage and GND to set the trigger point of PGOOD.
20	INVL	Internal 5V Linear Regulator and the Startup Circuitry Power Supply. Bypass V_{INVL} to GND with 0.22µF close to the IC.
21	VL	5V Internal Linear Regulator Output. Bypass VL to GND with 1µF minimum. Provides power for the internal MOSFET driving circuit, the PWM controllers, charge-pump regulators, logic, and reference and other analog circuitry. Provides 25mA load current when all switching regulators are enabled. VL is active whenever input voltage is high enough.
22	FSEL	Frequency Select Pin. Connect FSEL to VL or INVL or float FSEL pin for 750kHz operation. Connect to GND for 500kHz operation.
23	CLIM	Boost Current-Limit Setting Input. Connects a resistor from CLIM to GND to set current limit for boost converter.
24	SS	Soft-Start Input. Connects a capacitor from SS to GND to set the soft-start time for the step-up converter. A 5µA current source starts to charge C_{SS} when GD is done. See the *Step-Up Regulator External pMOS Pass Switch* section for description. SS is internally pulled to GND through 1kΩ resistance when EN is low OR when VL is below its UVLO threshold.
25, 26	LX1	Step-Up Regulator Power-MOSFET n-Channel Drain and Switching Node. Connects the inductor and Schottky catch diode to both LX1 pins and minimizes the trace area for lowest EMI.
27, 28	PGND	Step-Up Regulator Power Ground
29	GD_I	Step-Up Regulator External pMOS Pass Switch Source Input. Connects to the cathode of the step-up regulator Schottky catch diode.

Pin Description (continued)

PIN	NAME	FUNCTION
30	GD	Step-Up Regulator External pMOS Pass Switch Gate Input. A 10µA ≤ 20% current source pulls down on the gate of the external pFET when EN is high.
31	FB1	Boost Regulator Feedback Input. Connects FB1 to the center of a resistive voltage-divider between the boost regulator output and GND to set the boost regulator output voltage. Place the resistive voltage-divider within 5mm of FB1.
32	COMP	Compensation Pin for the Step-Up Regulator Error Amplifier. Connects a series resistor and capacitor from COMP to ground.
33	THR	VGHM Low-Level Regulation Set-Point Input. Connects THR to the center of a resistive voltage-divider between AVDD and GND to set the V_{GHM} falling regulation level. The actual level is 10 x V_{THR}. See the *Switch Control* section for details.
34	SUPP	Positive Charge-Pump Drivers Power Supply. Connects to the output of the boost regulator (AVDD) and bypasses to CPGND with a 0.1µF capacitor. SUPP is internally connected to GD_I.
35	CPGND	Charge Pump and Buck Power Ground
36	DRVP	Positive Charge-Pump Driver Output. Connects DRVP to the positive charge-pump flying capacitor(s).
37	DLY1	High-Voltage Switch Array Delay Input. Connects a capacitor from DLY1 to GND to set the delay time between when the positive charge pump finishes its soft-start and the startup of this high-voltage switch array. A 10µA current source charges C_{DLY1}. DLY1 is internally pulled to GND through 50Ω resistance when EN is low or when VL is below its UVLO threshold.
38	FBP	Positive Charge-Pump Regulator Feedback Input. Connects FBP to the center of a resistive voltage-divider between the positive charge-pump regulator output and GND to set the positive charge-pump regulator output voltage. Place the resistive voltage-divider within 5mm of FBP.
39	VGH	Switch Input. Source of the internal high-voltage p-channel MOSFET between VGH and VGHM.
40	VGHM	Internal High-Voltage MOSFET Switch Common Terminal. VGHM is the output of the high-voltage switch-control block.
41	DRN	Switch Output. Drain of the internal high-voltage p-channel MOSFET connected to VGHM.
42	SUPN	Negative Charge-Pump Drivers Power Supply. Bypass to CPGND with a 0.1µF capacitor. SUPN is internally connected to IN2.
43	DRVN	Negative Charge-Pump Driver Output. Connects DRVN to the negative charge-pump flying capacitor(s).
45	FBN	Negative Charge-Pump Regulator Feedback Input. Connect FBN to the center of a resistive voltage-divider between the negative output and REF to set the negative charge-pump regulator output voltage. Place the resistive voltage-divider within 5mm of FBN.
46	REF	Reference Output. Connects a 0.22µF capacitor from REF to GND. All power outputs are disabled until REF exceeds its UVLO threshold.
47	VREF_FB	Gamma Reference Feedback Input. Connect VREF_FB to the center of a resistive voltage-divider between VREF_O and GND to set the gamma reference output voltage. Place the resistive voltage-divider within 5mm of VREF_FB.
48	VREF_O	Gamma Reference Output
—	EP	Exposed Pad. Connects EP to GND, and ties EP to a copper plane or island. Maximizes the area of this copper plane or island to improve thermal performance.

Multi-Output Power Supplies with VCOM Amplifier and High-Voltage Gamma Reference for LCD TVs

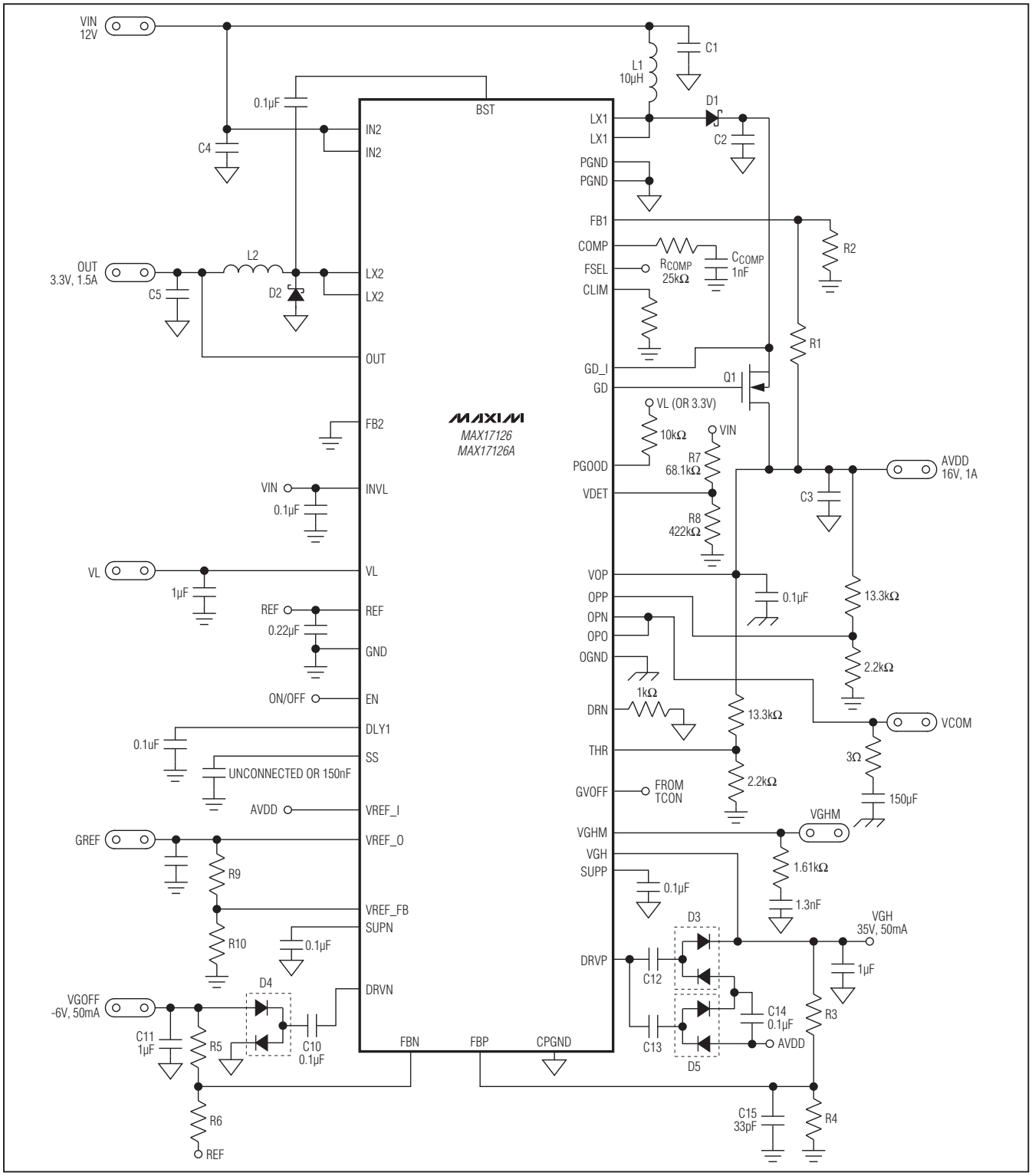


Figure 1. Typical Operating Circuit

Typical Operating Circuit

The typical operating circuit (Figure 1) of the MAX17126/MAX17126A comprise a complete power-supply system for TFT LCD TV panels. The circuit generates a +3.3V logic supply, a +16V source driver supply, a +35V positive gate-driver supply, a -6V negative gate-driver supply, and a ≤ 0.5% high-accuracy, high-voltage gamma reference. Table 1 lists some selected components and Table 2 lists the contact information for component suppliers.

Table 1. Component List

DESIGNATION	DESCRIPTION
C1–C4	10µF ≤ ±10%, 25V X5R ceramic capacitors (1206) Murata GRM31CR61E106K TDK C3216X5R1E106M
C5	22µF ±10%, 6.3V X5R ceramic capacitor (0805) Murata GRM21BR60J226K TDK C2012X5R0J226K
D1, D2	Schottky diodes 30V, 3A (M-flat) Toshiba CMS02
D3, D4, D5	Dual diodes 30V, 200mA (3 SOT23) Zetex BAT54S Fairchild BAT54S
L1	Inductor, 10µH, 3A, 45mΩ inductor (8.3mm x 9.5mm x 3mm) Coiltronics SD8328-100-R Sumida CDRH8D38NP-100N (8.3mm x 8.3mm x 4mm)
L2	Inductor, 4.7µH, 3A, 24.7mΩ inductor (8.3mm x 9.5mm x 3mm) Coiltronics SD8328-4R7-R Sumida CDRH8D38NP-4R7N (8.3mm x 8.3mm x 4mm)

Detailed Description

The MAX17126/MAX17126A are multiple-output power supplies designed primarily for TFT LCD TV panels. It contains a step-down switching regulator to generate the supply for system logic, a step-up switching regulator to generate the supply for source driver, and two charge-pump regulators to generate the supplies for TFT gate drivers, a high-accuracy, high-voltage reference supply for gamma correction. Each regulator features adjustable output voltage, digital soft-start, and timer-delayed fault protection. Both the step-down and step-up regulators use fixed-frequency current-mode control architecture. The two switching regulators are 180° out of phase to minimize the input ripple. The internal oscillator offers two pin-selectable frequency options (500kHz/750kHz), allowing users to optimize their designs based on the specific application requirements. The step-up regulator also features adjustable current limit that can be adjusted through a resistor at the CLIM pin. The MAX17126/MAX17126A include one high-performance operational amplifier designed to drive the LCD backplane (VCOM). The amplifier features high-output current (≤ 200mA), fast slew rate (45V/µs), wide bandwidth (20MHz), and rail-to-rail outputs. The high-accuracy, high-voltage gamma reference has its error controlled to within ≤ 0.5% and can deliver more than 60mA current. In addition, the MAX17126/MAX17126A feature a high-voltage switch-control block, an internal 5V linear regulator, a 1.25V reference output, well-defined power-up and power-down sequences, and fault and thermal-overload protection. Figure 2 shows the MAX17126/MAX17126A functional diagram.

Table 2. Operating Mode

SUPPLIER	PHONE	FAX	WEBSITE
Fairchild Semiconductor	408-822-2000	408-822-2102	www.fairchildsemi.com
Sumida Corp.	847-545-6700	847-545-6720	www.sumida.com
TDK Corp.	847-803-6100	847-390-4405	www.component.tdk.com
Toshiba America Electronic Components, Inc.	949-455-2000	949-859-3963	www.toshiba.com/taec

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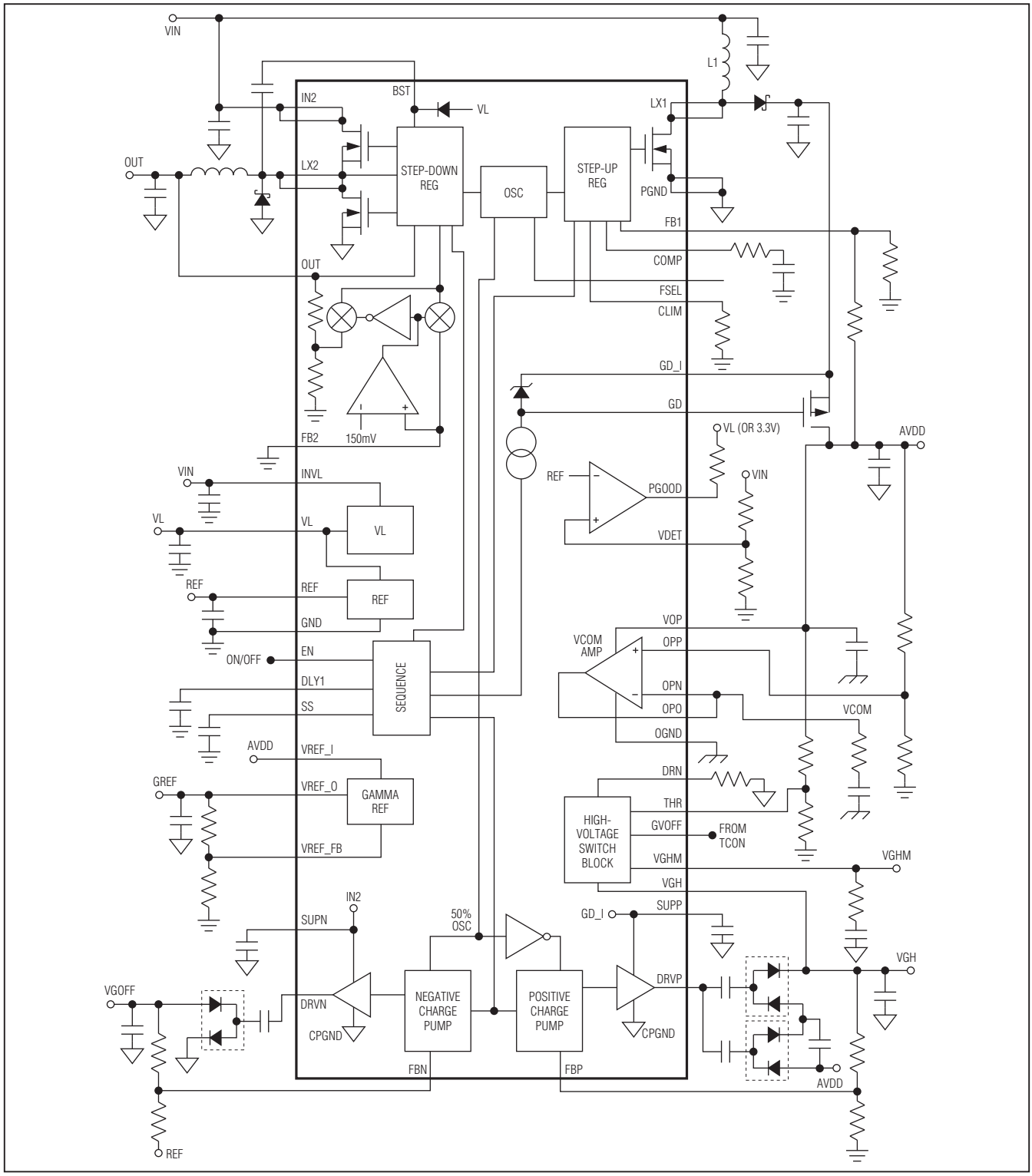

Figure 2. Functional Diagram

Step-Down Regulator

The step-down regulator consists of an internal n-channel MOSFET with gate driver, a lossless current-sense network, a current-limit comparator, and a PWM controller block. The external power stage consists of a Schottky diode rectifier, an inductor, and output capacitors. The output voltage is regulated by changing the duty cycle of the high-side MOSFET. A bootstrap circuit that uses a 0.1µF flying capacitor between LX2 and BST provides the supply voltage for the high-side gate driver. Although the MAX17126/MAX17126A also include a 10Ω (typ) low-side MOSFET, this switch is used to charge the bootstrap capacitor during startup and maintains fixed-frequency operation at light load and cannot be used as a synchronous rectifier. An external Schottky diode (D2 in Figure 1) is always required.

PWM Controller Block

The heart of the PWM control block is a multi-input, open-loop comparator that sums three signals: the output-voltage signal with respect to the reference voltage, the current-sense signal, and the slope-compensation signal. The PWM controller is a direct-summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage.

The step-down controller always operates in fixed-frequency PWM mode. Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch until the PWM comparator changes state. As the high-side switch turns off, the low-side switch turns on. The low-side switch stays on until the beginning of the next clock cycle.

Current Limiting and Lossless Current Sensing

The current-limit circuit turns off the high-side MOSFET switch whenever the voltage across the high-side MOSFET exceeds an internal threshold. The actual current limit is typically 3.2A for MAX17126 and 3.5A for MAX17126A.

For current-mode control, an internal lossless sense network derives a current-sense signal from the inductor DCR. The time constant of the current-sense network is not required to match the time constant of the inductor and has been chosen to provide sufficient current ramp signal for stable operation at both operating frequencies. The current-sense signal is AC-coupled into the PWM comparator, eliminating most DC output-voltage variation with load current.

Dual-Mode Feedback

The step-down regulator of the MAX17126/MAX17126A support both fixed output and adjustable output. Connect FB2 to GND to enable the 3.3V fixed-output voltage. Connect a resistive voltage-divider between OUT and GND with the center tap connected to FB2 to adjust the output voltage. Choose RB (resistance from FB2 to GND) to be between 5kΩ and 50kΩ, and solve for RA (resistance from OUT to FB2) using the equation:

$$RA = RB \times \left(\frac{V_{OUT}}{V_{FB2}} - 1 \right)$$

where V_{FB2} = 1.25V, and V_{OUT} may vary from 1.5V to 5V.

Because FB2 is a very sensitive pin, a noise filter is generally required for FB2 in adjustable-mode operation. Place an 82pF capacitor from FB2 to GND to prevent unstable operation. No filter is required for 3.3V fixed-mode operation.

Soft-Start

The step-down regulator includes a 7-bit soft-start DAC that steps its internal reference voltage from zero to 1.25V in 128 steps. The soft-start period is 3ms (typ) and FB2 fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup (see the Step-Down Regulator Soft-Start Waveforms in the *Typical Operating Characteristics*).

Step-Up Regulator

The step-up regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast-transient response to pulsed loads typical of TFT LCD panel source drivers. The integrated MOSFET and the built-in digital soft-start function reduce the number of external components required while controlling inrush currents. The output voltage can be set from V_{IN} to 16.5V with an external resistive voltage-divider. The regulator controls the output voltage and the power delivered to the output by modulating duty cycle D of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{AVDD} + V_{DIODE} - V_{IN}}{V_{AVDD} + V_{DIODE} - V_{LX1}}$$

where V_{AVDD} is the output voltage of the step-up regulator, V_{DIODE} is the voltage drop across the diode, and V_{LX1} is the voltage drop across the internal MOSFET.

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PWM Controller Block

An error amplifier compares the signal at FB1 to 1.25V and changes the COMP output. The voltage at COMP sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope compensation signal is summed with the current-sense signal.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceed the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on diode D1. The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Step-Up Regulator External pMOS Pass Switch

As shown in Figure 1, a series external p-channel MOSFET can be installed between the cathode of the step-up regulator Schottky catch diode and the V_{AVDD} filter capacitors. This feature is used to sequence power to AVDD after the MAX17126/MAX17126A have proceeded through normal startup to limit input surge current during the output capacitor initial charge, and to provide true shutdown when the step-up regulator is disabled. When EN is low, GD is internally pulled up to the GD_I through a 25Ω resistor. Once EN is high and the negative charge-pump regulator is in regulation, the GD starts pulling down with a 10µA (typ) internal current source. The external p-channel MOSFET turns on and connects the cathode of the step-up regulator Schottky catch diode to the step-up regulator load capacitors when GD falls below the turn-on threshold of the MOSFET. When V_{GD} reaches V_{GD_I} - 6V(GD done), the step-up regulator is enabled and initiates a soft-start routine.

When not using this feature, leave GD high impedance, and connect GD_I to the output of the step-up converter.

Soft-Start

The step-up regulator achieves soft-start by linearly ramping up its internal current limit. The soft-start is either done internally when the capacitance on pin SS is < 200pF or externally when capacitance on pin SS is > 200pF. The internal soft-start ramps up the current limit in 128 steps in 12ms. The external soft-start terminates when the SS pin voltage reaches 1.25V. The soft-start feature effectively limits the inrush current during startup (see the Step-Up Regulator Soft-Start Waveforms in the *Typical Operating Characteristics*).

Positive Charge-Pump Regulator

The positive charge-pump regulator (Figure 3) is typically used to generate the positive supply rail for the TFT LCD gate driver ICs. The output voltage is set with an external resistive voltage-divider from its output to GND with the midpoint connected to FBP. The number of charge-pump stages and the setting of the feedback divider determine

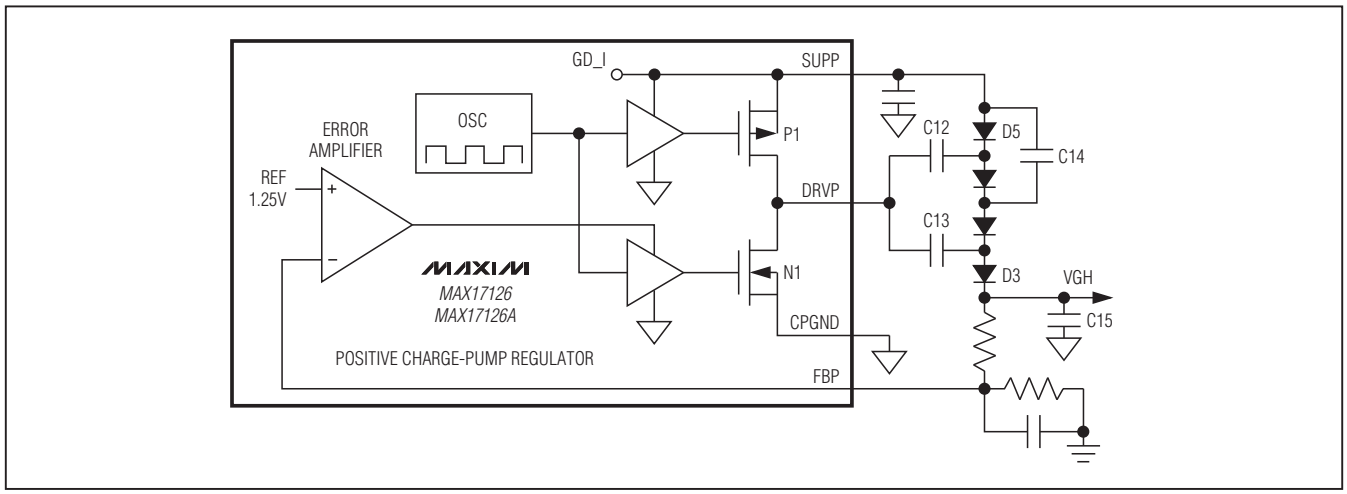

Figure 3. Positive Charge-Pump Regulator Block Diagram

the output voltage of the positive charge-pump regulator. The charge pump includes a high-side p-channel MOSFET (P1) and a low-side n-channel MOSFET (N1) to control the power transfer as shown in Figure 3.

During the first half cycle, N1 turns on and charges flying capacitors C12 and C13 (Figure 3). During the second half cycle, N1 turns off and P1 turns on, level shifting C12 and C13 by V_{SUPP} volts. If the voltage across C15 (V_{GH}) plus a diode drop (VD) is smaller than the level-shifted flying-capacitor voltage (VC13) plus V_{SUPP}, charge flows from C13 to C15 until the diode (D3) turns off. The amount of charge transferred to the output is determined by the error amplifier that controls N1's on-resistance.

Each time it is enabled, the positive charge-pump regulator goes through a soft-start routine by ramping up its internal reference voltage from 0 to 1.25V in 128 steps. The soft-start period is 2ms (typ) and FBP fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup.

Negative Charge-Pump Regulator

The negative charge-pump regulator is typically used to generate the negative supply rail for the TFT LCD gate driver ICs. The output voltage is set with an external resistive voltage-divider from its output to REF with the midpoint connected to FBN. The number of charge-pump stages and the setting of the feedback divider determine the output of the negative charge-pump regulator. The charge-pump controller includes a high-side p-channel MOSFET (P2) and a low-side n-channel MOSFET (N2) to control the power transfer as shown in Figure 4.

During the first half cycle, P2 turns on, and flying capacitor C10 charges to V_{SUPN} minus a diode drop (Figure 4). During the second half cycle, P2 turns off, and N2 turns on, level shifting C10. This connects C10 in parallel with reservoir capacitor C11. If the voltage across C11 minus a diode drop is greater than the voltage across C10, charge flows from C11 to C10 until the diode (D4) turns off. The amount of charge transferred from the output is determined by the error amplifier that controls N2's on-resistance.

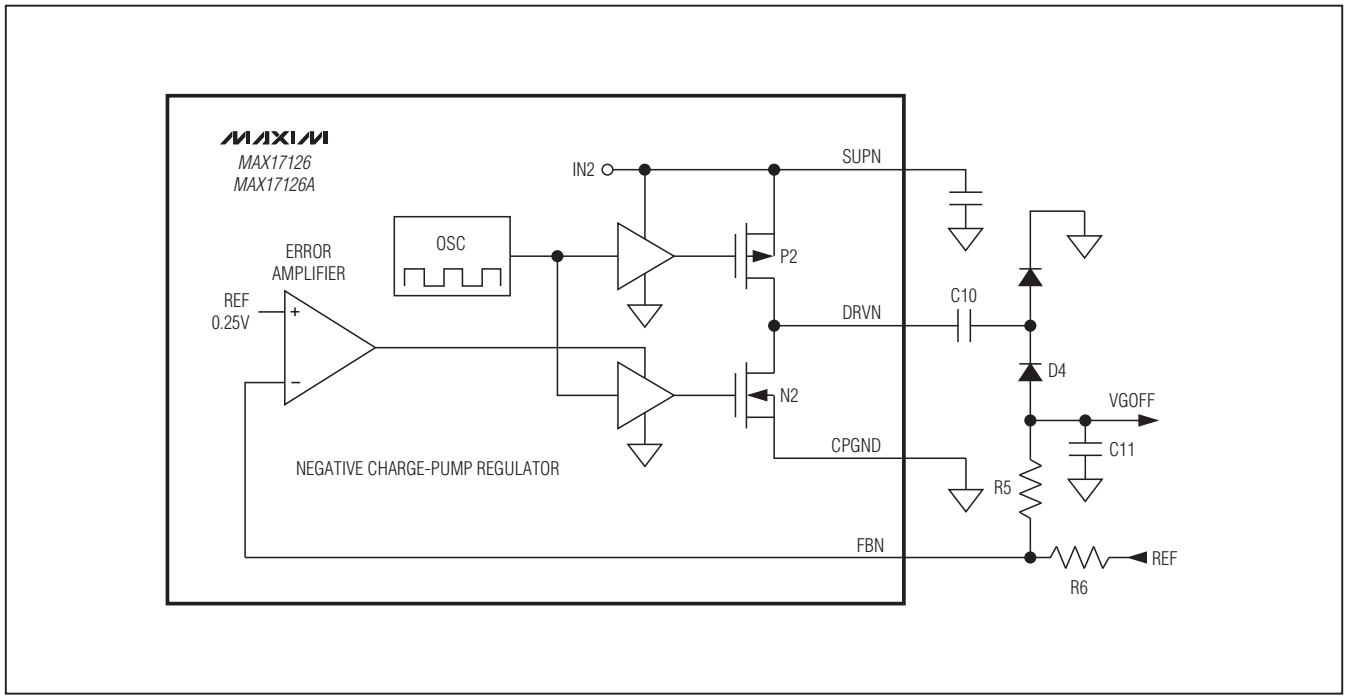

Figure 4. Negative Charge-Pump Regulator Block Diagram

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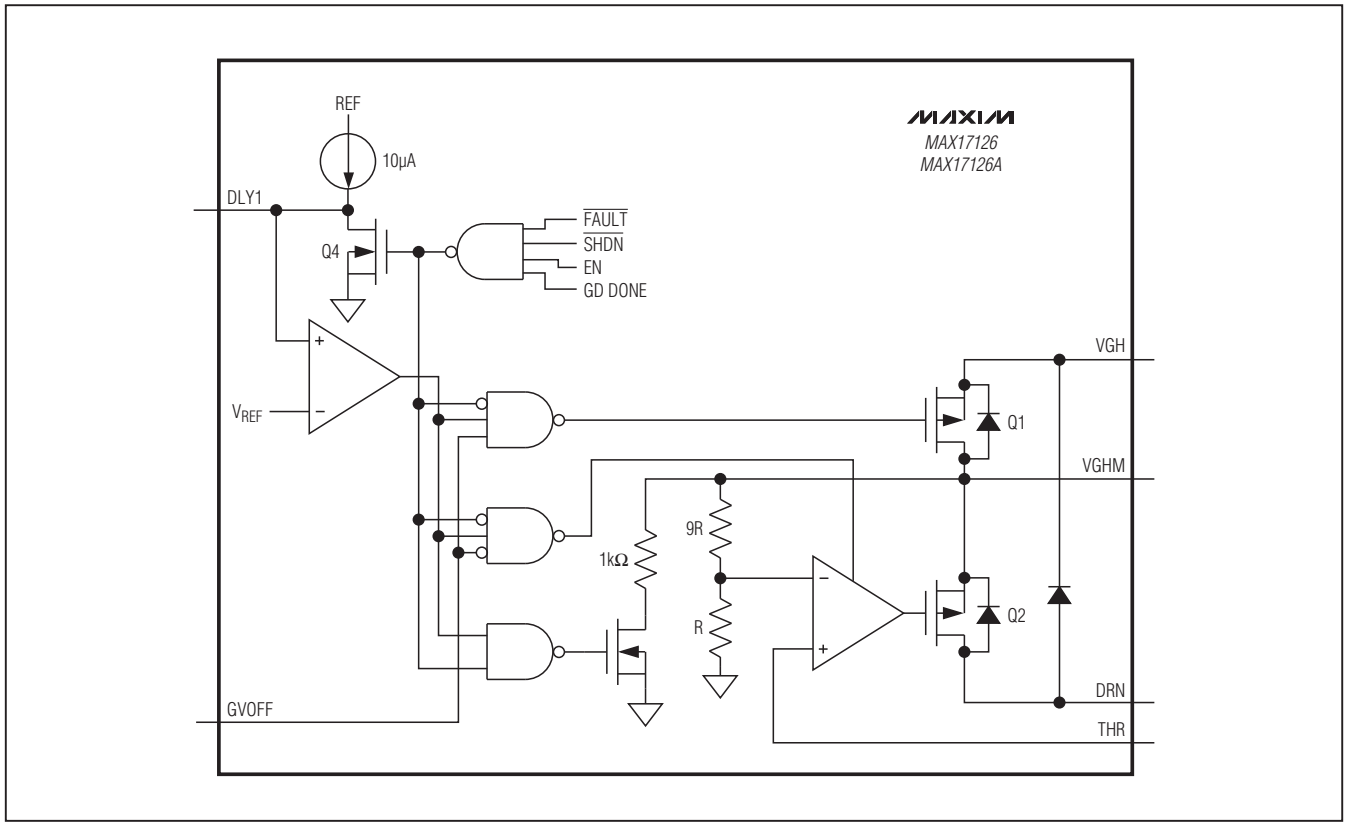

Figure 5. Switch Control

The negative charge-pump regulator is enabled after the step-down regulator finishes soft-start. Each time it is enabled, the negative charge-pump regulator goes through a soft-start routine by ramping down its internal reference voltage from 1.25V to 250mV in 128 steps. The soft-start period is 1.8ms (typ) and FBN fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup.

High-Voltage Switch Control

The MAX17126/MAX17126As' high-voltage switch control block (Figure 5) consists of two high-voltage p-channel MOSFETs: Q1, between VGH, and VGHM and Q2, between VGHM and DRN. The switch control block is enabled when V_{DLY1} exceeds V_{REF}. Q1 and Q2 are controlled by GVOFF.

When GVOFF is logic-high, Q1 turns on and Q2 turns off, connecting VGHM to VGH. When GVOFF is logic-low, Q1 turns off and Q2 turns on, connecting VGHM to DRN. VGHM can then be discharged through a resistor connected between DRN and GND or AVDD. Q2 turns off and stops discharging VGHM when VGHM reaches 10 times the voltage on THR.

The switch control block is disabled and DLY1 is held low when the LCD is shut down or in a fault state.

Operational Amplifier

The operational amplifier is typically used to drive the LCD backplane (VCOM). It features ±200mA output short-circuit current, 45V/µs slew rate, and 20MHz/3dB bandwidth. The rail-to-rail input and output capability maximizes system flexibility.

Short-Circuit Current Limit and Input Clamp

The operational amplifier limits short-circuit current to approximately ±200mA if the output is directly shorted to VOP or to OGND. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+160°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor immediately sets the thermal fault latch, shutting off all the IC's outputs. The device remains inactive until the input voltage is cycled. The operational amplifiers have 4V input clamp structures in series with a 500Ω resistance and a diode (Figure 6).

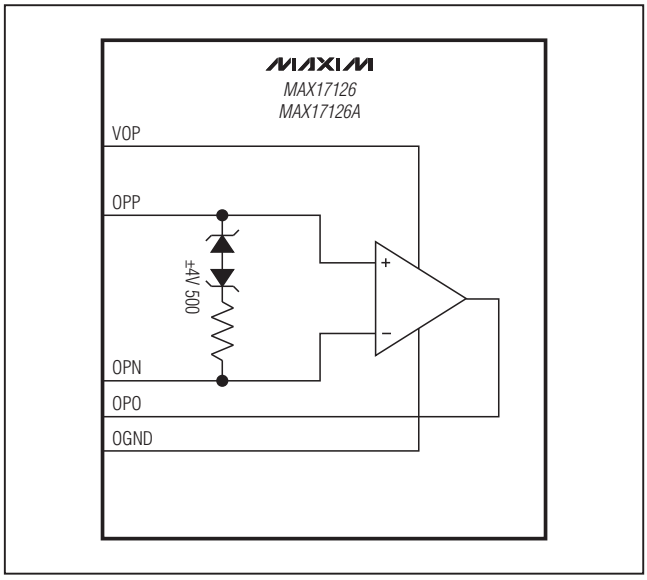

Figure 6. Op Amp Input Clamp Structure

Driving Pure Capacitive Load

The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation. As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between OPO and the capacitive load reduces peaking, but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω, and the typical value of the capacitor is 10nF.

Linear Regulator (VL)

The MAX17126/MAX17126A include an internal linear regulator. INVL is the input of the linear regulator. The input voltage range is between 8V and 16.5V. The output voltage is set to 5V. The regulator powers the internal MOSFET drivers, PWM controllers, charge-pump regulators, and logic circuitry. The total external load capability is 25mA. Bypass VL to GND with a minimum 1µF ceramic capacitor.

Reference Voltage (REF)

The reference output is nominally 1.25V, and can source at least 50µA (see *Typical Operating Characteristics*). VL is the input of the internal reference block. Bypass REF with a 0.22µF ceramic capacitor connected between REF and GND.

High-Accuracy, High-Voltage Gamma Reference

The LDO is typically used to drive gamma-correction divider string. Its output voltage is adjustable through a resistor-divider. This LDO features high output accuracy (±0.5%) and low-dropout voltage (0.25V typ) and can supply at least 60mA.

PGOOD Function

PGOOD is an open-drain output that connects to GND when VDET is below its detection threshold (1.25V typ). PGOOD is active after VL rises above UVLO threshold.

Frequency Selection and Out-of-Phase Operation (FSEL)

The step-down regulator and step-up regulator use the same internal oscillator. The FSEL input selects the switching frequency. Table 3 shows the switching frequency based on the FSEL connection. High-frequency (750kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. Low-frequency (500kHz) operation offers the best overall efficiency at the expense of component size and board space.

To reduce the input RMS current, the step-down regulator and the step-up regulator operate 180° out of phase from each other. The feature allows the use of less input capacitance.

Table 3. Frequency Selection

FSEL	SWITCHING FREQUENCY (kHz)
VL, INVL, OR FLOAT	750
GND	500

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Power-Up Sequence

The step-down regulator starts up when the MAX17126/MAX17126As' internal reference voltage (REF) is above its undervoltage lockout (UVLO) threshold. Once the step-down regulator soft-start is done, the FB2 fault-detection circuit and the negative charge pump are enabled. Negative charge-pump fault protection is enabled after its own soft-start is done.

When EN goes to logic-high, a 10µA current source starts to pull down on GD, turning on the external GD_I-AVDD PMOS switch. When V_{GD} reaches GD-done threshold (V_{GD_I} - 6V), the step-up regulator is enabled. Gamma reference is enabled at the same time.

The MAX17126/MAX17126A simplify system design by including an internal 12ms soft-start for the step-up regulator. When the capacitor on the SS pin is less than 200pF, the internal 12ms soft-start is in place. This saves one capacitor from system design. If an external capacitor greater than 200pF is used, a 5µA current source charges the SS capacitor pin and when the SS voltage reaches 1.25V, soft-start is done. The FB1 fault-detection circuit is enabled after this soft-start is done.

The positive charge pump is also enabled after the step-up regulator finishes its soft-start. After the positive charge pump's soft-start is done, the FBP fault-detection circuit is enabled, as well as the high-voltage switch delay block. C_{DLY1} is charged with an internal 10µA current source and V_{DLY1} rises linearly. When V_{DLY1} reaches REF, the high-voltage switch block is enabled.

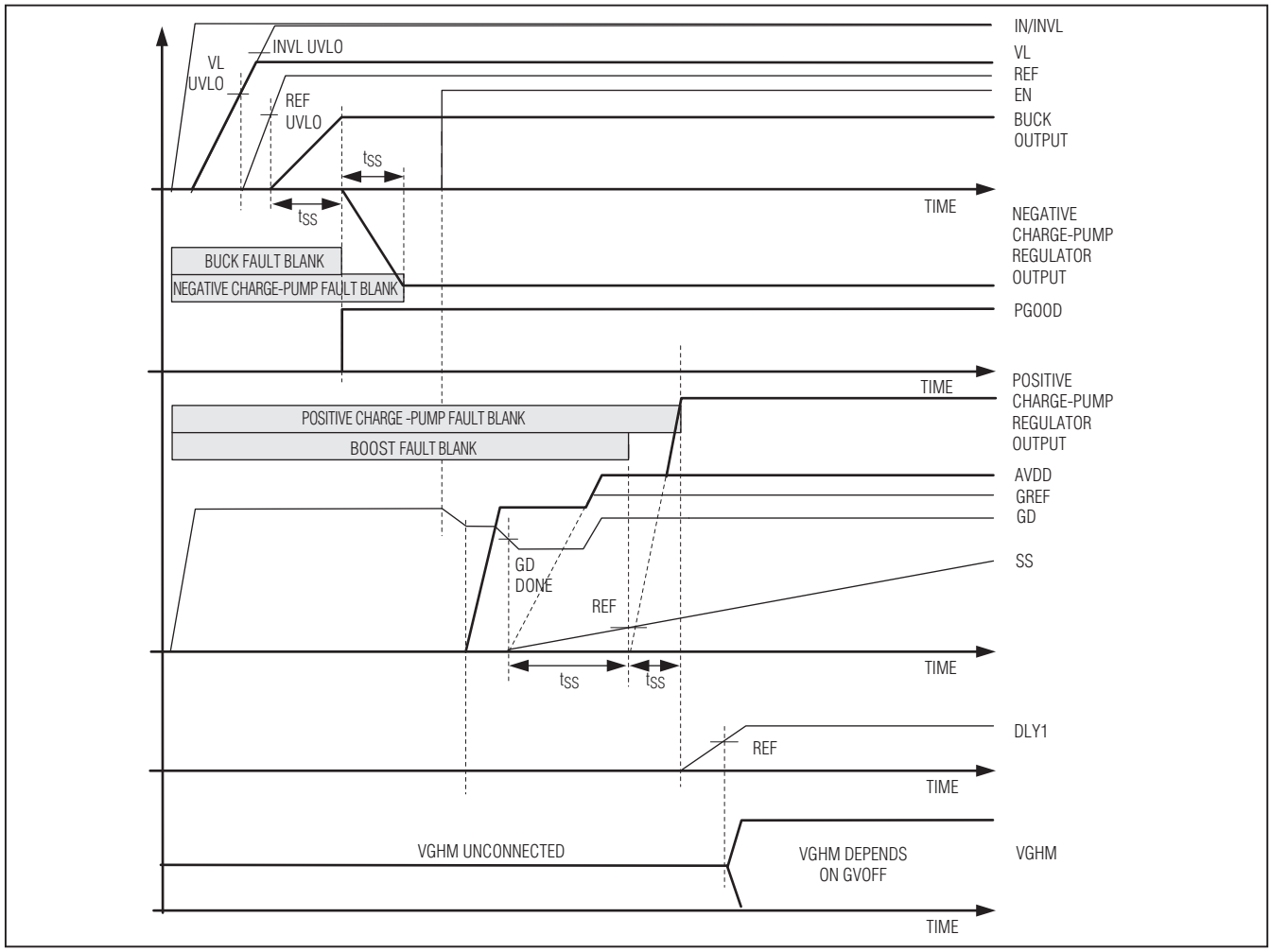

Figure 7. Power-Up Sequence

Power-Down Sequence

The step-down regulator, step-up regulator, positive charge pump, negative charge pump, and high-voltage switching block all start to shut down when INVL drops below its UVLO threshold. VL stays flat until INVL does not have enough headroom. Reference REF starts to fall after VL drops below its UVLO threshold.

Gamma reference GREF stays flat until AVDD does not have enough headroom. A pMOS switch turns on after VL drops below its UVLO threshold to guarantee GREF does not go over AVDD.

PGOOD is pulled low after its input voltage (buck output in this case) drops below the designed threshold. After VL drops below its UVLO threshold, PGOOD gives up control and is resistively pulled up to its input voltage.

The high-voltage switching block output VGHM falls until VL drops below its UVLO threshold, after which it is in high impedance.

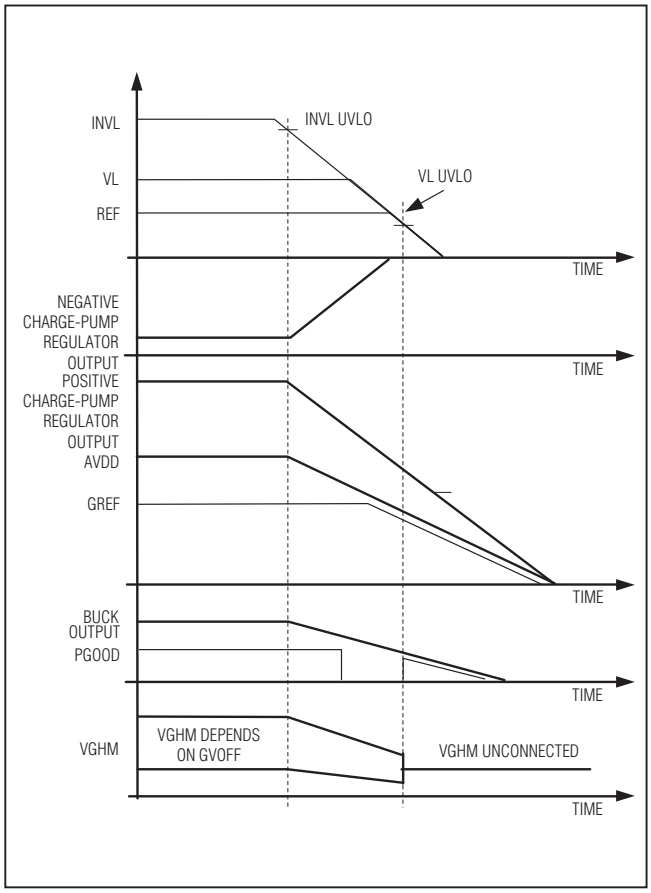

Figure 8. Power-Down Sequence

Fault Protection

During steady-state operation, if any output of the four regulators' output (step-down regulator, step-up regulator, positive charge-pump regulator, and negative charge-pump regulator) goes lower than its respective fault-detection threshold, the MAX17126 activates an internal fault timer. If any condition or the combination of conditions indicates a continuous fault for the fault timer duration (50ms typ), the MAX17126A latches off all its outputs while the MAX17126 latches off all the outputs except the buck regulator (latched off only when the fault happens on its output).

If a short has happened to any of the four regulator outputs, no fault timer is applied; the part latches off immediately. Pay special attention to shorts on the step-up regulator and positive charge pump. Make sure when a short happens, negative ringing on VREF_I (connected to step-up regulator output) and VGH (connected to positive charge-pump output) does not exceed *Absolute Maximum Ratings*. Otherwise, physical damage of the part may occur. Cycle the input voltage to clear the fault latch and restart the supplies.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the MAX17126/MAX17126A. When the junction temperature exceeds T_J = +160°C, a thermal sensor immediately activates the fault protection that shuts down all the outputs. Cycle the input voltage to clear the fault latch and restart the MAX17126/MAX17126A.

The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Design Procedure

Step-Down Regulator

Inductor Selection

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant, LIR, which is the ratio of peak-to-peak inductor ripple current to DC load current. A higher LIR value allows smaller inductance, but results in higher losses and higher ripple. A good compromise between size and losses is typically found at a 30% ripple current-to-load current ratio (LIR = 0.3) that corresponds to a peak inductor current 1.15 times the DC load current:

$$L_2 = \frac{V_{OUT} \times (V_{IN2} - V_{OUT})}{V_{IN2} \times f_{SW} \times I_{OUT(MAX)} \times LIR}$$

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where $I_{OUT(MAX)}$ is the maximum DC load current, and the switching frequency f_{SW} is 750kHz when FSEL is tied to VL, 500kHz when FSEL is tied to GND. The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but at some point resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels.

The inductor's saturation current must exceed the peak inductor current. The peak current can be calculated by:

$$I_{OUT_RIPPLE} = \frac{V_{OUT} \times (V_{IN2} - V_{OUT})}{f_{SW} \times L_2 \times V_{IN2}}$$

$$I_{OUT_PEAK} = I_{OUT(MAX)} + \frac{I_{OUT_RIPPLE}}{2}$$

The inductor's DC resistance should be low for good efficiency. Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice. Shielded-core geometries help keep noise, EMI, and switching waveform jitter low.

Considering the typical operation circuit in Figure 1, the maximum load current $I_{OUT(MAX)}$ is 1.5A with a 3.3V output and a typical 12V input voltage. Choosing an LIR of 0.4 at this operation point:

$$L_2 = \frac{3.3V \times (12V - 3.3V)}{12V \times 750kHz \times 1.5A \times 0.4} \approx 5.3\mu H$$

Pick L_2 = 4.7µH. At that operation point, the ripple current and the peak current are:

$$I_{OUT_RIPPLE} = \frac{3.3V \times (12V - 3.3V)}{750kHz \times 4.7\mu H \times 12V} = 0.68A$$

$$I_{OUT_PEAK} = 1.5A + \frac{0.68A}{2} = 1.84A$$

Input Capacitors

The input filter capacitors reduce peak currents drawn from the power source and reduce noise and voltage ripple on the input caused by the regulator's switching. They are usually selected according to input ripple current requirements and voltage rating, rather than capacitance value. The input voltage and load current determine the RMS input ripple current (I_{RMS}):

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{IN2} - V_{OUT})}}{V_{IN2}}$$

The worst case is I_{RMS} = 0.5 x I_{OUT} that occurs at V_{IN2} = 2 x V_{OUT}.

For most applications, ceramic capacitors are used because of their high ripple current and surge current capabilities. For optimal circuit long-term reliability, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current corresponding to the maximum load current.

Output Capacitor Selection

Since the MAX17126/MAX17126As' step-down regulator is internally compensated, it is stable with any reasonable amount of output capacitance. However, the actual capacitance and equivalent series resistance (ESR) affect the regulator's output ripple voltage and transient response. The rest of this section deals with how to determine the output capacitance and ESR needs according to the ripple voltage and load-transient requirements.

The output voltage ripple has two components: variations in the charge stored in the output capacitor, and the voltage drop across the capacitor's ESR caused by the current into and out of the capacitor:

$$V_{OUT_RIPPLE} = V_{OUT_RIPPLE(ESR)} + V_{OUT_RIPPLE(C)}$$

$$V_{OUT_RIPPLE(ESR)} = I_{OUT_RIPPLE} \times R_{ESR_OUT}$$

$$V_{OUT_RIPPLE(C)} = \frac{I_{OUT_RIPPLE}}{8 \times C_{OUT} \times f_{SW}}$$

where I_{OUT_RIPPLE} is defined in the *Step-Down Regulator Inductor Selection* section, C_{OUT} (C5 in Figure 1) is the output capacitance, and R_{ESR_OUT} is the ESR of the output capacitor C_{OUT}. In Figure 1's circuit, the inductor ripple current is 0.68A. If the voltage-ripple requirement of Figure 1's circuit is ≤ 1% of the 3.3V output, then the total peak-to-peak ripple voltage should be less than 66mV. Assuming that the ESR ripple and the capacitive ripple each should be less than 50% of the total peak-to-peak ripple, then the ESR should be less than 48.5mΩ and the output capacitance should be more than 3.4µF to meet the total ripple requirement. A 22µF capacitor with ESR (including PCB trace resistance) of 10mΩ is selected for the typical operating circuit in Figure 1, which easily meets the voltage ripple requirement.

The step-down regulator's output capacitor and ESR also affect the voltage undershoot and overshoot when the load steps up and down abruptly. The undershoot and overshoot also have two components: the voltage steps caused by ESR, and voltage sag and soar due to the finite capacitance and inductor slew rate. Use the following formulas to check if the ESR is low enough and the output capacitance is large enough to prevent excessive soar and sag.

The amplitude of the ESR step is a function of the load step and the ESR of the output capacitor:

$$V_{OUT_ESR_STEP} = \Delta I_{OUT} \times R_{ESR_OUT}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle:

$$V_{OUT_SAG} = \frac{L_2 \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times \left(V_{IN2(MIN)} \times D_{MAX} - V_{OUT}\right)}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value, and the output voltage:

$$V_{OUT_SOAR} = \frac{L_2 \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Keeping the full-load overshoot and undershoot less than 3% ensures that the step-down regulator's natural integrator response dominates. Given the component values in the circuit of Figure 1, during a full 1.5A step load transient, the voltage step due to capacitor ESR is negligible. The voltage sag and soar are 76mV and 73mV, respectively.

Rectifier Diode

The MAX17126/MAX17126As' high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 2A Schottky diode works well in the MAX17126/MAX17126A's step-up regulator.

Step-Up Regulator

Inductor Selection

The inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient response time, and output voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple, and therefore, reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire that increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size, but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full-load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{AVDD(MAX)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L_1 = \left(\frac{V_{IN}}{V_{AVDD}}\right)^2 \left(\frac{V_{AVDD} - V_{IN}}{I_{AVDD(MAX)} \times f_{SW}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{AVDD(MAX)} \times V_{AVDD}}{V_{IN(MIN)} \times \eta_{MIN}}$$

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Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{AVDD_RIPPLE} = \frac{V_{IN(MIN)} \times (V_{AVDD} - V_{IN(MIN)})}{L_{AVDD} \times V_{AVDD} \times f_{SW}}$$

$$I_{AVDD_PEAK} = I_{IN(DC,MAX)} + \frac{I_{AVDD_RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX17126/MAX17126As' LX1 current limit should exceed I_{AVDD_PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit (Figure 1), the maximum load current ($I_{AVDD(MAX)}$) is 1A with a 16V output and a typical input voltage of 12V. Choosing an LIR of 0.3 and estimating efficiency of 90% at this operating point:

$$L_1 = \left(\frac{12V}{16V}\right)^2 \left(\frac{16V - 12V}{1A \times 750kHz}\right)\left(\frac{90\%}{0.3}\right) = 9\mu H$$

Using the circuit's minimum input voltage (8V) and estimating efficiency of 85% at that operating point:

$$I_{IN(DC,MAX)} = \frac{1A \times 16V}{8V \times 85\%} \approx 2.35A$$

The ripple current and the peak current are:

$$I_{AVDD_RIPPLE} = \frac{8V \times (16V - 8V)}{10\mu H \times 16V \times 750kHz} \approx 0.53A$$

$$I_{AVDD_PEAK} = 2.35A + \frac{0.53A}{2} \approx 2.62A$$

Output Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{AVDD_RIPPLE} = V_{AVDD_RIPPLE(C)} + V_{AVDD_RIPPLE(ESR)}$$

$$V_{AVDD_RIPPLE(C)} \approx \frac{I_{AVDD}}{C_{AVDD}}\left(\frac{V_{AVDD} - V_{IN}}{V_{AVDD} f_{SW}}\right)$$

and:

$$V_{AVDD_RIPPLE(ESR)} \approx I_{AVDD_PEAK} R_{ESR_AVDD}$$

where I_{AVDD_PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{AVDD_RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered. Note that all ceramic capacitors typically have large temperature coefficient and bias voltage coefficients. The actual capacitor value in circuit is typically significantly less than the stated value.

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input supply and reduces noise injection into the IC. A 22µF ceramic capacitor is used in the typical operating circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, the input capacitance can be reduced below the values used in the typical operating circuit.

Rectifier Diode

The MAX17126/MAX17126As' high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 2A Schottky diode complements the internal MOSFET well.

Output Voltage Selection

The output voltage of the step-up regulator can be adjusted by connecting a resistive voltage-divider from the output (V_{AVDD}) to GND with the center tap connected to FB1 (see Figure 1). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{AVDD}}{V_{FB1}} - 1\right)$$

where V_{FB1}, the step-up regulator's feedback set point, is 1.25V. Place R1 and R2 close to the IC.

Loop Compensation

Choose R_{COMP} to set the high-frequency integrator gain for fast-transient response. Choose C_{COMP} to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{100 \times V_{IN} \times V_{AVDD} \times C_{AVDD}}{L_{AVDD} \times I_{AVDD(MAX)}}$$

$$C_{COMP} \approx \frac{V_{AVDD} \times C_{AVDD}}{10 \times I_{AVDD(MAX)} \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient response waveforms.

Charge-Pump Regulators

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meet the output requirement.

The number of positive charge-pump stages is given by:

$$n_{POS} = \frac{V_{GH} + V_{DROPOUT} - V_{AVDD}}{V_{SUPP} - 2 \times V_D}$$

where n_{POS} is the number of positive charge-pump stages, V_{GH} is the output of the positive charge-pump regulator, V_{SUPP} is the supply voltage of the charge-pump regulators, V_D is the forward voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the regulator. Use $V_{DROPOUT}$ = 300mV.

The number of negative charge-pump stages is given by:

$$n_{NEG} = \frac{-V_{GOFF} + V_{DROPOUT}}{V_{SUPN} - 2 \times V_D}$$

where n_{NEG} is the number of negative charge-pump stages and V_{GOFF} is the output of the negative charge-pump regulator.

The above equations are derived based on the assumption that the first stage of the positive charge pump is connected to V_{AVDD} and the first stage of the negative charge pump is connected to ground. Sometimes fractional stages are more desirable for better efficiency. This can be done by connecting the first stage to V_{OUT} or another available supply. If the first charge-pump stage is powered from V_{OUT}, then the above equations become:

$$n_{POS} = \frac{V_{GH} + V_{DROPOUT} - V_{OUT}}{V_{SUPP} - 2 \times V_D}$$

$$n_{NEG} = \frac{-V_{GOFF} + V_{DROPOUT} + V_{OUT}}{V_{SUPN} - 2 \times V_D}$$

Flying Capacitors

Increasing the flying capacitor CX (connected to DRVP and DRVN) value lowers the effective source impedance and increases the output current capability. Increasing the capacitance indefinitely has a negligible effect on output current capability because the internal switch resistance and the diode impedance place a lower limit on the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{CX} > n_{POS(NEG)} \times V_{SUPP(SUPN)}$$

where $n_{POS(NEG)}$ is the number of stages in which the flying capacitor appears. It is the same as the number of charge-pump stages.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT_CP} \geq \frac{I_{LOAD_CP}}{2 \times f_{SW} \times V_{RIPPLE_CP}}$$

where C_{OUT_CP} is the output capacitor of the charge pump, I_{LOAD_CP} is the load current of the charge pump, and V_{RIPPLE_CP} is the peak-to-peak value of the output ripple.

Output Voltage Selection

Adjust the positive charge-pump regulator's output voltage by connecting a resistive voltage-divider from VGH output to GND with the center tap connected to FBP (Figure 1). Select the lower resistor of divider R4 in the 10kΩ to 30kΩ range. Calculate upper resistor R3 with the following equation:

$$R3 = R4 \times \left(\frac{V_{VGH}}{V_{FBP}} - 1 \right)$$

where V_{FBP} = 1.25V (typ).

Adjust the negative charge-pump regulator's output voltage by connecting a resistive voltage-divider from V_{GOFF} to REF with the center tap connected to FBN (Figure 1). Select R6 in the 20kΩ to 68kΩ range. Calculate R5 with the following equation:

$$R5 = R6 \times \frac{V_{FBN} - V_{GOFF}}{V_{REF} - V_{FBN}}$$

where V_{FBN} = 250mV, V_{REF} = 1.25V. Note that REF can only source up to 50µA, using a resistor less than 20kΩ, for R6 results in a higher bias current than REF can supply.

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High-Accuracy, High-Voltage Gamma Reference

Output-Voltage Selection

The output voltage of the high-accuracy LDO is set by connecting a resistive voltage-divider from the output (V_{REF_O}) to AGND with the center tap connected to V_{REF_FB} (see Figure 1). Select R10 in the 10kΩ to 50kΩ range. Calculate R9 with the following equation:

$$R9 = R10 \times \left(\frac{V_{REF_O}}{V_{REF_FB}} - 1 \right)$$

where V_{REF_FB}, the LDO's feedback set point, is 1.25V. Place R9 and R10 close to the IC.

Input and Output Capacitor Selection

To ensure stability of the LDO, use a minimum of 1µF on the regulator's input (V_{REF_I}) and a minimum of 2.2µF on the regulator's output (V_{REF_O}). Place the capacitors near the pins and connect their ground connections directly together.

Set the PGOOD Threshold Voltage

PGOOD threshold voltage can be adjusted by connecting a resistive voltage-divider from input V_{IN} to GND with the center tap connected to V_{DET} (see Figure 1). Select R8 in the 10kΩ to 50kΩ range. Calculate R7 with the following equation:

$$R7 = R8 \times \left(\frac{V_{IN_PGOOD}}{V_{DET}} - 1 \right)$$

where V_{DET} = 1.25V is the V_{DET} threshold set point. V_{IN_PGOOD} is the desired PGOOD threshold voltage. Place R7 and R8 close to the IC.

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the area of respective high-current loops by placing each DC/DC converter's inductor, diode, and output capacitors near its input capacitors and its LX_ and PGND pins. For the step-down regulator, the high-current input loop goes from the positive terminal of the input capacitor to the IC's IN2 pin, out of LX2, to the inductor, to the positive terminals of the output capacitors, reconnecting the output capacitor and input capacitor ground terminals. The high-current output loop is from the inductor to the positive terminals of the output capacitors, to the negative terminals of the output capacitors, and to the Schottky diode (D2). For the step-up regulator, the high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX1 pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- Create a power ground island for the step-down regulator, consisting of the input and output capacitor grounds and the diode ground. Connect all these together with short, wide traces or a small ground plane. Similarly, create a power ground island (PGND) for the step-up regulator, consisting of the input and output capacitor grounds and the PGND pin. Create a power ground island (CPGND) for the positive and negative charge pumps, consisting of SUPP and output (V_{GH}, V_{GOFF}) capacitor grounds, and negative charge-pump diode ground. Connect the step-down regulator ground plane, PGND ground plane, and CPGND ground plane together with wide traces. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes.
- Create an analog ground plane (GND) consisting of the GND pin, all the feedback divider ground connections, the COMP, SS, and DLY1 capacitor ground connections, and the device's exposed backside pad. Connect the PGND and GND islands by connecting the two ground pins directly to the exposed backside pad. Make no other connections between these separate ground planes.
- Place all feedback voltage-divider resistors as close as possible to their respective feedback pins. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up switching noise. Care should be taken to avoid running any feedback trace near LX1, LX2, DRVP, or DRVN.
- Place IN2 pin, VL pin, REF pin, and V_{REF_O} pin bypass capacitors as close as possible to the device. The ground connection of the VL bypass capacitor should be connected directly to the GND pin with a wide trace.

- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Minimize the size of the LX1 and LX2 nodes while keeping them wide and short. Keep the LX1 and LX2 nodes away from feedback nodes (FB1, FB2, FBP, FBN, and VREF_FB) and analog ground. Use DC traces as shield if necessary.

Refer to the MAX17126 evaluation kit for an example of proper board layout.

Chip Information

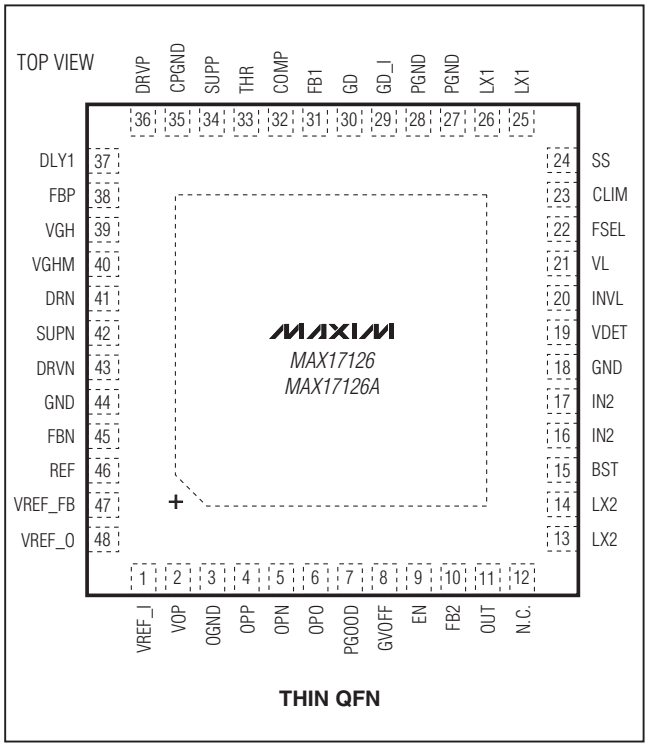
PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN	T4877-3	21-0144	90-0129

Pin Configuration



THIN QFN

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/09	Initial release	—
1	3/10	MAX17126A added to data sheet	1-33

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