

DATA SHEET

TDA3682

**Multiple voltage regulator with
power switches**

Product specification

2002 Mar 11

Supersedes data of 2000 Nov 20

Multiple voltage regulator with power switches

TDA3682

FEATURES

General

- Good stability for any regulator with almost any output capacitor
- Five voltage regulators (BU5V, illumination, AM, FM and audio)
- Mode selection by three enable control pins
- Low dropout voltage output stages (PNP output stage)
- High ripple rejection
- Low noise for all regulators
- Two power switches (power antenna and power control function).

Protections

- Reverse polarity safe (down to –18 V without high reverse current)
- Able to withstand voltages up to 18 V at the output (supply line may be short-circuited)
- ESD protection of all pins
- Thermal protection to avoid thermal break down
- Load dump protection
- Regulator outputs are DC short-circuited safe to ground and supply voltage
- Foldback current limit protection for all regulators
- Loss of ground protection for power switches.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3682ST	RDBS13P	plastic rectangular-DIL-bent-SIL power package; 13 leads	SOT528-2

GENERAL DESCRIPTION

The TDA3682 is a multiple output voltage regulator with power switches, intended for use in car radios with or without a microprocessor.

The TDA3682 contains the following:

- Four switchable regulators and one permanent active regulator (BU5V)
- Two power switches with loss of ground protection
- Three enable control inputs for selecting the regulators (illumination, audio, AM or FM) and the power switches (PANT and PCON); the standby mode is selected with all enable control inputs at LOW level.

The quiescent current has a very low level of 120 μ A (typical value) with the regulator 2 (BU5V) active.

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{P2}	supply voltage	regulator 1 on	11.4	14.4	18	V
		regulators 3, 4 and 5 on	10	14.4	18	V
		regulator 2 on	4	—	—	V
		jump start for $t \leq 10$ minutes	—	—	30	V
		load dump protection for $t \leq 50$ ms and $t_r \geq 2.5$ ms	—	—	50	V
		overvoltage for shut-down	20	—	—	V
$I_{q(tot)}$	total quiescent supply current	standby mode; $V_{P2} = 14.4$ V	—	120	150	μ A
Voltage regulators						
$V_{o(REG1)}$	output voltage of regulator 1	$0.5 \text{ mA} \leq I_o \leq 250 \text{ mA}$	9.89	10.3	10.71	V
$V_{o(REG2)}$	output voltage of regulator 2	$0.5 \text{ mA} \leq I_o \leq 300 \text{ mA}$	4.8	5.0	5.2	V
$V_{o(REG3)}$	output voltage of regulator 3	$0.5 \text{ mA} \leq I_o \leq 200 \text{ mA}$	7.87	8.2	8.53	V
$V_{o(REG4)}$	output voltage of regulator 4	$0.5 \text{ mA} \leq I_o \leq 50 \text{ mA}$	7.87	8.2	8.53	V
$V_{o(REG5)}$	output voltage of regulator 5	$0.5 \text{ mA} \leq I_o \leq 50 \text{ mA}$	7.87	8.2	8.53	V
Power switches						
$V_{drop(SW1)}$	dropout voltage of switch 1	$I_o = 200 \text{ mA}$	—	0.6	0.8	V
$V_{drop(SW2)}$	dropout voltage of switch 2	$I_o = 200 \text{ mA}$	—	0.6	0.8	V
Enable control inputs						
V_{IL}	LOW-level input voltage		-0.2	—	+1.0	V
V_{IM}	MID-level input voltage	not valid for pin EN1	2	—	3	V
V_{IH}	HIGH-level input voltage		4	—	—	V
R_i	input resistance	$0 \text{ V} \leq V_{EN} \leq V_{o(REG2)} + 0.3 \text{ V}$	50	—	—	$k\Omega$

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BLOCK DIAGRAM

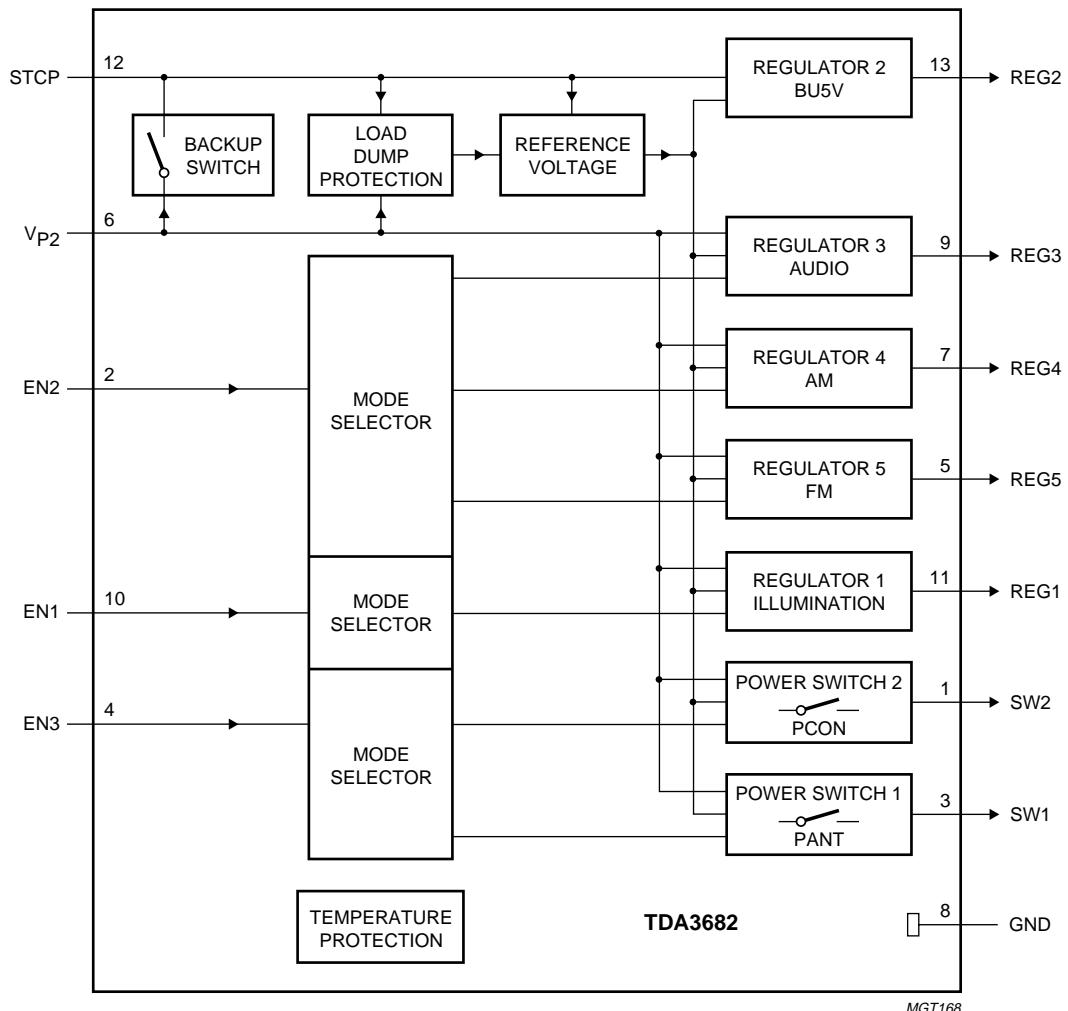


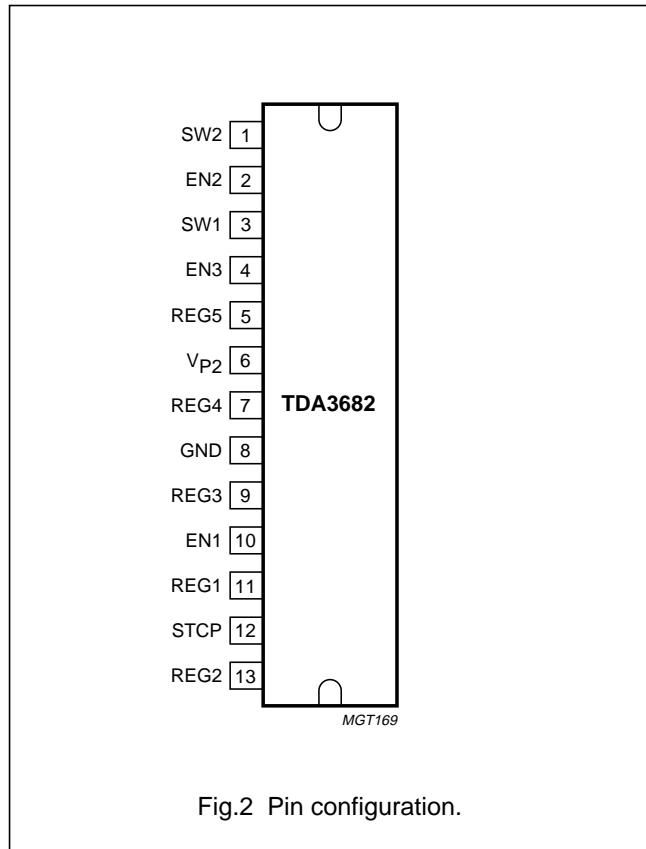
Fig.1 Block diagram.

Multiple voltage regulator with power switches

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PINNING

SYMBOL	PIN	DESCRIPTION
SW2	1	power control switch 2 (PCON) output
EN2	2	enable control input 2 for regulator 3 (audio), regulator 4 (AM) and regulator 5 (FM)
SW1	3	power antenna switch 1 (PANT) output
EN3	4	enable control input 3 for power switch 1 (PANT) and power switch 2 (PCON)
REG5	5	regulator 5 (FM) output
V_{P2}	6	supply voltage 2
REG4	7	regulator 4 (AM) output
GND	8	ground
REG3	9	regulator 3 (audio) output
EN1	10	enable control input 1 for regulator 1 (illumination)
REG1	11	regulator 1 (illumination) output
STCP	12	storage capacitor connection for supply voltage of regulator 2
REG2	13	permanent regulator 2 (BU5V) output



FUNCTIONAL DESCRIPTION

The TDA3682 is a multiple output voltage regulator with power switches, intended for use in car radios with or without a microprocessor.

It contains:

- Four switchable regulators and one permanent active regulator
- Two power switches with loss of ground protection
- Three enable control inputs EN1, EN2 and EN3.

The quiescent current has a very low level of $120 \mu\text{A}$ (typical value) with the regulator 2 (BU5V) active.

Because of low voltage operation of the application, low dropout voltage regulators are used in the TDA3682.

Output selection

Regulator 2 is always active and can not be controlled.

All the other regulators and both power switches can be controlled by using pins EN1, EN2 and EN3:

- Pin EN1 controls regulator 1 (illumination); see Table 1
- Pin EN2 selects regulator 3, 4 or 5 (audio, AM or FM); see Table 2
- Pin EN3 selects power switches 1 or 2 (PANT or PCON); see Table 3.

Pins EN2 and EN3 are three-state level control inputs:

- L means: $V_{EN} \leq 1 \text{ V}$
- M means: $2 \text{ V} \leq V_{EN} \leq 3 \text{ V}$
- H means: $V_{EN} \geq 4 \text{ V}$.

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Table 1 Enable control pin EN1

EN1	REGULATOR OUTPUT REG1
L	off
H	on

Table 2 Enable control pin EN2

EN2	REGULATOR OUTPUTS		
	REG3	REG4	REG5
L	off	off	off
M	on	off	on
H	on	on	off

Table 3 Enable control pin EN3

EN3	POWER SWITCHES	
	SW1	SW2
L	off	off
M	off	on
H	on	on

Backup function

A backup function is present. This is realized by a switch function which acts like a sort of ideal diode between pins V_{P2} and STCP. The forward voltage of this ideal diode depends on the current flowing through this diode. This function makes it possible to supply regulator 2 (BU5V) when no supply voltage is present on pin V_{P2} . A special application can be made using a backup function by connecting a capacitor between pin STCP and ground. When the supply voltage is present on pin V_{P2} this capacitor will be charged to a level of $V_{P2} - 0.3$ V. This charge can now be used to supply regulator 2 for a short period of time when V_{P2} is switched to 0 V.

The delay time can be calculated using the formula:

$$t_{\text{delay}} = C_{\text{backup}} \times R_L \times \frac{V_{P2} - V_{\text{REG2}} - 0.5}{V_{\text{REG2}}}$$

Example: $V_{P2} = 14.4$ V, $V_{\text{REG2}} = 5$ V, $R_L = 1$ k Ω and $C_{\text{backup}} = 100$ μF results in a delay time of 177 ms.

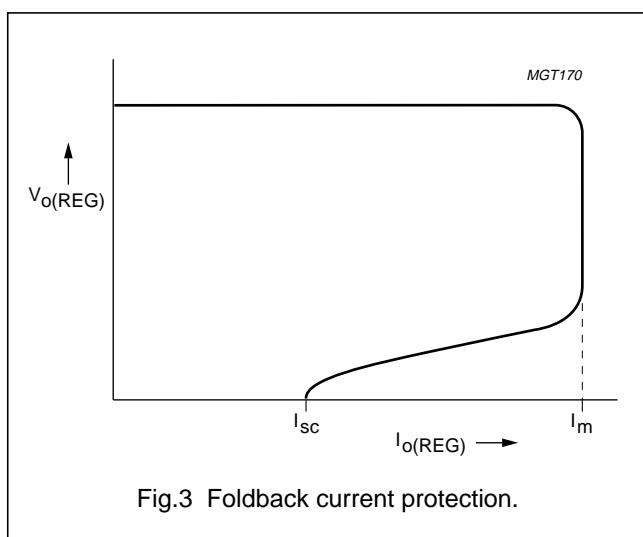
When an overvoltage condition occurs, the voltage on pin STCP will be limited to approximately 18 V.

Protections

All output pins are fully protected against load dump and short-circuit (foldback current protection); see Fig.3.

At load dump all regulator outputs will go low, except the output of regulator 2 (BU5V).

The power switches can withstand 'loss of ground'. This means that the ground pin is disconnected and the switch output is connected to ground.



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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{P2}	supply voltage	regulators on	–	18	V
		reverse polarity; non-operating	–	18	V
		jump start for $t \leq 10$ minutes	–	30	V
		load dump protection for $t \leq 50$ ms and $t_r \geq 2.5$ ms	–	50	V
P_{tot}	total power dissipation	$T_{amb} = 25$ °C infinite heatsink	–	17.8	W
		in free air	–	3.1	W
			–55	+150	°C
T_{stg}	storage temperature		–40	+85	°C
T_{amb}	ambient temperature		–40	+150	°C
T_j	junction temperature		–40	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case	7	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	40	K/W

QUALITY SPECIFICATION

In accordance with "SNW-FQ-611D".

CHARACTERISTICS

$V_{P2} = 14.4$ V; $T_{amb} = 25$ °C; measured in test circuit of Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{P2}	supply voltage	regulator 1 on	11.4	14.4	18	V
		regulators 3, 4 and 5 on	10	14.4	18	V
		regulator 2 switched on in regulation	4	–	–	V
			6.3	–	50	V
		overvoltage for shut-down	20	–	–	V
$I_{q(tot)}$	total quiescent supply current	standby mode; note 1	–	120	150	µA
Enable control inputs: pins EN1, EN2 and EN3						
V_{IL}	LOW-level input voltage		–0.2	–	+1.0	V
V_{IM}	MID-level input voltage	not valid for pin EN1	2	–	3	V
V_{IH}	HIGH-level input voltage		4	–	–	V
R_i	input resistance	$0 \text{ V} \leq V_{EN} \leq V_{o(REG2)} + 0.3 \text{ V}$	50	–	–	kΩ
		$V_{EN} > V_{o(REG2)} + 0.3 \text{ V}$	2	3	–	kΩ

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Regulator 1: pin REG1 ($I_o = 5 \text{ mA}$)						
$V_o(\text{REG1})$	output voltage of regulator 1	$0.5 \text{ mA} \leq I_o \leq 250 \text{ mA}$	9.89	10.3	10.71	V
		$12 \text{ V} \leq V_{P2} \leq 18 \text{ V}$	9.89	10.3	10.71	V
ΔV_{line}	line regulation voltage	$12 \text{ V} \leq V_{P2} \leq 18 \text{ V}$	—	—	50	mV
ΔV_{load}	load regulation voltage	$5 \text{ mA} \leq I_o \leq 250 \text{ mA}$	—	—	100	mV
SVRR	supply voltage ripple rejection	$f_i = 120 \text{ Hz}; V_i = 2 \text{ V (p-p)}$	60	70	—	dB
V_{drop}	dropout voltage	$V_{P2} = 10.0 \text{ V}; I_o = 250 \text{ mA}; \text{note 2}$	—	0.4	0.7	V
I_m	current limit	$V_o > 8.5 \text{ V}$	300	—	—	mA
I_{sc}	short-circuit current	$R_L \leq 0.5 \Omega; \text{note 3}$	50	—	—	mA
Regulator 2: pin REG2 ($I_o = 5 \text{ mA}$)						
$V_o(\text{REG2})$	output voltage of regulator 2	$0.5 \text{ mA} \leq I_o \leq 300 \text{ mA}$	4.8	5.0	5.2	V
		$10 \text{ V} \leq V_{P2} \leq 18 \text{ V}$	4.8	5.0	5.2	V
ΔV_{line}	line regulation	$10 \text{ V} \leq V_{P2} \leq 18 \text{ V}$	—	3	50	mV
ΔV_{load}	load regulation	$0.5 \text{ mA} \leq I_o \leq 300 \text{ mA}$	—	—	100	mV
SVRR	supply voltage ripple rejection	$f_i = 120 \text{ Hz}; V_i = 2 \text{ V (p-p)}$	60	70	—	dB
V_{drop}	dropout voltage	$I_o = 300 \text{ mA}$ $V_{\text{STCP}} = 5.5 \text{ V}; \text{note 4}$ $V_{P2} = 6 \text{ V}; \text{note 5}$	—	0.7	0.9	V
—	—	—	—	1.3	1.5	V
I_m	current limit	$V_o > 4.5 \text{ V}$	350	—	—	mA
I_{sc}	short-circuit current	$R_L \leq 0.5 \Omega; \text{note 3}$	80	100	—	mA
Regulator 3: pin REG3 ($I_o = 5 \text{ mA}$)						
$V_o(\text{REG3})$	output voltage of regulator 3	$0.5 \text{ mA} \leq I_o \leq 200 \text{ mA}$	7.87	8.2	8.53	V
		$10 \text{ V} \leq V_{P2} \leq 18 \text{ V}$	7.87	8.2	8.53	V
ΔV_{line}	line regulation	$10 \text{ V} \leq V_{P2} \leq 18 \text{ V}$	—	3	50	mV
ΔV_{load}	load regulation	$0.5 \text{ mA} \leq I_o \leq 200 \text{ mA}$	—	—	100	mV
SVRR	supply voltage ripple rejection	$f_i = 120 \text{ Hz}; V_i = 2 \text{ V (p-p)}$	60	70	—	dB
V_{drop}	dropout voltage	$V_{P2} = 8 \text{ V}; I_o = 200 \text{ mA}; \text{note 2}$	—	0.2	0.4	V
I_m	current limit	$V_o > 7 \text{ V}$	250	—	—	mA
I_{sc}	short-circuit current	$R_L \leq 0.5 \Omega; \text{note 3}$	40	—	—	mA
Regulator 4: pin REG4 ($I_o = 5 \text{ mA}$)						
$V_o(\text{REG4})$	output voltage of regulator 4	$0.5 \text{ mA} \leq I_o \leq 50 \text{ mA}$	7.87	8.2	8.53	V
		$10 \text{ V} \leq V_{P2} \leq 18 \text{ V}$	7.87	8.2	8.53	V
ΔV_{line}	line regulation	$10 \text{ V} \leq V_{P2} \leq 18 \text{ V}$	—	3	50	mV
ΔV_{load}	load regulation	$0.5 \text{ mA} \leq I_o \leq 50 \text{ mA}$	—	—	100	mV
SVRR	supply voltage ripple rejection	$f_i = 120 \text{ Hz}; V_i = 2 \text{ V (p-p)}$	65	70	—	dB
V_{drop}	dropout voltage	$V_{P2} = 8 \text{ V}; I_o = 50 \text{ mA}; \text{note 2}$	—	0.4	0.7	V
I_m	current limit	$V_o > 7 \text{ V}$	75	—	—	mA
I_{sc}	short-circuit current	$R_L \leq 0.5 \Omega; \text{note 3}$	20	—	—	mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Regulator 5: pin REG5 ($I_o = 5 \text{ mA}$)						
$V_o(\text{REG5})$	output voltage of regulator 5	$0.5 \text{ mA} \leq I_o \leq 50 \text{ mA}$	7.87	8.2	8.53	V
		$10 \text{ V} \leq V_{P2} \leq 18 \text{ V}$	7.87	8.2	8.53	V
ΔV_{line}	line regulation	$10 \text{ V} \leq V_{P2} \leq 18 \text{ V}$	—	3	50	mV
ΔV_{load}	load regulation	$0.5 \text{ mA} \leq I_o \leq 50 \text{ mA}$	—	—	100	mV
SVRR	supply voltage ripple rejection	$f_i = 120 \text{ Hz}; V_i = 2 \text{ V} (\text{p-p})$	60	70	—	dB
V_{drop}	dropout voltage	$V_{P2} = 8 \text{ V}; I_o = 50 \text{ mA}; \text{note 2}$	—	0.2	0.4	V
I_m	current limit	$V_o > 7 \text{ V}$	75	—	—	mA
I_{sc}	short-circuit current	$R_L \leq 0.5 \Omega; \text{note 3}$	20	—	—	mA
Power switch 1: pin SW1						
$V_{\text{drop(SW1)}}$	dropout voltage	$I_o = 200 \text{ mA}$	—	0.6	0.8	V
I_m	current limit	$V_o > 11.7 \text{ V}$	0.3	0.55	0.8	A
Power switch 2: pin SW2						
$V_{\text{drop(SW2)}}$	dropout voltage	$I_o = 200 \text{ mA}$	—	0.6	0.8	V
I_m	current limit	$V_o > 11.7 \text{ V}$	0.3	0.55	0.8	A

Notes

1. The quiescent current is measured when $R_L = \infty$ and $V_{\text{EN}} \leq 0.8 \text{ V}$.
2. The dropout voltage of a regulator is the voltage difference between V_{P2} and $V_o(\text{REG})$.
3. The foldback current protection limits the dissipation power at short-circuit.
4. The dropout voltage of regulator 2 is the voltage difference between V_{STCP} and $V_o(\text{REG2})$ and depends on the load current (see Fig.6).
5. The dropout voltage of regulator 2 is the voltage difference between V_{P2} and $V_o(\text{REG2})$ and depends on the load current (see Fig.7).

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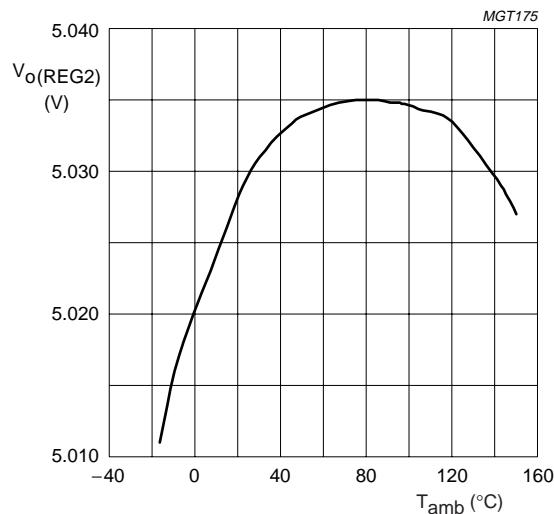


Fig.4 Output voltage of regulator 2 as a function of the ambient temperature.

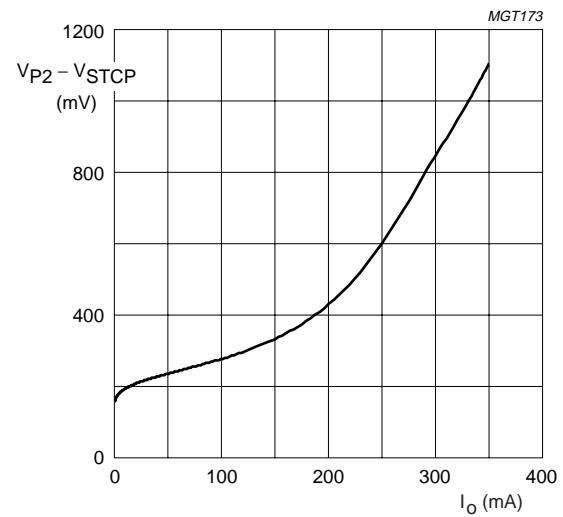


Fig.5 Voltage drop of V_P2 as a function of the output current of regulator 2.

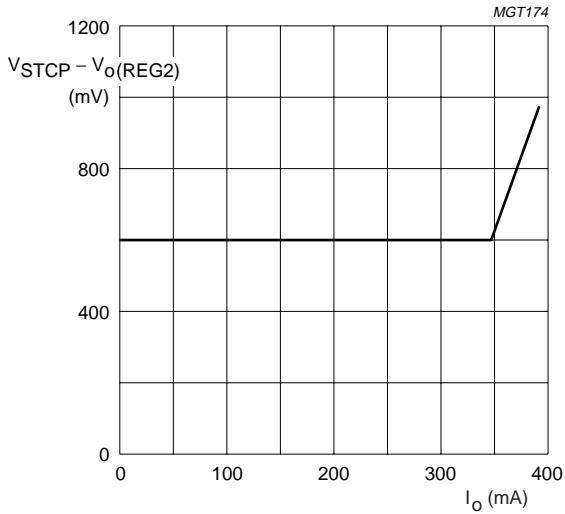


Fig.6 Dropout voltage of V_{STCP} as a function of the output current of regulator 2.

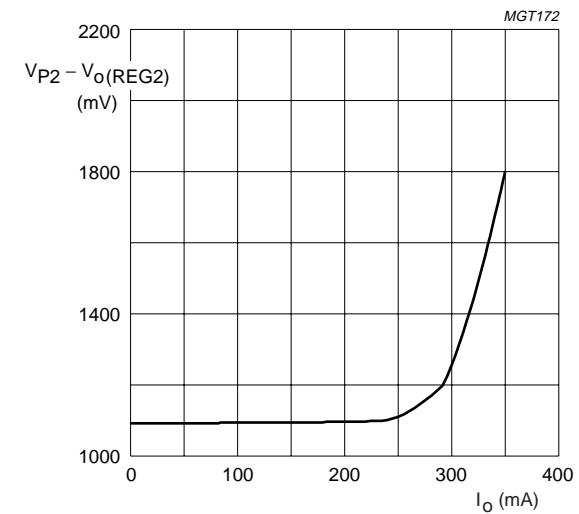
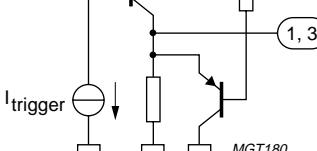
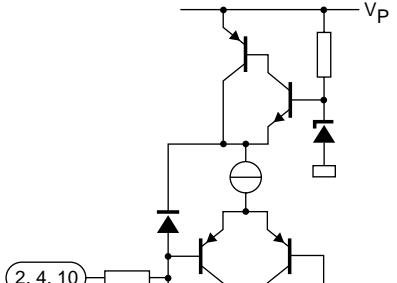
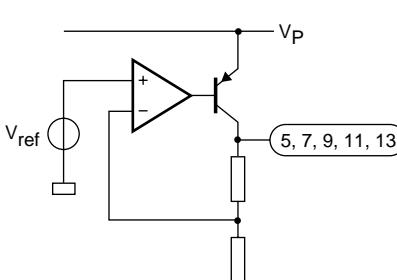
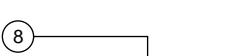


Fig.7 Dropout voltage of V_P2 as a function of the output current of regulator 2.

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INTERNAL PIN CONFIGURATION

PIN	SYMBOL	EQUIVALENT CIRCUIT
1	SW2	
3	SW1	
2	EN2	
4	EN3	
10	EN1	
5	REG5	
7	REG4	
9	REG3	
11	REG1	
13	REG2	
6	V_P2	
8	GND	
12	STCP	

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TEST AND APPLICATION INFORMATION

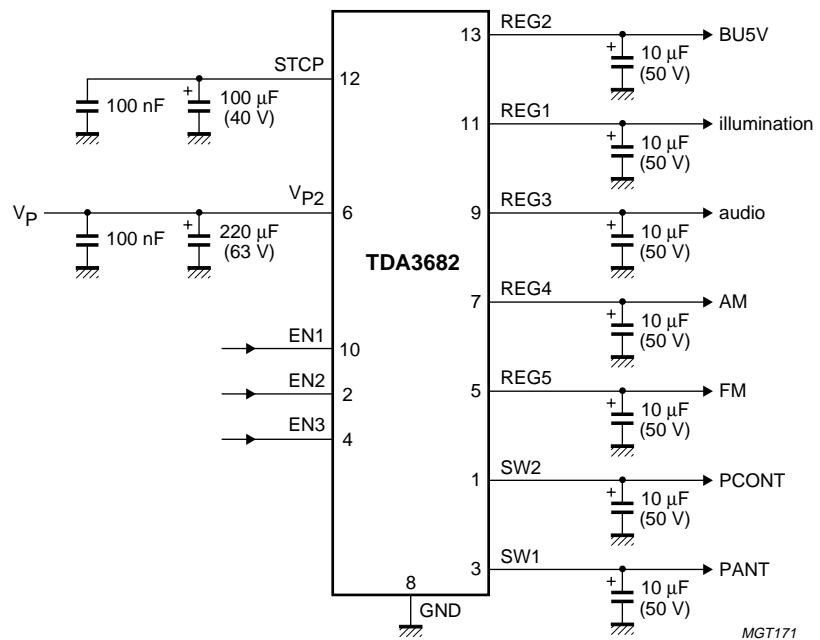


Fig.7 Test and application circuit.

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Application information

NOISE

The outputs of regulators 1 to 5 are designed in such a way that the noise is very low and the stability is very good. The noise output voltage depends on output capacitor C_o . Table 4 shows the influence of the output capacitor on the noise figure.

Table 4 Noise figures

REGULATOR	NOISE FIGURE (μV) ⁽¹⁾		
	$C_o = 10 \mu\text{F}$	$C_o = 47 \mu\text{F}$	$C_o = 100 \mu\text{F}$
1	170	130	120
2	110	100	95
3	140	110	100
4	140	110	100
5	140	110	100

Note

1. Measured at a bandwidth from 20 Hz to 20 kHz.

STABILITY

The regulators are made stable with the externally connected output capacitors. The stability can be guaranteed with almost any output capacitor. When only an electrolytic capacitor is used, the temperature behaviour of this output capacitor can cause oscillations at extreme low temperature. The following two examples show how an output capacitor value is selected. Oscillation problems can be avoided by adding a 47 nF capacitor in parallel with the electrolytic capacitor.

Example 1 (regulator 2)

Regulator 2 (BU5V) is stabilized with an electrolytic output capacitor of $10 \mu\text{F}$ ($\text{ESR} = 4 \Omega$). At $T_{\text{amb}} = -30^\circ\text{C}$ the capacitor value is decreased to $3 \mu\text{F}$ and the ESR is increased to 28Ω . As can be seen from Fig.8 the regulator will be unstable at $T_{\text{amb}} = -30^\circ\text{C}$.

Solution: To avoid problems with stability at low temperatures, the use of tantalum capacitors is recommended. Use a tantalum capacitor with a value of $10 \mu\text{F}$ or an electrolytic capacitor with a higher value.

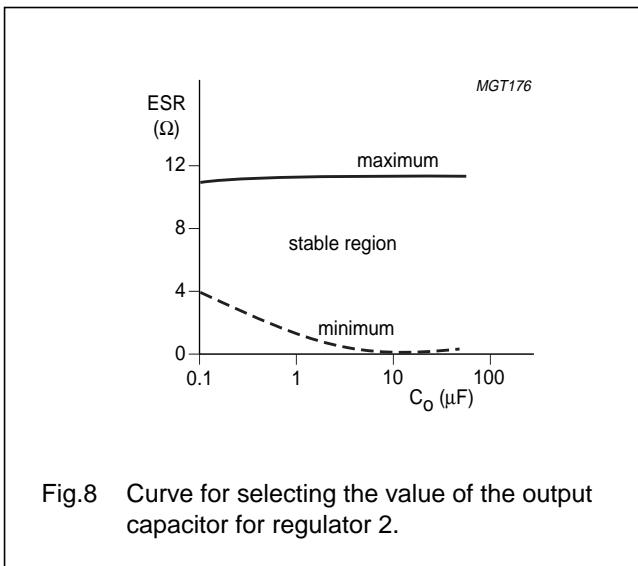


Fig.8 Curve for selecting the value of the output capacitor for regulator 2.

Example 2 (regulator 1)

Regulator 1 (illumination) is stabilized with an electrolytic capacitor of $2.2 \mu\text{F}$ ($\text{ESR} = 8 \Omega$). At $T_{\text{amb}} = -30^\circ\text{C}$ the capacitor value is decreased to $0.8 \mu\text{F}$ and the ESR is increased to 56Ω . As can be seen from Fig.9 the regulator will be stable at $T_{\text{amb}} = -30^\circ\text{C}$.

Even when only a small MKT capacitor of 47nF is used as the output capacitor, regulator 1 will remain stable over the temperature range.

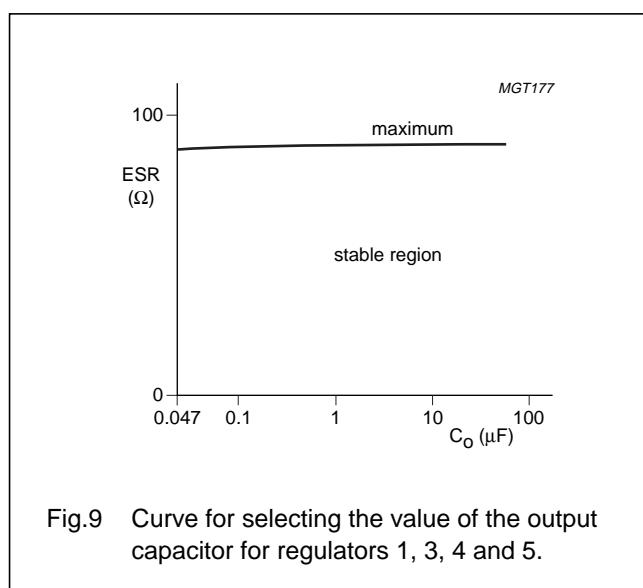


Fig.9 Curve for selecting the value of the output capacitor for regulators 1, 3, 4 and 5.

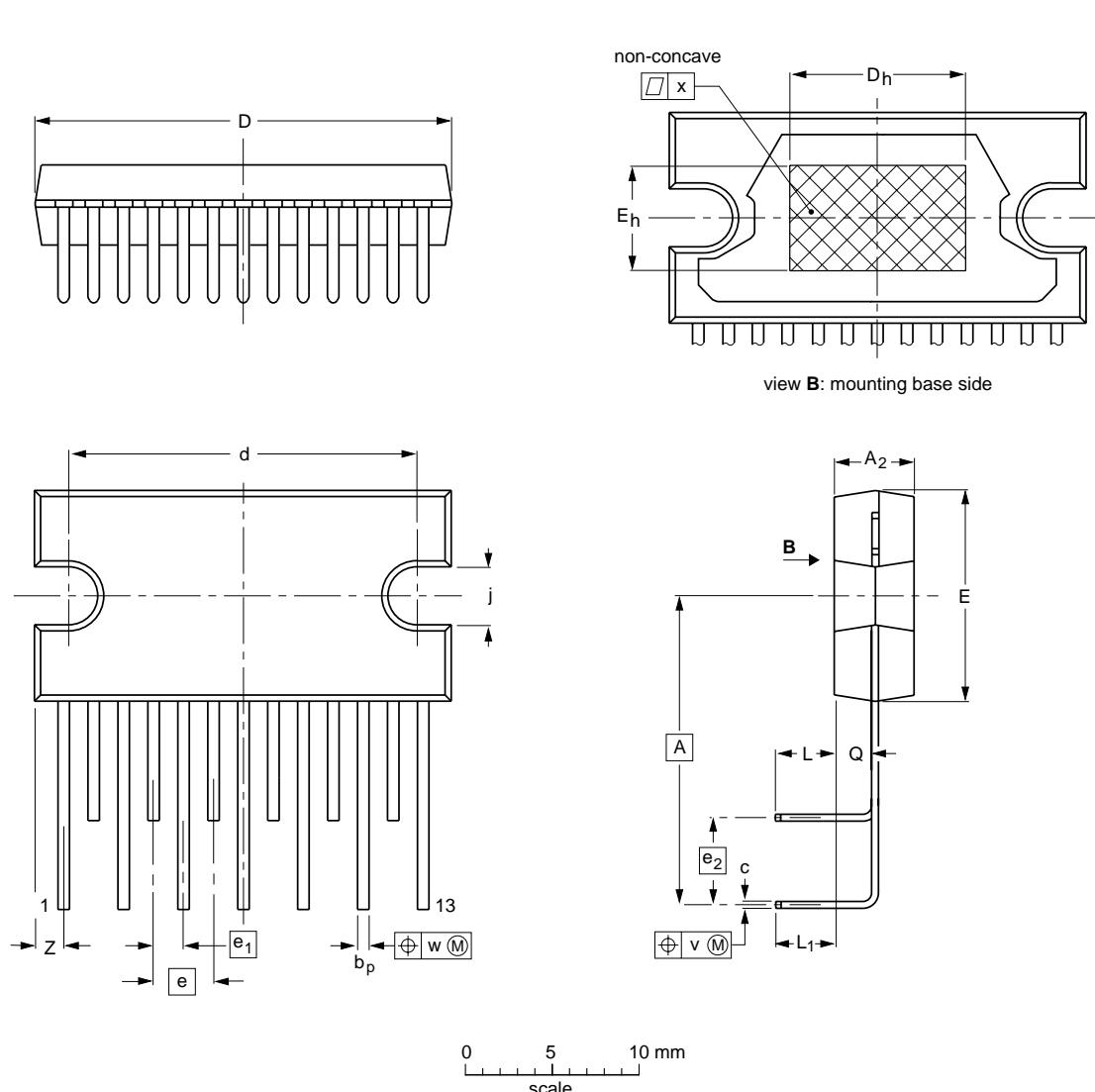
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PACKAGE OUTLINE

RDBS13P: plastic rectangular-DIL-bent-SIL power package; 13 leads

SOT528-2



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₁	Q	v	w	x	Z ⁽¹⁾
mm	17.7 4.4	4.6 0.60	0.75 0.38	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	3.75 3.15	3.75 3.15	2.1 1.8	0.6	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT528-2						00-10-19

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SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable ⁽¹⁾

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

Multiple voltage regulator with power switches

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DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
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Printed in The Netherlands

753503/02/pp20

Date of release: 2002 Mar 11

Document order number: 9397 750 09471

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