# 24-Bit, 156 kSPS, 112 dB Sigma-Delta ADC with On-Chip Buffers and Serial Interface

Data Sheet **AD7765**

## FEATURES

**High performance 24-bit Σ-Δ ADC**
**115 dB dynamic range at 78.125 kHz output data rate**
**112 dB dynamic range at 156 kHz output data rate**
**156 kHz maximum fully filtered output word rate**
**Pin-selectable oversampling rates of 128× and 256×**
**Low power mode**
**Flexible serial peripheral interface (SPI)**
**Fully differential modulator input**
**On-chip differential amplifier for signal buffering**
**On-chip reference buffer**
**Full band low-pass finite impulse response (FIR) filter**
**Overrange alert pin**
**Digital gain correction registers**
**Power-down mode**
**Synchronization of multiple devices via the $\overline{\text{SYNC}}$ pin**
**Daisy chaining**

## APPLICATIONS

**Data acquisition systems**
**Vibration analysis**
**Instrumentation**

## FUNCTIONAL BLOCK DIAGRAM

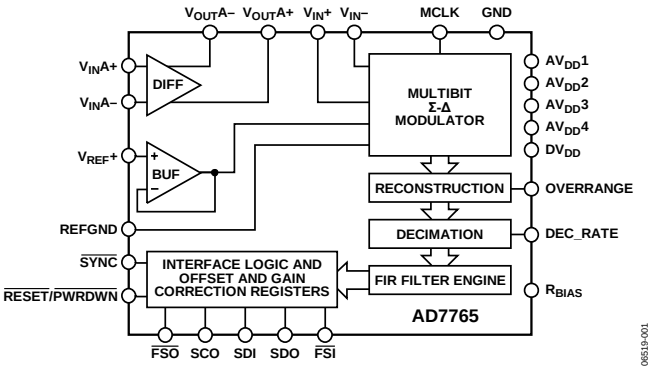


*Figure 1.*

**Table 1. Related Devices**

| Device No. | Description |
|---|---|
| AD7760 | 2.5 MSPS, 100 dB, parallel output, on-chip buffer |
| AD7762 | 625 kSPS, 109 dB, parallel output, on-chip buffer |
| AD7763 | 625 kSPS, 109 dB, serial output, on-chip buffers |
| AD7765 | 312 kSPS, 109 dB, serial output, on-chip buffers |
| AD7766 | 128 kSPS/64 kSPS/32 kSPS, 8.5 mW, 109 dB SNR |
| AD7767 | 128 kSPS/64 kSPS/32 kSPS, 8.5 mW, 109 dB SNR |

## GENERAL DESCRIPTION

The AD7765 is a high performance, 24-bit sigma-delta (Σ-Δ) analog-to-digital converter (ADC). It combines wide input bandwidth, high speed, and performance of 112 dB dynamic range at a 156 kHz output data rate. With excellent dc specifications, the converter is ideal for high speed data acquisition of ac signals where dc data is also required.

Using the AD7765 eases front-end antialias filtering requirements, simplifying the design process significantly. The AD7765 offers pin-selectable decimation rates of 128× and 256×. Other features include an integrated buffer to drive the reference, as well as a fully differential amplifier to buffer and level shift the input to the modulator.

An overrange alert pin indicates when an input signal exceeds the acceptable range. The addition of internal gain and internal overrange registers makes the AD7765 a compact, highly integrated data acquisition device requiring minimal peripheral components.

The AD7765 also offers a low power mode, significantly reducing power dissipation without reducing the output data rate or available input bandwidth.

The differential input is sampled at up to 40 MSPS by an analog modulator. The modulator output is processed by a series of low-pass filters. The external clock frequency applied to the AD7765 determines the sample rate, filter corner frequencies, and output word rate.

The AD7765 device boasts a full band on-board FIR filter. The full stop-band attenuation of the filter is achieved at the Nyquist frequency. This feature offers increased protection from signals that lie above the Nyquist frequency being aliased back into the input signal bandwidth.

The reference voltage supplied to the AD7765 determines the input range. With a 4 V reference, the analog input range is ±3.2768 V differential, biased around a common mode of 2.048 V. This common-mode biasing is achieved using the on-chip differential amplifier, further reducing the external signal conditioning requirements.

The AD7765 is available in a 28-lead TSSOP package and is specified over the industrial temperature range of −40°C to +85°C.

**Rev. C** **Document Feedback**


**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** 
**Technical Support** **www.analog.com**

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# SPECIFICATIONS

$AV_{DD}1 = DV_{DD} = 2.5$ V, $AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = 5$ V, $V_{REF}+ = 4.096$ V, MCLK amplitude = 5 V, $T_A = +25°C$, normal power mode, using the on-chip amplifier with components as shown in the Optimal row in Table 10, unless otherwise noted.[1]

**Table 2.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| Decimate 256× | | | | | |
| Normal Power Mode | MCLK = 40 MHz, output data rate (ODR) = 78.125 kHz, $f_{IN}$ = 1 kHz sine wave | | | | |
| Dynamic Range | Modulator inputs shorted | 110 | 115 | | dB |
| | Differential amplifier inputs shorted | | 113.4 | | dB |
| Signal-to-Noise Ratio (SNR)[2] | Input amplitude = −0.5 dB | 106 | 109 | | dB |
| Spurious-Free Dynamic Range (SFDR) | Nonharmonic | | 130 | | dBFS |
| Total Harmonic Distortion (THD) | Input amplitude = −0.5 dB | | −105 | | dB |
| | Input amplitude = −6 dB | | −103 | | dB |
| | Input amplitude = −60 dB | | −71 | | dB |
| Low Power Mode | MCLK = 40 MHz, ODR = 78.125 kHz, $f_{IN}$ = 1 kHz sine wave | | | | |
| Dynamic Range | Modulator inputs shorted | 110 | 113 | | dB |
| | Differential amplifier inputs shorted | | 112 | | dB |
| SNR[2] | Input amplitude = −0.5 dB | 106 | 109 | | dB |
| THD | Input amplitude = −0.5 dB | | −105 | | dB |
| | Input amplitude = −6 dB | | −111 | −100 | dB |
| | Input amplitude = −60 dB | | −76 | | dB |
| Decimate 128× | | | | | |
| Normal Power Mode | MCLK = 40 MHz, ODR = 156.25 kHz, $f_{IN}$ = 1 kHz sine wave | | | | |
| Dynamic Range | Modulator inputs shorted | 108 | 112 | | dB |
| | Differential amplifier inputs shorted | | 110.4 | | dB |
| SNR[2] | | 105 | 107 | | dB |
| SFDR | Nonharmonic | | 130 | | dBFS |
| THD | Input amplitude = −0.5 dB | | −105 | | dB |
| | Input amplitude = −6 dB | | −103 | | dB |
| Intermodulation Distortion (IMD) | Input amplitude = −6 dB, $f_{IN}$ A = 50.3 kHz, $f_{IN}$ B = 47.3 kHz | | | | |
| | Second-order terms | | −117 | | dB |
| | Third-order terms | | −108 | | dB |
| Low Power Mode | MCLK = 40 MHz, ODR = 156.25 kHz, $f_{IN}$ = 1 kHz sine wave | | | | |
| Dynamic Range | Modulator inputs shorted | 109 | 110 | | dB |
| | Differential amplifier inputs shorted | | 109 | | dB |
| SNR[2] | Input amplitude = −0.5 dB | 105 | 107 | | dB |
| THD | Input amplitude = −0.5 dB | | −105 | | dB |
| | Input amplitude = −6 dB | | −111 | | dB |
| | Input amplitude = −6 dB | | | −100 | dB |
| IMD | Input amplitude = −6 dB, $f_{IN}$ A= 50.3 kHz, $f_{IN}$ B = 47.3 kHz | | | | |
| | Second-order terms | | −134 | | dB |
| | Third-order terms | | −110 | | dB |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC ACCURACY | | | | | |
| Resolution | Guaranteed monotonic to 24 bits | | | 24 | Bits |
| Integral Nonlinearity | Normal power mode | | 0.0036 | | % |
| | Low power mode | | 0.0014 | | % |
| Zero Error | Normal power mode | | 0.006 | 0.03 | % |
| | Including on-chip amplifier | | 0.04 | | % |
| | Low power mode | | 0.002 | 0.024 | % |
| Gain Error | | | 0.018 | | % |
| | Including on-chip amplifier | | 0.04 | | % |
| Zero Error Drift | Does not include on-chip amplifier | | 0.00006 | | %FS/°C |
| Gain Error Drift | Does not include on-chip amplifier | | 0.00005 | | %FS/°C |
| DIGITAL FILTER CHARACTERISTICS | Normal and low power modes | | | | |
| Pass-Band Ripple | | | 0.1 | | dB |
| Pass Band[3] | −1 dB frequency | | | ODR × 0.4016 | kHz |
| −3 dB Bandwidth[3] | | | | ODR × 0.4096 | kHz |
| Stop Band[3] | Beginning of stop band | | | ODR × 0.5 | kHz |
| Stop-Band Attenuation | Decimate 128× | | −120 | | dB |
| | Decimate 256× | | −115 | | dB |
| Group Delay | See Table 8 and Table 9 | | | | |
| ANALOG INPUT | | | | | |
| Differential Input Voltage | Modulator input pins: $V_{IN}+ - V_{IN}-$, $V_{REF}+ = 4.096$ V | | | ±3.2768 | V p-p |
| Input Capacitance | At on-chip differential amplifier inputs | | 5 | | pF |
| | At modulator inputs | | 29 | | pF |
| REFERENCE INPUT/OUTPUT | | | | | |
| $V_{REF+}$ Input Voltage | $AV_{DD}3 = 5$ V ± 5% | | | 4.096 | V |
| $V_{REF+}$ Input DC Leakage Current | | | | ±1 | µA |
| $V_{REF+}$ Input Capacitance | | | 5 | | pF |
| DIGITAL INPUT/OUTPUT | | | | | |
| MCLK Input Amplitude | | 2.25 | | 5.25 | V |
| Input Capacitance | | | 7.3 | | pF |
| Input Leakage Current | | | | ±1 | µA/pin |
| $V_{INH}$ | | 0.8 × DVDD | | | V |
| $V_{INL}$ | | | | 0.2 × DVDD | V |
| $V_{OH}$[4] | | 2.2 | | | V |
| $V_{OL}$ | | | | 0.1 | V |
| ON-CHIP DIFFERENTIAL AMPLIFIER | | | | | |
| Input Impedance | | | >1 | | MΩ |
| Bandwidth for 0.1 dB Flatness | | | | 125 | kHz |
| Common-Mode Input Voltage | Common-mode voltage range at amplifier input pins $V_{IN}A-$ and $V_{IN}A+$ | 0.8 | | +2.2 | V |
| Common-Mode Output Voltage | On-chip differential amplifier pins: $V_{OUT}A+$ and $V_{OUT}A-$ | | 2.048 | | V |
| POWER REQUIREMENTS | | | | | |
| AVDD1 (Modulator Supply) | | 2.375 | 2.5 | 2.625 | V |
| AVDD2 (General Supply) | | 4.75 | 5 | 5.25 | V |
| AVDD3 (Differential Amplifier Supply) | 5 V supply required for 4.096 V reference | 3.15 | 5 | 5.25 | V |
| AVDD4 (Reference Buffer Supply) | 5 V supply required for 4.096 V reference | 3.15 | 5 | 5.25 | V |
| DVDD | | 2.375 | 2.5 | 2.625 | V |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Normal Power Mode | | | | | |
| $AI_{DD}1$ (Modulator) | | | 19 | | mA |
| $AI_{DD}2$ (General)[5] | MCLK = 40 MHz | | 13 | | mA |
| $AI_{DD}3$ (Differential Amplifier) | AVDD3 = 5 V | | 10 | | mA |
| $AI_{DD}4$ (Reference Buffer) | AVDD4 = 5 V | | 9 | | mA |
| $DI_{DD}$[5] | MCLK = 40 MHz | | 37 | | mA |
| Low Power Mode | | | | | |
| $AI_{DD}1$ (Modulator) | | | 10 | | mA |
| $AI_{DD}2$ (General)[5] | MCLK = 40 MHz | | 7 | | mA |
| $AI_{DD}3$ (Differential Amplifier) | $AV_{DD}3$ = 5 V | | 5.5 | | mA |
| $AI_{DD}4$ (Reference Buffer) | $AV_{DD}4$ = 5 V | | 5 | | mA |
| $DI_{DD}$[5] | MCLK = 40 MHz | | 20 | | mA |
| POWER DISSIPATION | | | | | |
| Normal Power Mode | MCLK = 40 MHz, decimate 128× | | 300 | 371 | mW |
| Low Power Mode | MCLK = 40 MHz, decimate 128× | | 160 | 215 | mW |
| Power-Down Mode[6] | $\overline{\text{PWRDWN}}$ pin held logic low | | 1 | | mW |

[1] See the Terminology section.
[2] SNR specifications in decibels are referred to a full-scale input, FS, and are tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[3] The output data rate (ODR) = [(MCLK/2)]/decimation rate. That is, the maximum ODR for AD7765 = [(40 MHz/2)/128] = 156.25 kHz.
[4] Tested with a 400 µA load current.
[5] Tested at MCLK = 40 MHz. This current scales linearly with the applied MCLK frequency.
[6] Tested at 125°C.

## TIMING SPECIFICATIONS

$AV_{DD}1 = DV_{DD} = 2.5$ V, $AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = 5$ V, $V_{REF}+ = 4.096$ V, $T_A = 25°C$, $C_{LOAD} = 25$ pF.

**Table 3.**

| | Limit at $T_{MIN}$, $T_{MAX}$ | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Min** | **Typ** | **Max** | **Unit** | **Description** |
| $f_{MCLK}$ | 500 | | | kHz | Applied master clock frequency |
| | | | 40 | MHz | |
| $f_{ICLK}$ | 250 | | | kHz | Internal modulator clock derived from MCLK |
| | | | 20 | MHz | |
| $t_1$ | | $1 \times t_{ICLK}$ | | sec | SCO high period |
| $t_2$ | | $1 \times t_{ICLK}$ | | sec | SCO low period |
| $t_3$ | | 1 | 2.5 | ns | SCO rising edge to $\overline{FSO}$ falling edge |
| $t_4$ | | 2 | 3.5 | ns | Data access time, $\overline{FSO}$ falling edge to data active |
| $t_5$ | | | 8 | ns | MSB data access time, SDO active to SDO valid |
| $t_6$ | 40 | | | ns | Data hold time (SDO valid to SCO rising edge) |
| $t_7$ | | | 9.5 | ns | Data access time (SCO rising edge to SDO valid) |
| $t_8$ | | 2 | 2.5 | ns | SCO rising edge to $\overline{FSO}$ rising edge |
| $t_9$ | | | $32 \times t_{SCO}$ | sec | $\overline{FSO}$ low period |
| $t_{10}$ | 12 | | | ns | Setup time from $\overline{FSI}$ falling edge to SCO falling edge |
| $t_{11}$ | $1 \times t_{SCO}$ | | | sec | $\overline{FSI}$ low period |
| $t_{12}$[1] | | | $32 \times t_{SCO}$ | sec | $\overline{FSI}$ low period |
| $t_{13}$ | 12 | | | ns | SDI setup time for the first data bit |
| $t_{14}$ | 12 | | | ns | SDI setup time |
| $t_{15}$ | | | 0 | ns | SDI hold time |
| $t_{R\ MIN}$ | $1 \times t_{MCLK}$ | | | sec | Minimum time for a valid $\overline{RESET}$ pulse |
| $t_{R\ HOLD}$ | 5 | | | ns | Minimum time between the MCLK rising edge and $\overline{RESET}$ rising edge |
| $t_{R\ SETUP}$ | 5 | | | ns | Minimum time between the $\overline{RESET}$ rising edge and MCLK rising edge |
| $t_{S\ MIN}$ | $4 \times t_{MCLK}$ | | | sec | Minimum time for a valid $\overline{SYNC}$ pulse |
| $t_{S\ HOLD}$ | 5 | | | ns | Minimum time between the MCLK falling edge and $\overline{SYNC}$ rising edge |
| $t_{S\ SETUP}$ | 5 | | | ns | Minimum time between the $\overline{SYNC}$ rising edge and MCLK falling edge |

[1] This is the maximum time $\overline{FSI}$ can be held low when writing to an individual device (a device that is not daisy-chained).

### *Timing Diagrams*

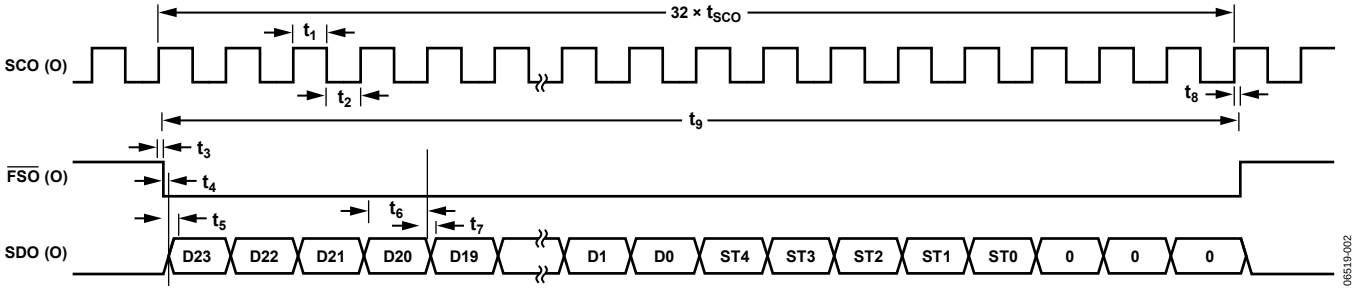



*Figure 2. Serial Read Timing Diagram*

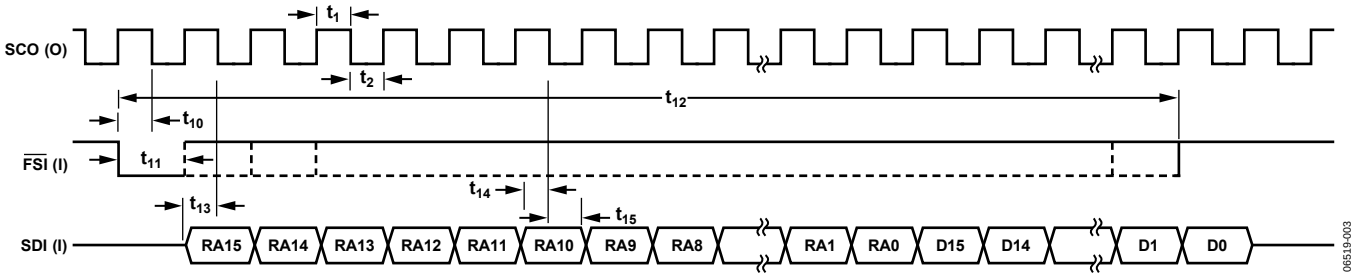



*Figure 3. Register Write Timing Diagram*

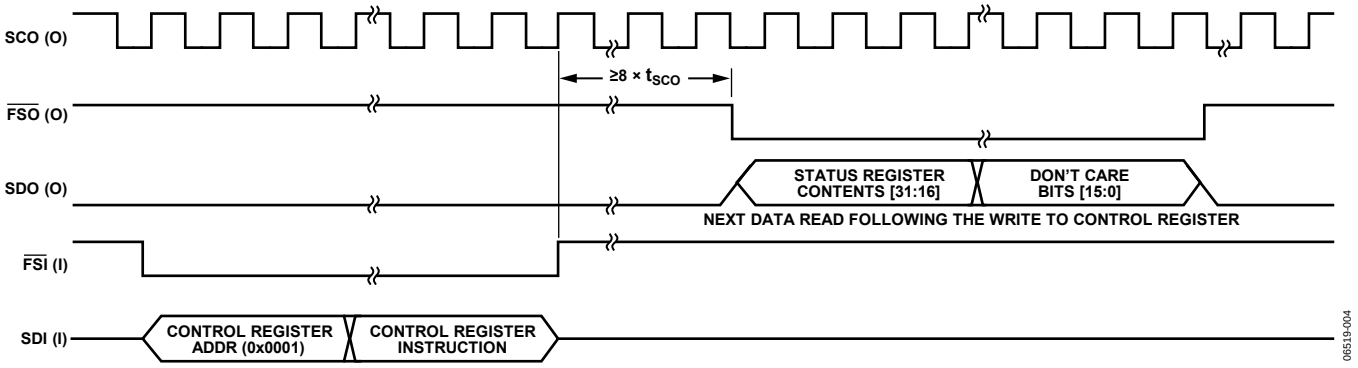



*Figure 4. Status Register Read Cycle Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 4.**

| Parameters | Rating |
|---|---|
| $AV_{DD}1$ to Ground | −0.3 V to +2.8 V |
| $AV_{DD}2$, $AV_{DD}3$, $AV_{DD}4$ to Ground | −0.3 V to +6 V |
| $DV_{DD}$ to Ground | −0.3 V to +2.8 V |
| $V_{IN}A+$, $V_{IN}A-$ to Ground[1] | −0.3 V to +6 V |
| $V_{IN}+$, $V_{IN}-$ to Ground[1] | −0.3 V to +6 V |
| Digital Input Voltage to Ground[2] | −0.3 V to +2.8 V |
| $V_{REF}+$ to Ground[3] | −0.3 V to +6 V |
| Input Current to Any Pin Except Supplies[4] | ±10 mA |
| Operating Temperature Range, Commercial | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| $\theta_{JA}$ Thermal Impedance (1s0p)[5] | 143°C/W |
| $\theta_{JA}$ Thermal Impedance (2s2p)[6, 7] | 71.1°C/W |
| $\theta_{JC}$[8] Thermal Impedance | 20°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |
| ESD | 1 kV |

[1] The absolute maximum voltage for $V_{IN}-$, $V_{IN}+$, $V_{IN}A-$, and $V_{IN}A+$ is 6.0 V or $AV_{DD}3$ + 0.3 V, whichever is lower.
[2] The absolute maximum voltage on the digital input is 3.0 V or $DV_{DD}$ + 0.3 V, whichever is lower.
[3] The absolute maximum voltage on the $V_{REF+}$ input is 6.0 V or $AV_{DD}4$ + 0.3 V, whichever is lower.
[4] Transient currents of up to 100 mA do not cause SCR latch-up.
[5] 1s0p means a single-layer printed circuit board (PCB), which includes one signal layer and zero power layers.
[6] 2s2p means a 4-layer PCB, which includes two signal layers and two power layers.
[7] $\theta_{JA}$ for a 2s2p PCB is derived from simulation.
[8] The revised $\theta_{JC}$ (thermal impedance) is derived from simulation.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

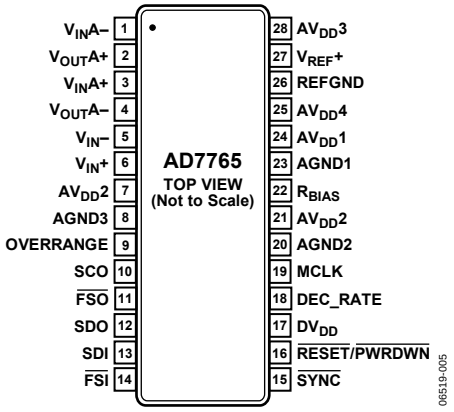



*Figure 5. Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{IN}A-$ | Negative Input to the Differential Amplifier. |
| 2 | $V_{OUT}A+$ | Positive Output from the Differential Amplifier. |
| 3 | $V_{IN}A+$ | Positive Input to the Differential Amplifier. |
| 4 | $V_{OUT}A-$ | Negative Output from the Differential Amplifier. |
| 5 | $V_{IN}-$ | Negative Input to the Modulator. |
| 6 | $V_{IN}+$ | Positive Input to the Modulator. |
| 7, 21 | $AV_{DD}2$ | 5 V Power Supply. Decouple Pin 7 to AGND3 (Pin 8) with a 100 nF capacitor. Decouple Pin 21 to AGND1 (Pin 23) with a 100 nF capacitor. |
| 8 | AGND3 | Power Supply Ground for the Analog Circuitry. |
| 9 | OVERRANGE | Overrange Pin. This pin outputs a logic high to indicate that the user applied an analog input that is approaching the limit of the analog input to the modulator. |
| 10 | SCO | Serial Clock Out. This clock signal is derived from the internal ICLK signal. The frequency of this clock is equal to ICLK. See the Clocking the AD7765 section for more information. |
| 11 | $\overline{FSO}$ | Frame Sync Out. This signal frames the serial data output and is 32 SCO periods wide. |
| 12 | SDO | Serial Data Out. Data and status are output on this pin during each serial transfer. Each bit is clocked out on an SCO rising edge and is valid on the falling edge. See the AD7765 Serial Interface section for more information. |
| 13 | SDI | Serial Data In. The first data bit (MSB) must be valid on the next SCO falling edge after the $\overline{FSI}$ event is latched. Thirty-two bits are required for each write; the first 16-bit word contains the device and register address, and the second word contains the data. See the AD7765 Serial Interface section for more information. |
| 14 | $\overline{FSI}$ | Frame Sync Input. The status of this pin is checked on the falling edge of SCO. If this pin is low, then the first data bit is latched in on the next SCO falling edge. See the AD7765 Serial Interface section for more information. |
| 15 | $\overline{SYNC}$ | Synchronization Input. A falling edge on this pin resets the internal filter. Use this pin to synchronize multiple devices in a system. See the Synchronization section for more information. |
| 16 | $\overline{RESET}/\overline{PWRDWN}$ | Reset/Power-Down Pin. When a logic low is sensed on this pin, the device is powered down and all internal circuitry is reset. |
| 17 | $DV_{DD}$ | 2.5 V Power Supply for the Digital Circuitry and FIR Filter. Decouple this pin to the ground plane with a 100 nF capacitor. |
| 18 | DEC_RATE | Decimation Rate Pin. This pin selects one of the three decimation rate modes. When 2.5 V is applied to this pin, a decimation rate of 128× is selected. Select a decimation rate of 256× by setting this pin to ground. |
| 19 | MCLK | Master Clock Input. A low jitter digital clock must be applied to this pin. The output data rate depends on the frequency of this clock. See the Clocking the AD7765 section for more information. |
| 20 | AGND2 | Power Supply Ground for the Analog Circuitry. |
| 22 | $R_{BIAS}$ | Bias Current Setting Pin. This pin must be decoupled to the ground plane. For more information, see the Bias Resistor Selection section. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 23 | AGND1 | Power Supply Ground for the Analog Circuitry. |
| 24 | $AV_{DD}1$ | 2.5 V Power Supply for the Modulator. Decouple this pin to AGND1 (Pin 23) with a 100 nF capacitor. |
| 25 | $AV_{DD}4$ | 3.3 V to 5 V Power Supply for the Reference Buffer. Decouple this pin to AGND1 (Pin 23) with a 100 nF capacitor. |
| 26 | REFGND | Reference Ground. This pin is the ground connection for the reference voltage. |
| 27 | $V_{REF}+$ | Reference Input. |
| 28 | $AV_{DD}3$ | 3.3 V to 5 V Power Supply for the Differential Amplifier. Decouple this pin to the ground plane with a 100 nF capacitor. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$AV_{DD}1 = DV_{DD} = 2.5$ V, $AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = 5$ V, $V_{REF}+ = 4.096$ V, MCLK amplitude = 5 V, $T_A = 25°C$. Linearity plots measured to 16-bit accuracy; input signal reduced to avoid modulator overload and digital clipping; fast Fourier transforms (FFTs) generated from 8,192 samples.

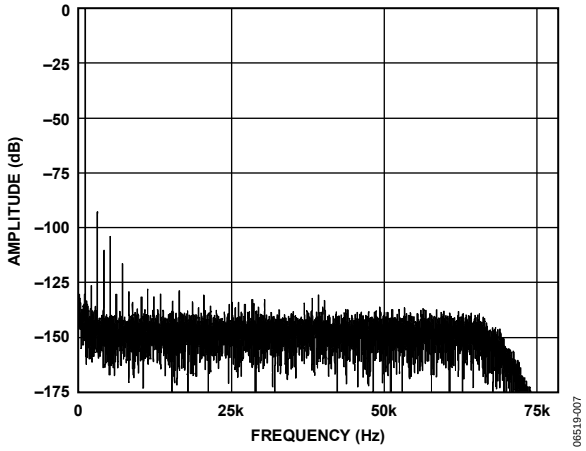



*Figure 6. Normal Power Mode; FFT, 1 kHz, −0.5 dB Input Tone, 128× Decimation Rate*

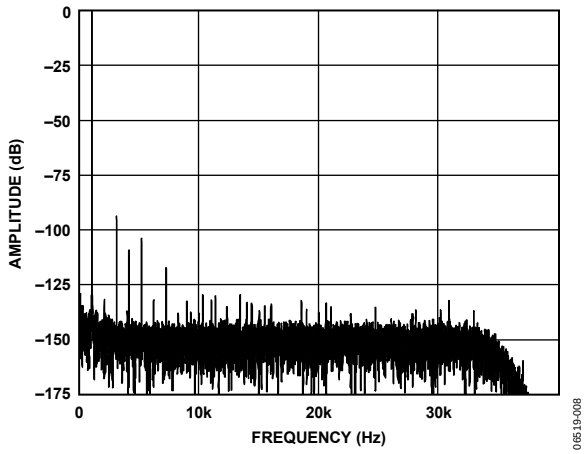



*Figure 7. Normal Power Mode; FFT, 1 kHz, −0.5 dB Input Tone, 256× Decimation Rate*

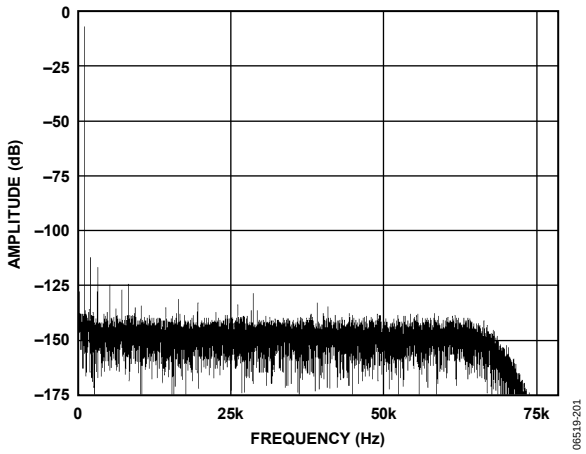



*Figure 8. Normal Power Mode; FFT, 1 kHz, −6 dB Input Tone, 128× Decimation Rate*

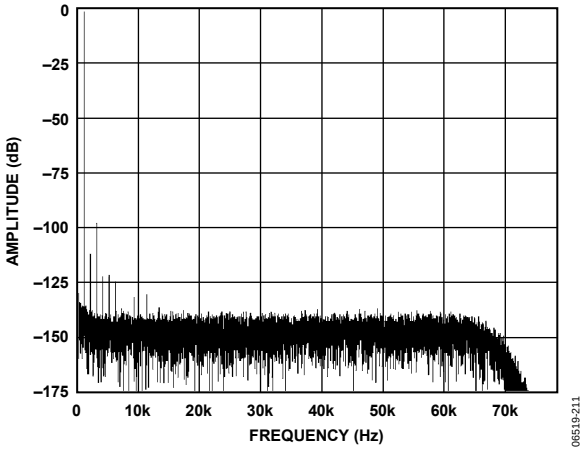



*Figure 9. Low Power Mode; FFT, 1 kHz, −0.5 dB Input Tone, 128× Decimation Rate*

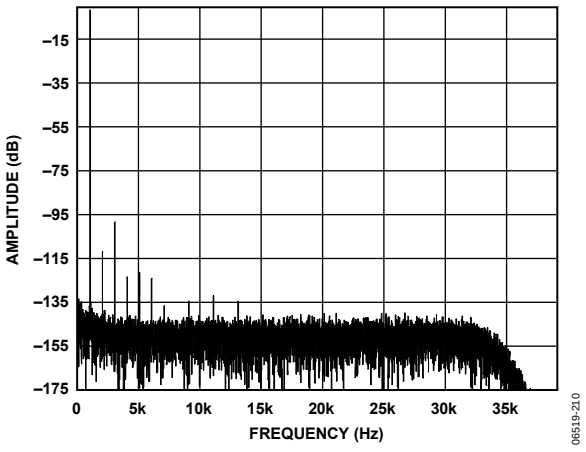



*Figure 10. Low Power Mode; FFT, 1 kHz, −0.5 dB Input Tone, 256× Decimation Rate*

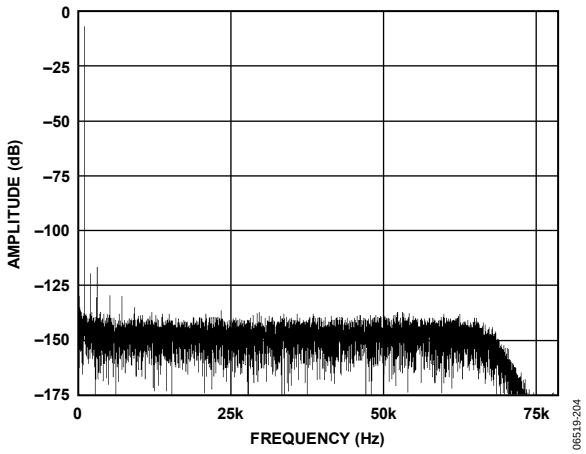



*Figure 11. Low Power Mode; FFT, 1 kHz, −6 dB Input Tone, 128× Decimation Rate*

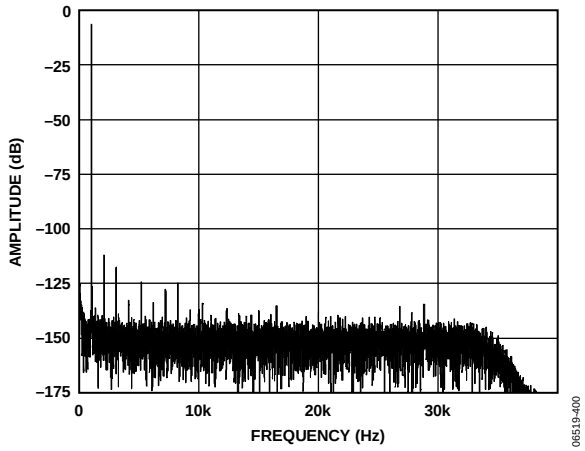



Figure 12. Normal Power Mode; FFT, 1 kHz, −6 dB Input Tone, 256× Decimation Rate

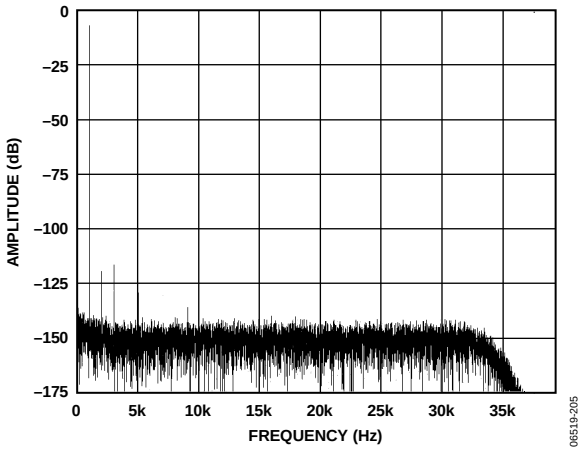



Figure 15. Low Power Mode; FFT, 1 kHz, −6 dB Input Tone, 256× Decimation Rate

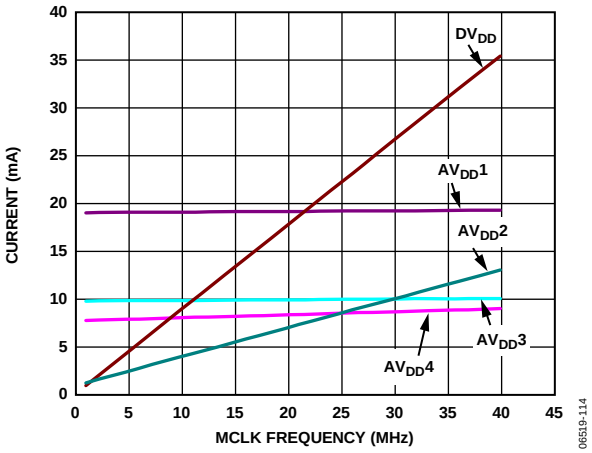



Figure 13. Normal Power Mode; Current Consumption vs. MCLK Frequency, 128× Decimation Rate

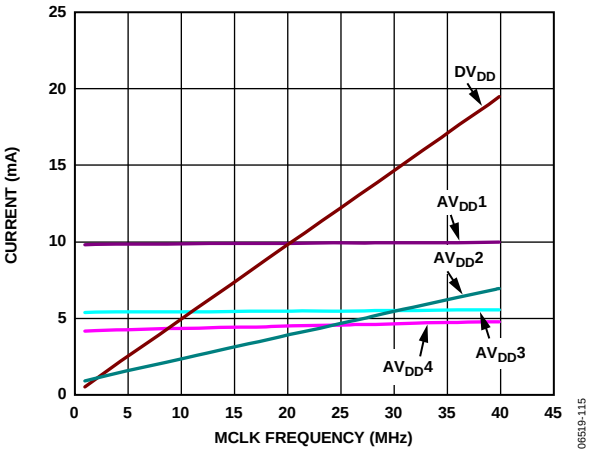



Figure 16. Low Power Mode; Current Consumption vs. MCLK Frequency, 128× Decimation Rate

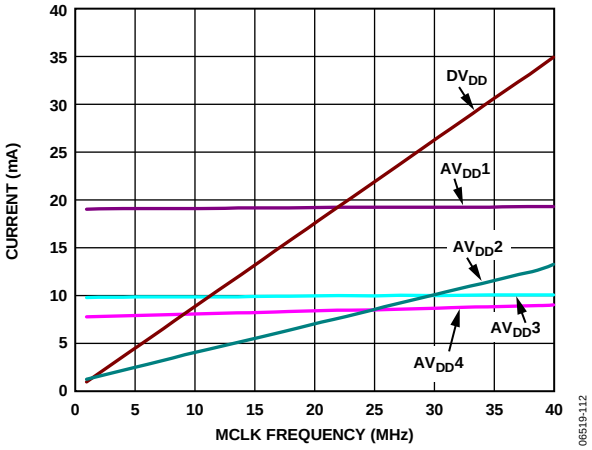



Figure 14. Normal Power Mode; Current Consumption vs. MCLK Frequency, 256× Decimation Rate

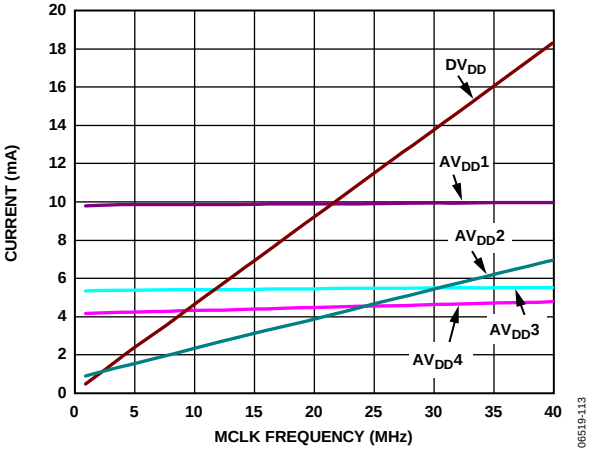



Figure 17. Low Power Mode; Current Consumption vs. MCLK Frequency, 256× Decimation Rate

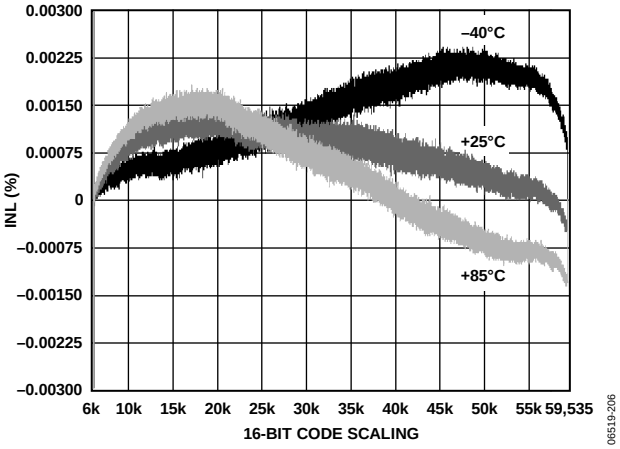



Figure 18. Normal Power Mode INL

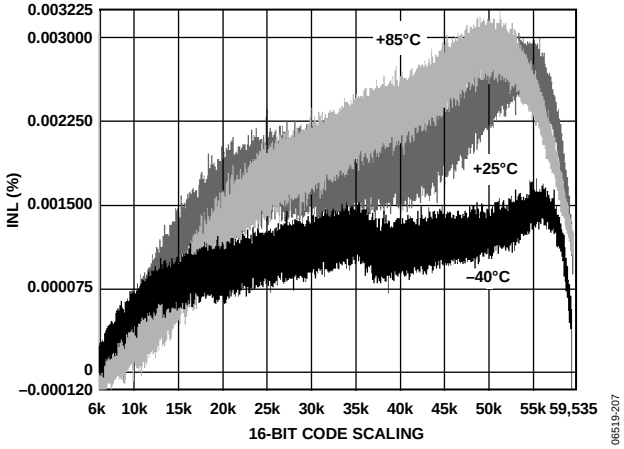



Figure 21. Low Power Mode INL

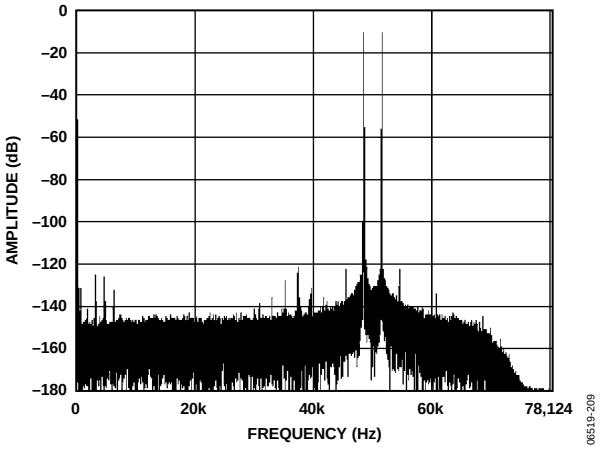



Figure 19. Normal Power Mode; IMD, $f_{IN}$ A = 49.7 kHz, $f_{IN}$ B = 50.3 kHz, 50 kHz Center Frequency, 128× Decimation Rate

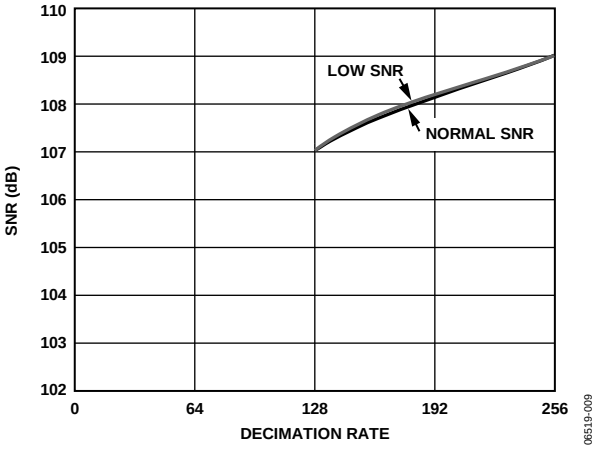



Figure 22. Normal and Low Power Mode; SNR vs. Decimation Rate, 1 kHz, −0.5 dB Input Tone

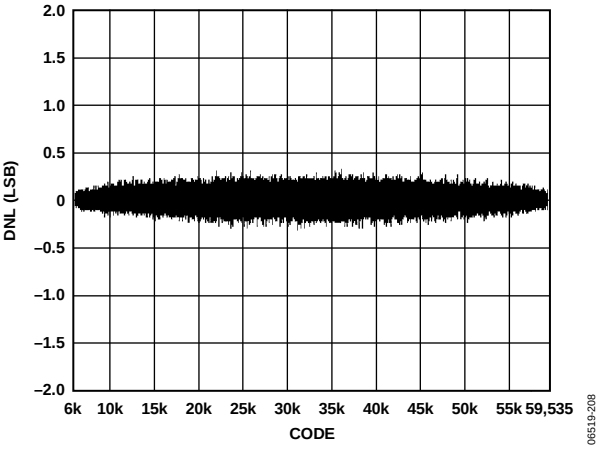



Figure 20. DNL Plot

# TERMINOLOGY

**Signal-to-Noise Ratio (SNR)**
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels (dB).

**Total Harmonic Distortion (THD)**
THD is the ratio of the rms sum of the harmonics to the fundamental. For the AD7765, THD is defined as

$$THD\ (\text{dB}) = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
$V_2$, $V_3$, $V_4$, $V_5$, and $V_6$ are the rms amplitudes of the second to the sixth harmonics.
$V_1$ is the rms amplitude of the fundamental.

**Nonharmonic Spurious-Free Dynamic Range (SFDR)**
Nonharmonic SFDR is the ratio of the rms signal amplitude to the rms value of the peak spurious spectral component, excluding harmonics.

**Dynamic Range**
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

**Intermodulation Distortion**
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n is equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7765 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are typically distanced in frequency from the original sine waves, and the third-order terms are typically at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is per the THD specification, where the calculation is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals, expressed in decibels.

**Integral Nonlinearity (INL)**
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

**Differential Nonlinearity (DNL)**
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

**Zero Error**
Zero error is the difference between the ideal midscale input voltage (when both inputs are shorted together) and the actual voltage producing the midscale output code.

**Zero Error Drift**
Zero error drift is the change in the actual zero error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

**Gain Error**
The first code transition (from 100 … 000 to 100 … 001) occurs for an analog voltage 1/2 LSB above the nominal negative full scale. The last code transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1 ½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition, from the difference between the ideal levels.

**Gain Error Drift**
Gain error drift is the change in the actual gain error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

# THEORY OF OPERATION

The AD7765 features an on-chip fully differential amplifier to feed the Σ-Δ modulator pins, an on-chip reference buffer, and a FIR filter block to perform the required digital filtering of the Σ-Δ modulator output. Using this Σ-Δ conversion technique with the added digital filtering, the analog input is converted to an equivalent digital word.

## Σ-Δ MODULATION AND DIGITAL FILTERING

The input waveform applied to the modulator is sampled, and an equivalent digital word is output to the digital filter at a rate equal to $f_{ICLK}$. By employing oversampling, the quantization noise is spread across a wide bandwidth from 0 to $f_{ICLK}$. This means that the noise energy contained in the signal band of interest is reduced (see Figure 23). To further reduce the quantization noise, a high-order modulator is employed to shape the noise spectrum so that most of the noise energy is shifted out of the signal band (see Figure 24).

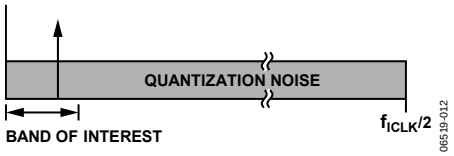



*Figure 23. Σ-Δ ADC, Quantization Noise*

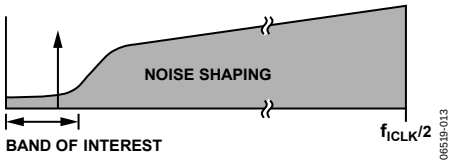



*Figure 24. Σ-Δ ADC, Noise Shaping*

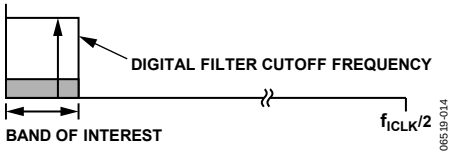



*Figure 25. Σ-Δ ADC, Digital Filter Cutoff Frequency*

The modulator sampling rate, $f_{ICLK}$, is dependent on the power mode chosen. Table 6 details the relationship between MCLK and $f_{ICLK}$ across power mode. The AD7765 low power mode divides the MCLK by a factor of 4, reducing current consumption in both the analog and digital domains.

**Table 6. Modulator Sampling Rate vs. Power Mode**

| Power Mode | Modulator Sampling Rate ($f_{ICLK}$) |
|---|---|
| Normal | MCLK/2 |
| Low | MCLK/4 |

The digital filtering that follows the modulator removes the large out-of-band quantization noise (see Figure 25) while also reducing the data rate from $f_{ICLK}$ at the input of the filter to $f_{ICLK}$ /64 or less at the output of the filter, depending on the decimation rate used.

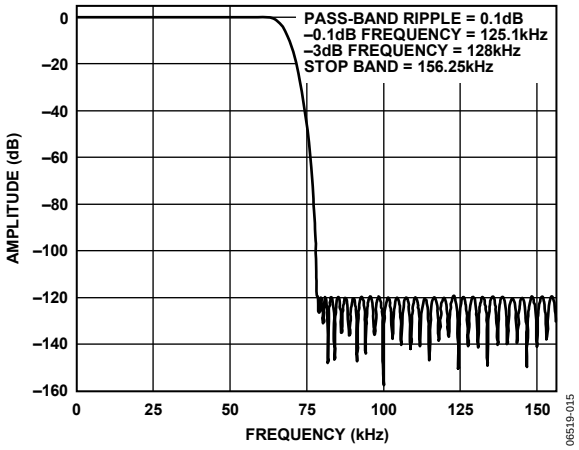



*Figure 26. Filter Frequency Response*

The AD7765 employs a sequence of three FIR filters in series to provide a digital filter with a low ripple pass band, a steep transition band, and excellent stop-band rejection, which starts at the Nyquist frequency. Achieving the stop-band rejection at the Nyquist frequency is beneficial because it prevents signals slightly greater than the Nyquist frequency, which are not protected by and external antialias filter from aliasing back in-band.

The AD7765 digital filter allows data to be output at three different output data rates (for any given MCLK input frequency) through setting the decimation ratio through the series of filters.

The first filter receives data from the modulator at $f_{ICLK}$ MHz, where it is decimated 4× to the output data at ($f_{ICLK}$/4) MHz. The second filter allows the decimation rate to be chosen from 8× to 32×. The third filter has a fixed decimation rate of 2×.

Digital filters exhibit a group delay and settling time. The group delay of the filter is the delay from the change in analog input to when it is output by the digital filter. It is comprised of the computation plus the filter delays. The delay until valid data is available (when the FILTER_SETTLE status bit is set) is approximately twice the filter delay plus the computation delay.

The group delay and settling time of a digital filter is apparent in the behavior of the ADC response to a $\overline{\text{SYNC}}$ input pulse.

and Table 9 describe the response of the AD7765 in both normal and low power modes to a SYNC pulse, in addition to providing the group delay and settling times. Figure 27 shows the effect of $\overline{\text{SYNC}}$ and the subsequent signals from the AD7765.

The $\overline{\text{SYNC}}$ rising edge sets a known point in time from which the digital filter begins to process inputs from the modulator. This is useful in building a simultaneous sampling solution with multiple AD7765 devices, all clocked by the same MCLK.

The logic level of the $\overline{\text{SYNC}}$ pin is sampled by the rising edge of MCLK. Transitioning $\overline{\text{SYNC}}$ from low to high on an MCLK falling edge is recommended. Following the rising edge of $\overline{\text{SYNC}}$, a number of MCLK periods pass before the first falling edge of $\overline{\text{FSO}}$ indicates a conversion output; this number of MCLK periods is defined as $t_{\text{SYNC OFFSET}}$. Beyond $t_{\text{SYNC OFFSET}}$, a number of conversion periods, each indicated by the falling edge of $\overline{\text{FSO}}$, occur before the data from the filter is fully settled. During this time, outputs from the ADC have data that is a filtered mix of inputs to the modulator both before and after the time at which the $\overline{\text{SYNC}}$ signal transitioned from logic low to logic high.

All outputs from the ADC exhibit a group delay. The constant delay, due to the digital filter, is described by the number of conversion periods ($t_{ODR}$) that pass between a change occurring on the analog input being seen on the digital conversion output.

Figure 27 illustrates the group delay, showing a scenario where there is a step change on the analog inputs after the filter initially settles. As shown, a given number of periods of the output data rate occur before the digital output shows the step change.

**Table 7. Group Delay ($t_{GD\_ODR}$) Expressed in Periods of the Output Data Rate**

| Decimation Rate | $t_{GD\_ODR}$ in Output Data Rate Periods | |
|---|---|---|
| | Normal Power Mode | Low Power Mode |
| 128× | 28 | 28 |
| 256× | 28 | 28 |

Because the group delay is not an exact number of conversion periods, a more precise way to describe the term is in MCLK periods. The exact region within a given conversion period where the analog input change occurs determines which output data period the ADC output responds to with a change in the digital output. Figure 27 shows that, if the step change on the input occurs at later point in time within the output period, the digital output remains updated within the same ODR period.

Described as the fine group delay, $t_{GDMCLK}$, this delay consists of computation delay added to the actual delay through the filter provided in MCLK periods. Expressing the group delay in this manner allows it to be shown independent of the discrete steps of the ADC output data rate.

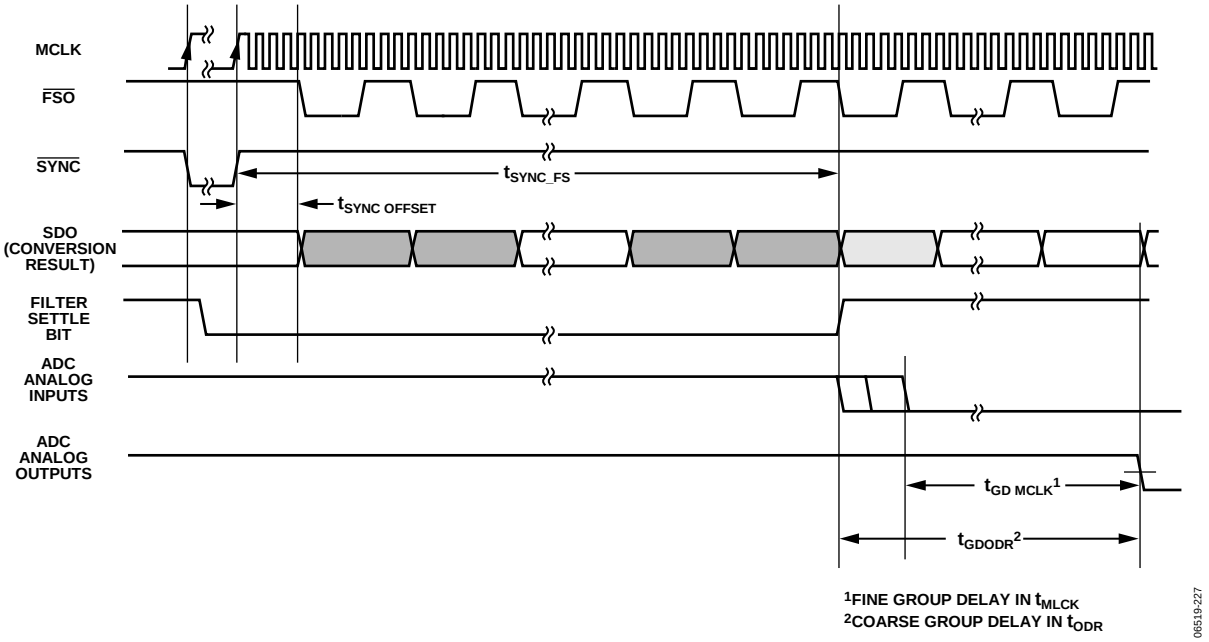



*Figure 27. AD7765 Digital Filtering; Response to $\overline{\text{SYNC}}$, Settling Time, and Group Delay*

**Table 8. Filter Group Delay and Settling Time in Normal Power Mode**

| Decimation Rate | Filter Computation Delay ($t_{MCLK}$) | Filter Delay ($t_{MCLK}$) | $t_{GDMCLK}$ ADC Group Delay ($t_{MCLK}$) | $t_{SYNC\ OFFSET}$ ($t_{MCLK}$) | $t_{SYNC\_FS}$ $\overline{SYNC}$ to FILTER_ SETTLE Bit ($t_{MCLK}$) | Modulator Sampling Rate ($f_{ICLK}$) | Oversampling Ratio (OSR) | Filter Pass Band | Output Data Rate (ODR) |
|---|---|---|---|---|---|---|---|---|---|
| 128× | 113 | 6960 | 7073 | 141 | 13,966 | MCLK/2 | 128 | ODR × 0.4 | MCLK/128 |
| 256× | 443 | 13,608 | 14,051 | 252 | 27,901 | MCLK/2 | 256 | ODR × 0.4 | MCLK/256 |

**Table 9. Filter Group Delay and Settling Time for Low Power Mode**

| Decimation Rate | Filter Computation Delay ($t_{MCLK}$) | Filter Delay ($t_{MCLK}$) | $t_{GDMCLK}$ ADC Group Delay ($t_{MCLK}$) | $t_{SYNC\ OFFSET}$ ($t_{MCLK}$) | $\overline{SYNC}$ to FILTER_ SETTLE Bit ($t_{MCLK}$) | Modulator Sampling Rate ($f_{ICLK}$) | Oversampling Ratio (OSR) | Filter Pass Band | Output Data Rate (ODR) |
|---|---|---|---|---|---|---|---|---|---|
| 128× | 162 | 7008 | 7170 | 167 | 14,248 | MCLK/4 | 64 | ODR × 0.4 | MCLK/128 |
| 256× | 224 | 13,920 | 14,144 | 277 | 27,926 | MCLK/4 | 128 | ODR × 0.4 | MCLK/256 |

## AD7765 ANTIALIAS PROTECTION

The decimation of the AD7765, along with its counterparts in the AD776x family, namely the AD7760, AD7762, AD7763, and AD7765, provides top of the range antialias protection.

The decimation filter of the AD7765 features more than 115 dB of attenuation across the full stop band, which ranges from the Nyquist frequency, namely ODR/2, up to ICLK − ODR/2 (where ODR is the output data rate). Starting the stop band at the Nyquist frequency prevents any signal component above Nyquist (and up to ICLK − ODR/2) from aliasing into the desired signal bandwidth.

Figure 26 shows the frequency response of the decimation filter when the AD7765 is operated with a 40 MHz MCLK in decimate 128× mode. Note that the first stop-band frequency occurs at Nyquist. The frequency response of the filter scales with both the decimation rate chosen and the MCLK frequency applied. When using low power mode, the modulator sample rate is MCLK/4.

Taking as an example the AD7765 in normal power and in decimate 128× mode, the first possible alias frequency is at the ICLK frequency minus the pass band of the digital filter (see Figure 28).

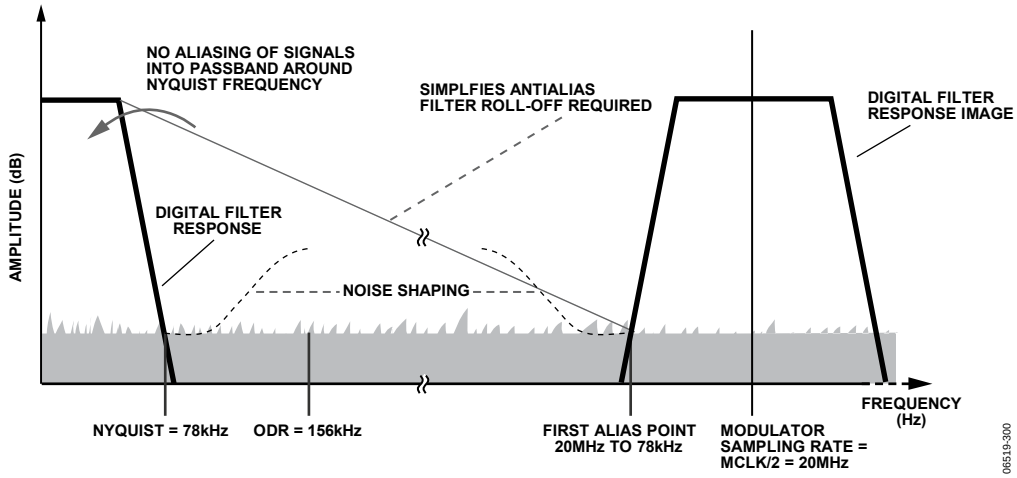



*Figure 28. Antialias Example Using the AD7765 in Normal Mode, Decimate 128× Using MCLK/2 = ICLK = 20 MHz*

# AD7765 INPUT STRUCTURE

The AD7765 requires a 4.096 V input to the reference pin, $V_{REF}+$, supplied by a high precision reference, such as the ADR444. Because the input to the Σ-Δ modulator of the device is fully differential, the effective differential reference range is 8.192 V.

$$V_{REF}+ (Diff) = 2 \times 4.096 = 8.192 \text{ V}$$

As is inherent in Σ-Δ modulators, only a certain portion of this full reference can be used. With the AD7765, 80% of the full differential reference can be applied to the differential inputs of the modulator.

$$Modulator\_Input_{FULL\ SCALE} = 8.192 \text{ V} \times 0.8 = 6.5536 \text{ V}$$

This means that a maximum of ±3.2768 V p-p full scale can be applied to each of the AD7765 modulator inputs (Pin 5 and Pin 6), with the AD7765 being specified with an input −0.5 dB down from full scale (−0.5 dBFS). The AD7765 modulator inputs must have a common-mode input of 2.048 V.

Figure 29 shows the relative scaling between the differential voltages applied to the modulator pins and the respective 24-bit, twos complement digital outputs.

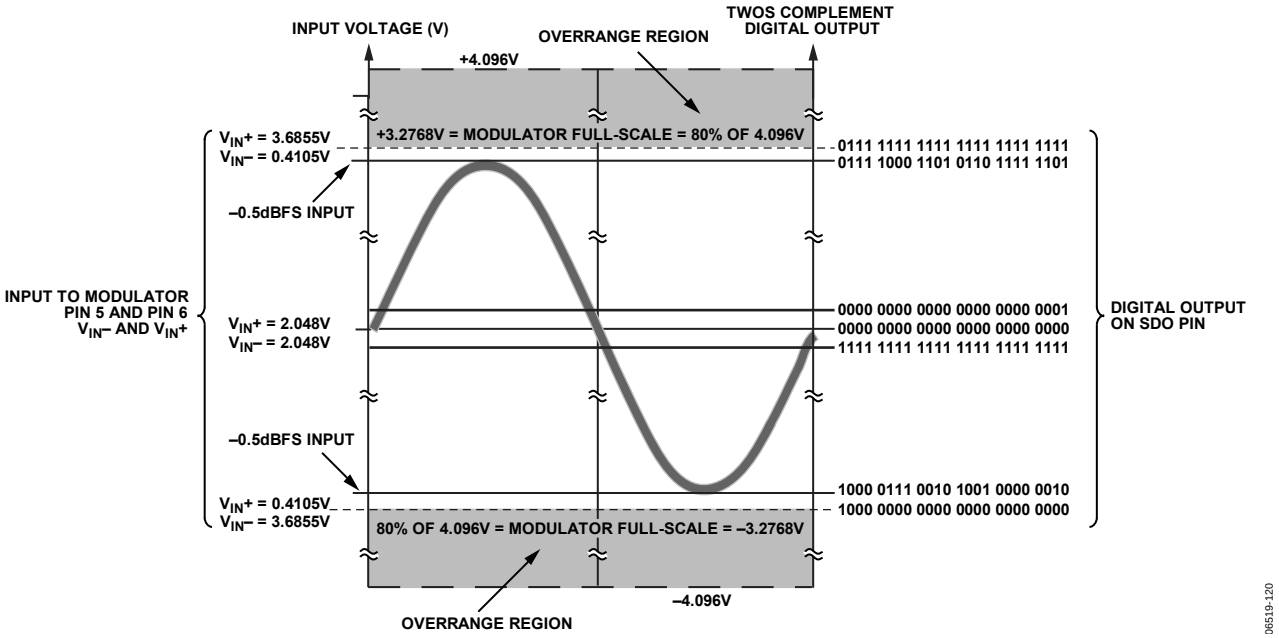



*Figure 29. AD7765 Scaling—Modulator Input Voltage vs. Digital Output Code*

## ON-CHIP DIFFERENTIAL AMPLIFIER

The AD7765 contains an on-board differential amplifier recommended to drive the modulator input pins. Pin 1, Pin 2, Pin 3, and Pin 4 on the AD7765 are the differential input and output pins of the amplifier. The external components, $R_{IN}$, $R_{FB}$, $C_{FB}$, $C_S$, and $R_M$, are placed around Pin 1 through Pin 6 to create the recommended configuration.

To achieve the specified performance, configure the differential amplifier as a first-order antialias filter, as shown in Figure 30, using the component values listed in Table 10. The inputs to the differential amplifier are then routed through the external component network before being applied to the modulator inputs, $V_{IN}-$ and $V_{IN}+$ (Pin 5 and Pin 6).

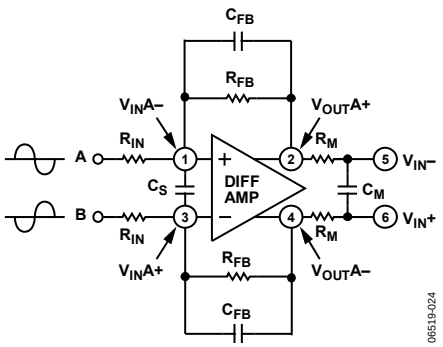



*Figure 30. Differential Amplifier Configuration*

**Table 10. On-Chip Differential Filter Component Values**

| Value | $R_{IN}$ (kΩ) | $R_{FB}$ (kΩ) | $R_M$ (Ω) | $C_S$ (pF) | $C_{FB}$ (pF) | $C_M$ (pF) |
|---|---|---|---|---|---|---|
| Optimal | 4.75 | 3.01 | 43 | 8.2 | 47 | 33 |
| Tolerance Range[1] | 2.37 to 5.76 | 2.4 to 4.87 | 36 to 47 | 0 to 10 | 20 to 100 | 33 to 56 |

[1] The values shown are the acceptable tolerances for each component when altered relative to the optimal values that achieve the stated specifications of the device.

The range of values for each of the components in the differential amplifier configuration is listed in Table 10. When using the differential amplifier to gain the input voltages to the required modulator input range, it is recommended to implement the gain function by changing $R_{IN}$ and leaving $R_{FB}$ as the listed optimal value.

The common-mode input at each of the differential amplifier input pins ($V_{IN}A+$ and $V_{IN}A-$) can range from 0.8 V dc to 2.2 V dc. The amplifier has a constant output common-mode voltage of 2.048 V, that is, $V_{REF}/2$, the requisite common-mode voltage for the modulator input pins ($V_{IN}+$ and $V_{IN}-$).

Figure 31 shows the signal conditioning that occurs using the differential amplifier configuration shown in Table 10 with a ±2.5 V input signal to the differential amplifier. The amplifier in this example is biased around ground and is scaled to provide ±3.0935 V p-p (−0.5 dBFS) on each modulator input with a 2.048 V common mode.

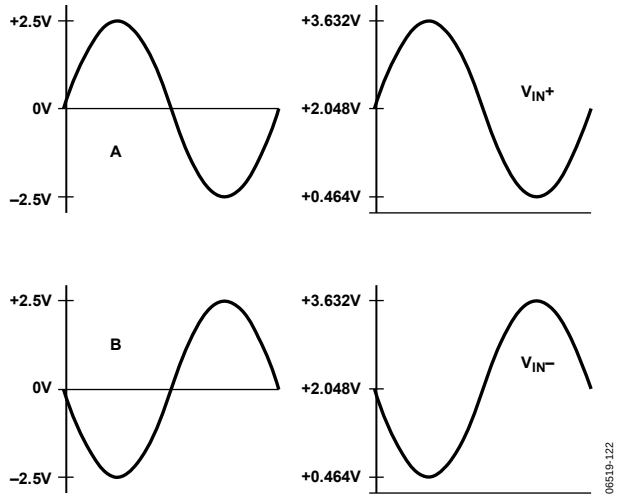



*Figure 31. Differential Amplifier Signal Conditioning*

To obtain maximum performance from the AD7765, it is recommended to drive the ADC with differential signals. Figure 32 shows how a bipolar, single-ended signal biased around ground drives the AD7765 with the use of an external operational amplifier, such as the AD8021.

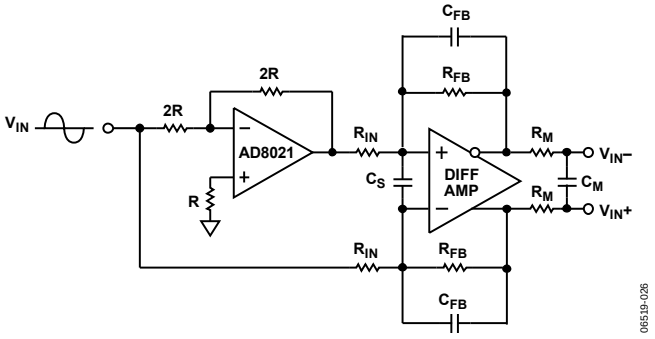



*Figure 32. Single-Ended-to-Differential Conversion*

## MODULATOR INPUT STRUCTURE

The AD7765 employs a double-sampling front end, as shown in Figure 33. For simplicity, only the equivalent input circuitry for $V_{IN}+$ is shown. The equivalent circuitry for $V_{IN}-$ is the same.

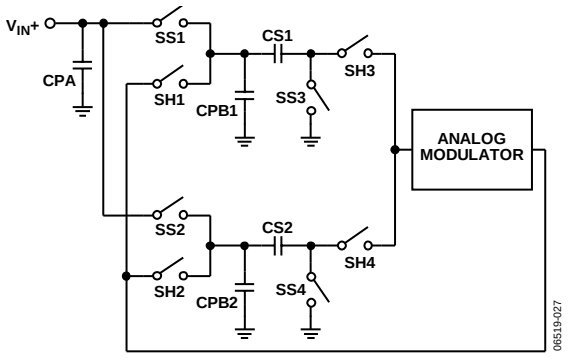



*Figure 33. Equivalent Input Circuit*

The SS1 and SS3 sampling switches are driven by ICLK, whereas the SS2 and SS4 sampling switches are driven by $\overline{ICLK}$. When ICLK is high, the analog input voltage is connected to CS1. On the falling edge of ICLK, the SS1 and SS3 switches open and the analog input is sampled on CS1. Similarly, when ICLK is low, the analog input voltage is connected to CS2. On the rising edge of ICLK, the SS2 and SS4 switches open, and the analog input is sampled on CS2.

The CPA, CPB1, and CPB2 capacitors represent parasitic capacitances that include the junction capacitances associated with the MOS switches.

**Table 11. Equivalent Component Values**

| CS1 (pF) | CS2 (pF) | CPA (pF) | CPB1/CPB2 (pF) |
|---|---|---|---|
| 13 | 13 | 13 | 5 |

## DRIVING THE MODULATOR INPUTS DIRECTLY

The AD7765 can be configured so that the on-board differential amplifier can be disabled and the modulator can be driven directly using discrete amplifiers. This allows the user to lower the power dissipation.

To power down the on board differential amplifier, the user issues a write to set the AMP OFF bit in the control register to logic high (see Figure 34).

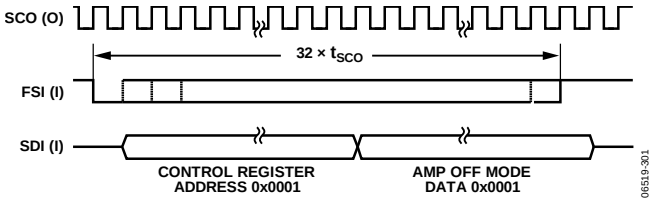
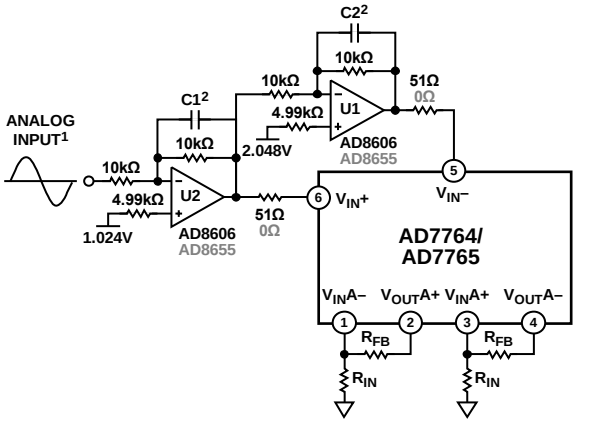



*Figure 34. Writing to the AD7765 Control Register Turning Off the On-Board Differential Amplifier*

The AD7765 modulator inputs must have a common-mode voltage of 2.048 V and adhere to the amplitudes as described in the AD7765 Input Structure section.

An example of a typical circuit to drive the AD7765 for applications requiring excellent ac and dc performance is shown in Figure 35. Either the AD8606 or AD8656 can drive the AD7765 modulator inputs directly.

Best practice is to short the differential amplifier inputs to ground through the typical input resistors and leave the typical feedback resistors in place.




1 –0.5dBFS INPUT SIGNAL AS DESCRIBED IN INPUT STRUCTURE SECTION.
2 SET C1 AND C2 AS REQUIRED FOR APPLICATION INPUT BW AND ANTI-ALIAS REQUIREMENT.

*Figure 35. Driving the AD7765 Modulator Inputs Directly from a Single-Ended Source (On-Board Differential Amplifier Powered Down)*

# AD7765 SERIAL INTERFACE

## READING DATA

The AD7765 uses a fully synchronous serial data interface where the ADC is the master providing frame, serial clock, and serial data outputs. The timing diagram in Figure 2 shows how the AD7765 transmits conversion results.

The data read from the AD7765 is clocked out using the serial clock output (SCO). The SCO frequency is half that of the MCLK input to the AD7765.

The conversion result output on the serial data output (SDO) line is framed by the frame synchronization output, $\overline{FSO}$, which is sent logic low for 32 SCO cycles. Each bit of the new conversion result is clocked onto the SDO line on the rising SCO edge and is valid on the falling SCO edge. The 32-bit result consists of the 24 data bits followed by five status bits followed further by three zeros. The five status bits are listed in Table 12 and described in this section.

**Table 12. Status Bits During a Data Read**

| D7 | D6 | D5 | D4 | D3 |
|---|---|---|---|---|
| FILTER-SETTLE | OVR | LPWR | DEC_RATE 1 | DEC_RATE 0 |

The FILTER-SETTLE bit indicates whether the data output from the AD7765 is valid. After resetting the device (using the $\overline{RESET}$ pin) or clearing the digital filter (using the $\overline{SYNC}$ pin), the FILTER_SETTLE bit goes logic low to indicate that the full settling time of the filter has not yet passed and that the data is not yet valid. The FILTER_SETTLE bit also goes to zero when the input to the device asserts the overrange alerts.

The OVR (overrange) bit is described in the Overrange Alerts section.

The LPWR bit is set to logic high when the AD7765 operates in low power mode. See the Power Modes section for further details.

The DEC_RATE 1 bit and the DEC_RATE 0 bit indicate the decimation ratio used. Table 13 is a truth table for the decimation rate bits.

**Table 13. Decimation Rate Status Bits**

| Decimate | DEC_RATE 0 |
|---|---|
| 128× | 1 |
| 256× | 0 |

## READING STATUS AND OTHER REGISTERS

The AD7765 features a gain correction register, an overrange register, and a read-only status register. To read back the contents of these registers, the user must first write to the control register of the device and set the bit that corresponds to the register to be read. The next read operation outputs the contents of the selected register (on the SDO pin) instead of a conversion result.

To ensure that the next read cycle contains the contents of the register written to, the write operation to that register must be completed a minimum of $8 \times t_{SCO}$ before the falling edge of $\overline{FSO}$, which indicates the start of the next read cycle. See Figure 4 for further details.

The AD7765 Registers section provides more information on the relevant bits in the control register.

## WRITING TO THE AD7765

A write operation to the AD7765 is shown in Figure 3. The serial writing operation is synchronous to the SCO signal. The status of the frame synchronization input, $\overline{FSI}$, is checked on the falling edge of the SCO signal. If the $\overline{FSI}$ line is low, then the first data bit on the serial data in (SDI) line is latched in on the next SCO falling edge.

Set the active edge of the $\overline{FSI}$ signal to occur at a position when the SCO signal is high or low to allow setup and hold times from the SCO falling edge to be met. The width of the $\overline{FSI}$ signal can be set to between 1 and 32 SCO periods wide. A second, or subsequent, falling edge that occurs before 32 SCO periods elapses is ignored.

Figure 3 details the format for the serial data being written to the AD7765 through the SDI pin. Thirty-two bits are required for a write operation. The first 16 bits select the register address that the data being read is intended for. The second 16 bits contain the data for the selected register.

Writing to the AD7765 is allowed at any time, even while reading a conversion result. Note that, after writing to the device, valid data is not output until after the settling time for the filter elapses. The FILTER_SETTLE status bit is asserted at this point to indicate that the filter has settled and that valid data is available at the output.

# FUNCTIONALITY

## SYNCHRONIZATION

The $\overline{\text{SYNC}}$ input to the AD7765 provides a synchronization function that allows the user to begin gathering samples of the analog front-end input from a known point in time.

The $\overline{\text{SYNC}}$ function allows multiple AD7765 devices, operated from the same master clock that use common $\overline{\text{SYNC}}$ and $\overline{\text{RESET}}$ signals, to be synchronized so that each ADC simultaneously updates its output register. Note that all devices being synchronized must operate in the same power mode and at the same decimation rate.

In the case of a system with multiple AD7765 devices, connect common MCLK, $\overline{\text{SYNC}}$, and $\overline{\text{RESET}}$ signals to each AD7765.

The AD7765 $\overline{\text{SYNC}}$ pin is polled by the falling edge of MCLK. The AD7765 device goes into $\overline{\text{SYNC}}$ when an MCLK falling edge senses that the $\overline{\text{SYNC}}$ input signal is logic low. At this point, the digital filter sequencer is reset to 0. The filter is held in a reset state (in $\overline{\text{SYNC}}$ mode) until the first MCLK falling edge senses $\overline{\text{SYNC}}$ to be logic high.

Where possible, ensure that all transitions of $\overline{\text{SYNC}}$ occur synchronously with the rising edge of MCLK (that is, as far away as possible from the MCLK falling edge, or decision edge). Otherwise, abide by the timing specified in Figure 36, which excludes the $\overline{\text{SYNC}}$ rising edge from occurring in a 10 ns window centered around the MCLK falling edge.

Keep $\overline{\text{SYNC}}$ logic low for a minimum of four MCLK periods. When the MCLK falling edge senses that $\overline{\text{SYNC}}$ has returned to logic high, the AD7765 filters begin to gather input samples simultaneously. The $\overline{\text{FSO}}$ falling edges are also synchronized, allowing for simultaneous output of conversion data.

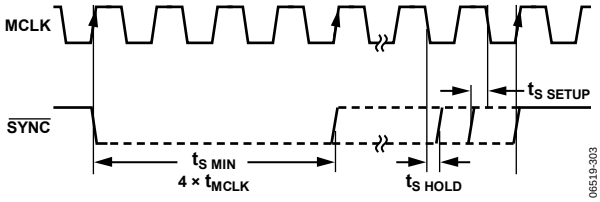



*Figure 36. $\overline{\text{SYNC}}$ Timing Relative to MCLK*

Following a $\overline{\text{SYNC}}$ pulse, the digital filter needs time to settle before valid data can be read from the AD7765. To ensure there is valid data on the SDO line, Check the FILTER_SETTLE status bit (see D7 in Table 12) that is output with each conversion result. The time from the rising edge of $\overline{\text{SYNC}}$ until the FILTER_SETTLE bit asserts depends on the filter configuration used. See the Theory of Operation section and the values listed in Figure 6 for details on calculating the time until FILTER_SETTLE asserts.

Note that the FILTER_SETTLE bit is designed as a reactionary flag to indicate when the conversion data output is valid.

## OVERRANGE ALERTS

The AD7765 offers an overrange function in both a pin and status bit output. The overrange alerts indicate when the voltage applied to the AD7765 modulator input pins exceeds the limit set in the overrange register, indicating that the voltage applied is approaching a level that places the modulator in an overage condition. To set this limit, the user must program the register. The default overrange limit is set to 80% of the $V_{REF}$ voltage (see the AD7765 Registers section).

The OVERRANGE pin outputs logic high to alert the user that the modulator has sampled an input voltage greater in magnitude than the overrange limit as set in the overrange register. The OVERRANGE pin is set to logic high when the modulator samples an input above the overrange limit. After the input returns below the limit, the OVERRANGE pin returns to zero. The OVERRANGE pin is updated after the first FIR filter stage. The output of OVERRANGE changes at the ICLK/4 frequency.

The OVR status bit is output as Bit D6 on SDO during a data conversion and can be checked in the AD7765 status register. This bit is less dynamic than the OVERRANGE pin output. It is updated on each conversion result output; that is, the bit changes at the output data rate. If the modulator samples a voltage input that exceeds the overrange limit during the process of gathering samples for a particular conversion result output, then the OVR bit is set to logic high.

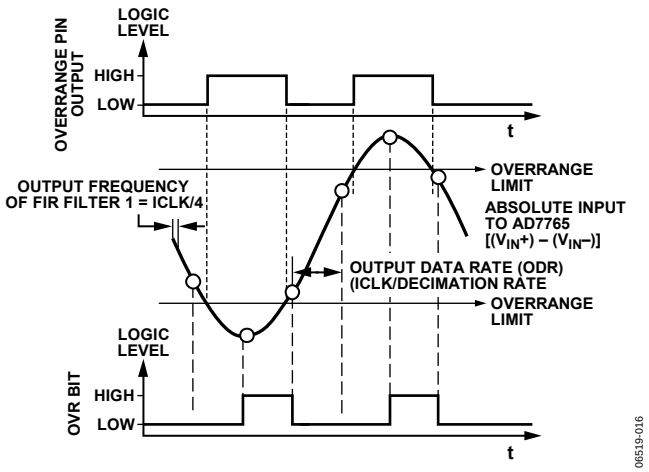



*Figure 37. OVERRANGE Pin and OVR Bit vs. Absolute Voltage Applied to the Modulator*

The output points from FIR Filter 1 in Figure 37 are not drawn to scale relative to the output data rate points. The FIR Filter 1 output is updated either 16×, 32×, or 64× faster than the output data rate, depending on the decimation rate in operation.

## POWER MODES

### *Low Power Mode*

During power-up, the AD7765 defaults to operate in normal power mode. There is no register write required.

The AD7765 also offers low power mode. To operate the device in low power mode, set the LPWR bit in the control register to logic high (see Figure 38). Operating the AD7765 in low power mode has no impact on the output data rate or available bandwidth.

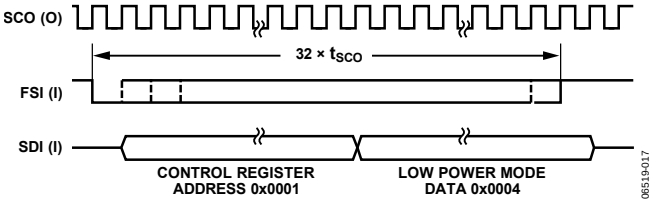



*Figure 38. Write Scheme for Low Power Mode*

### *$\overline{\text{RESET}}$/$\overline{\text{PWRDWN}}$ Mode*

The AD7765 features a $\overline{\text{RESET}}$/$\overline{\text{PWRDWN}}$ pin. Holding the input to this pin logic low places the AD7765 in power-down mode. All internal circuitry is reset. Apply a $\overline{\text{RESET}}$ pulse to the AD7765 after initial power-up of the device.

The AD7765 $\overline{\text{RESET}}$ pin is polled by the rising edge of MCLK. The AD7765 device goes into reset when an MCLK rising senses the $\overline{\text{RESET}}$ input signal to be logic low. AD7765 comes out of $\overline{\text{RESET}}$ on the first MCLK rising edge that senses $\overline{\text{RESET}}$ to be logic high.

The best practice is to ensure that all transitions of $\overline{\text{RESET}}$ occur synchronously with the falling edge of MCLK; otherwise, adhere to the timing requirements shown in Figure 39.

Keep $\overline{\text{RESET}}$ at logic low for a minimum of one MCLK period for a valid reset to occur.

In cases where multiple AD7765 devices are being synchronized using the $\overline{\text{SYNC}}$ pulse and in the case of daisy chaining multiple AD7765 devices, a common $\overline{\text{RESET}}$ pulse must be provided in addition to the common $\overline{\text{SYNC}}$ and MCLK signals.

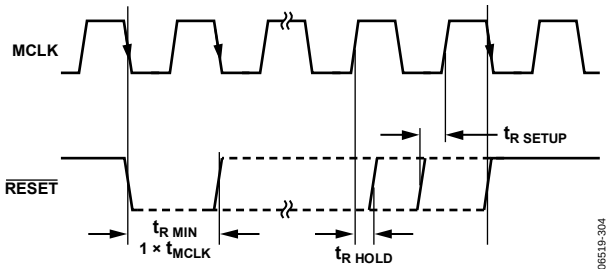



*Figure 39. $\overline{\text{RESET}}$ Timing Synchronous to MCLK*

## DECIMATION RATE PIN

The decimation rate of the AD7765 is selected using the DEC_RATE pin. Table 14 shows the voltage input settings required for each of the three decimation rates.

**Table 14. DEC_RATE Pin Settings**

| Decimation Rate | DEC_RATE Pin State | Maximum ODR (kHz) |
|---|---|---|
| 128× | $DV_{DD}$ | 156.25 |
| 256× | Ground | 78.125 |

# DAISY CHAINING

Daisy chaining allows numerous devices to use the same digital interface lines. This feature is especially useful for reducing component count and wiring connections, such as in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register. When daisy chaining is used, all devices in the chain must operate in a common power mode and at a common decimation rate.

The block diagram in Figure 40 shows how to connect devices to achieve daisy-chain functionality. Figure 40 shows four AD7765 devices daisy-chained together with a common MCLK signal applied. This configuration works in decimate 128× or decimate 256× mode only.

## READING DATA IN DAISY-CHAIN MODE

Referring to Figure 40, note that the SDO line of AD7765 (A) provides the output data from the chain of AD7765 converters. Also, note that for the last device in the chain, AD7765 (D), the SDI pin is connected to ground. All of the devices in the chain must use common MCLK and $\overline{\text{SYNC}}$ signals.

To enable the daisy-chain conversion process, apply a common $\overline{\text{SYNC}}$ pulse to all devices (see the Synchronization section).

After a $\overline{\text{SYNC}}$ pulse is applied to all devices, the filter settling time must pass before the FILTER_SETTLE bit is asserted indicating valid conversion data at the output of the chain of devices. As shown in Figure 41, the first conversion result is output from the device labeled AD7765 (A). This 32-bit conversion result is then followed by the conversion results from the AD7765 (B), AD7765 (C), and AD7765 (D) devices with all conversion results output in an MSB-first sequence. The signals output from the daisy chain are the stream of conversion results from the SDO pin of AD7765 (A) and the $\overline{\text{FSO}}$ signal output by the first device in the chain, AD7765 (A).

The falling edge of $\overline{\text{FSO}}$ signals the MSB of the first conversion output in the chain. $\overline{\text{FSO}}$ stays logic low throughout the 32 SCO clock periods needed to output the AD7765 (A) result and then goes logic high during the output of the conversion results from the AD7765 (B), AD7765 (C), and AD7765 (D) devices.

The maximum number of devices that can be daisy-chained is dependent on the decimation rate selected. Calculate the maximum number of devices that can be daisy-chained by simply dividing the chosen decimation rate by 32 (the number of bits that must be clocked out for each conversion). Table 15 provides the maximum number of chained devices for each decimation rate.

**Table 15. Maximum Daisy Chain Length for all Decimation Rates**

| Decimation Rate | Maximum Chain Length |
|---|---|
| 256× | 8 devices |
| 128× | 4 devices |

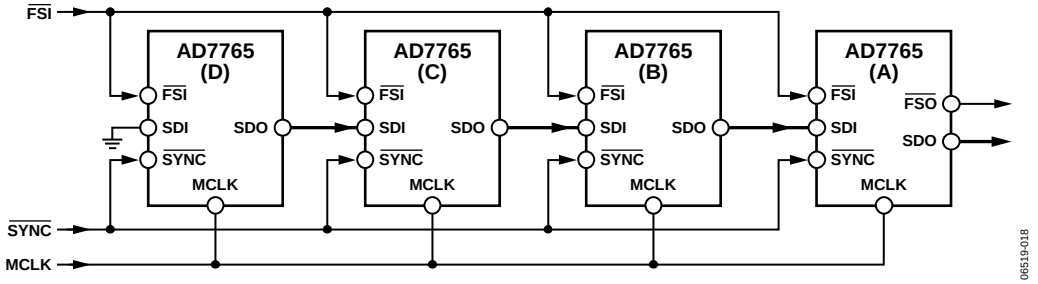



*Figure 40. Daisy Chaining Four Devices in Decimate 128× Mode Using a 40 MHz MCLK Signal*

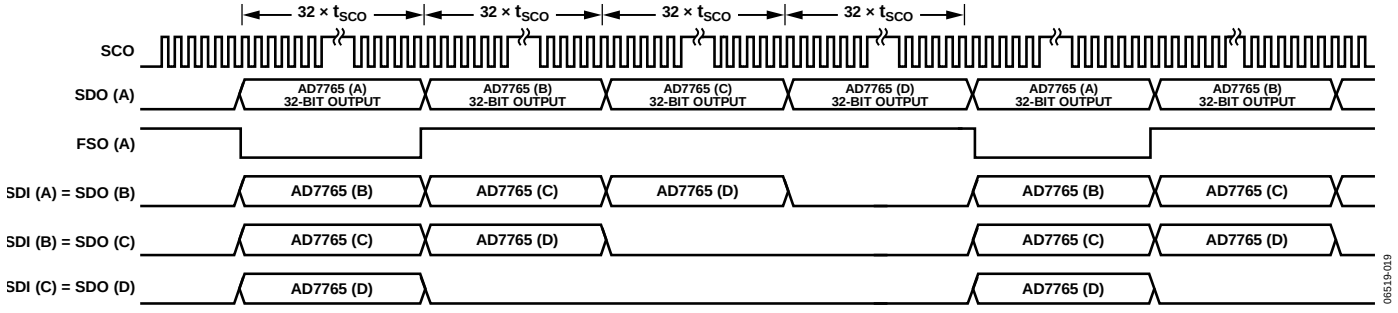



*Figure 41. Daisy-Chain Mode, Data Read Timing Diagram (for the Daisy-Chain Configuration Shown in Figure 40)*

## WRITING DATA IN DAISY-CHAIN MODE

Writing to AD7765 devices in daisy-chain mode is similar to writing to a single device. The serial writing operation is synchronous to the SCO signal. The status of the frame synchronization input, $\overline{FSI}$, is checked on the falling edge of the SCO signal. If the $\overline{FSI}$ line is low, then the first data bit on the serial data in the SDI line is latched in on the next SCO falling edge.

Writing data to the AD7765 in daisy-chain mode operates with the same timing structure as writing to a single device (see Figure 3). The difference between writing to a single device and writing to a number of daisy-chained devices is in the implementation of the $\overline{FSI}$ signal. The number of devices that are in the daisy chain determines the period for which the $\overline{FSI}$ signal must remain logic low. To write to n number of devices in the daisy chain, the period between the falling edge of $\overline{FSI}$ and the rising edge of $\overline{FSI}$ must be between 32 × (n − 1) to 32 × n SCO periods.

For example, if three AD7765 devices are being written to in daisy-chain mode, $\overline{FSI}$ is logic low for between 32 × (3 − 1) to 32 × 3 SCO pulses. This means that the rising edge of FSI must occur between the 64th and 96th SCO periods.

The AD7765 devices can be written to at any time. The falling edge of $\overline{FSI}$ overrides all attempts to read data from the SDO pin. In the case of a daisy chain, the $\overline{FSI}$ signal remaining logic low for more than 32 SCO periods indicates to the AD7765 device that there are more devices further on in the chain. This means that the AD7765 directs data that is input on the SDI pin to its SDO pin. This ensures that data is passed to the next device in the chain.

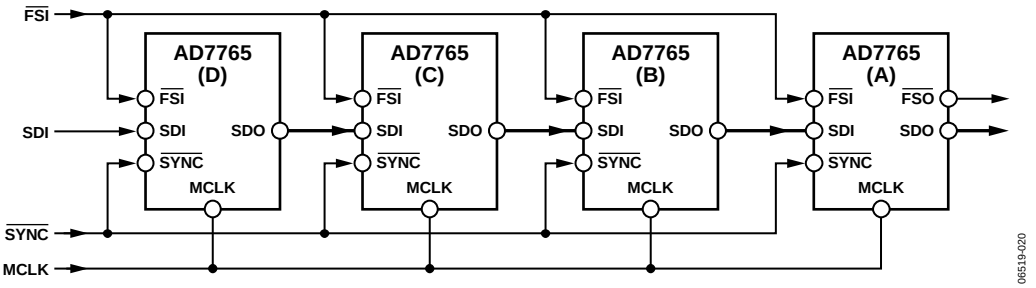



*Figure 42. Writing to an AD7765 Daisy-Chain Configuration*

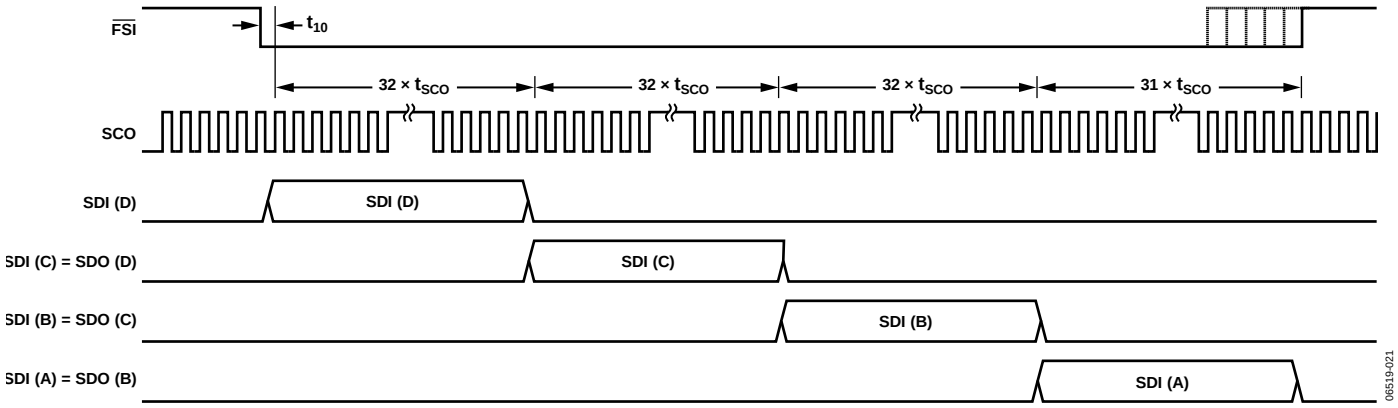



*Figure 43. Daisy-Chain Write Timing Diagram; Writing to Four AD7765 Devices*

# CLOCKING THE AD7765

The AD7765 requires an external low jitter clock source. This signal is applied to the MCLK pin. An internal clock signal (ICLK) is derived from the MCLK input signal. The ICLK controls the internal operation of the AD7765. The maximum ICLK frequency is 20 MHz. To generate the ICLK,

$$ICLK = MCLK/2$$

For output data rates equal to those used in audio systems, a 12.288 MHz ICLK frequency can be used. As shown in Table 6, output data rates of 96 kHz and 48 kHz are achievable with this ICLK frequency.

## MCLK JITTER REQUIREMENTS

The MCLK jitter requirements depend on a number of factors and are given by

$$t_{j(rms)} = \frac{\sqrt{OSR}}{2 \times \pi \times f_{IN} \times 10^{\frac{SNR\,(\text{dB})}{20}}}$$

where:
$t_{j(rms)}$ is rms jitter.
$OSR$ (the oversampling ratio) = $f_{ICLK}/ODR$.
$f_{IN}$ is the maximum input frequency.
$SNR$ (dB) is the target SNR.

### *Example 1*

Take Example 1 from Table 6, where:
$ODR$ = 156.25 kHz.
$f_{ICLK}$ = 20 MHz.
$f_{IN}$ (max) = 78.625 kHz.
$SNR$ = 104 dB.

$$t_{j(rms)} = \frac{\sqrt{128}}{2 \times \pi \times 78.625 \times 10^3 \times 10^{5.35}} = 102.29\,\text{ps}$$

This is the maximum allowable clock jitter for a full-scale, 78.625 kHz input tone with the given ICLK and output data rate.

### *Example 2*

Take Example 2 from Table 6, where:
$ODR$ = 48 kHz.
$f_{ICLK}$ = 12.288 MHz.
$f_{IN}$ (max) = 19.2 kHz.
$SNR$ = 109 dB.

$$t_{j(rms)} = \frac{\sqrt{256}}{2 \times \pi \times 19.2 \times 10^3 \times 10^{5.45}} = 470\ \text{ps}$$

The input amplitude also has an effect on these jitter figures. For example, if the input level is 3 dB below full scale, the allowable jitter is increased by a factor of √2, increasing the first example to 144.65 ps rms. This happens when the maximum slew rate is decreased by a reduction in amplitude.

Figure 44 and Figure 45 illustrate this point, showing the maximum slew rate of a sine wave of the same frequency but with different amplitudes.

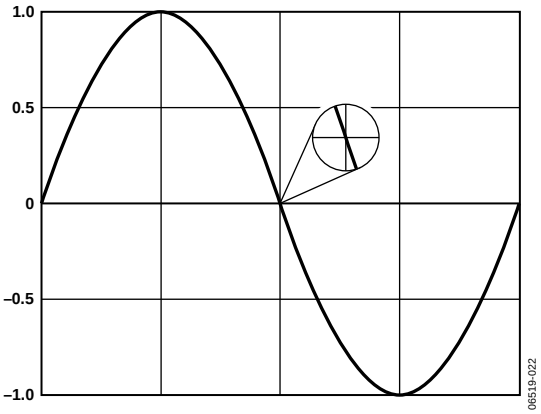



*Figure 44. Maximum Slew Rate of a Sine Wave with an Amplitude of 2 V p-p*

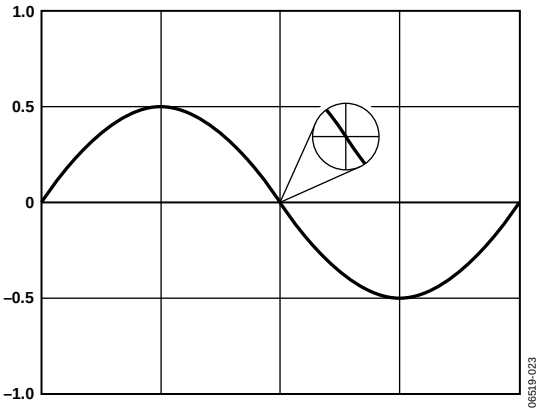



*Figure 45. Maximum Slew Rate of the Same Frequency Sine Wave as in Figure 44 with an Amplitude of 1 V p-p*

# DECOUPLING AND LAYOUT INFORMATION

## SUPPLY DECOUPLING

The decoupling of the supplies applied to the AD7765 is important in achieving maximum performance. Each supply pin must be decoupled to the correct ground pin with a 100 nF, 0603 case size capacitor.

Pay particular attention to decoupling Pin 7 ($AV_{DD}2$) directly to the nearest ground pin (Pin 8). The digital ground pin, AGND2 (Pin 20) is routed directly to ground. Also, connect REFGND (Pin 26) directly to ground.

Decouple the $DV_{DD}$ (Pin 17) and $AV_{DD}3$ (Pin 28) supplies to the ground plane at a point away from the device.

It is recommended to decouple the supplies that are connected to the following supply pins through 0603 size, 100 nF capacitors to a star ground point linked to Pin 23 (AGND1):

- $V_{REF}+$ (Pin 27)
- $AV_{DD}4$ (Pin 25)
- $AV_{DD}1$ (Pin 24)
- $AV_{DD}2$ (Pin 21)

A layout decoupling scheme for these supplies, which connect to the right side of the AD7765, is shown in Figure 46. Note the star-point ground created at Pin 23.

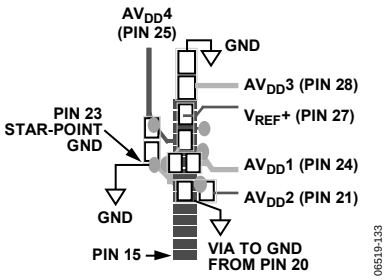



*Figure 46. AD7765 Supply Decoupling*

## REFERENCE VOLTAGE FILTERING

A low noise reference source, such as the ADR444 or ADR434 (4.096 V), is suitable for use with the AD7765. Decouple and filter the reference voltage supplied to the AD7765 as shown in Figure 47.

The recommended scheme for the reference voltage supply is a 200 Ω series resistor connected to a 100 µF tantalum capacitor, followed by a 10 nF decoupling capacitor very close to the $V_{REF}+$ pin.

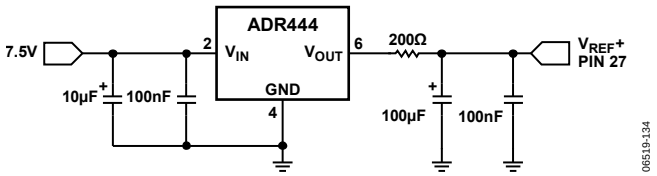



*Figure 47. Reference Connection*

## DIFFERENTIAL AMPLIFIER COMPONENTS

The components recommended for use around the on-chip differential amplifier are detailed in Table 10. Matching the components on both sides of the differential amplifier is important to minimize distortion of the signal applied to the amplifier. A tolerance of 0.1% or better is required for these components. Symmetrical routing of the tracks on both sides of the differential amplifier also assists in achieving the stated performance. Figure 48 shows a typical layout for the components around the differential amplifier. Note that the traces for both differential paths are as symmetrical as possible and that the feedback resistors and capacitors are placed on the underside of the PCB to enable the simplest routing.

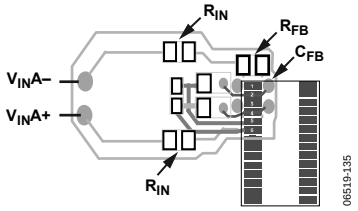



*Figure 48. Typical Layout Structure for Components Surrounding the Differential Amplifier*

## LAYOUT CONSIDERATIONS

The use of correct components is essential to achieve optimum performance, and the correct layout is equally important. The AD7765 product page contains the Gerber files for the AD7765 evaluation board. Use the Gerber files as a reference when designing any system using the AD7765.

Carefully consider the use of ground planes. To ensure that the return currents through the decoupling capacitors are flowing to the correct ground pin, place the ground side of the capacitors as close as possible to the ground pin associated with that supply as recommended in the Supply Decoupling section.

## USING THE AD7765

Use the following to power up and use the AD7765:

1. Apply power to the device.
2. Apply the MCLK signal.
3. Take $\overline{\text{RESET}}$ low for a minimum of one MCLK cycle, preferably synchronous to the falling MCLK edge. If multiple devices are to be synchronized, apply a common $\overline{\text{RESET}}$ to all devices.
4. Wait a minimum of two MCLK cycles after $\overline{\text{RESET}}$ is released.
5. If multiple devices are being synchronized, a $\overline{\text{SYNC}}$ pulse must be applied to the devices, preferably synchronous with the MCLK rising edge. In the case where devices are not being synchronized, no $\overline{\text{SYNC}}$ pulse is required; apply a logic high signal to the $\overline{\text{SYNC}}$ pin.

When applying the $\overline{\text{SYNC}}$ pulse, the issue of a $\overline{\text{SYNC}}$ pulse to the device must not coincide with a write to the device. Ensure that the $\overline{\text{SYNC}}$ pulse is taken low for a minimum of four MCLK periods.

Data can then be read from the device using the default gain and overrange threshold values. The conversion data read is not valid, however, until the settling time of the filter elapses. After time elapses, the FILTER_SETTLE status bit is set, indicating that the data is valid.

Values for the gain and overrange thresholds can be written to or read from the respective registers at this stage.

## BIAS RESISTOR SELECTION

The AD7765 requires a resistor to be connected between the $R_{BIAS}$ and AGNDx pins. Select the resistor value to give a current of 25 μA through the resistor to ground. For a 4.096 V reference voltage, the correct resistor value is 160 kΩ.

# AD7765 REGISTERS

The AD7765 has a number of user-programmable registers. The control register sets the functionality of the on-chip buffer and differential amplifier and provides the option to power down the AD7765.

There are also digital gain and overrange threshold registers. Writing to these registers involves writing the register address followed by a 16-bit data word. The register addresses, details of the individual bits, and default values are provided in the following sections.

## CONTROL REGISTER

**Table 16. Control Register (Address 0x0001, Default Value 0x0000)**

**MSB** **LSB**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | RD OVR | RD GAIN | 0 | RD STAT | 0 | SYNC | 0 | BYPASS REF | 0 | 0 | 0 | PWR DOWN | LPWR | REF BUF OFF | AMP OFF |

**Table 17. Bit Descriptions of the Control Register**

| Bit | Mnemonic | Description |
|---|---|---|
| 14 | RD OVR[1, 2] | Read overrange. If this bit is set, the next read operation outputs the contents of the overrange threshold register instead of a conversion result. |
| 13 | RD GAIN[2] | Read gain. If this bit is set, the next read operation outputs the contents of the digital gain register. |
| 11 | RD STAT[2] | Read status. If this bit is set, the next read operation outputs the contents of the status register. |
| 9 | SYNC[1] | Synchronize. Setting this bit initiates an internal synchronization routine. Setting this bit simultaneously on multiple devices synchronizes all filters. |
| 7 | BYPASS REF | Bypass reference. Setting this bit bypasses the reference buffer if the buffer is off. |
| 3 | PWR DOWN | Power-down. A logic high powers the device down without resetting. Writing a 0 to this bit powers the device back up. |
| 2 | LPWR | Low power mode. Set this bit to Logic 1 when the AD7765 is in low power mode. |
| 1 | REF BUF OFF | Reference buffer off. Asserting this bit powers down the reference buffer. |
| 0 | AMP OFF | Amplifier off. Asserting this bit switches the differential amplifier off. |

[1] Bit 14 to Bit 11 and Bit 9 are self-clearing bits.
[2] Only one of the bits from D14 to D11 can be set in any write operation. The user must select only one function from these bits. That bit, from one of Bit D14 to Bit D11, read determines the contents of the data output within the next FSO frame on the SDO pin.

## STATUS REGISTER

**Table 18. Status Register (Read Only)**

**MSB** **LSB**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PARTNO | 1 | 0 | 0 | 1 | FILTER_SETTLE | LPWR | OVR | 0 | 1 | 0 | REF BUF OFF | AMP OFF | 0 | 0 | DEC 0 |

**Table 19. Bit Descriptions of the Status Register**

| Bits | Mnemonic | Description |
|---|---|---|
| 15 | PARTNO | Part number. This bit is set to 1 for the AD7765. |
| 10 | FILTER_SETTLE | Filter settling bit. This bit corresponds to the FILTER_SETTLE bit in the status word output in the second 16-bit read operation. It indicates when data is valid. |
| 9 | LPWR | Low power mode. This bit is set when operating in low power mode. |
| 8 | OVR | Overrange. If the current analog input exceeds the current overrange threshold, this bit is set. |
| 4 | REF BUF OFF | Reference buffer off. This bit is set when the reference buffer is disabled. |
| 3 | AMP OFF | Amplifier off. This bit is set when the input amplifier is disabled. |
| 2 | 0 | Zero. This bit is set to Logic 0. |
| 0 | DEC 0 | Decimation rate. This bit corresponds to the decimation rate in use. Decimation rate x 256 = 0, Decimation rate x 128 = 1. |

## GAIN REGISTER—ADDRESS 0x0004

***Nonbit Mapped, Default Value: 0xA000***

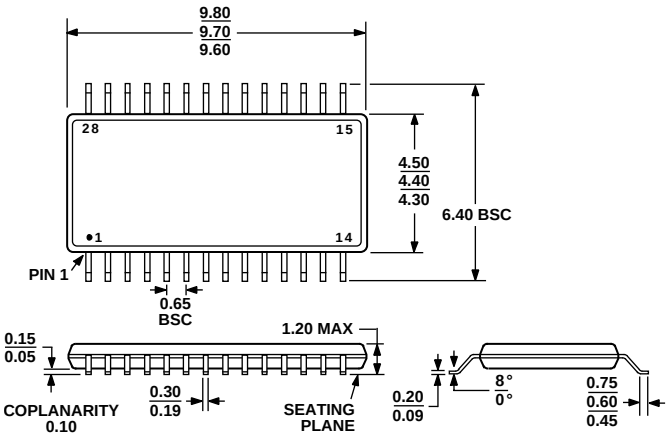
The gain register is scaled such that 0x8000 corresponds to a gain of 1.0. The default value of this register is 1.25 (0xA000). This value results in a full-scale digital output when the input is at 80% of $V_{REF}+$, tying in with the maximum analog input range of ±80% of $V_{REF}+$ p-p.

## OVERRANGE REGISTER—ADDRESS 0x0005

***Nonbit Mapped, Default Value: 0xCCCC***

The overrange register value is compared to the output of the first decimation filter to obtain an overload indication with minimum propagation delay. This comparison is prior to any gain scaling. The default value is 0xCCCC, which corresponds to 80% of $V_{REF}+$ (the maximum permitted analog input voltage). Assuming $V_{REF}+ = 4.096$ V, the bit is then set when the input voltage exceeds approximately 6.55 V p-p differential. The overrange bit is set immediately if the analog input voltage exceeds 100% of $V_{REF}+$ for more than four consecutive samples at the modulator rate.

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-153-AE

*Figure 49. 28-Lead Thin Shrink Small Outline [TSSOP]*
*(RU-28)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD7765BRUZ | −40°C to +85°C | 28-Lead Thin Shrink Small Outline [TSSOP] | RU-28 |
| AD7765BRUZ-REEL7 | −40°C to +85°C | 28-Lead Thin Shrink Small Outline [TSSOP] | RU-28 |
| EVAL-AD7765EDZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.